DEPARTMENT OF PHYSICS
UNIVERSITY OF JYVÄSKYLÄ
RESEARCH REPORT No. 13/2009

CARBON NANOTUBE MEMORY DEVICES WITH HIGH-κ GATE DIELECTRICS

BY
MARCUS RINKIÖ

Academic Dissertation
for the Degree of
Doctor of Philosophy

To be presented, by permission of the
Faculty of Mathematics and Science
of the University of Jyväskylä,
for public examination in Auditorium FYS-1 of the
University of Jyväskylä on December 11, 2009
at 12 o'clock noon

Jyväskylä, Finland
December 2009

Preface

The work reviewed in this thesis has been carried out during the years 2005-2009 at the Department of Physics at the University of Jyväskylä.

First, I wish to thank my supervisor Prof. Päivi Törmä for her valuable guidance and support through out the years starting from summer 2002, when I started to work in her group as a summer student. Without her believe in my work, her insight to physics and her outlook on the future I would not have succeeded in this endeavor. I whish to thank Dr. Andreas Johansson for his guidance, enthusiasm and believe in our common work and Dr. Jussi Toppari for being always willing to help on the problems I encountered in the lab. I'm grateful to Mr. Tommi Hakala, Dr. Anton Kuzyk and Mr. Veikko Linko for their valuable discussions and collegial support and friendship. I wish to thank Ms. Marina Zavodchikova, Dr. Gheorghe-Sorin Paraoanu, Mr. Ville Kotimäki, Mr. Tommi Isoniemi and Ms. Anna-Leena Latvala for their important contribution to this work and Prof. Esko Kauppinen's group for cooperation. I wish to thank our collaborators Nokia Oyj and Dr. Vladimir Ermolov, Vaisala Oyj and Dr. Eeva-Liisa Lakomaa and especially Beneq Oy and Dr. Olli Jylhä for the atomic layer depositions and for illuminating the chemistry behind the ALD processes. I wish to thank all the people in the Nanoscience Center together with all the former and present members of the Nanoele and Quantum Dynamics groups for creating friendly and open working atmosphere. I express my sincere gratitude to Prof.dr.ir. Leo Kouwenhoven for giving me the opportunity for the 6-month visit in the Quantum Transport group at the Delft University of Technology and Dr. Gary Steele and Mr. Georg Götz for their readiness to teach me the basics of quantum dot physics and all the people in the group for welcoming me with open arms.

Financial support from the Magnus Ehrnrooth Foundation, Finnish Foundation for Technology Promotion (TES), the Väisälä Fund of the Finnish Academy of Science and Letters and the Ulla Tuominen Foundation are gratefully acknowledged.

I wish to thank my parents, Seija and Terho, brother Ari and all my friends for their support. Finally, I give my heartfelt thanks to my wife Jonna and my children Niklas and Silja for their love and support and for always giving me something else to think about instead of physics.

Jyväskylä, December 2009

Marcus Rinkiö

Abstract

Rinkiö, Marcus
Jyväskylä: University of Jyväskylä, 2009, 110 p.
(Research report/Department of Physics, University of Jyväskylä,
ISSN 0075-465X; 13/2009)
ISBN 978-951-39-3719-5, PDF 978-951-39-3720-1
diss.

In this thesis the memory effect and negative differential resistance (NDR) rising from the hysteresis present in carbon nanotube field-effect transistors (CNT-FETs) with high-κ gate dielectrics is discussed. A high-yield fabrication method is developed where Hf-based gate dielectrics are used to control the memory effect by designing the gate dielectric in nm-thin layers. The first CNT-FETs with consistent and narrow distribution memory effects in their transfer characteristics are achieved, by using atomic layer depositions of HfO_2 and TiO_2 in a triple-layer configuration. The effect of humidity on the hysteresis of the triple-layer gate dielectric is found to be smaller than in CNT-FETs having the more common SiO_2 gate dielectric.

As a figure of merit, a 100 ns Write/Erase speed is achieved with CNT-FET memory elements having HfO_2 as a gate and passivation dielectric. This speed is high enough to compete with state of the art commercial Flash memories. Also the endurance of the memory elements is shown to exceed 10^4 cycles. A model where the hafnium oxide has defect states situated above, but close in energy to, the band gap of the CNT is discussed. The fast and effective charging and discharging of the defects is shown to be a likely explanation to the 100 ns operation speed, largely exceeding the CNT-FET memory speeds of 10 ms observed earlier.

By patterning the triple-layer high-κ gate oxide, quantum dots can be induced into the channel of CNT-FETs. This in turn is used to attain controllable and gate-tunable NDR in these devices. The method is fully scalable and opens up a new avenue for electronic nanoscale devices using NDR in their operation, e.g. nanoscale amplifiers, fast switching elements and high-frequency oscillators operating in the THz domain. All the above findings indicate strong charge trapping in the Hf-based gate dielectrics, which can be utilized in many ways by carefully designing the gate dielectric to suit the application.

Keywords Carbon nanotube, field-effect transistor, hysteresis, high-κ, memory, negative differential resistance, quantum dot, atomic layer deposition

Author's address Marcus Rinkiö
Department of Physics
Nanoscience Center
University of Jyväskylä
Finland

Supervisor Professor Päivi Törmä
Department of Applied Physics
Helsinki University of Technology
Finland

Reviewers Professor Pertti Hakonen
Low Temperature Laboratory
Helsinki University of Technology
Finland

Professor Markku Leskelä
Department of Chemistry
University of Helsinki
Finland

Opponent Dr. Ralph Krupke
Institut für Nanotechnologie
Forschungszentrum Karlsruhe GmbH
Karlsruhe
Germany

List of Publications

The main results of this thesis have been reported in the following articles:

A.I ZAVODCHIKOVA, M. Y., JOHANSSON, A., RINKIÖ, M. TOPPARI, J. J., NASIBULIN, A. G., KAUPPINEN, E. I. & TÖRMÄ P. *Fabrication of carbon nanotube-based field-effect transistors for studies of their memory effects*. Phys. Status Solidi B **244** (2007) 4188.

A.II RINKIÖ, M., ZAVODCHIKOVA, M. Y., TÖRMÄ, P. & JOHANSSON, A. *Effect of humidity on the hysteresis of single walled carbon nanotube field-effect transistors*. Phys. Status Solidi B **245** (2008) 2315.

A.III RINKIÖ, M., JOHANSSON, A., ZAVODCHIKOVA, M. Y., TOPPARI, J. J., NASIBULIN, A. G., KAUPPINEN, E. I. & TÖRMÄ, P. *High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric*. New J. Phys. **10** (2008) 103019.

A.IV RINKIÖ, M., JOHANSSON, A., PARAOANU, G. S. & TÖRMÄ, P. *High-speed memory from carbon nanotube field-effect transistors with high-κ gate dielectric*. Nano Lett. **9** (2009) 643.

A.V RINKIÖ, M., JOHANSSON, A., KOTIMÄKI, V., & TÖRMÄ, P. *Room temperature negative differential resistance in carbon nanotube field-effect transistors with novel gate oxide design*. Submitted to Nano Lett. (2009) .

Author's contribution

The author of this thesis has the main contribution in writing the papers A.II, A.IV and A.V and participated in writing the paper A.III. In A.IV and A.V the author carried out all the sample fabrication and electrical measurements and main part in the analysis of the results. In A.II and A.III the author carried out the main part of the sample fabrication and electrical measurements and participated in the analysis of the results. In A.I the author carried out part of the sample fabrication and the analysis of the results. In A.IV and A.V the author carried out the main part in creating the model for operation.

Other publications to which the author has contributed:

I VANHANEN, J., RINKIÖ, M., AUMANEN, J., KORPPI-TOMMOLA, J., KOLEHMAINEN, E., KERKKÄNEN, T. & TÖRMÄ, P. *Characterization of used mineral oil condition by spectroscopic techniques*. Appl. Opt. **43** (2004) 4718.

II TUUKKANEN, S., KUZYK, A., TOPPARI, J. J., HÄKKINEN, H., HYTÖNEN, V. P., NISKANEN, E., RINKIÖ, M. & TÖRMÄ, P. *Trapping of 27 bp-8 kbp DNA and immobilization of thiol-modified DNA using dielectrophoresis*. Nanotechnology **18** (2007) 295204.

List of Abbreviations

A	anisole
ALD	atomic layer deposition
AFM	atomic force microscope
BJT	bipolar junction transistor
CG	control gate
CNL	charge neutrality level
CNT	carbon nanotube
CNT-FET	carbon nanotube field-effect transistor
CVD	chemical vapor deposition
DOS	density of states
DRAM	dynamic random access memory
EEPROM	electrically erasable programmable read-only memory
EL	ethyl lactate
EPROM	erasable programmable read-only memory
ES	exited state
FG	floating gate
GPC	growth per cycle
GS	ground state

IPA	isopropyl alcohol
MIBK	methylisobutylketone
MIGS	metal induced gap states
MOSFET	metal-oxide-semiconductor field-effect transistor
MWCNT	multi-walled carbon nanotube
NDR	negative differential resistance
ONO	oxide-nitride-oxide
PMMA	poly(methyl methacrylate)
PMMA-MMA	polymethyl methacrylate-co-methacrylic acid
PRAM	phase-change random access memory
QD	quantum dot
QPC	quantum point contact
RTD	resonant tunneling diode
SB	Schottky barrier
SEM	scanning electron microscope
SRAM	static random access memory
SWCNT	single-walled carbon nanotube
TEMA-Hf	tetrakis(ethylmethylamino)hafnium
TMA	trimethylaluminum
USB	universal serial bus
WA	working area

Contents

Chapter 1

Introduction

The story of carbon nanotubes (CNTs) began already in the 1970's and 1980's, when a chemical vapor deposition synthesis of carbon filaments (with diameter less than 10 nm) was reported [1, 2]. However, the gold rush of carbon nanotube research started about twenty years later at 1991, when S. Iijima from NEC laboratories (Japan) observed carbon nanotubes using high-resolution transmission electron microscope. These nanotubes were made of several concentric cylindrical shells spaced by about 3.4 Å [3]. Later this kind of carbon nanotubes with multiple walls became known as multi-walled carbon nanotubes (MWCNTs). Shortly after the discovery of MWCNTs, single-walled carbon nanotubes (SWCNTs) were discovered [4,5]. Even though carbon nanotubes are made with many different methods, conceptually SWCNTs can be thought to be made of a single graphite layer (a graphene sheet) that is rolled up into a hollow cylinder. The SWCNTs have quite small diameter, on the order of $1 - 2\,\mathrm{nm} = 10^{-9}\mathrm{m}$, but the length can be even centimeters [6]. In addition, the crystalline perfection of their atomic network makes them ideal systems to study phenomena related their one-dimensionality. Moreover, depending on how SWCNTs are rolled up, they can be either metallic or semiconducting, opening many possibilities for applications. In the following discussion I will be considering only single-walled carbon nanotubes.

One possible application that is studied in this thesis is the carbon nanotube field-effect transistor (CNT-FET) which is suggested as one possible candidate to continue the downscaling of conventional metal-oxide-semiconductor field-effect transistor (MOSFET) [7–9]. In the scaling of MOSFETs, their dimensions and supply voltage need to be reduced with the same factor. This increases their speed and packing density while keeping the power density the same. A number of limitations arise when the dimensions reach nanometer level. Namely, leakage current and power dissipation are increased and the channel potential control by gate bias is hindered. The CNT-FET can in prinsiple answer to these issues. The small diameter and cylindrical shape enhances the gate's ability to control the channel potential, especially in wrap-around gate configuration. This also reduces the possibility for

leakage currents. Also the power dissipation is lower in CNT-FETs due to the much lower capacitance compared to the MOSFET.

In this thesis I will be concentrating on the properties of single-walled carbon nanotubes and field-effect transistors based on CNTs. Especially, focusing on understanding and controlling the charging of the gate oxide, on the properties of CNT-FET-based memories and on introducing negative differential resistance in CNT-FETs by utilizing the charging of the gate oxide. The chapters are organized as follows. The structure and electrical properties of carbon nanotubes are described in Chapter 2. The operation principles of MOSFETs and CNT-FETs are compared in Chapter 3, especially describing the interesting phenomena arising from the 1D nature of the CNT when incorporating it to these devices. In Chapter 4, I describe the details related to the fabrication of our devices. The operation of Flash memories is described in Chapter 5, although, the focus is in understanding of the origin of hysteresis in CNT-FETs and the properties of memories made out of them. In Chapter 6, the charging of the gate oxide is used to introduce quantum dots in the CNT channel, thus producing negative differential resistance in the current vs. voltage characteristics of CNT-FETs. Also the basics of quantum dots are discussed. Finally, the conclusions are presented in Chapter 7.

Chapter 2

Electrical properties of carbon nanotubes

The production of carbon nanotubes can be done in many different ways. Most of these synthesis methods can be classified by the main technology behind the growth and divided into three groups. These are arc discharge [4, 10, 11], laser ablation [12–14] and chemical vapor deposition methods [15–18]. Both of the arc discharge and laser ablation methods generate a hot gaseous carbon from a solid carbon target after which the gaseous carbon is cooled down thus forming the CNTs [19]. In chemical vapor deposition method metal-nanoparticles catalyze the decomposition of a gaseous or volatile compounds containing carbon. The metal-nanoparticles also serve as a nucleation centers for the carbon nanotube growth [15]. This method can be easily scaled up and has become the most important commercial method for producing CNTs. Although, huge improvements have been made in synthesizing CNT since their discovery, there are still remaining four main challenges related to the carbon nanotube synthesis: (1) the development of low-cost, large-scale mass-fabrication processes for high-quality CNT synthesis, (2) Controlling the location and orientation of produced nanotubes on substrates [15], (3) fully understanding the processes involved in the nanotube growth and (4) controlling the structure and thus the electronic properties of carbon nanotubes [19]. In this chapter the discussion is concentrated on the electrical properties of carbon nanotubes arising from their structure. I will build a basic understanding of the mechanisms governing the electrical devices made out of CNTs by briefly examining the electrical properties of carbon nanotubes [20].

2.1 Structure of carbon nanotube

In order to understand the electrical properties of carbon nanotubes and the resulting characteristics of devices made out of CNTs, it is important to examine the microscopic structure of the nanotube. Since the structure of CNT is closely related to

that of graphene, which is a two dimensional single layer of graphite, we can start by viewing the lattice of graphene [21]. Nanotubes can be expressed in terms of graphene lattice vectors. Forming of a carbon nanotube can be thought to be done by rolling of a graphene ribbon to form a seamless hollow cylinder. The resulting nanotube structure in the rolling process can be specified by a pair of integers (n, m), defining the chiral vector $\boldsymbol{C}_h = n\boldsymbol{a_1} + m\boldsymbol{a_2}$ between two crystallographically equivalent sites. Here $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ are the unit vectors of the graphene honeycomb lattice, shown in Figure 2.1. The chiral vector defines the circumference of the nanotube, which gives an access to determine the diameter (d) of the CNT, as $|\boldsymbol{C}_h| = \pi d$. The chiral vector assigns a particular (n, m) to individual tube, together with its chiral angle θ defined as the angle between $\boldsymbol{a_1}$ and $\boldsymbol{C}_h$. The chiral angle is in the range of $0\,^\circ \leq |\theta| \leq 30\,^\circ$, due to the hexagonal symmetry of the graphene lattice. Nanotubes having indices $(n, 0)$ and angle $\theta = 0\,^\circ$ are called zigzag tubes, because they show a zigzag pattern along the tube perimeter. When the nanotube type is (n, n) and the angle $\theta = 30\,^\circ$, the tube is called armchair, due to the armchair pattern along the circumference. Other tube types ($n, m \neq n \neq 0$ and $0\,^\circ < |\theta| < 30\,^\circ$) are called chiral tubes (Figure 2.5).

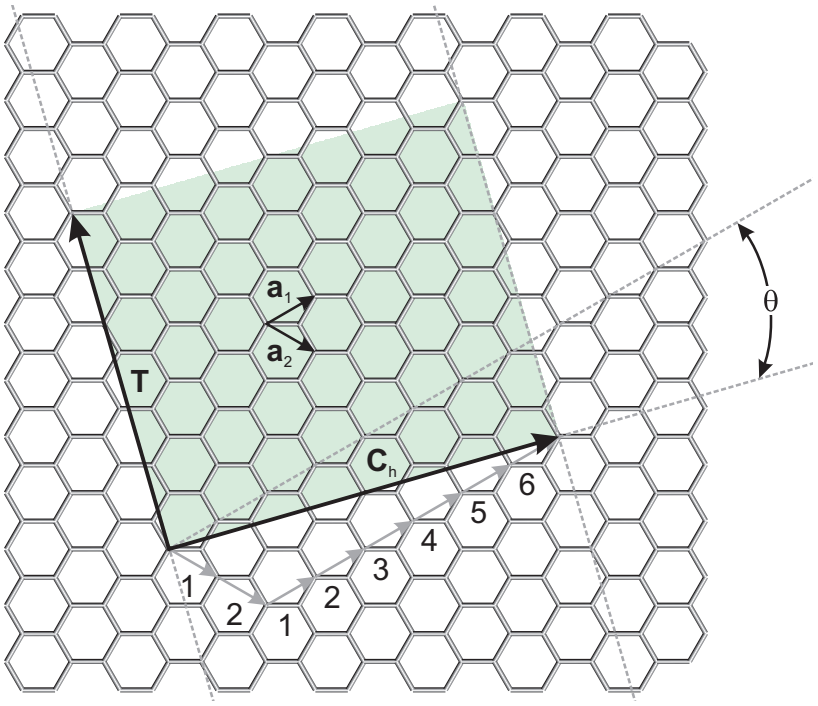

FIGURE 2.1 Graphene honeycomb network with lattice vectors. The chiral vector $\boldsymbol{C}_h = 6\boldsymbol{a_1} + 2\boldsymbol{a_2}$ shows the wrapping of the sheet in to CNT. Translational vector **T** perpendicular to $\boldsymbol{C}_h$ runs along the tube axis. The angle between $\boldsymbol{C}_h$ and $\boldsymbol{a_1}$ defines the chiral angle θ.

Carbon atoms in nanotubes exhibit sp^2 hybridization, analogous to that of graphene (Figure 2.2). Out of the four orbitals of carbon, the $2s$, $2p_x$, $2p_y$, and $2p_z$

orbitals, only three orbitals along the lattice ($2s$, $2p_x$ and $2p_y$) combine to form strong covalent bonds. These are called σ bonds, featuring occupied σ and unoccupied σ^* bands. σ bonds are responsible for most of the binding energy and mechanical and thermal properties of carbon nanotubes, e.g. high thermal conductivity [22]. The left-over p_z orbital couples with its neighboring p_z orbitals to form delocalized occupied (valence) π and unoccupied (conduction) π^* bands. The σ bands are far away from the Fermi energy (E_F) and do not contribute to the electrical conduction through the tube. In contrast, the π bands touch at six points that lie at the Fermi energy and are responsible of electronic properties of CNTs.

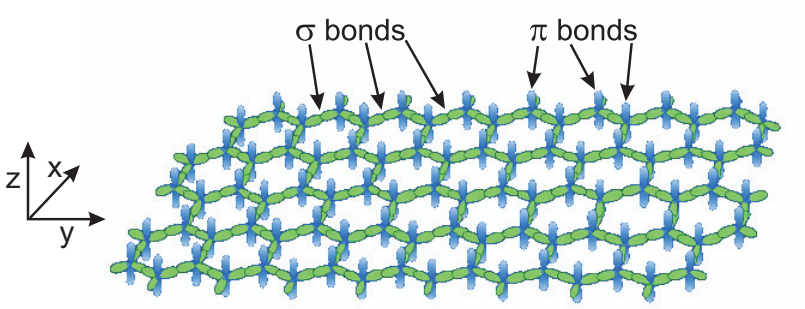

FIGURE 2.2 sp^2 hybridization of graphene sheet. The σ bonds along the surface of the sheet connect the carbon atoms and are responsible for the elastic properties and the binding energy of the graphene sheet. Perpendicular to the surface of the sheet are the π bonds which are responsible for the conduction through the tube.

Due to the hexagonal symmetry of graphene, there exists symmetry points ($M,\ \Gamma,\ K$) in the hexagonal Brillouin zone, as presented in Figure 2.3a. The electronic structure of graphene along the $\Gamma - M$ and $\Gamma - K - M$ directions is shown in Figure 2.3b. The σ bands are well separated in energy, more than 10 eV at Γ point. Since they are far away from the Fermi energy, they do not contribute to the electrical conduction through the tube. On the other hand, the first valence (π) band and the first conduction (π^*) bands cross at the K points of the Brillouin zone. Due to the hexagonal symmetry of graphene lattice, there exist two equivalent (degenerate) K points in graphene labelled K and K' points. At the K points, the density of states (DOS) goes to zero but everywhere else there is a finite DOS. This is why graphene can be considered as a semimetal or zero band gap semiconductor. At energies close to the Fermi energy, the dispersion of π and π^* bands is linear. The effective mass of a particle in a semiconductor is proportional to the curvature of the bands, graphene is said to host massless Dirac particles due to the linear relationship between energy and momentum. This explains the extremely good conductivity of graphene.

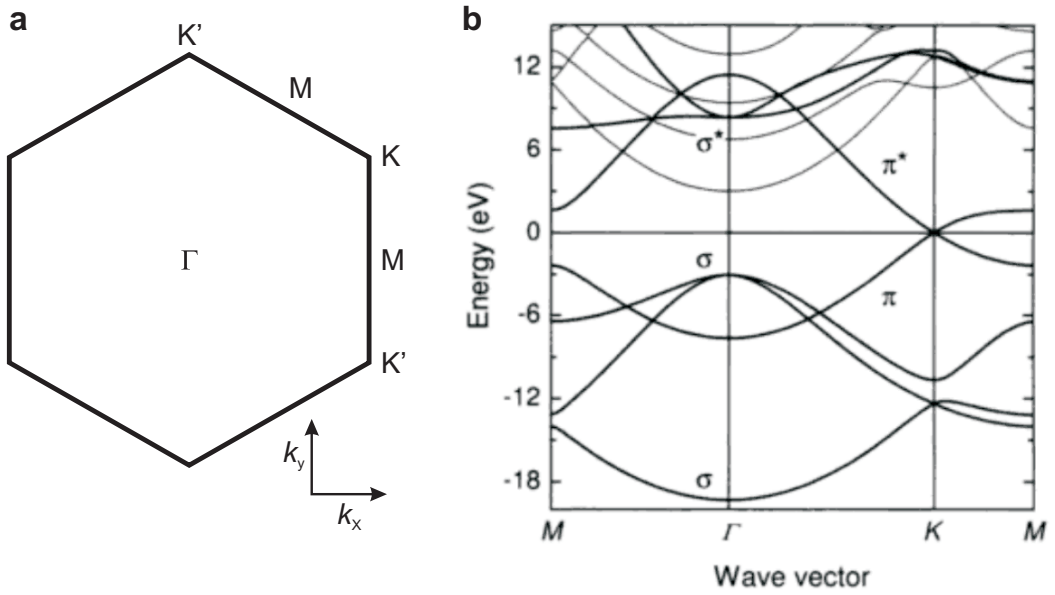

FIGURE 2.3 Electronic band structure of graphene. **a,** The Brillouin zone of graphene with the points Γ, K', M and K indicated. **b,** The band structure of graphene. The bonding π (last valence) and π^* (first conduction) bands cross at the K points of the Brillouin zone. The Fermi energy (E_F) is set at zero. Adapted with permission form [23].

2.2 Zone folding approximation

The hollow cylindrical structure of carbon nanotube induces periodic boundary conditions around the circumference of a nanotube. These boundary conditions quantize the component of momentum along the circumference ($k_\perp$) with the relation

$$\boldsymbol{k} \cdot \boldsymbol{C}_h = 2\pi\eta, \tag{2.1}$$

where η is a non-zero integer. Along the tube the wave vector ($k_\parallel$) is continuous and there are no restrictions for motion of the charge carriers. When plotting the allowed wave vectors onto the Brillouin zone of the graphene, a series of parallel lines is generated (Figure 2.4). The idea behind the zone-folding approximation is that these allowed lines are superimposed with the dispersion relation of π orbitals of graphene thus creating a discrete set of sub-bands in energy.

Depending on how the tube is rolled up, e.g. on the chiral vector $\boldsymbol{C}_h$, the tube is either metallic or semiconducting. The relation between the chirality and electronic properties of a CNT can be quantitatively seen if we consider a general (n, m) nanotube. The reciprocal lattice vectors can be defined with unit vectors as [20]

$$\boldsymbol{a}_i \cdot \boldsymbol{k}_j = 2\pi\delta_{ij}. \tag{2.2}$$

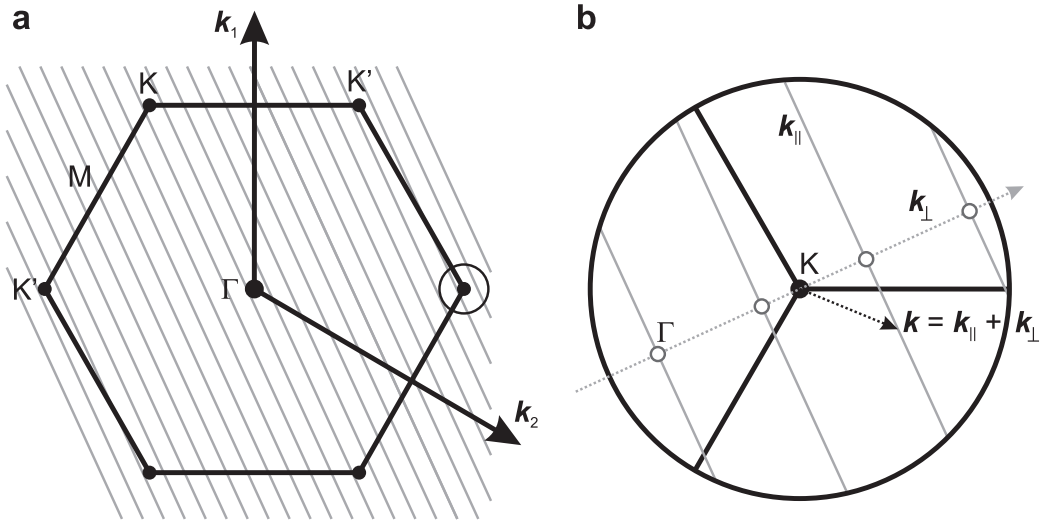

FIGURE 2.4 Allowed k-lines of a nanotube. **a,** The Brillouin zone of graphene with CNT k-lines. Also the reciprocal lattice vectors ($\boldsymbol{k}_1$ and $\boldsymbol{k}_2$) are indicated. **b,** Magnification around K point. The allowed wave vectors $\boldsymbol{k}$ consist of wave vector components $\boldsymbol{k}_\perp$ (quantized along the direction around the circumpherence of the CNT) and $\boldsymbol{k}_\parallel$ (continuous along the axis of the tube). The open dots show points where $\boldsymbol{k}_\parallel = 0$, i.e. the Γ point of the Brillouin zone of the nanotube.

For $i, j = 1, 2$, this gives $\boldsymbol{k}_1 = 2\pi\boldsymbol{a}_1 = (2\pi, 0)$ and $\boldsymbol{k}_2 = 2\pi\boldsymbol{a}_2 = (0, 2\pi)$. Now, the K point can be expressed with reciprocal lattice vectors as [23]

$$\boldsymbol{K} = \frac{1}{3}(\boldsymbol{k}_1 - \boldsymbol{k}_2) = \frac{2\pi}{3}(1, -1). \tag{2.3}$$

Thus, combining Equations 2.1 and 2.3, we get a condition for a nanotube to be metallic

$$\boldsymbol{K} \cdot \boldsymbol{C}_h = 2\pi\eta = \frac{2\pi}{3}(1, -1) \cdot (n, m) = \frac{2\pi}{3}(n - m), \tag{2.4}$$

indicating that $n-m$ must be divisible by three. All other (n, m) nanotubes are semiconducting. For example, the tube obtained by rolling a graphene sheet in Figure 2.1 would be $(6-2 \neq 3\eta)$ semiconducting. The dependence of chirality on indexes (n, m) and the resulting electronic properties of CNTs are presented in Figure 2.5. The condition for CNT to be metallic is always satisfied for armchair. The condition is valid also for the subset of $(n, 0)$ zigzag tubes with n multiples of 3, but in reality they exhibit a small band gap due to reasons explained in detail in Section 2.2.2. Metallic tubes exhibit similarities with graphene, e.g. a linear energy-momentum relation.

In the information technology applications (e.g. electronics and optoelectronics) [19] point of view, the more interesting class of tubes constitutes 2/3 of all CNTs, namely the semiconducting carbon nanotubes. The band gap (E_g) of a semiconduct-

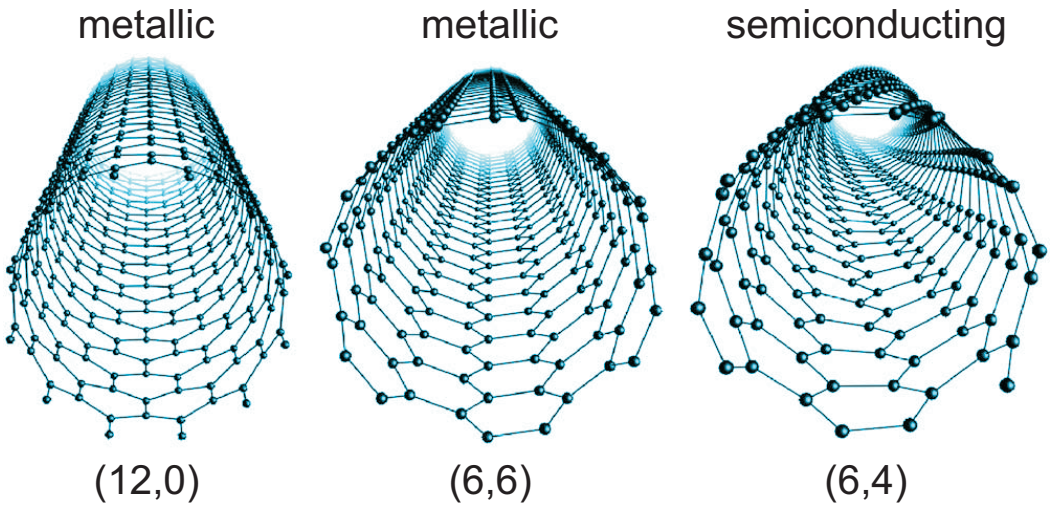

FIGURE 2.5 Carbon nanotubes with chirality vectors (n, m) assigned. From the left: Metallic zigzag, metallic armchair and semiconducting chiral CNTs.

ing CNT can be expressed as [7]

$$E_g = \frac{2a_{cc}\gamma_0}{d} = \frac{4\hbar\nu_F}{3d}, \tag{2.5}$$

where a_{cc} is the carbon-carbon bond length (1.42 Å), γ_0 is the transfer integral between first-neighbor π orbitals (having a typical value of 2.9 eV), $\hbar$ is the reduced Planck's constant ($h/(2\pi)$) and ν_F is the Fermi velocity (8.1×10^5 m/s). The dependence of the band gap on the diameter of the CNT leans on the assumption that the dispersion of the nanotube bands is linear around the Fermi energy. In reality the band gap also depends on the (n, m) indices as well, but the main contribution comes from the diameter. The position of valence and conduction band edges in energy are determined by the wave vectors $\boldsymbol{k}$ located on the allowed line closest to the K point. In the next section we will look more closely on the electronic band structure of carbon nanotubes.

2.2.1 Band structure and density of states

Due to the one-dimensionality of the nanotubes, also their Brillouin zone is one dimensional. The graphene has two π orbitals. In the zone folding model the allowed k-lines are superimposed with the dispersion relation of these π orbitals. This creates a superposition of all allowed momentum values, with two bands per k-line.

The band structures together with the density of states are shown in Figure 2.6a for (5,5) metallic armchair nanotube and in Figure 2.6b for (10,0) zigzag nanotube. As discussed above, the armchair tube is metallic with finite DOS at Fermi energy. The density of states describes the number of available states at a given energy in-

terval. The shape of DOS depends on the dimensionality of the object. For example, in 1D the density of states diverges close to the band maxima and minima. This can be seen as spikes in the DOS in Figure 2.6. These spikes are called van Hove singularities and they manifest due to the confinement along the circumference. They demonstrate the 1 dimensionality of CNTs.

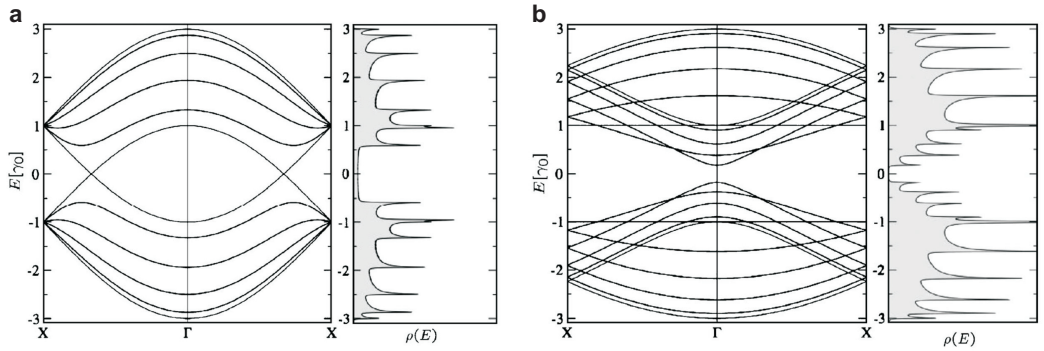

FIGURE 2.6 Band structure and density of states for **a,** a (5,5) armchair and **b,** a (10,0) zigzag tube calculated within the zone folding model and normed with γ_0. The Brillouin zone edges are here marked with X and the center with Γ. The energy bands are presented in $X - \Gamma - X$ direction. The Fermi energy is placed at zero energy. Adapted with permission from [20].

In the case of (10,0) zigzag nanotube a finite energy gap shows up at Γ. For general case of semiconducting nanotubes the band gaps are located at the Γ point. The corresponding DOS have a zero value at the Fermi energy, as shown for (10,0) zigzag nanotube in Figure 2.6. The density of states also exhibits the van Hove singularities, just as in the case of the armchair nanotube.

2.2.2 Curvature effects and tube-tube interaction

As shown earlier in Section 2.2 carbon nanotubes are not just 1D stripes but more cylinders with all carbon atoms on the surface. This cylindrical curvature induces interesting effects to the electrical properties of CNT. So far in the zone folding model the band structure of a CNT was attained by superimposing the allowed k-lines with the dispersion relation of π orbitals of planar graphene sheet. The curvature of CNT induces small deformation to the hexagonal lattice, e.g. the bond lengths and bond angles slightly change so that π and σ orbitals can mix, which was not possible in the case of planar graphene. These curvature effects shift the point where π and π^* orbitals cross away from the K points at the corners of the Brillouin zone of graphene. For armchair tubes this shift is along the $k_{\parallel}$ line that cross the K point. In the case of metallic zigzag tubes the shift is in the direction of $k_{\perp}$. This induces a secondary band gap to these zigzag tubes that scales as $1/r^2$ as shown in Figure 2.7b. Since the secondary band gap is much smaller than the primary band gap (only a

few tenths of eV), these CNTs are called small band gap nanotubes. The secondary band gap can be analytically expressed as [20]

$$E_{g2} = \frac{3a_{cc}^2\gamma_0}{4d^2}. \tag{2.6}$$

Carbon nanotubes get easily stuck together as bundles or ropes (Figure 2.8a) of tubes during the growth process or in the post-treatment. Their detaching from each other requires some effort but it can be done by ultrasonication and/or chemistry [24]. This usually does not give 100% yield and also many experiments are done with bundled CNTs [25–28]. For these reasons it is important also to understand the properties of CNT bundles.

Nanotubes in a bundle are separated by a distance so small that each nanotube can feel the potential due to all other nanotubes. The π bonds, which are perpendicular to the surface of the nanotube, are responsible for this weak interaction between CNTs in a bundle. This is similar to the weak interaction between carbon layers in pure graphite. The interactions between the tubes in a bundle opens up a band gap of $\sim$0.1 eV at the Fermi energy and drastically change the electrical properties of armchair tubes making most of the bundles somewhat semiconducting [20].

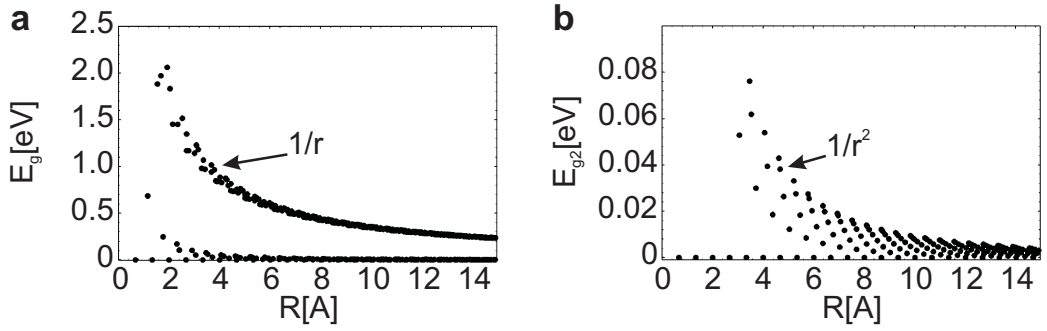

FIGURE 2.7 Comparison of the magnitudes of primary and secondary band gaps of CNTs as a function of the radius. **a,** The primary gap (E_g, top curve) scales as $1/r$. **b,** The secondary, curvature induced gap (E_{g2}) scales as $1/r^2$. The scale is expanded for the lower curve in a. The armchair nanotubes are always metallic with zero band gap corresponding to the dots at zero energy. Adapted with permission from [29].

2.3 Conductance, capacitance and inductance of carbon nanotube

Many of the electrical properties of devices can be characterized by the capacitance, inductance and resistance of the particular device. This is also true for carbon nanotubes and devices made out of them. Due to the geometrical and electrical prop-

erties of CNTs and the interaction of nanotubes with the surroundings, important implications to their electrical properties arise. We will now discuss some of the implications on the conductance, capacitance and inductance of a nanotube.

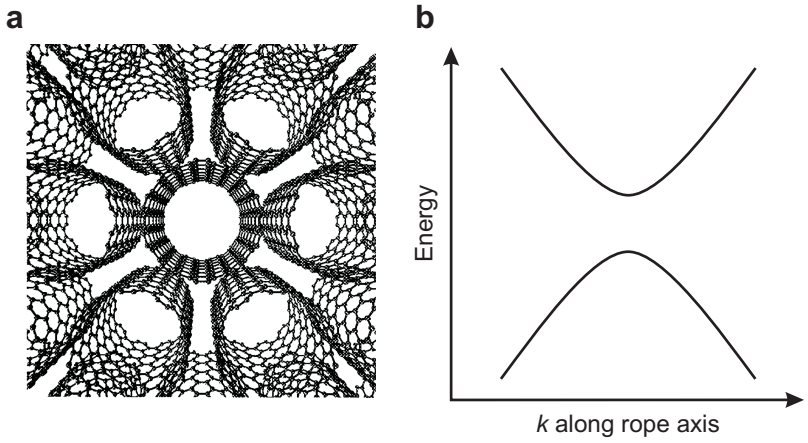

FIGURE 2.8 Carbon nanotube bundle. **a,** Schematic of a (10,10) carbon nanotube bundle **b,** Interaction between (n, n) nanotubes in a bundle results in a repulsion of the bands. Adapted with permission from [30].

2.3.1 Conductance

The current flow through the nanotube is also strongly affected by the 1D nature of the tube. The mismatch between the large number of modes in the 3D macroscopic metallic contacts and a few one-dimensional sub-bands available in the CNT leads to conductance quantization. The conductance through the tube is given by the number of available quantum channels. Each channel adds a quantum of conductance of $G_0 = \frac{2e^2}{h}$ (including spin degeneracy) to the total conductance. In addition, the total conductance needs to account all the sub-bands and additional modes taking part to the current flow. For a CNT, additional modes need to be taken into account due to the degeneracy of the graphene lattice (equivalent K and K' points). For example, at the Fermi energy or charge neutrality level (CNL) of armchair nanotubes, there are present two quantum channels. This gives a conductance value of

$$G_Q = 2G_0 = \frac{4e^2}{h}, \tag{2.7}$$

usually referred as the quantum conductance in the case of nanotubes. The corresponding resistance is $R_Q = \frac{h}{4e^2} = 6.45\ k\Omega$. If higher sub-bands take part in the conduction the conductance increases. This possibility is discussed in more detail below in Section 3.2.

In the previous approach the CNT was assumed to be perfect so that the conduction through it is ballistic (no carrier scattering in the channel) together with

transmission probability of unity at the metallic contacts. If the transmission at the Fermi level in the contacts is not perfect, the reduced probability ($T_P(E_F) < 1$) needs to be taken into account and one gets for the conductance the Landauer formula [31]

$$G(E_F) = \frac{4e^2}{h} T_P(E_F). \tag{2.8}$$

The properties of the nanotube-metal contact will be discussed more deeply in the Section 3.3 and for now we will concentrate on the conduction in the tube. The Equation 2.8 can be expressed as resistance $R = \frac{h}{4e^2}\frac{1}{T_P(E_F)}$.

The length over which a nanotube behaves as a ballistic conductor depends on temperature and the size of the driving electric field, and as mentioned, the structural perfection of the CNT. Ballistic transport can be achieved even in CNTs with lengths of a few 100 nm's. On the other hand, if there is a scattering present in the nanotube (scattering from a potential in one dimension), the resistance of the CNT can be expressed as [32]

$$R = \frac{h}{4e^2}\frac{1}{T_P(E_F)} = \frac{h}{4e^2} + \frac{h}{4e^2}\frac{1 - T_P(E_F)}{T_P(E_F)} = \frac{h}{4e^2} + \frac{h}{4e^2}\frac{R_P(E_F)}{T_P(E_F)} = R_Q + R_{sc}, \tag{2.9}$$

where $R_P(E_F) = 1 - T_P(E_F)$ is the reflection probability that causes a voltage drop in the CNT and R_{sc} is the resistance from a scattering collision in the nanotube.

In long CNTs, or at high bias, many scattering collisions can take place. This is called diffusive transport and it is typical to conventional conductors. The resistances given by single scattering collisions R_{sc} are additive and the total resistance is a series connection of resistances for every momentum relaxation length λ_m. In the diffusive limit, for N collisions, the Equation 2.9 can be expressed as [32]

$$R = \frac{h}{4e^2} + \frac{h}{4e^2}\sum_i^N \frac{R_{P\_i}(E_F)}{T_{P\_i}(E_F)} \sim R_Q + NR_Q\frac{R_{P\_avg}(E_F)}{T_{P\_avg}(E_F)} = R_Q + R_{Classical}, \tag{2.10}$$

where $R_{P\_avg}(E_F)$ and $T_{P\_avg}(E_F)$ are the respective average reflection and average transmission probabilities for an individual scattering collision within a momentum relaxation length λ_m. Since the resistance $R_{Classical}$ depends on the length of the nanotube L, it can be thought of as the Ohm's law in one dimension. When $\lambda_m \ll L$, the classical resistance dominates. On the other hand, in the ballistic limit $\lambda_m \gg L$ and Equation 2.10 reduces to the quantum resistance R_Q.

2.3.2 Capacitance

The capacitance of a carbon nanotube can be divided into two components: The quantum capacitance (C_Q) is related to the density of states of the tube and the electrostatic capacitance (C_E) arises from the coupling of the CNT to the surrounding

conductors and depends on the dielectric structure and the geometry of the surroundings.

When an electron is added to a 1D conductor, a finite energy is required to get the electron in the next available quantum state. This energy per unit length in a nanotube can be calculated as [33,34]

$$\delta E' = \frac{\delta E}{\delta N(E)} = \frac{1}{D(E_F)L} = \frac{h\nu_F}{8L}, \tag{2.11}$$

where $N(E)$ is the total number of states with energy less than E, $D(E_F)$ is the density of states, h is the Planck's constant and ν_F is the Fermi velocity (8.1×10^5 m/s) of CNT. The quantum capacitance is caused by this energy addition related to the 1D density of states of the CNT [33]. For each mode in the CNT a quantum of capacitance need to be added similarly as in the case of conductance. When spin and lattice degeneracy is taken into account, the quantum capacitance per unit length when adding an amount of charge $\delta Q = \delta N(E)e$ has the form of [34]

$$C_Q = \frac{1}{L}\frac{\delta Q}{\delta V} = \frac{1}{L}\frac{\delta Q}{\delta(E/e)} = e^2 D(E_F) = \frac{8e^2}{h\nu_F}, \tag{2.12}$$

where e is the electron charge. The quantum capacitance is small, and experimentally measured to be in the order of 10^{-16} F μm^{-1} [35]. For semiconducting carbon nanotubes the quantum capacitance is not quantized (as in the case of metallic CNTs) but rather continuous [36–38].

If a nanotube is placed on a conducting substrate with a dielectric between the CNT and the substrate, an electrostatic gate capacitance (C_G) is introduced. This gate capacitance per unit length has the form of [39]

$$C_G \approx \frac{2\pi\varepsilon\varepsilon_0}{ln(\frac{4h}{d})}, \tag{2.13}$$

where d is the nanotube diameter, h and ε the thickness and the average dielectric constant of the dielectric, and ε_0 is the dielectric permittivity. When a nanotube is placed in a field-effect configuration, also the capacitances of the source (C_S) and drain (C_D) electrodes connected to the CNT need to be taken into account to get the full electrostatic capacitance of the system as

$$C_E = C_S + C_D + C_G. \tag{2.14}$$

The total capacitance has both the quantum capacitance and electrostatic capacitance components in series and has the form of [40]

$$\frac{1}{C} = \frac{1}{C_Q} + \frac{1}{C_E}. \tag{2.15}$$

2.3.3 Inductance

A magnetic field is induced around the conductor when current flows through it. When the current changes also the magnetic field changes and in turn induces a current and an electromotive force (EMF) that opposes the initial change in the current. This EMF is related to the initial change in the current through magnetic inductance (L_M) [41]. This is the classical part of the inductance of nanotubes, and it has a form [42]

$$L_M = \frac{\mu_0}{2\pi} ln \left(\frac{4h}{d} \right), \tag{2.16}$$

where $\mu_0 = 4\pi \times 10^{-7}\ \mathrm{H/m}$ is the permeability of vacuum.

At the electronic level, an additional inductance exists that can be thought as a resistance to the change of the kinetic energy of the electrons in the CNT. This is called the kinetic inductance and it makes the electron velocities lag in phase with respect to the external driving field [7]. In ballistic CNTs the kinetic inductance is proportional to the density of states and can be thought of as quantum inductance (L_Q) similar as in the case of the quantum capacitance. First, we consider the average excess energy of electrons in bias window [43]:

$$\delta E = \frac{1}{2} \left(\mu_S - \mu_D \right), \tag{2.17}$$

where μ_S is the electrochemical potential of the left lead and μ_D is the electrochemical potential of the right lead with equilibrium Fermi energy E_F. Using Equation 2.11, the number of electrons in the bias window is

$$\delta N = \frac{1}{2} D(E_F) \left(\frac{\mu_S - \mu_D}{2} \right), \tag{2.18}$$

where a factor of $1/2$ is included since only right moving carriers contribute to the current. From Equations 2.17 and 2.18, we obtain the excess kinetic energy in the nanotube

$$E_K = \delta N \delta E = \frac{1}{8} D(E_F) \left(\mu_S - \mu_D \right)^2. \tag{2.19}$$

When taking into account the spin and lattice degeneracies, the current in the ballistic CNT is given by

$$I = \frac{V}{R_Q} = \frac{4e^2}{h} \left(\frac{\mu_S - \mu_D}{e} \right) = \frac{4e}{h} \left(\mu_S - \mu_D \right), \tag{2.20}$$

giving the excess kinetic energy the form of

$$E_K = \frac{h^2 I^2 D(E_F)}{128 e^2}. \tag{2.21}$$

Equating 2.21 and the inductive energy $L_Q I^2/2$, the kinetic inductance becomes

$$L_Q = \frac{h^2 D(E_F)}{64e^2}. \tag{2.22}$$

Using Equation 2.11 we obtain the kinetic inductance of the nanotube per unit length [43, 44]

$$L_Q = \frac{h}{8e^2 \nu_F}. \tag{2.23}$$

In normal wires, the magnetic inductance is usually significantly larger than the kinetic inductance due to short electron collision time that makes the ohmic resistance to dominate below frequencies of $\sim 10^{13}$ Hz [45]. In CNTs, on the other hand, the kinetic inductance is larger than the self inductance for all frequencies. Since the total inductance is a combination of the two inductances in series as $L = L_Q + L_M$, the larger inductance dominates. The value of the kinetic inductance in the case of CNTs is $L_Q \approx 4$ nH μm^{-1}, while the L_M is more than four orders of magnitude smaller. A ballistic nanotube would behave like a lossless transmission line in response to AC signal, with the characteristic impedance of $Z_0 = \sqrt{\frac{L}{C}}$ [42, 46]. Thus, the kinetic inductance is important in the high-frequency applications of nanotube transistors.

Chapter 3

Carbon nanotube field-effect transistors

The history of transistors began when the point-contact transistor was invented by John Bardeen, Walter Brattain and William Shockley at Bell Telephone Laboratories in 1947. This discovery brought the Nobel Prize in physics to the inventors in 1959. The first integrated circuit was demonstrated in 1958 containing two bipolar junction transistors (BJT), although the researchers at Bell laboratories had already learned how to make working field-effect transistors. It took still more than ten years before the modern metal-oxide-semiconductor field-effect transistor (MOSFET) was used in integrated circuits and finally in 1971 the first microprocessor was announced by Intel [47]. The downscaling of MOSFET has enabled modern high-speed, low-cost, highly integrated microprocessors and helped us to attain the modern way of living with e.g. personal computers, virtual environments and magnitude of different applications requiring microprocessors. This down scaling will continue with the current design type of MOSFET well into the next decade, but ultimately new transistor technologies need to found to continue miniaturization [48]. Carbon nanotube is one of the suggested materials to continue this downscaling. Field-effect transistors made from carbon nanotubes (CNT-FETs) feature many desirable attributes like ballistic transport over considerable distances. Due to the cylindrical form of the CNT it enables the ideal transistor, a "gate-all-around" transistor, and large ON/OFF ratios. CNT-FETs are also amenable to band-to-band tunneling which could provide high subthreshold slopes, leading to faster transistors with lower dissipated power. In this chapter, I will discuss the above-mentioned attributes of CNT-FETs. The role of the nanotube-metal contact, how CNT-FETs are usually made and also some more novel CNT-FET designs together with integrated circuits made with CNT-FETs will be discussed.

3.1 Operation of a metal-oxide-semiconductor field-effect transistor

In a conventional MOSFET the switching of current through the device is produced by modulation of electric fields. A MOSFET has three terminals (electrodes). Two of these, called source (S) and drain (D), are connected to the semiconducting channel. A third metal gate (G) electrode is separated from the semiconducting channel by an oxide layer and the modulation of the current is done with the gate. A schematic of a p-type MOSFET is shown in Figure 3.1a. Negative voltage applied to the gate (V_G) electrode creates an electric field that induces a positive charge near the semiconductor surface. These mobile positive charges form an inversion layer called the "channel" to the n-type substrate, shown in Figure 3.1b. For this to happen, there is a threshold voltage (V_T) that the gate voltage needs to exceed. Beyond this threshold voltage, V_G is used to control the number of induced positive charges and the conductivity of the channel.

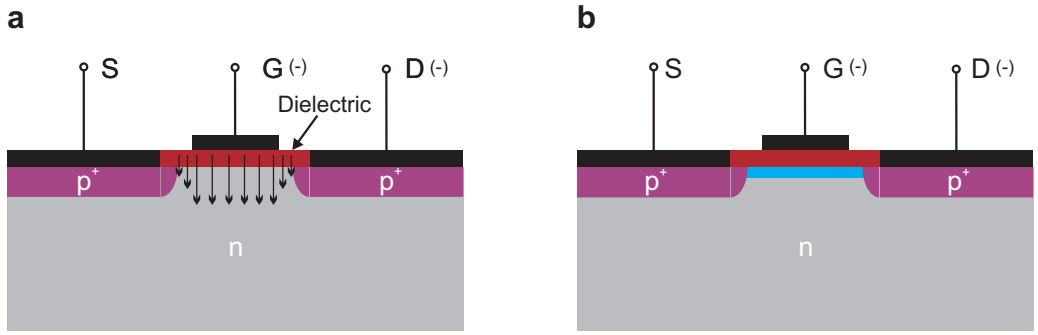

FIGURE 3.1 A schematic of a p-type MOSFET transistor. **a,** Negative voltage applied to the gate (G) induces an electric field pulling positive charges near the surface of the semiconductor. **b,** When a bias voltage ($V_{DS} = V_D - V_S$) is applied between the source (S) and the drain (D) electrodes, the current can flow through the device.

When a negative drain-source voltage (V_{DS}) is applied the current starts to flow through the transistor. For small drain-source voltages, the current through the transistor is dependent on the magnitude of V_{DS} and resembles a resistance. Thus this region is called the ohmic region. The situation changes when V_{DS} is large. When further increasing the V_{DS}, the voltage drop between the gate and the drain electrode decreases. This reduced potential difference results in a fewer inversion charges on the drain side of the channel and the channel is in pinch-off. This causes the current to increase much more slowly and the current depends almost solely on the gate voltage. Therefore this region is called the saturation region [49]. The output characteristics of a p-type MOSFET are shown in Figure 3.2.

A few important physical device parameters, called figures of merit, can be

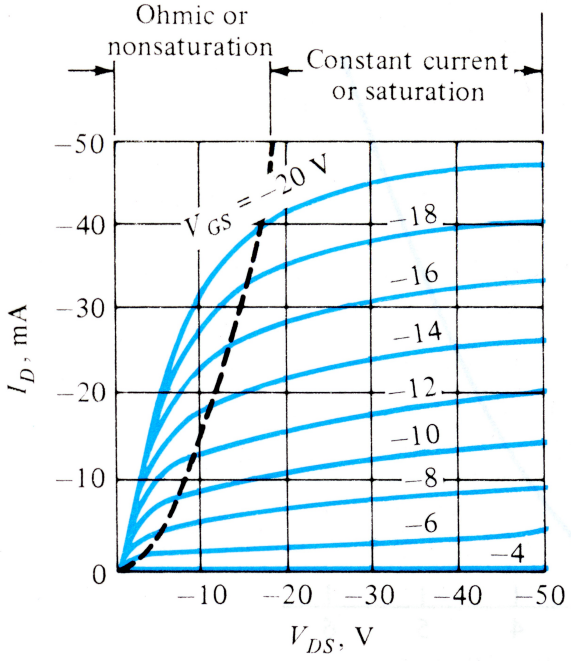

FIGURE 3.2 Output characteristics of a p-MOSFET showing usual operation with negative voltages. The current in the saturation still grows slowly. This is due to channel length modulation, an effect analogous to the Early effect in bipolar junction transistors. Adapted with permission from [49].

used to describe the performance of a transistor, namely the ON/OFF ratio, the subthreshold slope and the carrier mobility. The ratio between the ON and OFF current of a transistor is given as the ON/OFF ratio. This parameter gives information about how well the transistor closes e.g. how small the OFF state current is, which relates to gate leakage and band-to-band tunneling.

The inverse subthreshold slope gives valuable information about the switching behavior of the transistor. It describes the change in drain-source current (I_D) induced by the modulation of the gate voltage (V_G) when the transistor is operated with gate voltages below the threshold. The subthreshold current is caused by thermal emission of electrons over the conduction band (n-FET) or valence band (p-FET) of the semiconductor and it has an exponential dependence on the V_G. In an ideal case, the subthreshold slope does not depend either on the gate to channel coupling or the drain-source voltage, but the exponent depends only on temperature (T) [50]. The inverse subthreshold slope is defined as [9]

$$S = \frac{\partial V_G}{\partial(logI_D)} \approx \frac{k_B T}{e} ln(10), \tag{3.1}$$

where k_B is the Boltzmann constant and e is the elementary charge. The subthreshold slope shows how easily small changes in V_G increase the current when the tran-

sistor is in OFF state. At room temperature S = 60 $\frac{\mathrm{mV}}{\mathrm{dec}}$ and with decreasing temperature the subthreshold slope also decreases.

To be able to get faster microprocessors the size of the transistor needs to continuously become smaller. The operation speed of a transistor is primarily limited by the internal RC time constants, where the capacitance is directly proportional to the geometry and the dielectric structure of the transistor. On the other hand, to be able to get high currents for small dimension transistors, high carrier mobility is necessary. For silicon MOSFETs, the usual mobility for electrons is about $\mu = 1300\ \frac{cm^2}{Vs}$ and the hole mobility is about $\mu = 500\ \frac{cm^2}{Vs}$ [49]. So, for a transistor having the same dimensions, n-MOSFET has more than twice the ON current of a p-MOSFET. For a comparison, CNT-FETs can have hole mobilities up to $79000\ \frac{cm^2}{Vs}$ [51].

3.2 Operation of a carbon nanotube field-effect transistor

An enhancement of current through a semiconductor requires an activation of charge carriers over the band gap (e.g. heat or light absorption) or modulation of the band gap by an external factor, such as doping [52–54], applied strain [55], magnetic field [56] or electric field as in the common field-effect transistors. The first carbon nanotube field-effect transistors were demonstrated by Tans *et al.* [57] and was soon followed by other groups at IBM [39] and Stanford [58]. Up to date the field has expanded continuously from research of intrinsic properties of CNT-FETs to making advanced CNT-FET structures and even integrated circuits [7–9].

A typical conventional CNT-FET is shown in Figure 3.3. A carbon nanotube is connected to metallic drain and source electrodes. The current through the tube is monitored while modulating it with the gate voltage connected to the silicon wafer. The most commonly used dielectric layer is $\mathrm{SiO_2}$ but also other types of oxides can be used, e.g. $\mathrm{HfO_2}$.

The output characteristics of a typical p-type CNT-FET are shown in Figure 3.4a resembling those of p-type MOSFET having ohmic and saturation regions. The two curve sets belong to the same device. The difference between them is the exchanging of the source and drain. Exchanging the source with drain is not the same as reversing the polarity of V_{DS}, since the gate voltage breaks the field symmetry. If the current saturation would be caused by channel pinch-off as in the case of MOSFET, this difference could not exist. This feature is one evidence of Schottky barriers between the CNT and the metal electrode, which are described in more detail on the next section.

As mentioned earlier, carbon nanotube field-effect transistors are amenable to bipolar behavior [60–62] (see Section 3). This is illustrated in Figure 3.4b exhibiting transfer characteristics with large ON/OFF ratio of 10^5 attainable in CNT-FETs.

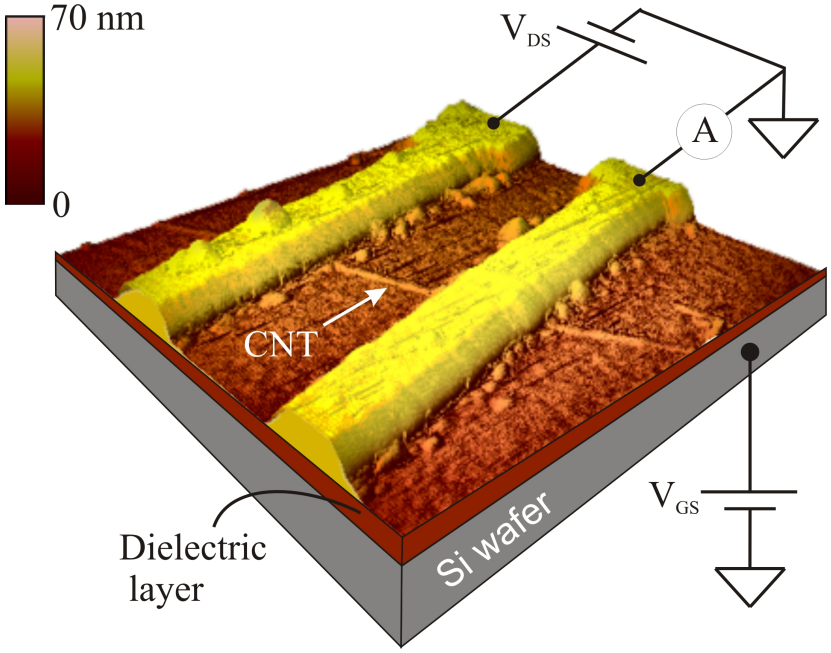

FIGURE 3.3 An atomic force microscope (AFM) image of a typical CNT-FET studied in this thesis together with a schematic of a measurement setup. The drain and source electrodes are connected to a semiconducting carbon nanotube and the current through the tube is modulated with the gate voltage connected to the silicon wafer.

Starting from a negative gate voltage, the current first decreases until it becomes immeasurably small and finally increases again. This shows that the Fermi level of the system is successively shifted from the valence band (Figure 3.5b) through the band gap (Figure 3.5c) to the conduction band of the nanotube (Figure 3.5d), and the transfer characteristics displays both p-type and n-type conduction [59]. This bipolar behavior originates from the valence and the conduction bands of the CNT both taking part in the conduction through the transistor. The change in the electric field required to achieve this bipolarity depends on the band gap of the tube, initial Fermi level placement and the gate capacitance.

In addition to the bipolar behavior, CNT-FETs have also other differences compared to conventional MOSFETs. At a given V_{DS}, the profile of energy bands in CNT-FETs is determined by V_G and the total capacitance (C) of the device. As mentioned earlier (see Section 2.3.2), the total capacitance has two contributions: electrostatic capacitance (C_E) and quantum capacitance (C_Q) that are coupled in series. In a conventional CNT-FETs $C_E \ll C_Q$ and the electrostatic capacitance is controlling the total capacitance. This is also true for conventional MOSFETs, where the ability of the gate to control the potential in the channel is limited once V_G exceeds the threshold voltage. The potential in the channel no longer rises since the increased charge pulled into the channel by an increase in V_G cancels the potential increase [9]. In a scaled down CNT-FETs the case is different. There $C_E \approx C_Q$ or even $C_E > C_Q$

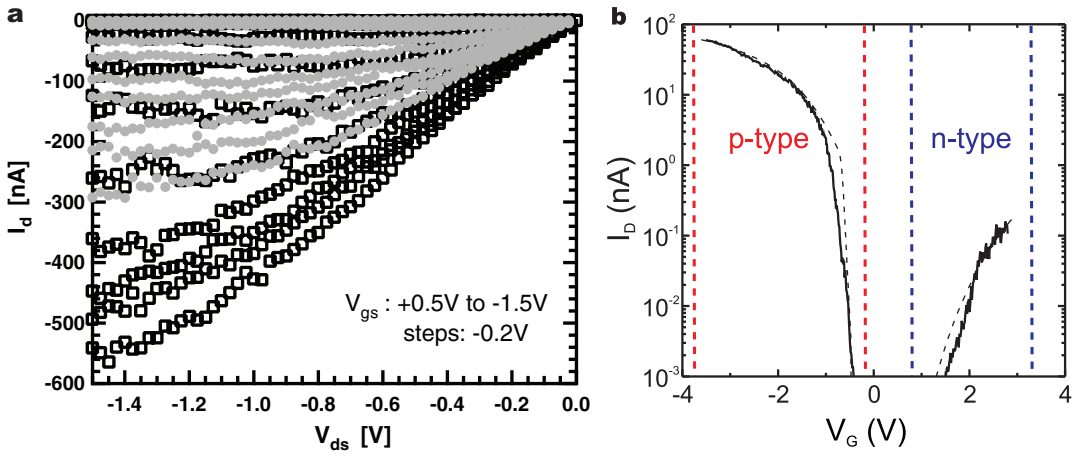

FIGURE 3.4 Electrical characteristics of conventional CNT-FETs. **a,** Output characteristics of a p-type CNT-FET having a channel length of 300 nm. The silicon wafer was used as a backgate and between the gate and the CNT there was 20 nm of HfO_2. The two curve sets belong to the same device while exchanging the source and drain electrode. Adapted with permission from [50]. **b,** Transconductance of an Al gated CNT-FET with $V_{DS} = 5\,mV$ measured at room temperature in vacuum of $\sim 10^{-4}$ mbar. The carrier doping of the semiconducting nanotube can be changed from p-doped to n-doped. Adapted with permission from [59].

and the quantum capacitance can be dominant. In this situation, gate can still control the potential in the CNT channel when the device is in ON-state. Thus, higher conduction bands can be pulled below the Fermi level of the source electrode [63].

3.3 Carbon nanotube-metal contact

In order to study the intrinsic transport properties and the performance limits of carbon nanotubes, it is important to form ohmic contacts without any significant scattering or energy loss of the carriers at the source/drain interfaces. Already at the time of the first CNT-FETs the necessity of ohmic contacts to the carbon nanotube was recognized and research on the contact properties began.

3.3.1 Schottky barriers

According to the Schottky-Mott theory, when a metal and a semiconductor is brought in contact, the difference in the work function of the metal (ϕ_M), and the electron affinity (EA) of the semiconductor (χ_S) determines a barrier height (called Schottky barrier) for charge carriers [64]

$$\phi_{M-S} = \phi_M - \chi_S. \tag{3.2}$$

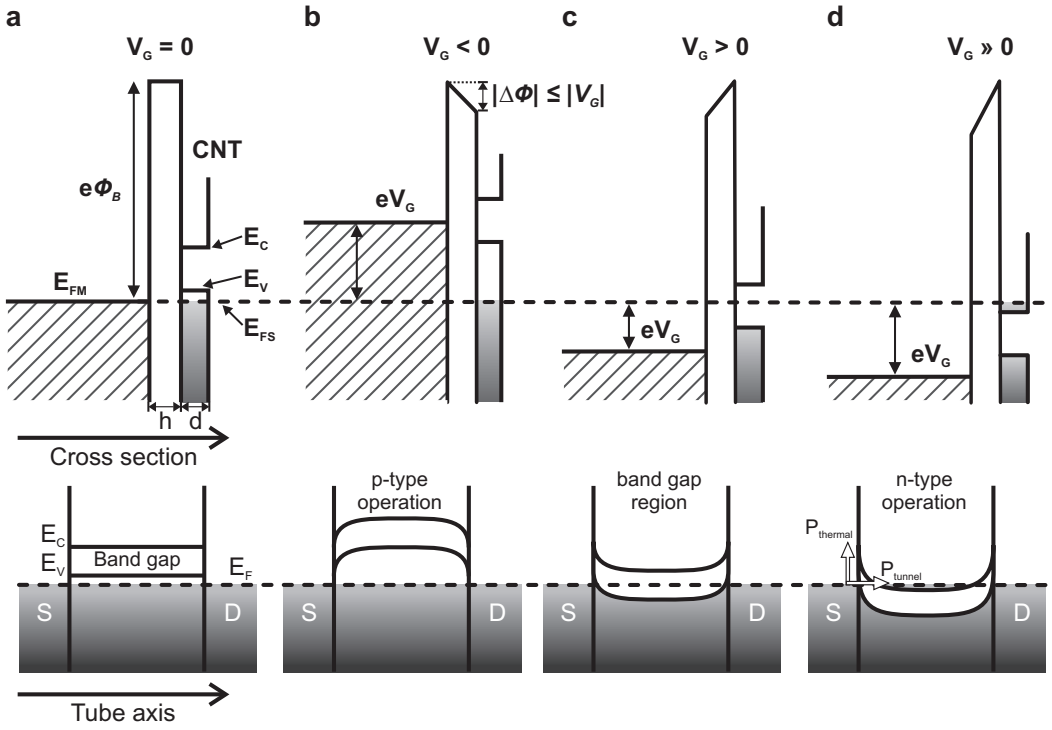

FIGURE 3.5 Operation of a CNT-FET. A cross section perpendicular to the device is shown on top and a schematic along the device on bottom. **a,** we assume that there is no built-in potential due to the work function difference between the nanotube and the gate conductor. The Fermi levels (E_F) of the system align and there is no voltage drops in the dielectric. A nanotube of diameter d is connected with Pd source (S) and drain (D) electrodes and separated from the gate by a dielectric with thickness h. The potential barrier for electrons to cross the dielectric from the gate conductor is ϕ_B. Initially, the Fermi level of the system lies in the valence band (E_V) of the CNT and the nanotube is p-doped. Already a small drain-source voltage makes the current flow through the device. **b,** A negative voltage applied to the gate increases the conduction through the tube since the nanotube becomes more positively charged. **c,** When applying a positive gate voltage, the Fermi level is driven into the band gap and the CNT is depleted from carriers. Now the conduction can only happen as a result of thermally excited carriers ($P_{thermal}$). **d,** Further increasing the gate voltage drives the Fermi level in the conduction band (E_C) and n-type conduction becomes possible. The main mechanisms for n-type conduction are tunneling from metal electrode states to conduction band states (P_{tunnel}) and thermal activation of electrons over the barrier. Since the band gap is inversely proportional to diameter, both conduction types become more relevant in large-diameter nanotubes. The larger barrier for n-type carriers explains the experimentally observed lower n-type conduction compared to p-type conduction.

The Schottky barrier forms in the vicinity of the junction due to equalization of the chemical potentials that induces bending of the valence and conduction bands (Figure 3.6). In p-type devices the Schottky barrier (SB) height is determined for

holes and in n-type devices for electrons. However, in traditional semiconductor-metal contacts the SB height has a much weaker dependence on the metal work function than is expected from the Schottky-Mott theory. This is known as Fermi level pinning and there are several different theories developed that try to explain the pinning phenomenon [65]. One of the most popular theory is the metal induced gap states (MIGS) model. At the metal-semiconductor interfaces, the metal induces gap states, which result in planar dipoles due to charge transfer at the interface and pin down the Fermi level making SB heights nearly independent of the contact metal work function [66]. It has been theoretically predicted that for MIGS to induce any pinning of the Fermi level in a metal-CNT contact, their density needs to be very large in CNTs [67]. In end-bonded CNTs even for strong pinning the width of the depletion area is only nanometers, and will result in a barrier height which is determined only by the metal work function and the CNT band gap [68], as in Equation 3.2. This enables the control of the barrier height by an appropriate choice of contact metal work function, just as if there were no pinning and no interface dipole. Recently, in Pd contacted CNT-FETs the Schottky barrier heights were found to follow the size of the CNT band gap indicating little or no influence of Fermi level pinning [69].

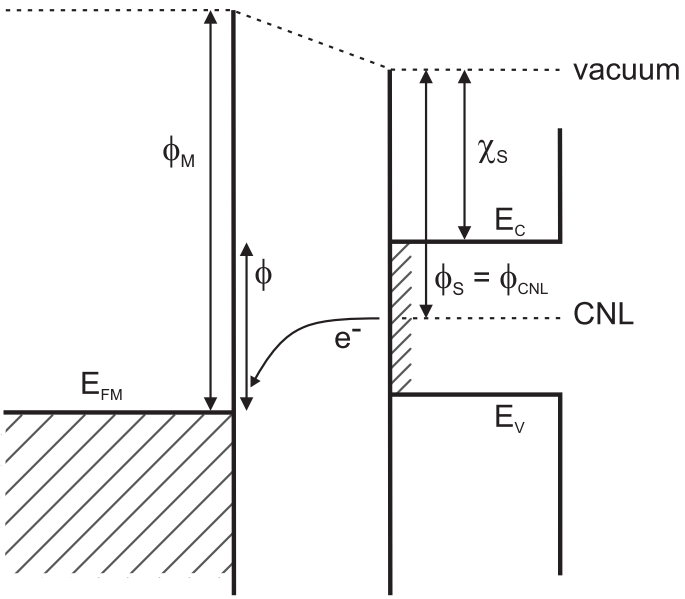

FIGURE 3.6 Schematic of the charge transfer in the Schottky barrier.

Typically, carrier transport through the metal-CNT interface is dominated by quantum mechanical tunneling through the Schottky barrier rather than thermally activated emission over the Schottky barrier (Figure 3.5d) [61,70,71]. Therefore, the thickness of the Schottky barrier becomes critical. The thickness of the Schottky barrier can be modified by external electric fields. In sufficiently short nanotube transis-

tors the modulation of Schottky barrier can be used for the transistor operation [61].

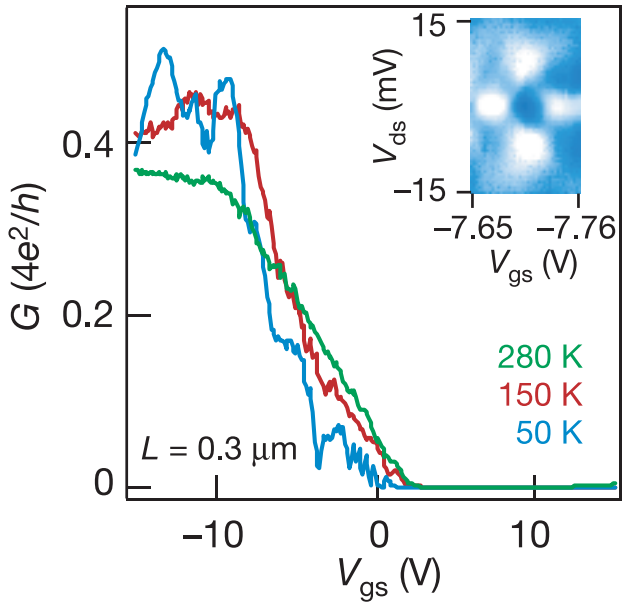

FIGURE 3.7 Conductance versus V_G for a 300 nm long CNT-FET at various temperatures. In the inset, a differential conductance plot of dI_{DS}/dV_{DS} versus V_{DS} and V_G at $\mathrm{T} = 1.5$ K shows a Fabry-Perot like interference pattern with bright peaks $G \approx 0.5 \times 4e^2/h$ and dark region $G \approx 0.4 \times 4e^2/h$. Adapted with permission from [72].

The existence of barriers between semiconducting CNTs and the metal contact together with the correlation between the CNT diameter and the barrier height were first reported by Zhou *et al.* [73]. The first nearly zero SB contacts to the valence band of intrinsic semiconducting nanotubes with diameters $d \gtrsim 1.6$ nm (band gap $E_g \lesssim 0.5$ eV) were reported by Javey *et al.* [72]. They found that with palladium (Pd) the ON-state exhibits metallic-like behavior, as the low drain-source bias conductance linearly increases with decreasing temperature (Figure 3.7). Below 50 K pronounced Fabry-Perot interference oscillations appear having a peak conductance close to the quantum conductance limit of $G_Q = 4e^2/h$, as shown in the inset of Figure 3.7. This corresponds to ballistic transport in the p-type semiconducting CNT. The interference pattern shows that the nanotube acts as coherent electron waveguide, with the resonant cavity formed between the two nanotube-electrode interfaces. The Fabry-Perot interference forms when electron waves multiply reflected between two nanotube-metal interfaces interfere with each other [74]. The V_G modulates the Fermi level position and the charge density in the nanotube. This in turn gives electrons, propagating in the two π and π^* bands, different phase shifts as they travel a round trip in the nanotube. The phase change as a function of electron energy is responsible for the interference patterns as a function of V_{DS} and V_G [75] as shown in the inset of Figure 3.7.

Similarly to the Schottky barrier height calculation for metal-semiconductor interfaces (see Equation 3.2) also the band line-ups for semiconductor-oxide interface can be calculated by the Schottky barrier theory. To do this, we first generalize the Schottky barrier Equation 3.2 which was given for metal-semiconductor interface without a charge transfer. Generally though, there is some charge transfer between the metal and semiconductor interface states lying in the band gap, as shown in Figure 3.6. This charge transfer creates a dipole (e.g. like in the MIGS model), which reduces the electron Schottky barrier height to

$$\phi_{M-S} = S_P(\phi_M - \phi_S) + (\phi_S - \chi_S), \tag{3.3}$$

where ϕ_S is the energy of semiconductor interface states below the vacuum level and S_P is so called Schottky pinning parameter. Empirically S_P was found to depend on the electronic part of the dielectric constant (ε_∞) of the semiconductor according to [76–79]

$$S_P \simeq \frac{1}{1 + 0.1(\varepsilon_\infty - 1)^2}. \tag{3.4}$$

The pinning parameter S_P is characteristic of the semiconductor. There are two limits for S_P. When there is no charge transfer and thus no dipole, $S_P = 1$ and the Equation 3.3 reduces to the Equation 3.2. For the well screened and strongly pinned case, the metal Fermi level is pinned by the charge transfer to ϕ_S and $S_P = 0$.

The energy of semiconductor interface states below the vacuum level (ϕ_S) can be thought as broken surface bonds that are dispersed as dangling bond states across the band gap of the semiconductor, or as evanescent states of the metal wave functions continued into the forbidden energy gap of the semiconductor. The ϕ_S is then the charge neutrality level (ϕ_{CNL}) of these interface states, defined as the energy above which the states are empty for a neutral surface [66, 76]. The CNL is the balance point of the weights of the valence and conduction band density of states. A high density of states in the valence band tends to push the ϕ_{CNL} towards the conduction band and vice versa.

To be able to apply this theory to semiconductor-oxide interface, we treat the oxides as wide band gap semiconductors. This way the interface of an oxide and a semiconductor can be treated as an interface of two semiconductors 'a' and 'b'. The band alignment between two semiconductors depends on the charge transfer, just as in the case of Schottky barriers in metal-semiconductor junction. The charge transfer across the interfacial bonds creates a dipole, which modifies the band line-up according to [78, 79]

$$\phi_{S-S} = (\chi_a - \phi_{CNL,a}) - (\chi_b - \phi_{CNL,b}) + S_P(\phi_{CNL,a} - \phi_{CNL,a}), \tag{3.5}$$

where S_P depends on the ε_∞ of the wider gap material. The band line-up is now

described by matching the charge neutrality levels of each semiconductor, modified by the S_P parameter. Again, as in the metal-semiconductor interface, the band alignment for strongly pinned case is just given by the alignment of the two charge neutrality levels.

3.3.2 Contact with different metals

As mentioned earlier, the barrier height can be controlled with the choice of contact metal work function ϕ_M [80], which is the difference of the vacuum level energy and the Fermi level of the material. Some work functions for metals typically used to contact CNTs are listed in Table 3.1. For nanotubes, the work function is approximately ϕ_{CNT} = 4.8 eV , close to that of graphite [81]. If metals have work functions outside the range of $\phi_{CNT} \pm E_G/2$ of nanotube, the contacts should be ohmic. This is the case for metals having $\phi_M < 4.5$ eV or $\phi_M > 5.1$ eV. For example, palladium falls outside this range and therefore it forms an ohmic contact to the valence band of a CNT (Figure 3.5a).

TABLE 3.1 Work function ranges of metals used in CNT-FETs [82].

Metal	Work function
Al	4.06 - 4.26
Au	5.1 - 5.47
Ni	5.04 - 5.35
Pd	5.22 - 5.6
Pt	5.12 - 5.93
Sc	3.5
Ti	4.33

In reality the barrier depends also on the atomic configuration of the contact [83], explaining the different ON currents in p-type CNT-FETs contacted with metals having similar work functions (e.g. Pd, Au or Pt) [72, 84]. Nevertheless, n-type CNT-FETs have been demonstrated with low work function metals, e.g. Al or Sc [85, 86], and a diode behavior with CNT-FET having metallic source and drain electrodes of different work function [87]. The operation of the CNT-FET can also be influenced in-situ by metal work function modulation, thus modulating the Schottky barrier height. For example, the surface work function of Pd can be reversibly modified upon exposure to molecular hydrogen or oxygen [61,72,84]. These results provide a clear experimental proof of the lack of Fermi level pinning at the interfaces and demonstrates the large sensitivity of the Schottky barrier height on the work function of the metal contacts.

The behavior of conventional CNT-FET transfer characteristics is nearly independent on whether the reason for current increase is band gap or Schottky barrier

modulation [88]. The difficulty in determining which one is actually dominating in the nanotube is creating much discussion. It is generally agreed that the Schottky effect is present in large band gap CNTs at all times which makes for example the mobility determination from the slope of the I_D *vs* V_G curves no longer appropriate.

3.4 Advanced carbon nanotube field-effect transistors and integrated circuits

The conventional CNT-FET design with global backgate is no longer sufficient when trying to scale down CNT-FETs and incorporate carbon nanotubes into logic gates. Since the first CNT-FETs, a number of different CNT-FET designs have been implemented, attempting to optimize their performance. First local gated devices were produced by Wind *et al.* [89]. They also showed later a significant improvement to the subthreshold slope of local gated devices having p-doped source and drain sections of the same CNT, compared to a global gated device [90]. The thermionic emission limited subthreshold slope of 60 mV/dec was first achieved with a double gated CNT-FET, where a global backgate selectively thinned the Schottky barriers in the contacts while a central gate was independently used to modify the band structure in the middle of the CNT-FET [91]. With further improving the same design, values below the thermal limit were achieved. In a device incorporating band-to-band tunneling (Figure 3.8), p-n junction tunneling barriers between the valence and conduction bands of the CNT could be controlled with the central gate voltage. This produced an inverse subthreshold slope of ∼40 mV/dec [92].

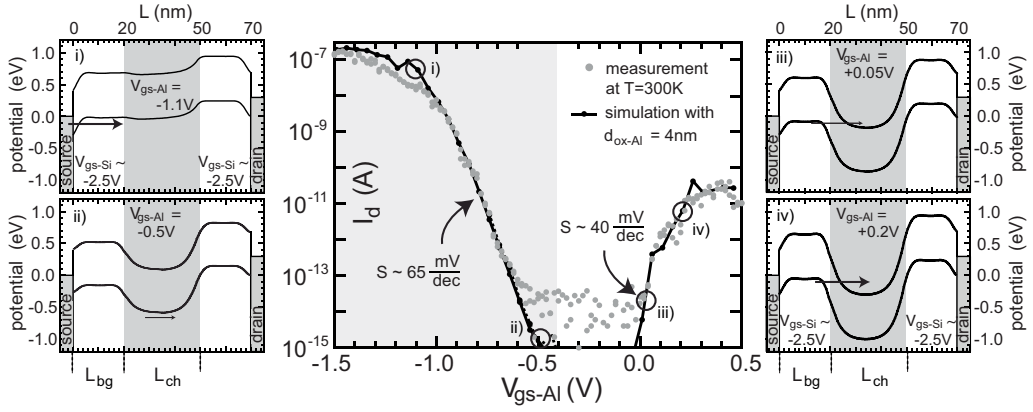

FIGURE 3.8 Transfer characteristics of a double gated CNT-FET. For negative gate voltages the device shows S ∼ 65 mV/dec. For positive gate voltages the device incorporates band-to-band tunneling with S ∼ 40 mV/dec. On the left and right side of the figure band profiles for the respective operation modes are shown. Adapted with permission from [9].

First CNT-FET with patterned gate of Al were fabricated by Bachtold *et al.* [59]. Using multiple CNT-FETs together with off-chip resistors, they could simulate a variety of logic elements, e.g. inverter, NOR gate, SRAM and a ring oscillator. Soon this was followed by other designs showing logic gates [27,86,93–95]. To build these circuits energy-efficiently, pairs of n- and p-type transistors in complementary-MOS architecture is preferred. This design was used to fabricate a ring oscillator on a single CNT by controlling the polarity of transistors with the gate metal work function. The gate metal for p-FET was Pd and for n-FET Al. Frequency response of the ring oscillator shows a strong dependence on the bias voltage. With a supply voltage of about 1 V a signal of about 400 μV and 72 MHz was measured (Figure 3.9a).

Technologically the most relevant are the alternating current properties of CNT-FETs, although so far most of the work has been concentrated on their direct current properties. It has been theoretically proposed that the unity-current-gain frequency (f_T) of a CNT-FET operating in the ballistic regime and in the quantum capacitance limit approaches a maximum value of $\nu_F/2\pi L \sim$ 130 GHz/L (μm) [96]. However, directly measuring alternating current performance of a CNT-FET is very difficult since the capacitance is typically in the range of aF/μm and the input impedance is much higher than 50 Ω. Experimentally f_T of a 300 nm channel-length CNT-FET has been shown to be 50 GHz [97]. The observed behavior was determined by the parasitic capacitances of the setup. This again underscores the need for the optimization of the CNT-FET and the whole circuit before the unique properties of the nanotube can be effectively utilized.

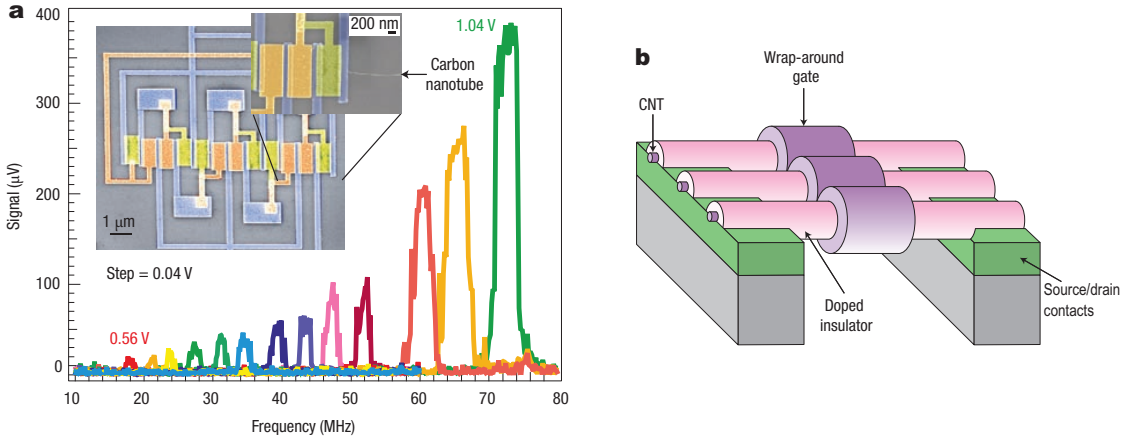

FIGURE 3.9 **a,** A ring oscillator circuit based on a single nanotube showing the change in ringing frequency as a function of the supply voltage. The supply voltage is increased from 0.56 V to 1.04 V in 0.04 V steps. **b,** A schematic of an array of nanotube transistors with wrap-around gates and doped drain-source extensions. This could be one way of optimizing the nanotube transistor structure. Adapted with permission from [7].

One possible way in trying to optimize the structure of a CNT-FET is shown in Figure 3.9b. A wrap-around gate configuration together with a thin oxide optimizes the electrostatic capacitance so that the condition $C_E > C_Q$ is fulfilled. This allows an optimum coupling between the gate and the channel, so that the gate can control the potential of the channel in the ON-state and the use of higher conduction bands in the transport through the device is possible. Furthermore, doped insulator wrapped onto the source and drain extensions of the tube gives a possibility to electrostatically dope these sections to n-type and p-type, respectively. This can be used to induce band-to-band tunneling in the device. With these optimizations, a high ON-state performance together with extremely steep inverse subthreshold slopes ($S \ll 60$ mV/dec) can be attained [9].

Chapter 4

Fabrication of carbon nanotube field-effect transistor memory devices

The nearly perfect, quasi-one-dimensional, crystalline structure of carbon nanotubes (CNTs) make them promising candidates to extend the down-scaling of electronic components beyond the limitations of present Si-based technology (see Section 3). They can in principle replace both active components as well as their interconnects, since they feature both semiconducting and metallic transport properties. For CNT-FET-based memories, a suggested integration level of up to 10^{12} cm^{-2} could be achieved [98], which is about four orders of magnitude higher density than in current technology. But there are many challenges with incorporating CNTs into logic devices, such as being able to separate a certain chirality semiconducting CNTs from the metallic ones [24, 99–103] and to control their placement with high accuracy [104–107].

Another challenge is that CNT-FETs are known to frequently display undesirable hysteresis in their transfer characteristics between the forward and reverse sweeps of V_G (see Section 5.2.1). This hysteresis allows the device to function as a memory cell. For this purpose the hysteretic behavior of a CNT-FET is a favorable feature and could be utilized in the fabrication of memory elements. In this chapter, I will describe high-yield fabrication techniques to control the reproducibility of the hysteresis phenomenon in CNT-FETs (papers A.I, A.II and A.III of this thesis). These techniques enabled 100 ns operation speed of a CNT-FET memory element, fastest CNT-based device reported to date (paper A.IV of this thesis). With a novel gate oxide design, phenomena related to negative differential resistance can also be studied (paper A.V of this thesis).

4.1 Atomic layer deposition of gate dielectrics

A chemical vapor deposition (CVD) technique called atomic layer deposition (ALD) is a powerful tool, capable to conformally coat complex shapes with a high qual-

ity material layer. With ALD, it is possible to manufacture inorganic material layers with precisely controlling the thickness down to a monolayer. These capabilities make ALD unique among thin-film deposition techniques, and as a consequence ALD-grown materials [108–110] are used in a wide range of applications [111], from electroluminescent displays [112] to microelectronics and phase-change memories [113–118], even nanoelectronics [94, 119–122].

Atomic layer deposition is based on successive reactions from the gas phase to the substrate to produce thin films and overlayers in the nanometer range. The film deposition is surface-controlled, self-terminating, gas-solid reaction which consists of repeating the following four separate steps. In step (1), the substrate is exposed to gas phase precursor molecules (precursor 1) which ideally adsorb as a monolayer on the surface. In step (2), excess of precursor 1 that is still in the gas phase is removed by inert purging gas. In step (3), the substrate is exposed to gas phase precursor 2 which reacts with the adsorbed precursor 1 to form a layer of desired material on the surface. In step (4), excess of precursor 2 and the reaction by-products are removed by purging. These four steps constitute a reaction cycle that is illustrated schematically in Figure 4.1. Each reaction cycle adds a given amount of material to the surface and is referred to as the growth per cycle (GPC). This reaction cycle is repeated until the desired thickness of the desired material is obtained [111].

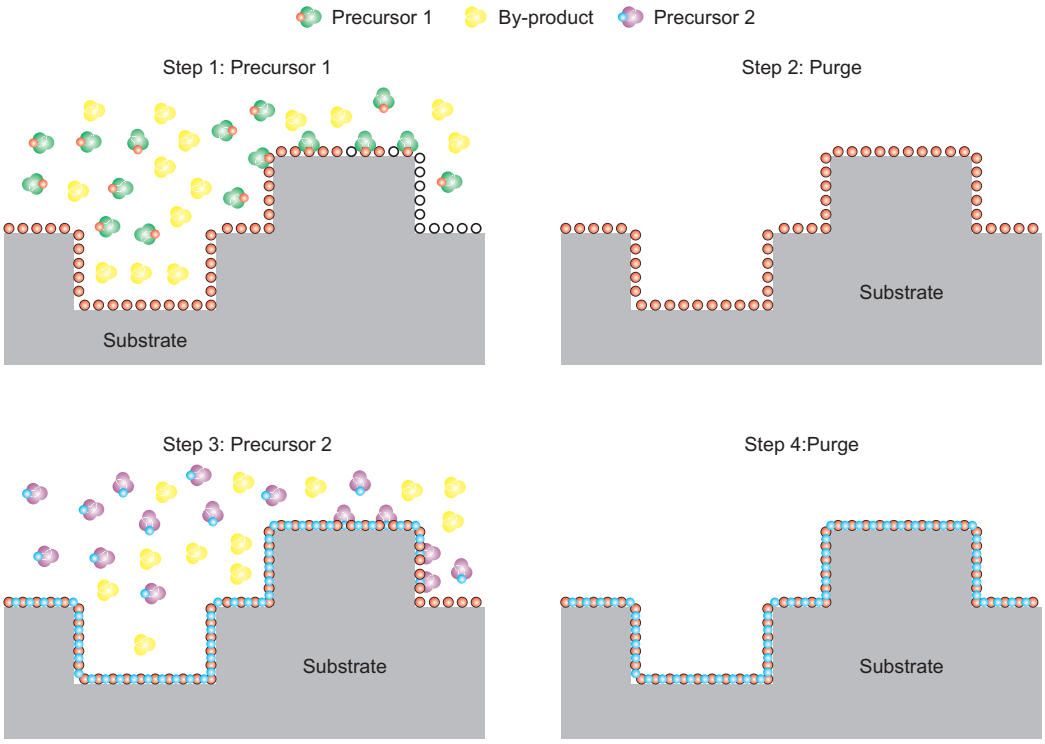

FIGURE 4.1 A schematic of one ALD reaction cycle.

When starting the ALD growth process, the surface is first stabilized to a known

controlled state. This can be done, for example, by a heat treatment or chemical modification of the surface. Because the reactions are surface-controlled and self-terminating, other process parameters than the reactants, substrate, and temperature have little or no influence to the growth. Due to the surface control, ALD-grown films are extremely conformal and uniform in thickness [123].

Carbon nanotubes are structurally chemically extremely inert and lack the functional groups on the surface needed for their conformal and uniform coating by ALD. This is why first experiments used chemically functionalized CNTs as templates to grow ALD layers on them [120,124,125]. Also other types of functionalizations are used, e.g. functionalization with DNA results in enhanced nucleation and growth of the high-κ oxide $\mathrm{HfO_2}$ by ALD at 90 $^\circ\mathrm{C}$. The thickness of the high-κ gate oxide could be pushed down to $2-3$ nm, which makes it possible to approach the ultimate vertical scaling limit of nanotube FETs [121].

Our devices were built on a highly boron-doped Si wafer. All ALD depositions were carried out on top of the wafer without removing the native $\mathrm{SiO_2}$ layer from the surface, by Beneq Oy (Vantaa, Finland), using a Beneq P400A ALD deposition tool. This thesis is based on studies were ALD grown gate oxides of $\mathrm{Al_2O_3}$, $\mathrm{HfO_2}$ and/or $\mathrm{TiO_2}$ were used. In paper A.III of this thesis, we used these three oxides as gate dielectrics together with the combination of $\mathrm{HfO_2-TiO_2-HfO_2}$, all grown at 300 $^\circ\mathrm{C}$. Gate oxide of $\mathrm{HfO_2-TiO_2-HfO_2}$ was also used in paper A.II of this thesis. The precursors used for $\mathrm{HfO_2}$ growth were hafnium tetrachloride ($\mathrm{HfCl_4}$) and water. For the single $\mathrm{HfO_2}$ layer the thickness of 20 $\pm$ 1 nm, and the refractive index of 2.05 $\pm$ 0.01, was measured with Rudolph Research AutoEL III ellipsometer with an excitation wavelength of 632.8 nm. This method produces amorphous $\mathrm{HfO_2}$ having the refractive index specified for $\mathrm{HfO_2}$ in the literature which shows that the quality of the oxide is good [126]. Precursors used for $\mathrm{TiO_2}$ growth were titanium tetrachloride ($\mathrm{TiCl_4}$) and water. The nominal thickness of this layer was in all studies 0.5 nm. For $\mathrm{Al_2O_3}$ growth, the precursors were trimethylaluminum ($(\mathrm{AlMe_3})_2$) or the abbreviation TMA and water, with a nominal thickness of 20 nm.

In paper A.IV of this thesis, the previously described single 20 nm $\mathrm{HfO_2}$ layer grown at 300 $^\circ\mathrm{C}$ using hafnium tetrachloride ($\mathrm{HfCl_4}$) and water as precursors, was used as a gate dielectric. Another $\mathrm{HfO_2}$ layer with nominal thickness of 20 nm was used as a passivation layer on top of the device. This passivation layer was grown at a lower temperature of 100 $^\circ\mathrm{C}$ from precursors of tetrakis(ethylmethylamino)hafnium (TEMA-Hf) and water. In paper A.V of this thesis, an ALD deposition of the first 20 nm $\mathrm{HfO_2}$ layer was done at 300 $^\circ\mathrm{C}$ using hafnium tetrachloride ($\mathrm{HfCl_4}$) and water as precursors. Subsequently an e-beam lithography step (see Section 4.2) was done to open squares in poly(methyl methacrylate) with 495,000 molecular weight dissolved in anisole (495PMMA A 3%, purchased from MicroChem Corp., Newton, USA) with nominal dimensions of 150×150 nm. Then another ALD deposition together with a lift-off procedure was performed to produce more than 20 000 ALD

islands comprising of $TiO_2 - HfO_2$, having nominal thicknesses of 0.5 nm and 1 nm, respectively. The use of the structure is explained in more detail in Section 6.3. The precursors used were titanium tetrachloride ($TiCl_4$) and water for TiO_2 growth, and TEMA–Hf and water for HfO_2 growth, both done at a deposition temperature of 100 °C. The pressure was ∼0.5 mbar and N_2 was used as a carrier gas in all the processes.

4.2 Fabrication of carbon nanotube field-effect transistors

Our CNT-FETs were fabricated in a bottom-up approach as described in paper A.I of this thesis. A highly boron-doped silicon substrate serving as a backgate was covered with a thin dielectric layer. The emphasis was made on developing fabrication techniques which are compatible with the use of nanometer thin dielectric materials as the gate insulator film, grown by the atomic layer deposition technique (see Section 4.1). In addition, reference devices on a highly boron-doped Si substrate, covered with a thermally grown SiO_2 layer with a thickness of ∼300 nm, have been fabricated.

Two positive resist layers were used in our experiments for covering the substrate as a mask. As a first layer, the wafer was uniformly coated by spinning with polymethyl methacrylate-co-methacrylic acid dissolved in ethyl lactate (PMMA-MMA EL 3%, purchased from MicroChem Corp.) or poly(methyl methacrylate) with 495,000 molecular weight dissolved in anisole (495PMMA A 3%) using a rotation speed of 3000 rpm for the time period of 50 sec. Then the second resist layer of poly(methyl methacrylate) with 950,000 molecular weight dissolved in anisole (950PMMA A 2%, purchased from MicroChem Corp.) was spun on top with a rotation speed of 6000 rpm for a period of 50 sec. The resist was soft baked on a hot plate at 160 °C for 3 min after each deposition layer. Standard electron beam lithography and subsequent evaporation of Ti/Pd was used in order to fabricate a 6×6 alignment mark matrix surrounded by 28 electrodes, as seen in Fig. 4.2. In total, the patterned structure measures 2.5×2.5 mm. The alignment marks were around 650 nm long with a separation of 7 μm between them (see Figure 4.2d).

Patterning of this structure was carried out with a Raith e–line electron–beam writer (equipped with Elphy Quantum 4.0 –lithography software) with an acceleration voltage of 20 kV and a dose of ∼200 – 220 $\mu A/cm^2$. The patterned structure was exposed using two different working areas (WA). The smaller features (alignment marks and inner electrodes) had a WA of 500 μm and exposure was carried out with a beam aperture size of 30 μm. For the larger structural elements (outer electrodes and bonding pads) 2500 μm WA and 120 μm beam aperture size were used. For all exposures the write field was 500 μm. The working distance was near 6 mm. The

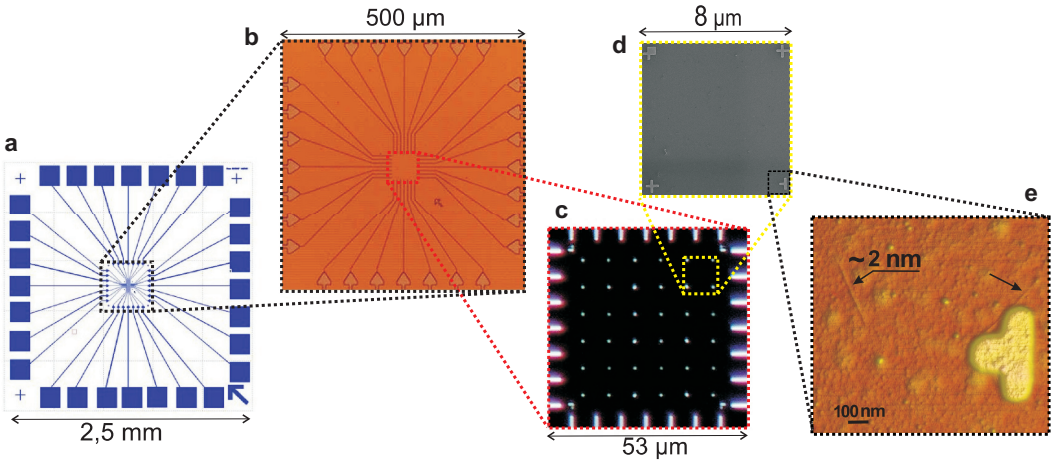

FIGURE 4.2 Overview of the patterned design. **a,** Optical microscope image of the overall design (2.5×2.5 mm). **b,** Enlarged optical microscope image of the fabricated structure, including inner electrodes and a matrix of alignment marks (500×500 μm area). **c,** Enlarged optical microscope image of a 6×6 alignment mark matrix in the middle of the structure (53×53 μm area). **d,** Enlarged scanning electron microscope (SEM) image of four alignment marks (8×8 μm area). **e,** Enlarged AFM image of two CNTs located close to an alignment mark. Adapted with permission from the paper A.I of this thesis.

spot size of the focused electron beam was estimated to be in the range of 10 – 40 nm, which allows to perform an accurate exposure with a good linewidth control.

After exposing the desired pattern with the electron beam, the resists were developed. For the PMMA resists (950PMMA and 495PMMA), a 1:3 solution of methylisobutylketone:isopropyl alcohol (MIBK:IPA) was used for ∼40 – 50 sec. For the PMMA-MMA EL 3% resist, a 2:1 solution of methanol:methoxyethanol for 5 sec was used. The development step was followed by washing the chip with IPA and drying under a nitrogen flow. A bilayer technique of depositing two layers of resist was applied for creating a so-called undercut profile, which is due to an increased developing of the more sensitive bottom layer (PMMA-MMA EL 3% or 495PMMA A 3% in our case), helpful during the lift-off process.

After the development process, two metal layers, 5 nm Ti (evaporation rate ∼0.15 nm/s) and 25 nm Pd (evaporation rate ∼0.12 nm/s) were thermally evaporated using Balzers Evaporator System. The Ti layer was evaporated below the Pd layer in order to improve adhesion of the latter. Lift-off was carried out in acetone for about 15 min. The sample was washed with IPA and dried under a nitrogen flow. Figure 4.2a-d shows an overview of the patterned design, giving a close-up look at the smaller structural elements.

Subsequently deposited CNTs were precisely located with respect to the alignment mark matrix using an atomic force microscope. Figure 4.2e shows two CNTs mapped in the vicinity of one of the alignment marks. In our studies, either com-

mercial CNTs (purchased from a CNT producing company NanoCyl, Sambreville, Belgium) or CNTs produced by a hot wire generator (HWG) method (from Helsinki University of Technology (HUT), NanoMaterials group) were used. The original powder–like NanoCyl CNTs (with an average diameter of 2 nm), produced via catalytic carbon vapor deposition process, were first dispersed in a 1,2-dichloroethane suspension and then deposited onto the substrate after a mild sonication for 10 – 15 min. CNTs from HUT were produced by an aerosol method by means of introducing catalyst particles, formed by a hot wire generator, into a laminar flow reactor, where suitable conditions for the nanotube formation were maintained. An electrostatic filter was used for the separation of individual (electrically neutral) CNTs from bundled ones (charged). CNTs of an average diameter of $\sim$1.4 nm and length of $\sim$1 μm were deposited onto the substrate, directly from the reactor without any suspension [127].

After mapping the locations of the CNTs with an AFM, Pd source and drain electrodes (25 nm thick) were fabricated on top of the selected CNTs by a second e-beam lithography step with the processing parameters similar to the ones used for the primary pattern. An AFM image of a typical fabricated device is shown in Figure 3.3. Since the sample processing incorporates two steps of electron beam lithography, nanometer scale accuracy in spatial alignment between the consecutive layers is important. We have achieved an alignment precision of a few tens of nanometers. Finally, thin Au wires were carefully bonded to the contact pads at the end of each electrode in order to electrically connect the device terminals to the measurement setup.

Chapter 5

Properties of carbon nanotube memories

In the past decade the semiconductor industry has continuously grown, with ∼10 billion dollar revenues at 1996 to ∼20 billion dollar revenues at 2009 [128]. A large section of the industry is the semiconductor memories, which can be divided into the following two branches, both based on the complementary metal-oxide-semiconductor field-effect transistor technology [129]. (1) Volatile memories, like static random access memory (SRAM) and dynamic random access memory (DRAM). Volatile memories are very fast in writing and reading (SRAM) or very dense (DRAM) but both lose their data content when the power supply is turned off. (2) Nonvolatile memories, like erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM) or Flash memory. These memories are slower in operation in comparison to volatile memories. The advantage in these memories is the capability to retain their data content even without power supply. These memories suffer from the same scaling limits as MOSFET circuits and the current trend of downscaling will also eventually stop. In addition to these traditional semiconductor memories there are many new types of memories [130–133] that try to continue the downscaling beyond traditional memory designs. Examples of these are e.g. phase-change random access memory (PRAM), where the material has two different stable and distinct phases [115, 116], or charge trap Flash, where the charges responsible for changing the state of a bit are stored in multilayer dielectric gate stack instead of floating polysilicon gate as in the traditional Flash memory [133, 134].

Carbon nanotube field-effect transistors often display some degree of hysteresis in their transfer characteristics. For a CNT-FET this is an unwanted feature, rendering it unpredictable in its output, and it has motivated several studies to find ways to prevent or remove hysteresis [135–139]. On the other hand, the presence of hysteresis opens up a possibility to use them as a memory cell. In this section, I will discuss the properties of conventional Flash memory together with the idea behind

charge trap flash. However, the main focus of this chapter is on the properties of carbon nanotube memories based on CNT-FETs, where we are trying to understand the reasons for the hysteresis and how we can control it. Finally, I will show some results of figures of merit for CNT-FET memories, especially the speed of CNT-FET memories with the proper choice of gate and passivation oxides, and try to build a model of the operation. The discussion is based on papers A.II, A.III and A.IV of this thesis.

5.1 Basics of Flash memory

The most important phenomenon of this past decade in the field of semiconductor memories has been the explosive growth of the Flash memory production, driven by USB drives, cellular phones and other types of electronic portable equipment (laptops, palm computers, MP3 audio players, digital cameras, and so on). Today there are two types of Flash memory architectures [140]: common ground NOR Flash, which is used for code execution and data storage due to its versatility, and more commonly used NAND Flash [133], that is optimized for data storage having the smallest cell size among the semiconductor memory devices commercially available [130].

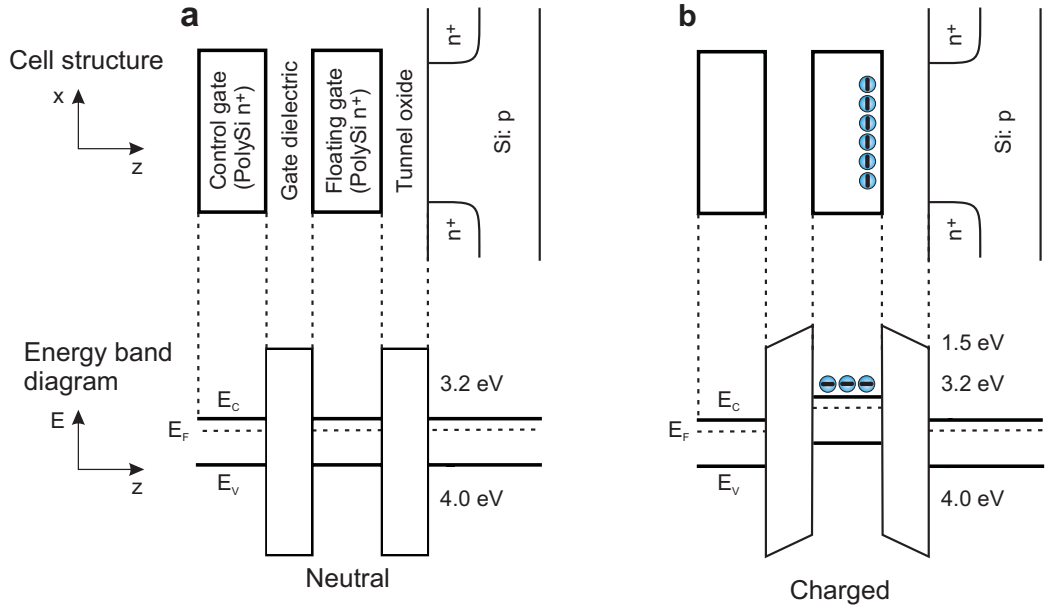

FIGURE 5.1 Schematic cross section of a Flash cell together with a schematic energy band diagram of the floating gate MOSFET. **a,** Neutral cell corresponding to bit "1". **b,** Negatively charged cell corresponding to bit "0".

Both Flash architectures are based on the same kind of cell, so called floating-gate MOS transistor. A schematic of the cell together with a corresponding energy

band diagram is shown in Figure 5.1. The cell is comprised of source, drain and control gate electrodes, just like a MOSFET, but between the control gate and the channel there exists a polysilicon island completely surrounded by dielectric [110] called a floating gate (FG). The floating gate is electrically governed by the capacitively coupled control gate (CG). Due to electrical isolation of the FG, it acts as a charge storing electrode for the memory cell. The charge injected to the FG is maintained there, allowing a capacitive modulation of the V_T (see Section 3.1) and, thus, causing hysteresis to the transfer characteristics. The quality of the dielectrics guarantees the nonvolatility and the different thicknesses of gate and tunnel dielectrics allow the possibility to Write and Erase the cell by electrical pulses. Usually the dielectric between the channel and the FG is a thin oxide, called the tunnel oxide, and the dielectric between the gates is considerably thicker to allow electrical integrity of the device [129].

The energy band diagram for a Flash cell is presented in Figure 5.1. It can be seen that the FG acts as a potential well for the charge. Once the charge has tunneled to FG, the tunnel and the gate dielectrics form potential barriers that keep the charge stored in the FG. When the charge is stored in the floating gate by applying a positive voltage to the control gate, the threshold voltage of the device changes. When the charge is erased from the FG by negative gate voltage, the threshold of the device returns to its original value. This phenomenon is called hysteresis. Together with the change in V_T in the I-V characteristics of the device, also the current through the device changes. The change in current is used to read the state of the memory, with high current representing bit "1" (Figure 5.1a) and a low current representing bit "0" (Figure 5.1b) [140].

In addition to the speed of the memory, there are two parameters that describe how "good" and reliable the memory cell is. Endurance tells the capability of the cell to maintain the stored information after many Erase/Write/Read cycles. Retention shows the capability of the cell to keep the stored information in time. As the Flash cells are scaled down, the performance in terms of endurance and retention is becoming weaker. The high electric fields required for the Write and Erase operations are making the strict leakage requirements for long term charge storage difficult, since the gate dielectrics are getting thinner and there should not be any charge transfer between the FG and the CG during Write and Erase operations [141]. Also, as the spacing between adjacent floating gates reduces, the FG to FG coupling increases. Thus the data stored in one cell can influence the operation of an adjacent cell. Non-conductive floating gate structures, where the floating gate is replaced by a dielectric, are being actively investigated in the industry as ways to replace the floating gate [141]. These are called charge trapping memories and they offer advantages for scaling flash memories. Charge trapping memory cells are usually based on a n-MOSFET transistor with a multilayer dielectric serving as gate dielectric and charge storage layer. The most common multilayer dielectric used is so called oxide-

nitride-oxide (ONO) stack where the cell is written by channel hot electron injection into the nitride layer [133]. Otherwise, the operation principle in these memories is similar to that of a Flash memory.

5.2 Hysteresis in carbon nanotube field-effect transistors

Since the first demonstration of an electro–mechanical carbon nanotube memory [98], there have also been reports of CNT-FETs showing memory effects [119, 138, 142–150]. These effects are based on hysteresis in their transfer characteristics between the forward and reverse sweeps of V_G, as shown in Figure 5.2. CNT-FET memories have been demonstrated with ON and OFF states which are well separated and addressable with positive or negative gate voltage pulses [142–146].

However, the challenge is to be able to control the presence of hysteresis, which so far has been reported as a widely varying property among the studied CNT-FETs [144, 151, 152]. This is why several different models, which all can explain hysteresis in the transfer characteristics of a CNT-FET, have been suggested. These include: (1) Surface chemistry models, where for instance water molecules adhered to the surface of the dielectric have been shown to give a large contribution to the hysteresis for some CNT-FETs [138, 147, 149, 152, 153]. (2) It was pointed out that, especially for CNT-FETs with a gate insulator of SiO_2, it may have the same origin as the hysteresis sometimes seen in conventional Si-MOSFETs [142, 143, 151]. There it is known that mobile ions or charges within the SiO_2 layer can relocate in response to the applied gate voltage, and as a result modify the local electric field sensed by the charge carriers in the conduction channel. (3) Charging centers like defects in the nanotube itself could cause hysteresis when filled or emptied in response to the gate modulation [154–156]. A charging center in this case may be a carbon atom substituted with a different atom or molecule, which can donate or accept electrons from the conduction channel. (4) It has also been suggested that the charge traps within the gate dielectric may not be mobile, but stationary in the near vicinity of the carbon nanotube [142, 153, 157]. An applied gate voltage could then assist in filling or emptying the charge traps with charge carriers moving in the CNT, which in turn screens the applied electric field and causes hysteresis to appear in the gate voltage response.

All of these four scenarios may contribute in varying degree to hysteresis in the transfer characteristics of a CNT-FET. One way of controlling the memory response would be to tailor one mechanism to dominate the electrostatic charging around the carbon nanotube conduction channel. In this section, I will discuss how this tailoring of one mechanism to govern the others by gate oxide design could be done and show results that support this idea. The discussion in this section follows papers A.II and

A.III of this thesis.

5.2.1 Characterization of hysteresis

The focus in this chapter is on the appearance of hysteresis in the transfer characteristics of our CNT-FETs. A typical example of a CNT-FET exhibiting hysteresis is shown in Figure 5.2a, where a CNT is resting on a backgate dielectric of 20 nm thick HfO_2 with 10 mV applied between the drain and source electrodes. Most of the studied CNT-FETs displayed typical unipolar p-type behavior [39, 57], with strongly suppressed conductance at positive gate voltages and a transition into a highly conducting state at negative gate voltages. A few devices showed ambipolar dependence, with a somewhat increased conductance at high positive backgate voltages, which in this section are attributed to semiconducting nanotubes with a small band gap [60, 88]. Upon scanning the backgate voltage back and forth, the threshold voltage attains in some, but not all, of the CNT-FETs a higher value for the reverse sweep than for the forward sweep, which results in a highly reproducible hysteresis loop with different conductance values at zero backgate voltage depending on the sweep direction. In Figure 5.2b is shown a demonstration of switching a hysteretic CNT-FET between the two states at zero gate voltage by sending either a positive or negative voltage pulse to the backgate. The working memory devices included in this section were subjected to slow switching frequencies of up to 10 Hz. This switching speed is not yet suitable for a memory operation of a real device. Some of the devices were also tested for charge stability, with no change in ON or OFF state for several days, while others have a retention time of a few hours.

All measurements in this chapter were carried out at room temperature in an electrically shielded room, either under ambient conditions or in a chamber containing a gas inlet for dry nitrogen gas flow. A Honeywell relative humidity sensor (HIH-3602-A) with a $\pm 2\%$ total accuracy was incorporated for monitoring the relative humidity and temperature. For measuring in dry conditions the relative humidity was reduced below 1% (below the resolution of our humidity sensor). We performed two-terminal measurements, with the Si substrate acting as a backgate. For dc measurements, all the applied voltages were given by a home-built voltage distribution box, powered by batteries and computer controlled via a data acquisition card with the current response measured through the nanotube. $I - V_{DS}$ characteristics and transconductance response to an applied backgate voltage were collected from all samples. A schematic of the measurement setup is shown in Figure 3.3. The samples with linear $I - V_{DS}$ characteristics and transconductance insensitive to an applied backgate voltage were considered to have metallic CNTs. Achieving low contact resistance between the source and drain electrode and a nanotube is often a problematic part in CNT sample processing [71]. We sampled the total two-terminal resistances of the metallic CNTs, as an upper limit measure of the contact resistances

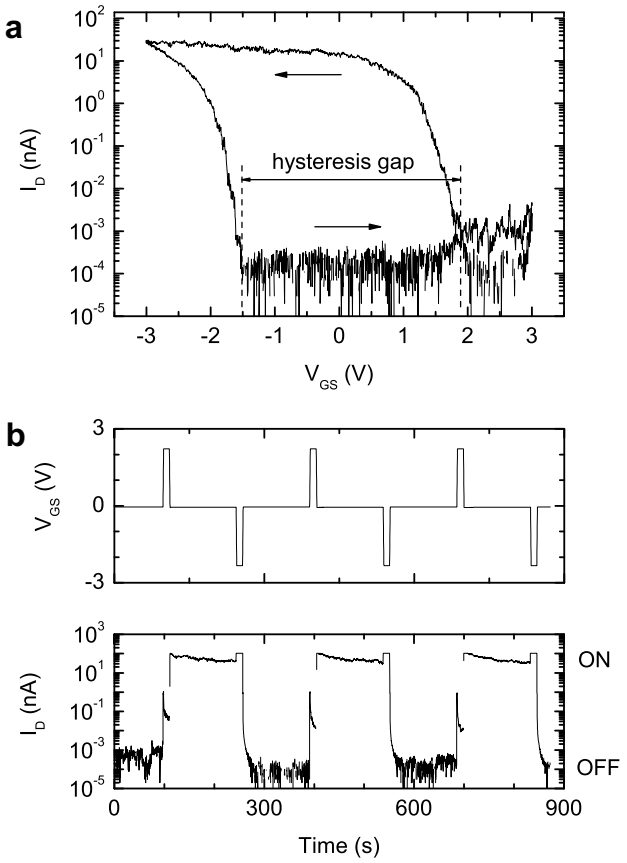

FIGURE 5.2 Memory effect for a typical CNT-FET with a gate dielectric of HfO_2. **a,** Drain current versus backgate voltage at a constant drain-source voltage of 10 mV. The arrows mark the scan direction within the loop. The hysteresis gap is given by the difference in threshold voltage (V_T) between the reverse and the forward gate voltage scan direction. **b,** Demonstration of its memory function. The upper pane displays the voltage applied to the backgate as a function of time. The lower pane shows with a constant V_{DS} of 0.1 V the current response through the CNT switching to an ON state or an OFF state in response to a positive or negative voltage pulse on the backgate, respectively. Adapted with permission from the paper A.III of this thesis.

in our devices. Resistances were found to be in the range of 14 – 160 kΩ. This is close to the theoretical minimum resistance for CNTs of $R_Q = h/4e^2 \approx 6.45$ kΩ, e is the charge of the electron and h is Planck's constant.

We quantify the memory effect in each device in terms of the shift in threshold voltage (V_T), called the hysteresis gap (see figure 5.2a). This measure relates directly to the reconfiguration of charges trapped in the close vicinity of the CNT, and is sensitive to the gate voltage scan rate, the scan range, as well as the hold time at the turning points of the scanning interval before starting the next scan. While the scan rate was kept at 10 mV/s and the hold time at the turning points was close to 1 second throughout the study, the gate voltage scan range was altered between

the samples having different gate insulator thicknesses. The samples with 300 nm thick SiO_2 dielectric were measured with a gate voltage scan range of ± 10 V, while the ALD based samples with gate insulator thicknesses of 20 – 43.5 nm had gate voltage scan ranges of ± 2 V to ± 3 V. It has been shown that for CNT-FETs with hysteresis, the threshold voltage value scales roughly linearly with the scan range for quite large voltage ranges [138, 152]. Therefore, to allow comparison between samples having different dielectrics, we calculated the relative hysteresis gap, where the hysteresis gap is normalized by the gate scan range. The measured threshold voltages, relative hysteresis gap and the ON and OFF conductance values for the CNT devices are presented in the next section.

5.2.2 Effect of gate oxide on hysteresis

For studying how the hysteresis changes with different gate oxides, we first determined the physical dimensions of each CNT-FET using AFM imaging. A pie chart of nanotube diameters in the field-effect transistors is presented in Figure 5.3a. Most of the nanotubes have diameters between 0.8 nm and 3 nm (altogether 73 nanotubes, or 78 %). These are interpreted as single-walled nanotubes. The rest of the tubes fall between 3 nm and 10 nm and are probably comprised of large diameter single-walled and/or multi-walled carbon nanotubes and nanotube bundles. A pie chart of transistor channel lengths is presented in Figure 5.3b. Most of the channel lengths fall in between 70 nm and 600 nm (altogether 86 nanotubes, or 91 %), leaving only 8 devices in the range from 600 nm to 2.5 μm.

There are many different reasons why hysteresis could appear in the transfer characteristics of a CNT-FET, as mentioned in Section 5.2. We wanted to assess what kind of dielectrics always causes hysteresis, and whether tailored gate oxides could make one of the mechanisms causing hysteresis to be dominant. For this we made CNT-FETs having different gate dielectrics. In total 94 semiconducting CNT-FETs were manufactured, comprising about 82% of all the samples. This is a bit higher than the expected 67% for randomly picked CNT chiralities. Eight of the eleven devices having CNTs grown with hot wire generator reactor show clear metallic behavior. Characteristics of the two CNT-FETs made with CNTs grown with the hot wire generator reactor did not deviate notably compared to the other 25 devices with the same gate dielectric. Here 7 of the 94 samples had the backgate covered with ALD of Al_2O_3 (nominal thickness: 20 nm), 14 with an ALD of HfO_2 (20 nm), 11 with an ALD of $HfO_2 - TiO_2 - HfO_2$ (40-0.5-3 nm), 27 with an ALD of $HfO_2 - TiO_2 - HfO_2$ (40-0.5-1 nm), and the remaining 25 with thermally grown SiO_2 (300 nm).

The threshold voltages from all samples used in this study are presented in Figure 5.4. The values are extracted from the I_D vs V_G data taken at ambient conditions (see Figure 5.2a). When sweeping the backgate voltage in forward and reverse direction, different threshold voltages are seen for most of the samples. Both forward (blue) and reverse (red) sweep threshold voltage values are displayed in

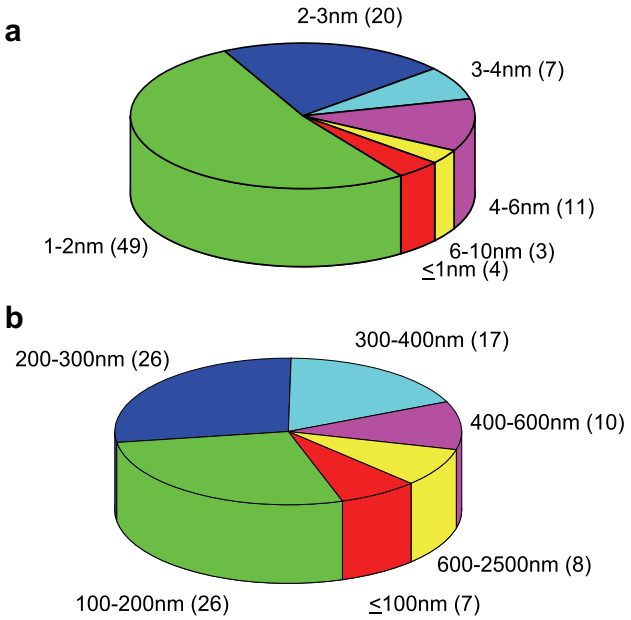

FIGURE 5.3 Distribution of the conduction channel diameter and length for the CNT devices. **a,** CNT diameters, with the interval displayed in nanometers followed by the number of CNTs within that range. The CNT diameters were determined from AFM images. **b,** The channel lengths, the interval is followed by the number of devices in that range. Adapted with permission from the paper A.III of this thesis.

Figure 5.4, and divided into different panes according to the used gate oxide. The last 12 samples in pane a and the last 5 samples in pane b show no shift in threshold voltage. The remaining samples have a shift in threshold voltage between forward and reverse scan directions. As mentioned earlier in the case of the significantly thicker SiO_2 (300 nm) compared to the other gate dielectrics (20 – 43.5 nm), a higher backgate voltage range was used to produce the electric field strength required for reaching the saturation plateau in the ON state. All the SiO_2 based CNT-FETs in Figure 5.4a have a scan range of ± 10 V and the samples in the remaining panes have a scan range of ± 3 V, except for a few exceptions. The exceptions are samples 11 in pane c with 17, 25, and 26 in pane e, which have a scan range of ± 2.5 V and sample 12 in pane c which has a scan range of ± 2 V.

The corresponding ON and OFF conductance values for the CNT-FET memory devices are displayed in Figure 5.5. The ON and OFF values are taken at zero gate voltage, as appropriate for nonvolatile memory readout. The last samples in pane a and in pane b have no shift in threshold voltage, and thus show the same conductance value for both forward and reverse scan directions. The best memory devices fabricated have an ON/OFF ratio of about 4 orders of magnitude, while some of the others have a value just above 1. We would like to point out that in these cases the ON and OFF states were clearly separated and reproducible in the data. The small ON/OFF ratios in some of the samples are caused by a “bad“ or

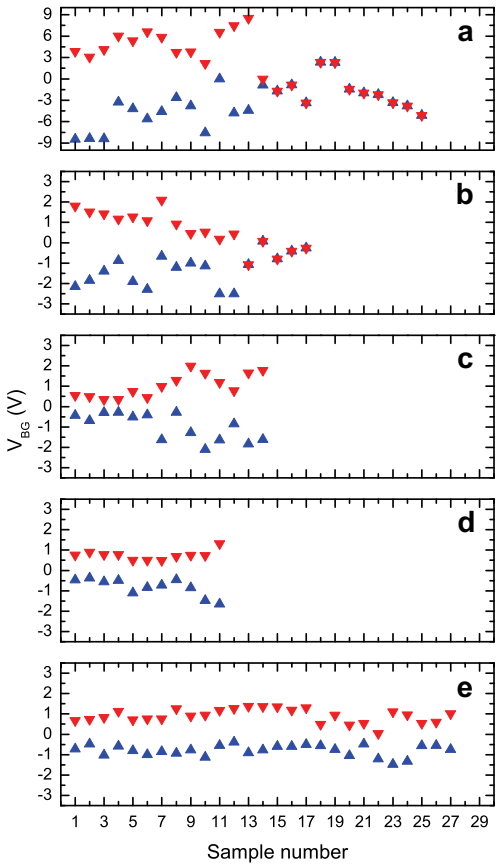

FIGURE 5.4 Threshold voltages for forward (blue) and reverse (red) gate voltage scan direction for all samples. The scan range was in **a,** ±10 V and in the rest of the panes ±2 to ±3 V. The gate dielectric is in **a,** SiO_2 (300 nm), **b,** Al_2O_3 (20 nm), **c,** HfO_2 (20 nm), **d,** $HfO_2 - TiO_2 - HfO_2$ (40-0.5-3 nm) and **e,** $HfO_2 - TiO_2 - HfO_2$ (40-0.5-1 nm). Adapted with permission from the paper A.III of this thesis.

highly conducting OFF state, which could be explained by these devices consisting of either a small band gap CNT or a bundle of several CNTs instead of a single tube. But for the memory application, a large ON/OFF ratio is of much smaller importance than having a narrowly distributed hysteresis gap. We therefore valued also these samples and included them in the study.

All mass-fabricated electronic devices have a natural variation of characteristic parameters. This is acceptable as long as the parameter distribution is narrow enough not to interfere with its intended function. The large number of devices allows us to estimate the distribution of hysteresis seen for differing gate dielectrics. As mentioned earlier, the threshold voltage value scales roughly linearly with the scan range for quite large voltage ranges for CNT-FETs with hysteresis [138, 152]. Therefore, we calculate the hysteresis gap and normalize it with the scan range to include all the samples having a differing scan range. The normalization also makes comparison of the hysteresis gap distribution between different sample sets easier.

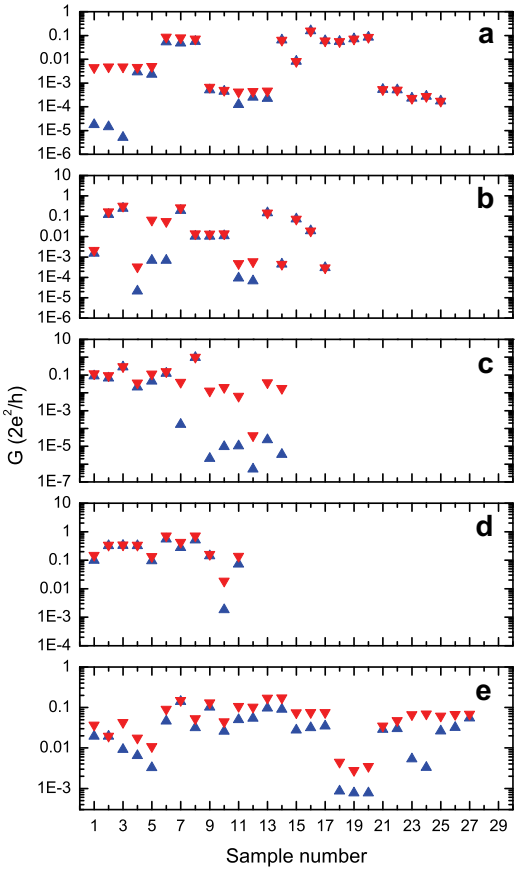

FIGURE 5.5 ON (red) and OFF (blue) conductances for the CNT memories at zero gate voltage. The gate dielectrics are **a,** SiO_2 (300 nm), **b,** Al_2O_3 (20 nm), **c,** HfO_2 (20 nm), **d,** $HfO_2 - TiO_2 - HfO_2$ (40-0.5-3 nm) and **e,** $HfO_2 - TiO_2 - HfO_2$ (40-0.5-1 nm). Adapted with permission from the paper A.III of this thesis.

Our results are plotted in Figure 5.6. Each column represents a 5% interval (bin) of the relative hysteresis gap along the x-axis. We show in Figure 5.6a that from 25 SiO_2-based CNT-FETs, 12 devices do not exhibit hysteresis at all. The remaining 13 display a relative hysteresis gap almost evenly spread within the interval 30 – 65%. The results are in agreement with earlier reports [144,151] on SiO_2-based CNT-FETs, finding that only a fraction of the produced devices show hysteresis in their transfer characteristics. The picture is very similar in Figure 5.6b, where the CNT-FETs have a gate dielectric of 20 nm thick ALD grown Al_2O_3. There 5 devices show no hysteresis while 12 devices have their relative hysteresis gap within the interval 25 – 65%.

For the remaining three panes of Figure 5.6, there is a distinct difference in that *all* the fabricated devices display a clear relative hysteresis gap. With memory devices in mind, this translates into a 100 % fabrication yield. In Figure 5.6c, the gate dielectric is 20 nm thick ALD grown HfO_2. The 14 devices made have their relative hysteresis gaps spread from 10% up to 70% of the total gate scan range. While all

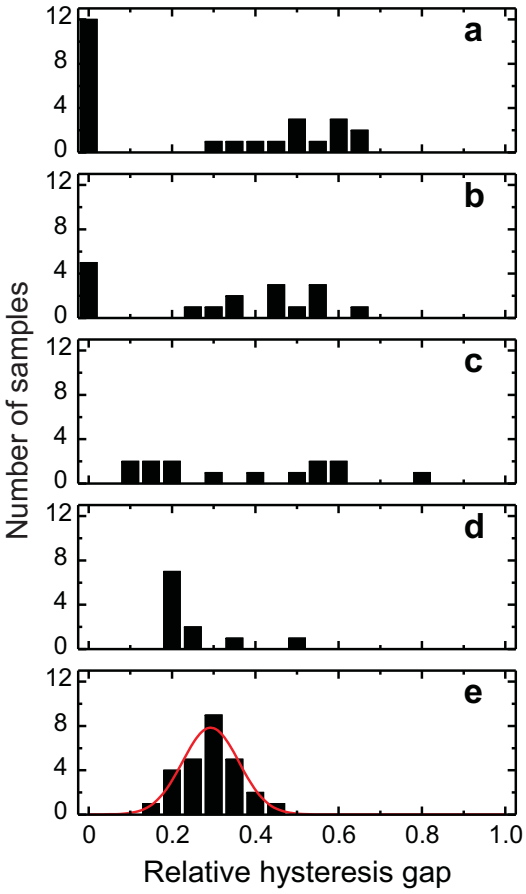

FIGURE 5.6 Statistics of the relative hysteresis gap from 94 devices with varying gate dielectric. Each column covers a 5% interval of the full gate voltage scan range. The gate dielectric is in **a,** SiO_2 (300 nm), **b,** Al_2O_3 (20 nm), **c,** HfO_2 (20 nm), **d,** $HfO_2 - TiO_2 - HfO_2$ (40-0.5-3 nm) and **e,** $HfO_2 - TiO_2 - HfO_2$ (40-0.5-1 nm). Adapted with permission from the paper A.III of this thesis.

CNT-FETs in this set show a memory effect, the distribution of the relative hysteresis gaps is very wide, having a standard deviation of 22%. The following two panes of Figure 5.6 show data from a specially designed three-layered ALD structure. It was made in order to study the hypothesis that the lower interface of the top-most HfO_2 layer can play an important role in controlling the amount of charge traps available. The first deposited layer is a 40 nm thick buffer layer of HfO_2 with the purpose of providing a stable dielectric which can withstand the physical stress of sample processing. Next a 0.5 nm thick layer of TiO_2 was deposited with the intent of creating an interface to the top-most layer. Finally another layer of HfO_2 was deposited, with a thickness of 3 nm in Figure 5.6d and 1 nm in Figure 5.6e. While the total thicknesses of the ALD dielectrics in Figures 5.6d and 5.6e are about twice the thickness in Figure 5.6c, the lower interface of the top HfO_2 layers are moved considerably closer to the CNT. The resulting relative hysteresis gap distributions show strongly

decreased standard deviations of 0.09 and 0.06 for Figure 5.6d and Figure 5.6e, respectively. More so, the latter pane with a top layer of only 1 nm thickness displays a distribution of relative hysteresis gap values that closely resembles the normal distribution as indicated by the Gaussian fit (red). This indicates that the distribution is not likely to change noticeably if we were to add more samples to the study.

TABLE 5.1 Statistics taken from data in Figure 5.6, with the lettering of gate dielectric in the first column according to that of the panes. The following columns display the total number of samples, the mean relative hysteresis gap, and its standard deviation.

gate dielectric	no. of samples	mean rel. hyst. gap	standard deviation
a	25	0.27	0.27
b	17	0.32	0.24
c	14	0.38	0.22
d	11	0.26	0.09
e	27	0.29	0.06

Our results are summarized in Table 5.1, showing the number of samples, the mean of the relative hysteresis gap, and its standard deviation for each gate dielectric type according to the lettering in Figure 5.6. Clearly, the triple layer with thinner upper HfO_2 layer is the best choice as gate insulator from studied dielectrics when preparing a memory storage device. More important, we show here that memory effects in CNT-FETs can be controlled in ambient conditions, even without applying any kind of surface passivation layer. The reason for the differences seen between single layer dielectrics of SiO_2, Al_2O_3 and HfO_2 is difficult to discern, but may be related to differing charge trap densities, or even types of charge traps. While we have not made direct measurements of the charge trap densities, this could possibly be done for charge traps close to the surface using either scanning probe microscopy or conductive AFM.

Turning our attention to the rapidly narrowing distribution in hysteresis gap when going from single layer HfO_2 to a triple-layered dielectric structure, the most significant difference in the surrounding of the CNT is the closely located interface between the HfO_2 and the TiO_2 layer. It is commonly known that the interface between two different materials may carry defects or charge traps and also on the basis of these data, it is reasonable to assume that moving the lower interface of the upper HfO_2 layer closer to the CNT provides a layer of stationary charge traps at a well calibrated distance from the CNT. It is supported by the notion that a layer of stationary charge traps in the vicinity of the CNT will screen the action from mobile charge carriers, thus creating well defined device geometry with a narrow hysteresis gap distribution. We therefore conclude that the most probable dominating charge

storage mechanism in the triple layer structure is due to stationary charge traps at the lower interface of the uppermost HfO_2 layer which are filled and emptied by charge carriers from the CNT in response to application of a negative or positive gate voltage.

Since there is also some longer channel lengths within our Pd contacted CNT-FET where the Schottky barrier effect might be comparable or even smaller than the field effect, we made estimates of field-effect mobility and subthreshold slope from the measured hysteresis loops shown in Figure 5.2a. For determining mobilities for our devices we first calculated the nanotube gate capacitances (see Equation 2.13) per unit length with respect to the backgate. For the SiO_2 samples the calculated capacitances were around $C_G/L \sim 0.33\ \frac{\mathrm{pF}}{\mathrm{cm}}$ and for the Al_2O_3 samples $C_G/L \sim 1.1\ \frac{\mathrm{pF}}{\mathrm{cm}}$. In the capacitance calculation we used average dielectric constant values of 3.95 for thermally grown SiO_2 and 7.5 for the ALD grown Al_2O_3 gate dielectric. For the ALD grown HfO_2-based gate dielectrics we used ε value of 25 for all. The corresponding capacitances are $C_G/L \sim 4.0\ \frac{\mathrm{pF}}{\mathrm{cm}}$ for the HfO_2 (20 nm) samples and for the $HfO_2 - TiO_2 - HfO_2$ (40-0.5-3 nm) and (40-0.5-1 nm) samples $C_G/L \sim 3.2\ \frac{\mathrm{pF}}{\mathrm{cm}}$, and $C_G/L \sim 3.7\ \frac{\mathrm{pF}}{\mathrm{cm}}$, respectively. As most of the calculated capacitances are close to the quantum capacitance of a carbon nanotube having a value in the order of $C_Q/L = 4e^2/\pi\hbar\nu_F \sim 4\ \frac{\mathrm{pF}}{\mathrm{cm}}$, we need to take C_Q into account (see Equation 2.15). For devices having SiO_2 as a gate dielectric the contribution from the gate capacitance clearly dominates over the quantum capacitance.

For calculating the mobility of our devices we used the so-called "field-effect mobility" μ_{fe}, which is used to compare device properties. It is device specific and includes e.g. surface effects, contact resistances, etc. The field-effect mobility of a CNT-FET can be calculated by [51]

$$\mu_{fe} = \frac{L^2}{C}\frac{\partial G}{\partial V_G}, \tag{5.1}$$

where V_G is the backgate voltage. Purewal *et al.* reported electron mean free paths for semiconducting CNTs ranging from ∼250 nm to ∼800 nm at room temperature [158]. The majority of our CNT devices have lengths that fall between 70 nm and 600 nm, and are thus in the ballistic limit where the field-effect mobility does not apply. We therefore calculated the mobility for our longest device of 2.5 μm, which has $HfO_2 - TiO_2 - HfO_2$ (40-0.5-1 nm) as its gate dielectric. Using Equation 5.1, we extracted a value of 200 $\frac{\mathrm{cm}^2}{\mathrm{Vs}}$, which corresponds well to previously reported mobilities for similar devices [39, 72, 138, 142, 143]. Using equation 3.1, we also calculated the subthreshold slope S. We found for our CNT-FETs values as small as 100 $\frac{\mathrm{mV}}{\mathrm{dec}}$, e.g. from the data shown in Figure 5.2a. This is close to the theoretical limit of 60 $\frac{\mathrm{mV}}{\mathrm{dec}}$ [135].

5.2.3 Effect of environment on hysteresis

There are several models explaining the hysteresis seen in the transfer characteristics in the CNT-FETs, as mentioned earlier in Section 5.2. One suggested model indicates that surface chemistry effects play an important role in introducing hysteresis to CNT-FETs. Water molecules adhered to the surface has been shown to give a large contribution to the hysteresis of CNT-FETs. So far the studies have concentrated on CNT-FETs having SiO_2 as a gate dielectric [136, 138, 160]. In this section I will discuss how the ambient humidity changes the hysteresis in CNT-FETs having Hf-based gate dielectric and compare it to the more conventional SiO_2. The discussion is based on paper A.II of this thesis.

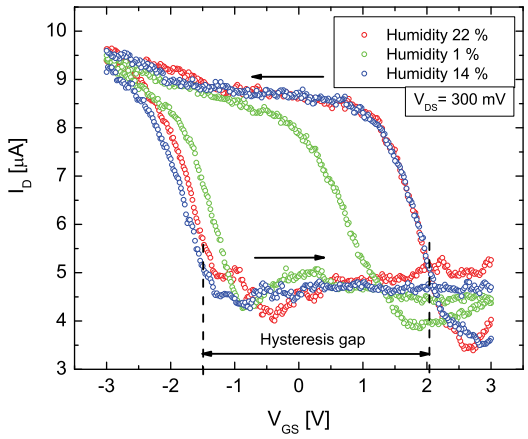

FIGURE 5.7 Memory effect of CNT-FET in different relative humidities. Drain current versus backgate voltage at a constant drain-source voltage of 300 mV for a typical device having a gate dielectric of $HfO_2 - TiO_2 - HfO_2$. The arrows mark the scan direction to produce the loop. Hysteresis loop is shown for three different relative humidity values; red trace for 22%, green trace for 1% and blue trace for 14%. The hysteresis gap is presented for the humidity value of 14% and is given by the difference in threshold voltages (V_T) between reverse and forward scan directions. Adapted with permission from paper A.II of this thesis.

A typical example of the influence of humidity on CNT-FETs is shown in Figure 5.7 for a CNT resting on an ALD grown oxide of $HfO_2 - TiO_2 - HfO_2$, with nominal thickness of 40-0.5-1 nm, and 300 mV applied between the drain and source electrodes. All of the measured CNT-FETs in this study displayed a typical unipolar p-type behavior with highly conducting state at negative gate voltages that develops into a suppressed conductance at positive gate voltages [39, 57]. As previously, when scanning the backgate from positive to negative voltages and back, the threshold voltage attains a higher value for reverse (towards negative gate voltages) than forward (towards positive gate voltages) sweep direction.

For studying the effects of humidity on these transfer characteristics, the hysteresis loop presented in 5.7 was taken at different relative humidity values. We

TABLE 5.2 Hysteresis gap in dry N_2 flow (in % of hysteresis gap in ambient conditions). The accuracy used here is $\pm 2\%$

Sample	Gate dielectric $HfO_2 - TiO_2 - HfO_2$	Gate dielectric SiO_2
1	51 %	67 %
2	61 %	28 %
3	91 %	77 %
4	68 %	47 %
5	71 %	56 %
6	67 %	
7	85 %	
Average	71 %	55 %
Sd	14 %	19 %

quantify the hysteresis loops in the same way as previously in Section 5.2.1, in terms of the shift in threshold voltage, called the hysteresis gap (see Figures 5.2 and 5.7) and they are taken consecutively as follows: the first trace (red) was recorded under ambient conditions with a relative humidity of 22%. Then a dry nitrogen flow was introduced to the chamber and the humidity was monitored until it reached a value under 1%, which is below the lower sensing limit of our humidity sensor. The samples were kept at this point under N_2 flow from 0.5 to 18 hours depending on a sample, after which a second hysteresis loop trace (green) was measured. Finally the chamber was opened to ambient air. When the relative humidity reached 14% the third trace (blue) was measured. When relative humidity is lowered close to zero the hysteresis diminishes but does not vanish as can be seen from Figure 5.7. In this case the hysteresis gap is 68% of the original value. One sample from each dielectric was held in N_2 for longer than 0.5 hours. During this procedure the development of the hysteresis gap was followed, and no noticeable change was observed. After the CNT-FET was exposed to ambient conditions again the hysteresis loop quickly attained the original shape. The shift of threshold voltage to lower gate voltage for the reverse gate sweep in low humidity compared to higher humidity is observed. This can be attributed to the desorption of water molecules around the CNT-FET, including surface-bound water in the vicinity of the nanotube [136, 160].

These measurements were repeated for 7 CNT-FETs with ALD grown triple layer of $HfO_2 - TiO_2 - HfO_2$ as a gate dielectric. As a comparison the hysteresis loop of 5 CNT-FETs with SiO_2 as a gate dielectric was measured in ambient conditions and in dry nitrogen flow. Not all CNT-FETs having gate oxide of SiO_2 show hysteresis, as shown in Section 5.2.2. In this study only devices showing hysteresis in ambient conditions were chosen. Our results are presented in Table 5.2, display-

ing the change in hysteresis gap in dry N_2 flow compared to the original value under ambient conditions for samples having either ALD-based triple-stack or SiO_2 gate dielectrics. From Table 5.2 can be seen that in dry N_2 flow the hysteresis gap of CNT-FETs having gate dielectric of $HfO_2 - TiO_2 - HfO_2$ decreases less than that of CNT-FETs with SiO_2 as a gate dielectric, when compared to original gap size. The low humidity hysteresis gaps of devices having $HfO_2 - TiO_2 - HfO_2$ have a mean of 71%, while the devices having SiO_2 as a gate dielectric have a mean of 55% of the original gap. The standard deviations are 14% and 19%, respectively. This indicates that the devices having an ALD-based gate dielectric retain their hysteresis gap better and have smaller distribution than devices on SiO_2.

It is known that water molecules can bind on the hydroxylated silica surface [161]. On the other hand, Lee *et al.* have shown that surface-bound water on SiO_2 alone is not the only cause of gate hysteresis in CNT-FETs [160] contradicting the earlier finding of Kim *et al.* [136]. On HfO_2, this specific surface chemistry is absent but Raghu *et al.* have shown that moisture adsorbs better on HfO_2 than on SiO_2 due to the polar nature of amorphous HfO_2 and also desorbs slower from HfO_2 than from SiO_2. In both cases almost all adsorbed water could be removed in a $300\,^{\circ}C$ bake-out [126]. This is one possibility of explaining our findings, that more moisture is desorbed from the SiO_2 than from the $HfO_2 - TiO_2 - HfO_2$ gate dielectric. On the other hand, we showed in Section 5.2.2 that the hysteresis gap can be controlled by carefully designing the gate dielectric in nm-thin layers. By using the same ALD grown $HfO_2 - TiO_2 - HfO_2$ gate oxide used here, we achieved the first CNT-FETs with consistent and narrowly distributed hysteresis gap in their transfer characteristics "paper A.III of this thesis". This indicates that the majority of the hysteresis would come from the stationary charge traps located at the lower interface of the uppermost HfO_2 layer, which can be filled and emptied by charge carriers from the CNT by modulating the gate voltage. ALD is known to produce a very conformal coating, while the preparation of thermally grown SiO_2 may produce a more porous film. This could also have an influence on the adsorption/desorption behavior of water. The magnitude of hysteresis caused by adsorbed water on CNT-FETs and the effect it has on different gate dielectrics is still under debate. The role of humidity on CNT-FETs is important for their possible memory and sensor applications and it needs to be studied further to improve the reliability and operation of these devices.

5.3 Figures of merit in carbon nanotube field-effect transistor memories

In the past few years, there has been a steady progress in boosting the performance of the CNT-FETs [19]. The single-walled carbon nanotube field-effect transistors have been shown to be very fast, with transit frequency as high as 50 GHz [97] and

could theoretically approach a maximum value of $\nu_F/2\pi L \sim 130$ GHz/L (μm) [96]. The high sensitivity of CNT-FETs has been also demonstrated by monitoring single-electron tunneling events between a gold particle and a nearby nanotube [162, 163]. Since the first demonstration of an electro-mechanical carbon nanotube memory by Rueckes *et al.* [98], there has also been a steady progress of CNT-FET memories [138, 142–148, 150]. While the mobility of these devices is excellent (79 000 cm^2/Vs) [51], the charge storage stability of at best 14 days [147] for CNT-FET memories leaves room for improvement. In this section, I will concentrate on another key property for a high-performance nonvolatile memory, namely the speed with the Write and Erase operations are executed together with the endurance of these memories. To date the operation frequency in CNT-FET memories is reported to be in the order of 10 ms [143, 146]. This figure of merit needs to be improved before a CNT-FET memory can compete with conventional silicon-based Flash memories with Write and Erase times of 100 μs [164]. The discussion in this section follows paper A.IV of this thesis.

The devices used to study the operation speed of CNT-FET memories are introduced in Figure 5.8. An AFM image of a device taken before the 2nd ALD deposition (as described in Section 4.1) with a schematic of the measurement setup is shown in Figure 5.8b. The drain-source and gate-source voltage bias was supplied by a computer-controlled home-made voltage distribution box powered by batteries. A drain-source bias of 10 mV was used for all the CNT-FET measurements. The current response through the tube was monitored while modulating the voltage on the gate. The Si backgate was operated in two different ways. The transfer characteristics of CNT-FETs were measured while the backgate was scanned from positive to negative voltages and back. The memory operation was performed with voltage pulses applied to the backgate by manually triggering either positive or negative voltage pulse from an Agilent 33250A 80 MHz function generator. All measurements were carried out at room temperature in an electrically shielded room.

Even though the focus on this section is on the Write/Erase speed of memory elements made out of CNT-FET and operated with a backgate, also other device parameters such as operation endurance and retention time are considered. But before starting to test the different parameters, we again measured the hysteresis loop of these memories. A typical example of such transfer characteristics is presented in Figure 5.9. As shown previously, again the threshold voltage where the current response starts to rise attains a higher gate voltage value for reverse than forward sweep, producing an advanced p-type hysteresis loop. This results in a different current (indicated as I_{ON} and I_{OFF}) at zero backgate voltage depending on the sweep direction. We define these two states as the ON- and the OFF-state of the memory device. In this device, the ON and OFF currents are separated by more than three orders of magnitude. In the inset of Figure 5.9, an I-V curve taken at $V_{GS} = 0$ in the OFF-state is shown.

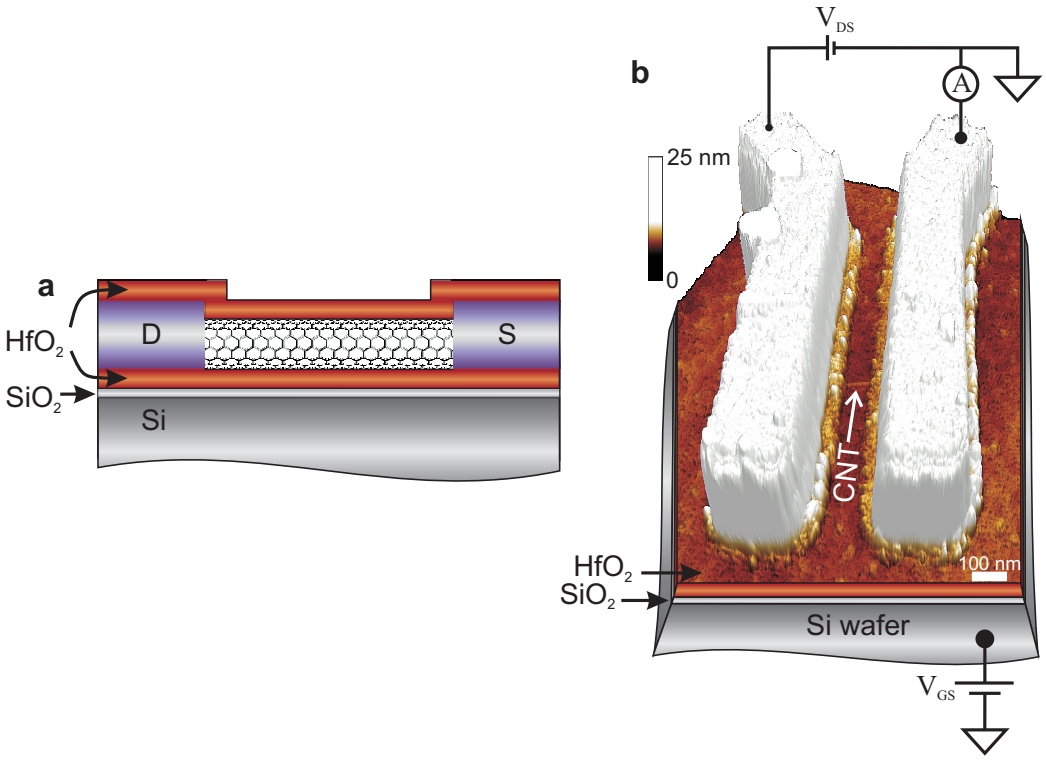

FIGURE 5.8 Overview of devices used to study the figures of merit in the CNT-FET memories. **a,** Sideview of a CNT-FET having ALD grown HfO_2 gate and passivation layers together with drain (D) and source (S) electrodes. The nominal thicknesses of both HfO_2 layers was 20 nm. **b,** AFM image of a typical device, where a CNT is resting on a HfO_2 layer and contacted with Pd source and drain electrodes having a spacing of 140 nm. The measurement setup is also schematically illustrated. The bias voltage is applied between the drain and source electrodes and the backgate voltage to the Si wafer. The current response is measured through the CNT. Adapted with permission from the paper A.IV of this thesis.

Having a stable hysteresis loop with well separated states at zero gate voltage enables us to use this device as a memory element. Similar devices have previously been studied with different gate insulators, device geometries and varying parameters [142–148, 150]. So far these CNT-FET memory elements have been subjected to slow Write and Erase times, the fastest being 10 ms [143, 146]. The Write and Erase-pulses with a duration of 100 ns and an amplitude of ± 4 V, respectively, were sent to the backgate. The Write-pulse is shown in the inset of Figure 5.10. The ON and OFF states are separated by more than two orders of magnitude and monitored for $\sim$25 s before switching to the other state. This 100 ns operation speed was limited by our measurement setup, therefore the CNT device itself may allow even higher speeds.

As a comparison for our high speed CNT-FET memory devices on HfO_2, we also performed similar operation speed measurements for CNT-FET memories hav-

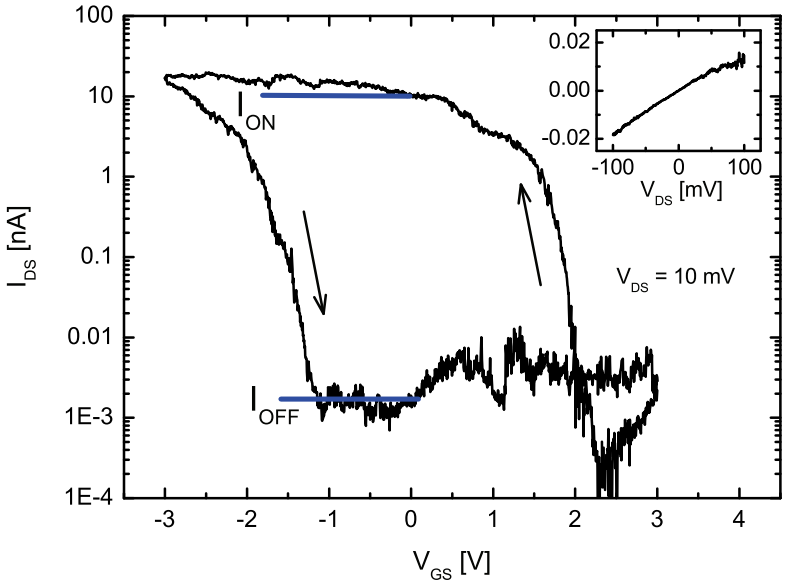

FIGURE 5.9 Hysteresis loop of a typical CNT-FET used in this study with $V_{DS} = 10$ mV. The device has a hysteresis gap of 3.2 V, subthreshold slope of 120 mV/dec and an ON/OFF ratio more than 10^3. The arrows mark the backgate scan direction within the loop. The inset shows the I-V curve of the device in the OFF-state. Adapted with permission from the paper A.IV of this thesis.

ing more commonly used SiO_2 as a gate oxide. The CNTs in these reference devices were produced by arc-discharge and spin coated onto a thermally grown SiO_2 having thickness of about 300 nm. Results on memory operation speed for these CNT-FETs are shown in Figure 5.11. The device has an ON/OFF ratio of about 10 at $V_{GS} = 0$ V, as shown in the inset of Figure 5.11a. The 1 s pulsing is writing well to both of these states but already at 1 ms pulsing these states deviate distinctly from the original. As the pulse length is still lowered to 100 μs the states cannot be anymore resolved as shown in Figure 5.11b. The drain-source bias voltage was 10 mV and the pulse amplitude was $\pm$10 V in all the measurements done with CNT-FET memory devices having SiO_2 as gate dielectric.

We also investigated how the memory devices perform under continuous operation. The endurance of another device (that also showed 100 ns operation speed) is presented in Figure 5.12, where 10 ms long Write- and Erase-pulses with an amplitude of $\pm$3 V and rise and fall times of 3 μs were used. The state readout time was 0.5 s. The states stayed well separated for more than 10^4 cycles, until after 18 000 cycles a failure of operation was observed and the device was broken. The pulse duration in this endurance measurement is 100 000 times longer (for reasons explained below) than the fastest operation speed achieved. Compared to the 100 ns operation, this adds an extra static stress on the gate oxide that is also contributing to the aging of the device. In addition, breaking of the nanotube is likely to be caused by the

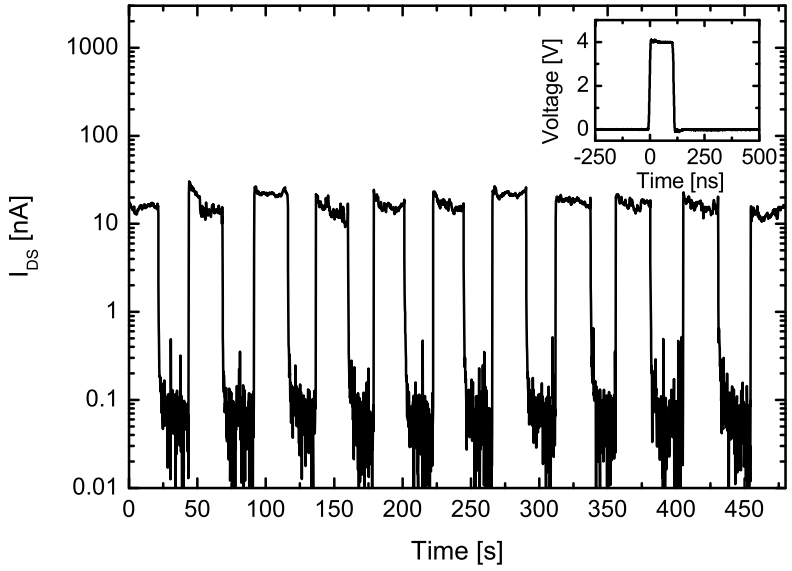

FIGURE 5.10 Memory operation of the CNT-FET. Writing and erasing the memory was done with 100 ns pulsing to the gate, and the state was recorded between the pulsing with $V_{GS} = 0$ V. In the inset is shown the Write-pulse for high current state. Adapted with permission from the paper A.IV of this thesis.

backgate operation since due to large parasitic capacitances and small rise and fall times of the pulses, a transient pulse is induced in the source and drain electrodes. To ensure that this transient response is not seen in our measurements, a 10 Hz low-pass filter was placed between the CNT-FET and the current amplifier. This response also sets the higher limit for our readout speed and the readout needed to be done below the lowpass filter's cutoff frequency of 10 Hz. This also affected the choices for our pulse duration and readout time of a state in the endurance test. Since in our function generator the pulse width and waiting period before the next pulse are related through a finite number of points in an arbitrary wave function, for us to be able to get 0.5 s readout period we used 10 ms pulses in the endurance test. When studying the fast memory operation, we obtained the 100 ns pulse width combined with a long readout time by triggering the pulses manually, which was not feasible in the endurance test consisting of a large number (18 000) pulses. Previously, it has been demonstrated by Chaste *et al.* that the CNT is capable of giving accurate readout response in the GHz regime when gated with a local gate [97], which could probably be attainable with CNT-FET memory devices on HfO_2 having a top gated device configuration.

To represent a more detailed development of the memory endurance data we constructed a histogram containing more than 13 000 cycles, which was assembled from the ON and OFF state plateaus in each cycle. To show single state with one value, we calculated averages from the ON and OFF states in each cycle. From this

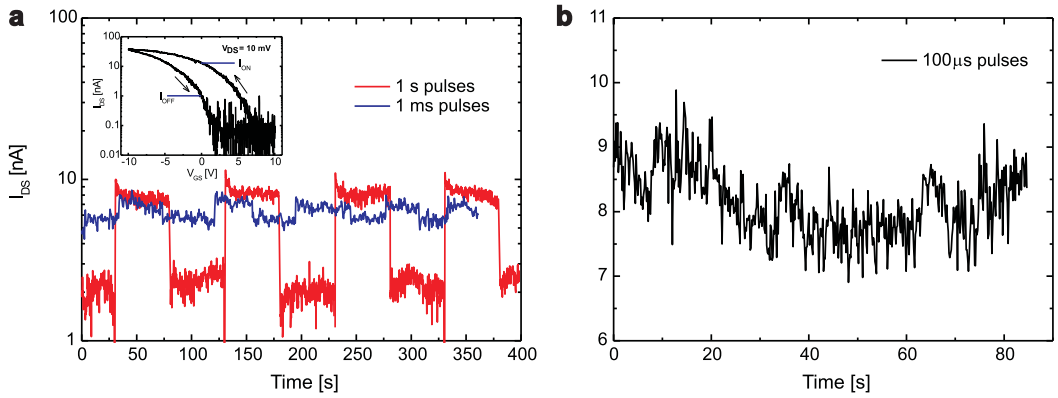

FIGURE 5.11 Memory operation of the CNT-FET having SiO_2 as a gate dielectric with different pulsing speeds. **a,** Writing and erasing the memory was done with 1 s pulsing (red) and with 1 ms pulsing (blue) to the gate, both having an amplitude of ± 10 V. After a pulse the state was recorded with $V_{GS} = 0$ V. The timescale in data with 1 ms pulsing is multiplied by three to allow better comparison with data having 1 s pulsing, which expands longer in time. In the inset is shown the hysteresis loop for the same device with $V_{DS} = 10$ mV. The arrows mark the scan directions. The device has an ON/OFF ratio of about 10 at $V_{GS} = 0$ V, which the 1 s pulsing is still retaining but when having 1 ms pulsing the ON/OFF ratio is almost vanished. **b,** Trial of memory operation of the CNT-FET on SiO_2 with 100 μs pulsing speed and ± 10 V amplitude. As seen from the graph, the states are no longer resolved. Adapted with permission from the paper A.IV of this thesis.

data we constructed the histogram shown in Figure 5.13. Since the endurance data is logarithmic in nature, the bin intervals in this histogram are also logarithmic. This way we can produce equal size bins in logarithmic I_{DS} scale and do not distort the number of counts in each bin. In Figure 5.13 two distinct peaks are observed. These peaks correspond to the ON-state (red) centered at 4.80 nA with a standard deviation of 4.47 and to the OFF-state (blue) centered at 0.14 nA with a standard deviation of 0.11. In between these two peaks is a valley containing a few counts that overlap with each other. These are indicated by purple bins around $I_{DS} = 1$ nA which occur as the device is aging. For example commercial Flash memories are usually specified more than 10^5 Write/Erase cycles. The main reason there for limited endurance is the tunnel oxide degradation due to trap generation in the oxide and interface state generation on the drain side of the channel [129].

To investigate the volatility of the memories, the retention times of both ON and OFF states were recorded after the hysteresis loop sweep shown in Figure 5.9. The OFF-state does not change remarkably during the measurement, as seen in Figure 5.14. In contrast to the OFF-state, the ON-state has an exponential decay, with fast relaxation in the beginning and a slower tail, until it reaches the OFF-state. Here we considered the two states to be separated as long as they differed by more than a

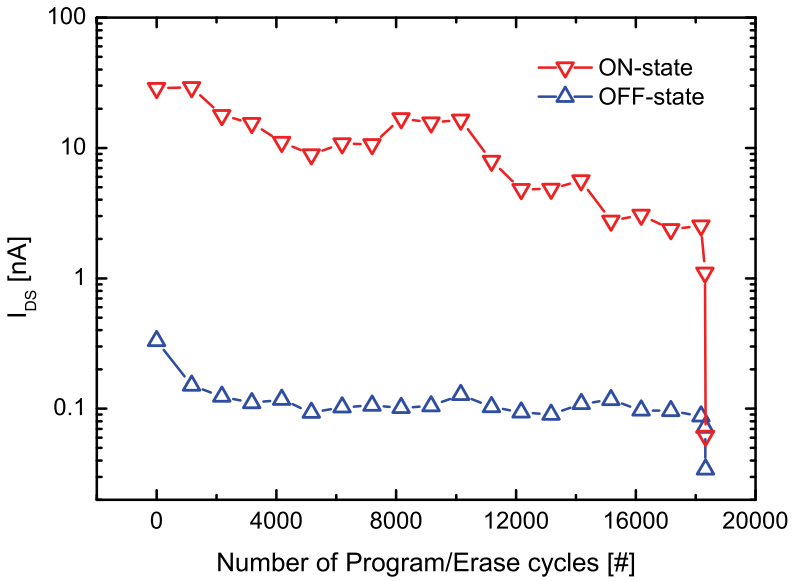

FIGURE 5.12 Memory operation endurance of a CNT-FET. Write and Erase cycles operated with ±3 V and 10 ms pulses. The memory can be operated for more than 18 000 cycles before a failure. The OFF-state stays unchanged while the ON-state is lowered by about a decade before a failure of operation. Adapted with permission from the paper A.IV of this thesis.

factor of 10, and with this threshold the retention time of the device was $\sim 1.5 \times 10^4$ s ($>$ 4h). This relaxation time is not sufficient for a nonvolatile memory element but it could be improved by an additional insulator layer as will be discussed below.

Finally, we discuss the origin of the extremely fast operation speeds observed. The hysteresis in the transfer characteristics of CNT-FETs has previously been explained by several different models as mentioned in Section 5.2. (1) Surface chemistry effects (e.g. water molecules adhered to the surface of the dielectric) can give a large contribution to the hysteresis for some CNT-FETs [136, 138]. Our studied devices have on top of the CNT a 20 nm passivation layer of HfO_2 to reduce the surface chemistry effects to a minimum. Also, screening of the applied gate voltage by adsorbed water molecules is a relatively slow process and already 500 μs pulsing was shown to remove completely the hysteresis induced by surface effects [165]. In summary, the passivation layer and the fast operation speed in our experiments make significant contribution of surface effects unlikely. (2) Mobile charges or ions that can be relocated within the dielectric layer by modulating the gate voltage are known from Si MOSFETS to cause retarded hysteresis (clockwise) [159]. Here we see advanced hysteresis (anticlockwise), which indicates that this mechanism is not the main reason for the memory effect. (3) Charging centers like defects in the nanotube itself could cause hysteresis when filled or emptied with the applied gate voltage [154–156]. However in Section 5.2.2, using several different layer structures

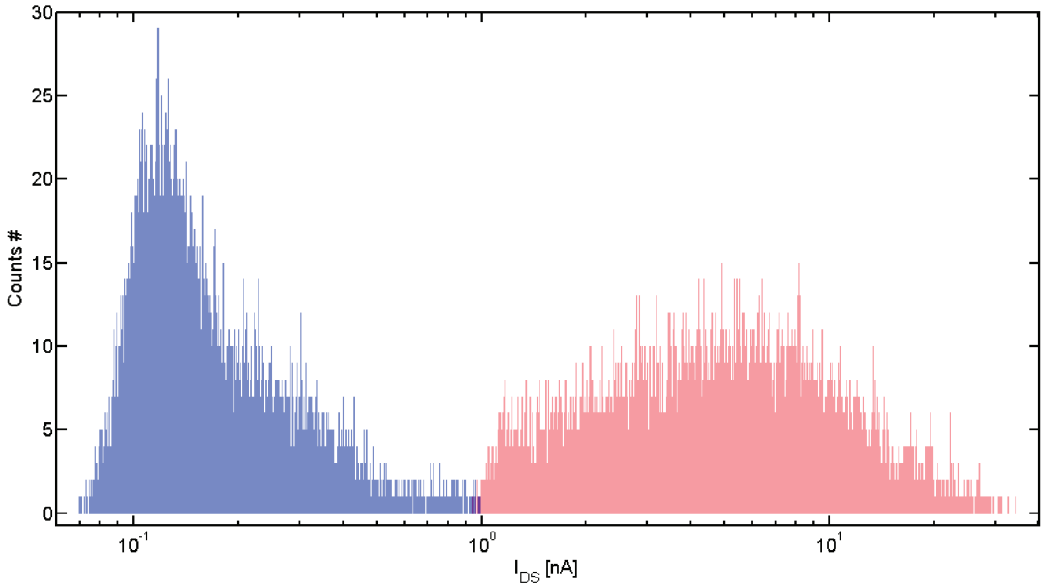

FIGURE 5.13 A histogram showing variation in the ON-state (red) and OFF-state (blue) when testing the endurance of CNT-FET memory device. The ON-state is centered at 4.80 nA with a standard deviation of 4.47 and the OFF-state is centered at 0.14 nA with a standard deviation of 0.11. In the valley between these two peaks bins that contain counts from both states are shown in purple. These occur due to aging of the device. Adapted with permission from the paper A.IV of this thesis.

of oxides as gate insulators, we showed that the amount of hysteresis in CNT-FETs can be controlled by the design of the gate dielectric (paper A.II of this thesis). That study thus indicates that defects in the nanotube are a minor contributor in the hysteresis. (4) Therefore, in the present case and as in the case in Section 5.2.2, the most likely explanation remains a model where stationary charge traps within the dielectric are dominating the hysteresis. An applied gate voltage could fill these charge traps with charge carriers moving in the CNT.

As high-κ dielectrics are being introduced to increase the physical thickness of the Si-MOSFET gate dielectric, a lot of recent research has focused on studying charge trapping, particularly in HfO_2 [166]. It has been shown that HfO_2 has fast, significant charge trapping [167] and thicker oxide layers exhibit stronger charge trapping [168, 169]. This indicates that the traps are located at the bulk of the HfO_2. The fast charge trapping and detrapping we observe could be due to charging and discharging of pre-existing bulk defects since no defect generation has been observed in measurements [170]. Based on their measurements, Kerber *et al.* suggested a defect states model to explain the experimental data [170]. This model is also supported by spectroscopic ellipsometry measurements, where an additional absorption peak exists in the range 0.7 – 1.2 eV below bottom of the conduction band of HfO_2 [171]. These defect states, available within the band gap of HfO_2, are attributed to oxygen

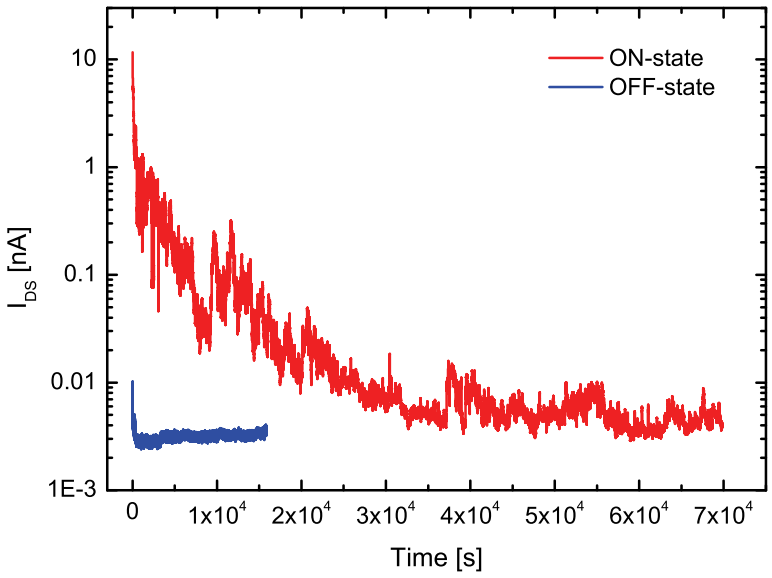

FIGURE 5.14 Retention time for the ON and OFF states of a CNT-FET memory device. The ON state has an exponential decay to the OFF state with a retention time of about $\sim 1.5 \times 10^4$ s, while the OFF state stays relatively unchanged throughout the measurement. Adapted with permission from the paper A.IV of this thesis.

vacancies which have a large electron affinity [171, 172] and they can function as electron traps [171].

To show that charge trapping in the HfO_2 defects is a likely process in our case for the high speed operation, we estimated the band alignments for our devices, see Figure 5.15. The flat band case for the $Si/SiO_2/HfO_2/CNT/HfO_2$ energy band diagram together with the defect states in HfO_2 layers are depicted in Figure 5.15a. We calculated the semiconductor band alignments using the Schottky barrier theory presented in Section 3.3.1. The oxides were considered as wide-band-gap semiconductors and their conduction band offsets determined by matching the charge neutrality levels of each semiconductor, modified by the Schottky pinning parameter as presented in Equation 3.5. For the CNT, we took into account that it is in contact with electrodes made of palladium which has the work function of 5.12 eV. Note that we used the values for intrinsic Si although in our experiment the substrate was highly doped p-type Si; the result for p-type Si would be modified only slightly and, especially, this does not affect the $CNT - HfO_2$ alignment which is the main point here. Also, for HfO_2 we used the experimentally determined band gap of 5.7 eV [171], which is slightly smaller than the theoretical band gap of 6 eV. The location and width of the HfO_2 defect states is also taken from the experiment in Ref. [171]. The charge traps located above the CNT can be efficiently charged with positive gate bias by electron tunneling from the conduction and valence bands of the CNT as shown in Figures 5.15b and 5.15c, even for rather small gate voltages.

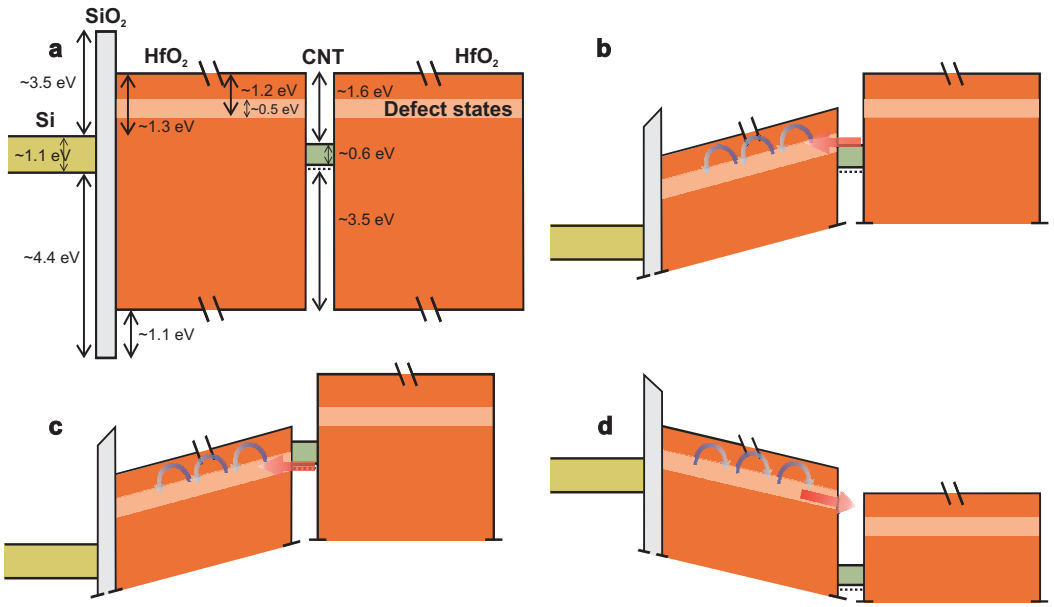

FIGURE 5.15 Schematic energy band diagram for a $Si/SiO_2/HfO_2/CNT/HfO_2$ gate stack containing defect states in the HfO_2 layers. **a,** The flat band condition without taking into account voltage drops within the dielectric. The CNT band gap is calculated for a 1.4 nm diameter tube. **b,** and **c,** Band profile when writing with positive gate voltage. The electrons tunnel from the conduction and the valence band of CNT to the defect states in HfO_2. **d,** Band profile when the stored electrons are erased from the HfO_2 by applying a negative gate voltage. The band bending induced by the gate operation in **b, c,** and **d,** is omitted for clarity and the diagram represents the positions of bands away from the interface. Adapted with permission from the paper A.IV of this thesis.

This corresponds to the Write-sequence of the memory. During the Erase-sequence, depicted in Figure 5.15d, the defect states can be discharged by tunneling to the CNT. This model can also explain qualitatively the observed short ON state retention time. When the memory is written to ON state with a positive gate voltage, the HfO_2 layer stores negative charge. As there is no additional tunneling oxide between the CNT and trapped charges in the HfO_2 layer, the electrons have only a small barrier to cross in order to tunnel back to the CNT. The thermal energy could assist this tunneling process. The retention time could possibly be made longer by having a thin, large band gap, and defect-free tunneling oxide between the CNT and HfO_2 charge trap layer.

Chapter 6

Transport through double barrier structures in carbon nanotubes

A one-dimensional periodic potential barrier structure, or superlattice, in monocrystalline semiconductors was first considered theoretically by Esaki *et al.* in 1970 [173]. They predicted that this kind of structure would host intriguing transport properties such as negative differential resistance (NDR). When the Fermi energy of the electrode coincides with the quasistationary states of the potential well, the resonance is shown to give rise to current maxima [174].

The first demonstration of NDR was done by Chang *et al.* in a GaAs double barrier structure, just four years after the prediction [175]. Since then, NDR has been observed in molecular devices as well [176–178]. More recently, carbon nanotube devices have been emerging that exhibit NDR in their electrical characteristics due to many different phenomena. These consist of chemical doping [179], introducing defects [180] or having heterojunctions within the same tube [181, 182]. NDR is observed also in bundled or multi-walled CNTs [25, 183] and in CNT devices with quantum dots between the metal contact and the CNT [184]. So far the NDR in these devices has been uncontrolled and not suitable for mass production. In this chapter, I will discuss and demonstrate controllable and gate-tunable NDR in CNT field-effect transistors, both at room temperature and at 4.2 K. This is achieved by creating quantum dots into the CNT channel by patterned, high-κ gate oxide. This method can be easily scaled up to mass production and it opens up a possibility for a new avenue for nanoscale electronic devices. The devices exhibiting NDR could be used for fast switching elements [185], nanoscale amplifiers [186], and oscillators working with THz frequencies. The discussion in this chapter follows paper A.V of this thesis.

6.1 Introduction to quantum dots

For understanding properties of double barrier structures, we can consider a so called quantum dot. A quantum dot (QD) [187–189] is a small electron box in a solid-state device or material, with sizes typically ranging from nanometers to a few microns. The focus in this section will be on properties of QDs that are coupled via two tunnel barriers to reservoirs, with which electrons can be exchanged as shown in Figure 6.1. Otherwise, the QD has similar structure as e.g. MOSFET, with the reservoirs being the source and drain, and the dot is coupled capacitively to one or more gate electrodes. By biasing the device, the electronic properties of the QD can be measured with gate electrodes tuning the electrostatic potential of the dot with respect to the reservoirs.

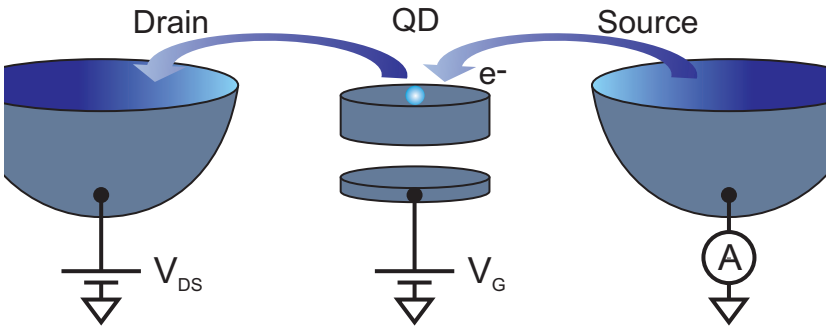

FIGURE 6.1 A schematic of a quantum dot in a lateral configuration. The quantum dot (shown as disk) is connected to source and drain reservoirs via tunnel barriers. The current through the device is measured in response to a bias voltage V_{SD} and a gate voltage V_G.

Quantum dots contain an integer number of conduction electrons, and in semiconductor QDs the number of trapped electrons can be reduced to 0, or 1, 2, etc. or extended to a puddle of several thousands. Two effects dominate the electronic properties of quantum dots. First, the Coulomb repulsion between electrons on the dot leads to an energy cost for adding an extra electron to the dot, called the charging energy (E_C). Due to charging energy, tunneling of electrons to or from the reservoirs can be suppressed at low temperatures. This phenomenon is known as the Coulomb blockade [190, 191]. Second, the confinement of electrons in all three spatial directions leads to quantum effects namely to quantized energy spectrum. This makes the electronic properties of quantum dots similar with those of atoms and therefore quantum dots are regarded as artificial atoms [192].

There are two electrical measurement techniques usually used in QD measurements: (1) transport of electrons through the dot while measuring the current and (2) detection of changes in the number of electrons on the dot with a nearby electrometer, so-called charge sensing. With the second technique, the dot can be probed

without the need of current flow through the dot. The charge sensing can be implemented in different ways: a single-electron transistor [193,194], a second electrostatically defined quantum dot [195] or a quantum point contact (QPC) [196] can be fabricated next to the dot. The QPC is the most widely used because of its ease of fabrication and experimental operation. For quantum information purposes, charge detection is preferred since it still functions for very small couplings to reservoirs. For studying transport properties of double barrier structures we concentrate on the current measurement technique but both techniques can be conveniently understood with the constant interaction model. In the next section, I will use this model to describe the physics of single quantum dots and show how relevant device parameters can be extracted from measurements.

6.2 The constant interaction model

The constant interaction model is based on two assumptions. First, the Coulomb interactions among electrons on the dot and with all other electrons in the environment are parameterized by a constant capacitance C. This capacitance is the sum of the capacitances between the dot and the source C_S, the drain C_D, and the gate C_G: $C = C_S + C_D + C_G$. Note here for CNT QDs, when operating in the quantum capacitance limit, the C_Q needs to be taken into account (see Section 2.3.2). Secondly, the discrete single-particle energy spectrum is independent of Coulomb interactions and therefore of the number of electrons on the dot. Under these assumptions, the total energy $U(N)$ of a dot having N electrons in the ground state is given by [189]

$$U(N) = \frac{[-|e|(N - N_0) + C_S V_S + C_D V_D + C_G V_G]^2}{2C} + \sum_{n=1}^{N} E_n(B), \tag{6.1}$$

where e is the electron charge, $N = N_0$ for $V_G = 0$ and B is the applied magnetic field. The voltages V_S, V_D, and V_G applied to the source, drain, and gate, respectively are taken into account in Equation 6.1. The terms $C_S V_S$, $C_D V_D$, and $C_G V_G$ represent an effective induced charge on the dot. These terms can be changed continuously in order to change the electrostatic potential on the dot. The last term of Equation 6.1 depends on the characteristics of the confinement potential and is the sum over the occupied single-particle energy levels $E_n(B)$, which can be neglected from now on in the discussion.

The electrochemical potential $\mu(N)$ of the dot can be defined as [189]

$$\begin{aligned} \mu(N) &\equiv U(N) - U(N-1) \\ &= (N - N_0 - \frac{1}{2})E_C - \frac{E_C}{|e|}(C_S V_S + C_D V_D + C_G V_G) + E_N, \end{aligned} \tag{6.2}$$

where the charging energy $E_C = e^2/C$. The first two terms in electrochemical potential are describing the electrostatics of $\mu(N)$ and the last term (E_N) is the chemical potential of the system, giving the energy of the topmost filled single-particle level. Here $\mu(N)$ denotes the transition energy between the N-electron ground state ($GS(N)$), and the $(N-1)$-electron ground state ($GS(N-1)$).

Examination of Equations 6.1 and 6.2 shows that the energy has a quadratic dependence on the gate voltage, whereas the electrochemical potential has a linear dependence . This makes the dependence the same for all N electrons and the whole "ladder" of electrochemical potentials can be moved up or down while the distance between the levels remains constant. Sometimes deviations from this model are observed when both the source-drain voltage and gate voltage are varied over a very wide range, e.g. in carbon nanotube quantum dots. [197]. Anyway, the linear dependence of $\mu(N)$ on the gate makes the electrochemical potential the most convenient quantity for describing electron tunneling.

The energy difference between the consecutive electrochemical potentials of the ground states is called addition energy, given by

$$E_{add}(N) = \mu(N+1) - \mu(N) = E_C + \Delta E, \tag{6.3}$$

where ΔE is the energy spacing between two discrete quantum levels. If two electrons are added to the same spin-degenerate level, the ΔE can also be zero.

When a bias voltage is applied between the source and drain reservoir, a window in energy opens up between μ_S and μ_D of $\mu_S - \mu_D = -|e|V_{DS}$. This energy window is conveniently called the bias window. When an electrochemical potential level enters to the bias window, electrons can tunnel from the filled reservoir onto the dot and off to the empty states in the other reservoir and a flow of current is established. For a quantum dot to be well defined with discrete energy levels the temperature needs to be negligible compared to the energy-level spacing ΔE. When this condition is fulfilled, the size of the bias window separates two regimes. In the low-bias regime only one level on the dot is within the bias window at a given time ($-|e|V_{DS} < \Delta E$). In the high-bias regime multiple levels on the dot can be in the bias window at the same time ($-|e|V_{DS} \geq \Delta E$ and/or $-|e|V_{DS} \geq E_{add}$).

6.2.1 Low-bias regime

An electron transport through a quantum dot is only possible when an electrochemical potential level is in bias window, i.e. $\mu_S \geq \mu(N) \geq \mu_D$ (Figure 6.2b). If there is no level in the bias window, the number of electrons on the dot remains fixed and no current flows through the dot (Figure 6.2a). This is known as the Coulomb blockade. The condition between these two states can be continuously varied by changing applied gate voltage. When $\mu(N)$ level is on the bias window, an electron from the source can tunnel to the dot and then to the drain. This cycle is known

as single-electron tunneling and during the cycle the electron number on the dot is varied between $N-1$ and N.

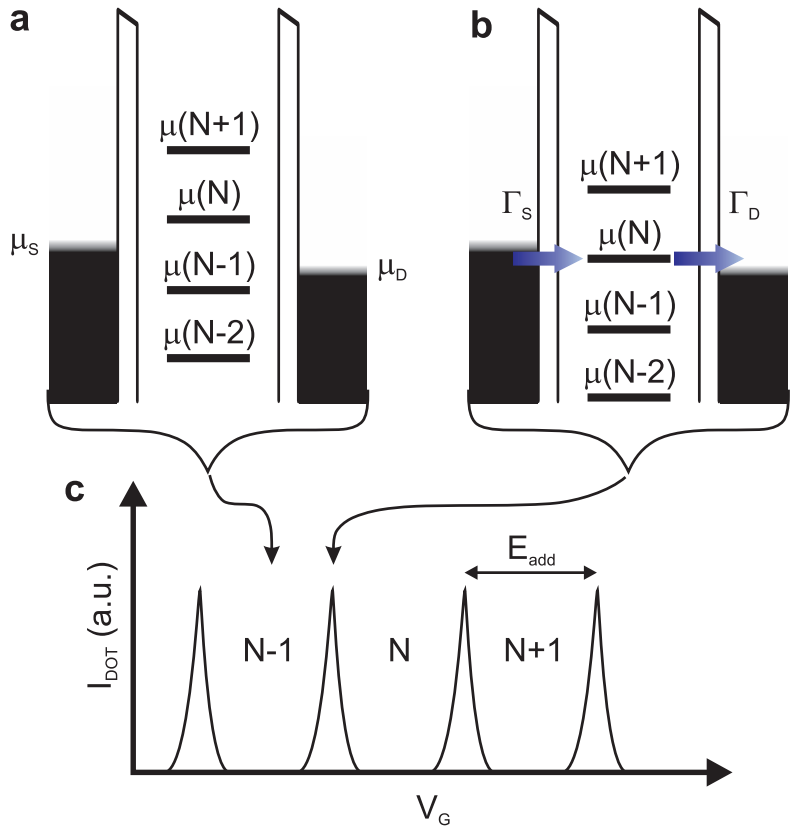

FIGURE 6.2 Schematic of a quantum dot in the low bias regime. **a,** No electrochemical level is in the bias window. The electron number is fixed to $N-1$ due to Coulomb blockade. **b,** The $\mu(N)$ level has entered to the bias window and the electron number fluctuates between $N-1$ and N. As a result, tunneling current flows through the dot, with the magnitude of the current depending on the tunnel rate between the dot and the reservoirs on the left (Γ_S) and on the right (Γ_D). **c,** The current (I_{DOT}) through the dot as a function of gate voltage V_G and with constant V_{DS}. The arrows mark the places where the level alignments of a and b occur.

With constant drain-source bias, when the gate voltage is swept while measuring the current through the dot (I_{DOT}) a trace is obtained as schematically shown in Figure 6.2c. Between the peaks the number of electrons on the dot is fixed due to Coulomb blockade. At the gate voltage corresponding to the Coulomb peaks, a level is aligned with the bias window and tunneling current flows. By tuning the voltage between consecutive valleys, the electron number on the dot can be varied. The distance between peaks corresponds to E_{add} through the proportionality factor $\alpha = (C_G/C)$, as can be seen by examining Equations 6.2 and 6.3. The addition energy can be determined from the peak spacing by $E_{add}(N) = e\alpha(V_G^{N+1} - V_G^N)$, where V_G^N and V_G^{N+1} are gate voltages corresponding to the Coulomb peaks N and $N+1$.

Thus, this approach gives a way to examine the energy spectrum of the dot.

6.2.2 High-bias regime

A more straightforward and more informative way to examine the energy spectrum of the dot is to include multiple dot levels in electron tunneling. This can be done by increasing V_{DS} so high that many levels fall into the bias window. In the following the drain electrode is considered to be grounded, i.e. $\mu_D = 0$. When a negative voltage is applied between the source and the drain, μ_S increases, as shown in Figure 6.2a and b. Also the levels in the dot increase in energy, due to the capacitive coupling between the source and the dot, as can be seen from Equation 6.2. This increase of the dot levels is so called lever arm effect. When V_{DS} is further increased a second conduction path corresponding to an exited state can fall into the window as shown in Figure 6.3a. Usually this will lead in increase in current, which enables energy spectroscopy of the excited states. When further increasing the V_{DS} until the bias window is larger than the addition energy, a second ground state can enter to the window leading to double-electron tunneling (Figure 6.3b) where the electron number alternates between $N-1$, N, and $N+1$.

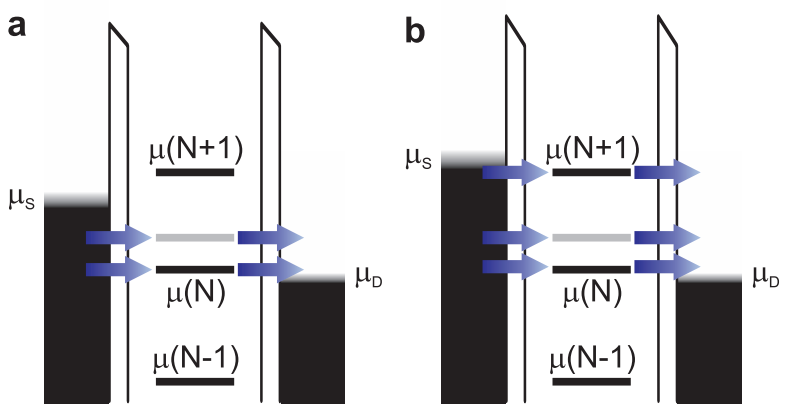

FIGURE 6.3 Schematic of a quantum dot in the high bias regime. The level in grey corresponds to the exited state of $GS(N)$. **a,** Applied V_{DS} exceeds ΔE and electrons can tunnel via both the ground and the exited state. **b,** Increasing the V_{DS} further to exceed the E_{add} leads to double-electron tunneling via two ground states.

To use the multiple dot levels effectively, both the V_{DS} and the V_G voltage can be changed continuously, in order to map out the current spectrum of the dot. If we consider two successive ground states $GS(N)$ and $GS(N+1)$ and the corresponding excited states $ES(N)$ and $ES(N+1)$, separated from the ground states in energy by $\Delta E(N)$ and $\Delta E(N+1)$, respectively (see Figure 6.4a), we end up having the electrochemical potential ladder illustrated in Figure 6.4b. The transition between the two excited states is omitted for clarity. The electrochemical potential ladder (in Fig-

ure 6.4b) can also be used to define the places of transitions in the gate voltage axis of the differential conductance plot, shown in Figure 6.4c. At the positions of the transitions in V_G the electrochemical potential level in the dot is aligned with μ_S and μ_D with $V_{DS} = 0$. When sweeping the gate with low V_{DS}, the electron tunneling is only possible at the gate voltage indicated by $GS(N) \leftrightarrow GS(N+1)$, similarly as shown in Figures 6.2b and c. For all other gate voltage values shown in the Figure 6.4c the quantum dot will be in the Coulomb blockade.

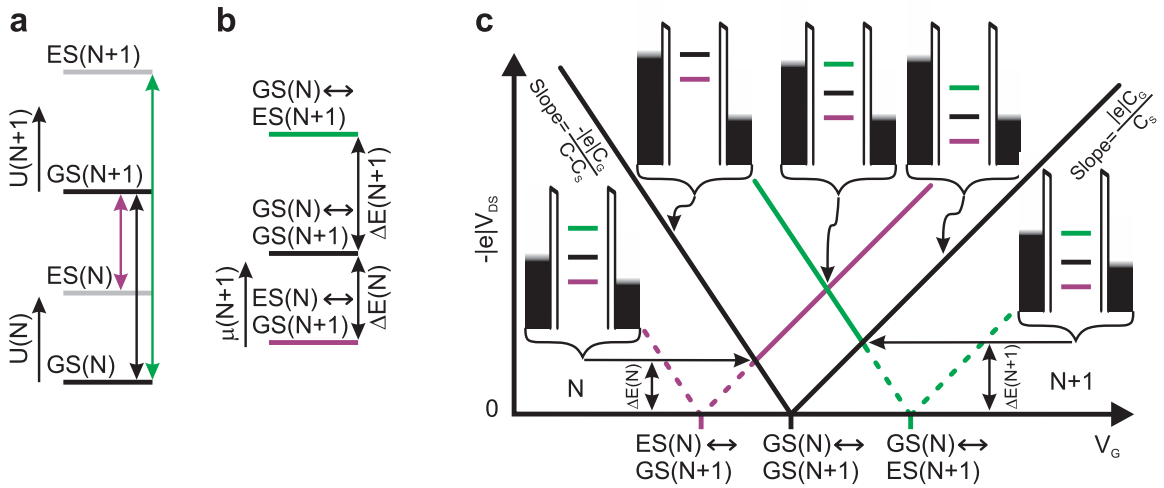

FIGURE 6.4 Schematic of a quantum dot measurement in the high bias regime. **a,** Possible transitions (indicated with arrows) between the consecutive ground and excited states. **b,** The transitions depicted in a, shown as an electrochemical potential ladder. **c,** A schematic of the differential conductance $\partial I_{DOT}/\partial V_{DS}$ as a function of both $-|e|V_{DS}$ and V_G. The level alignment is indicated at several positions with schematic diagrams of electrochemical potential levels.

In the differential conductance plot, $\partial I_{DOT}/\partial V_{DS}$, versus ($-|e|V_{DS}$, V_G) plane (Figure 6.4c), a V-shaped area is outlined for each transition, where the electrochemical potential corresponding to the particular transition enters to the bias window. Within this area, the $\mu(N)$ level stays in the window. The transition between N and $N+1$ electron ground states defines the region within where tunneling is possible (V-shaped black line). For all other gate and bias voltages shown in the Figure 6.4c the quantum dot will be in Coulomb blockade. The colored solid lines show the places where an exited state enters to the bias window and the current changes. In the measurement such a data set is assembled by first taking a trace of $\partial I_{DOT}/\partial V_{DS}$ versus V_{DS} while keeping a fixed value for V_G. For the next trace, V_G is changed slightly and the bias voltage trace is taken again. This procedure is repeated until the desired V_G range is acquired. The slopes of the edges of transitions depend on capacitances of the system. When the drain reservoir is grounded, i.e. $V_D = 0$, the two slopes of $\partial(-|e|V_{DS})/\partial V_G$ corresponding to a transition are $-C_G/(C - C_S)$ and

C_G/C_S.

The lines in Figure 6.4c indicate the places of finite $\partial I_{DOT}/\partial V_{DS}$. The line terminating to the N electron Coulomb blockade region outside the V-shaped transition region, involving the two ground states, is a transition involving N electron excited state. Similarly, the $N+1$ electron excited state terminates on the $N+1$ electron Coulomb blockade region. The bias window exactly equals to the energy level spacing at the points where a transition line involving an excited state touches the Coulomb blockade region and the level spacing can be read off straight from the $-|e|V_{DS}$ axis.

When also the positive bias voltages are swept in the measurement, producing similar plot than in Figure 6.4c, the Coulomb blockade regions appear as diamond shapes in the differential conductance plot. These are called Coulomb diamonds. Since inside the diamonds the number of electrons is fixed and the charge (eN) on the dot is stable, this plot is often called a stability diagram.

6.3 Negative differential resistance in carbon nanotube field-effect transistors

In semiconducting carbon nanotube, the forbidden band gap offers a possibility to use the intrinsic properties of CNTs in inducing quantum confinement. In this section I will discuss how we can use the band gap to induce p-n junctions in the channel of a CNT-FET, and more importantly, the consequent NDR in CNT-FETs and the implications of it. We induce NDR to the CNT-FETs by patterning the atomic layer deposited gate oxide (described in Section 4.1) of the device, resulting in strong charge trapping at specific places within the gate oxide. With sufficient gate voltages the charge trapping induces p-n junctions in the channel of the CNT-FET and quantum confinement.

A cross-section of the devices together with the patterned profile of the grown ALD layers is illustrated in Figure 6.5a. The patterned high-κ gate oxide was used to influence the local electrical properties of our transistors. An AFM image of the ALD structure together with a cross shaped AFM marker is shown in Figure 6.5b. In the dark grooves, there is only a layer of $\mathrm{HfO_2}$ (20 nm) on top of the silicon wafer. Between the lines, additional layers are grown comprising of $\mathrm{TiO_2} - \mathrm{HfO_2}$ with nominal thickness of 0.5–1 nm, called ALD islands (AI) in the following.

An AFM image of a device together with a schematic of the measurement setup and the ALD islands is shown in Figure 6.5c, where a CNT is connected with Pd (30 nm) drain (D) and source (S) electrodes. The silicon wafer was used as a backgate for three terminal operation. The drain-source and gate-source voltage bias was supplied for all the measurements from a home-made voltage distribution box powered by batteries and computer-controlled via a data acquisition card. We studied these

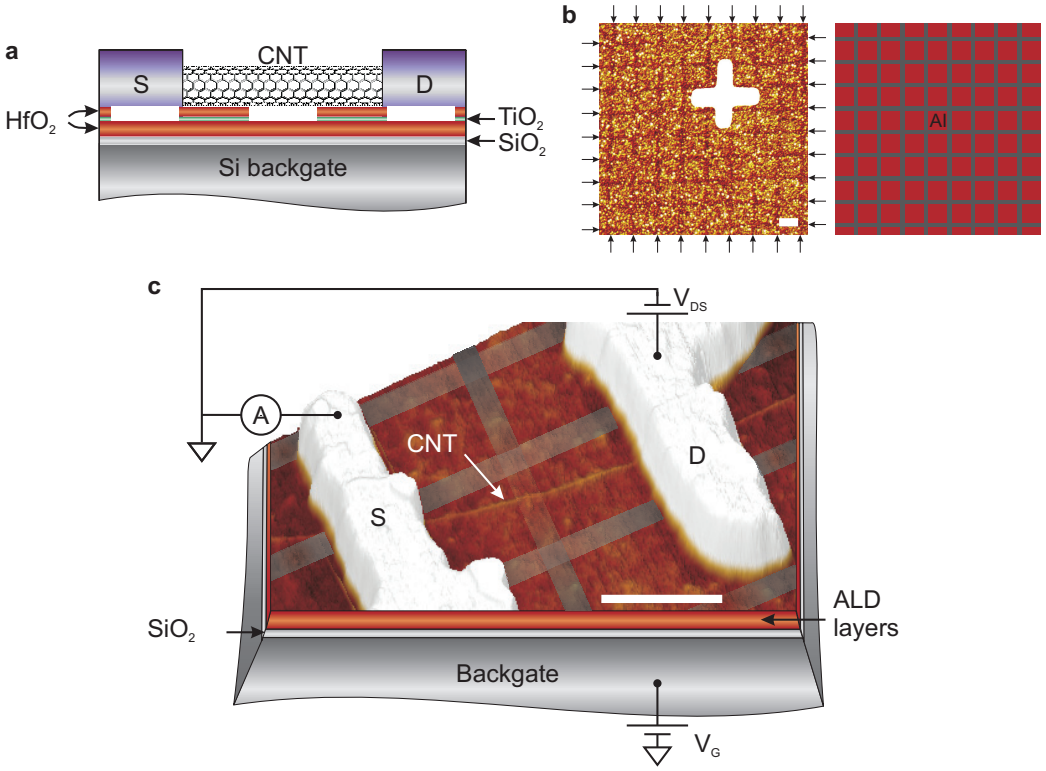

FIGURE 6.5 Integrating patterned gate oxide with CNT-FETs. **a,** A cross-section of our CNT-FETs having ALD grown triple layer of $HfO_2 - TiO_2 - HfO_2$ with patterned upper two layers of $TiO_2 - HfO_2$. The nanotube is contacted with palladium (30 nm) drain (D) and source (S) electrodes. **b,** An AFM image together with a schematic of ALD grown $TiO_2 - HfO_2$ islands. In the grooves highlighted with arrows, there is a single layer of HfO_2 (20 nm) and between these grooves are additional layers of $TiO_2 - HfO_2$ (0.5 – 1 nm) forming squares of $\sim$200 $\times$ 200 nm. The width of the groove between the islands is measured with AFM to be $\sim$50 nm. Also an AFM marker is visible in the image (see Section 4.2). **c,** An AFM image of a device where a CNT is connected to drain (D) and source (S) electrodes having channel length of $\sim$400 nm. The measurement setup is also schematically illustrated. Between the CNT and the gate we have the ALD island structure. Scale bars are 200 nm.

devices both at room temperature and at 4.2 K. The room temperature measurements were done at ambient conditions as well as in vacuum for reducing surface chemistry effects, e.g. adsorbed water. Vacuum measurements were done in a home-made vacuum chamber at a pressure of 1.3×10^{-2} mbar. The liquid helium measurements at 4.2 K were done with a home-made dip-stick, where the sample was situated in a helium atmosphere of a few mbar, isolated from the liquid helium. All measurements were carried out in an electrically shielded room. The gate voltage sweep direction was in Figures 6.7, 6.8, 6.12 and 6.13 from negative to positive. The CNT-FET channel lengths in this study were 400 $\pm$ 10 nm and the diameters of the CNTs ranged from 1.3 – 3.4 nm, based on AFM images.

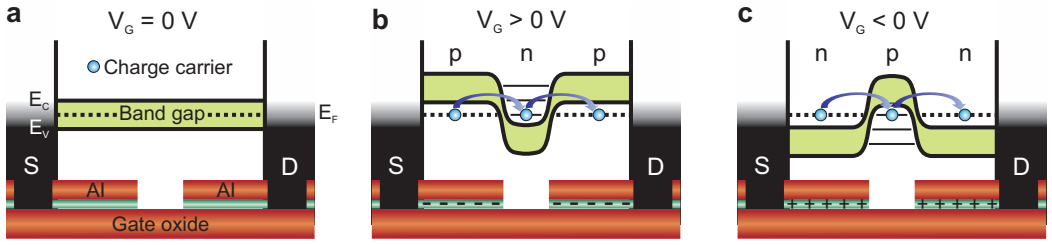

FIGURE 6.6 Quantum dots defined by charging the ALD island structure. **a,**The flat band case at zero gate voltage. The Fermi level (E_F) within the band gap of the CNT is aligned with the drain (D) and source (S) electrodes and the ALD islands (AI) are neutral. **b,** A positive gate voltage pulls electrons from the CNT to the ALD islands which in turn screens the applied V_G. Between the islands, the oxide stays uncharged and the conductance band (E_C) is pulled below the Fermi level. The resulting p-n junctions define a quantum dot with discrete electronic states. When a resonant level is aligned with the Fermi level the charge carriers can flow. **c,** The electrons are ejected from the ALD islands by applying a negative gate voltage and the remaining positive charge screens the V_G above these sections. Between these islands, the valence band (E_V) is pulled above the Fermi level and the resulting p-n junctions form a quantum dot.

When the ALD islands become charged due to modulation of the gate voltage, p-n junctions are formed in the conduction channel of the CNT. These p-n junctions form tunnel barriers, effectively forming a quantum dot in the middle of the CNT [197]. The resonant electrochemical potential levels on the dot enable the NDR phenomenon [198]. This is schematically illustrated in Figure 6.6. With zero gate voltage, the ALD islands are neutral (Figure 6.6a), corresponding to the flat band case. When the gate voltage is increased, electrons can tunnel from the CNT to the ALD islands making them charged (Figure 6.6b). The charge stored within the islands screens the applied gate voltage. Thus, the sections above these regions, forming the drain and source sections of the CNT, see a weaker electric field. On the other hand, the region between the islands stays uncharged and in this region the positive gate voltage can lower the bands in energy. When a sufficiently high voltage is applied to the gate, the CNT band gap descends below the Fermi level (E_F) and forms an n-type quantum dot with discrete electronic states. At a fixed gate voltage, with increasing amplitude of the drain voltage ($V_S = 0$), the current increases at first, until a resonant tunneling level aligns with the Fermi level and the current reaches a local maximum. When further increasing the amplitude of the drain voltage, the resonant level moves below the Fermi level of the p-type CNT drain section and the current drops, until the next resonant level enters to the bias window. This is analogous to the negative differential resistance observed in double barrier structures like GaAs quantum dots [175, 199, 200]. Similarly, we can have a p-type quantum dot (Figure 6.6c).

A differential conductance plot measured for device D2, at 4.2 K, is shown in

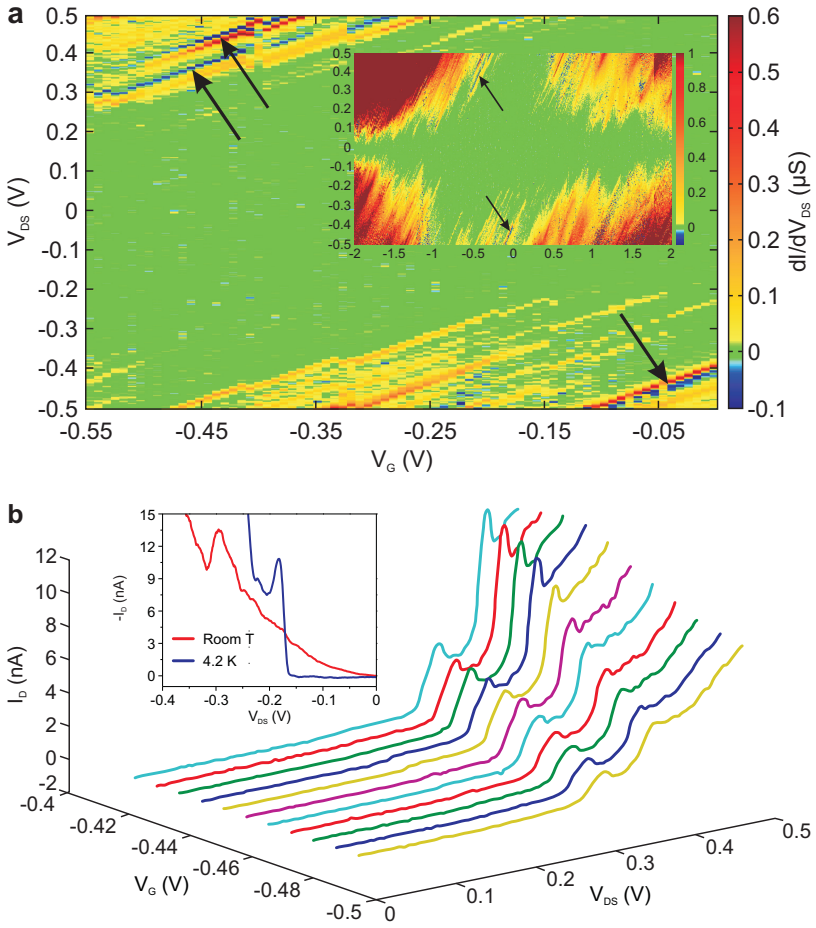

FIGURE 6.7 Negative differential resistance in gate-oxide designed CNT-FETs. **a,** Differential conductance for device D2 measured at 4.2 K. The NDR regions are shown with blue and indicated with arrows. NDR is visible in both positive and negative bias voltages. In positive bias the NDR is related to two different resonant tunneling levels. In the inset is shown a larger parameter space from the same device. The NDR occurs in the vicinity of the CNTs band gap as indicated by arrows. **b,** The development of the NDR related to the two resonant levels. When sweeping the gate to more positive voltages, the NDR corresponding to the first resonant level increases only slightly while the NDR related to the second localized level has a twenty-fold increase. In the inset: current vs voltage curves for the device D1 measured at room temperature (red) and at 4.2 K (blue). Clear NDR peaks are visible for both, situated at around -0.3 V at room temperature and around -0.18 V at 4.2 K. The peak to valley ratio is 1.38 for room temperature and 1.45 at 4.2 K.

Figure 6.7a. The NDR is visible with both positive and negative drain-source voltages as diagonal lines that occur after a resonant level enters to the bias window, as highlighted with arrows. For positive drain-source bias we observe strong NDR peaks related to two resonant levels. Also the charging of the gate oxide is visible in the images as abrupt horizontal displacements of the slopes while sweeping the gate voltage. The inset of Figure 6.7a shows that the NDR emerges in the vicinity of the

band gap edge of the CNT which is also indicated by the p-n junction model. In Figure 6.7b, the first NDR feature is increased only slightly while changing the gate to more positive voltages, whereas the second NDR feature has a twenty-fold increase. These results show that the place of the NDR and more importantly its magnitude are tunable with the gate voltage. Moreover, this approach to induce NDR to CNT-FETs is fully scalable and the ALD islands providing the effect can be accurately positioned at any desired location on the underlying wafer. In the inset of Figure 6.7b two typical I_D versus V_{DS} curves are shown, measured in 1.3×10^{-2} mbar vacuum at room temperature and at 4.2 K. Clear NDR peaks are visible in both traces, situated at around -0.3 V at room temperature and around -0.18 V at 4.2 K. The difference between the peak and the valley current is $\sim$3.5 nA at room temperature and $\sim$4 nA for the same device measured in cold. In this study, we measured three large-band-gap CNT-FETs, all showing NDR.

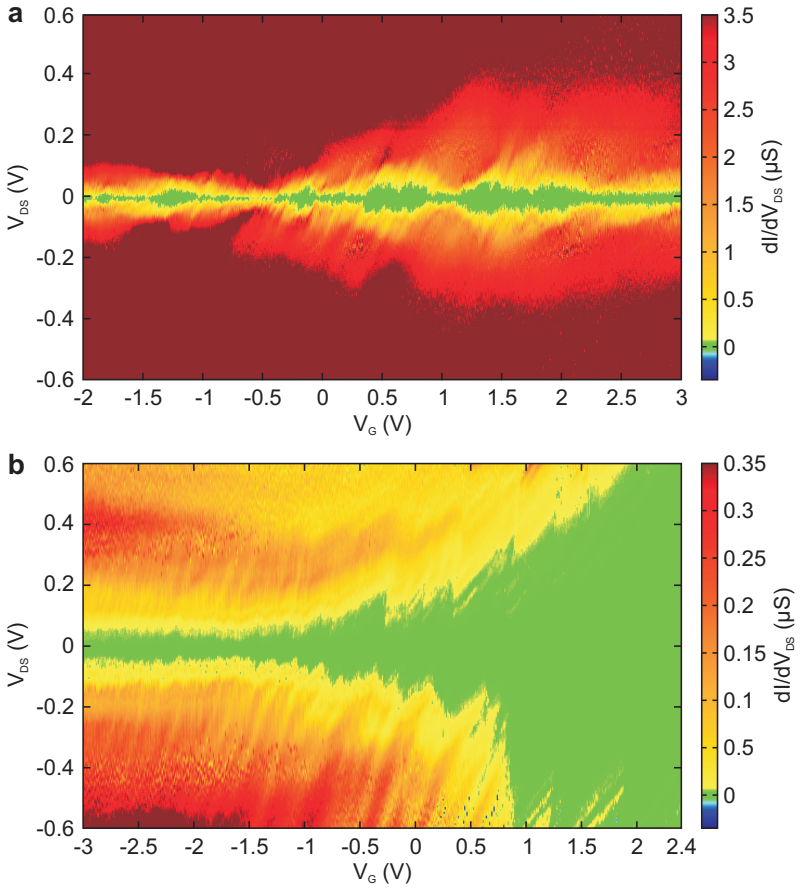

FIGURE 6.8 Differential conductance plots measured at 4.2 K for the devices RD1 and RD2 with non-patterned $HfO_2 - TiO_2 - HfO_2$ gate dielectric. **a,** Stability diagram of RD1. No clear band gap is visible in the measurement, showing the small band gap nature of the CNT. **b,** For the device RD2 band gap opens up at positive gate voltages, illustrating the large band gap nature of the CNT. There was no evidence of NDR in these devices.

For further evidence that the engineered structures within the gate oxide are causing the negative differential resistance in our devices, we also measured reference devices on a continuous $HfO_2 - TiO_2 - HfO_2$ (nominal thickness 40-0.5-1 nm) gate oxide, without the atomic layer deposition island patterning. The oxide was the same used in CNT-FET hysteresis study in Section 5.2. We performed the same measurements for these reference devices as for the ALD island samples. The results at 4.2 K are shown in Figure 6.8 in the form of differential conductance plots. For RD1 (Figure 6.8a), there is no wide band gap visible which is in agreement with the small ON/OFF ratio in of the transconductance measurements in Figure 6.10. This demonstrates the small band gap nature of the CNT. For the device RD2 (Figure 6.8b), the band gap gradually opens up at positive gate voltages, resulting in a completely closed structure for $V_G > 2$ V, illustrating the large band gap nature of the CNT. All together we measured three devices having the unpatterned triple layer gate oxide and in these reference devices we did not see any evidence of NDR.

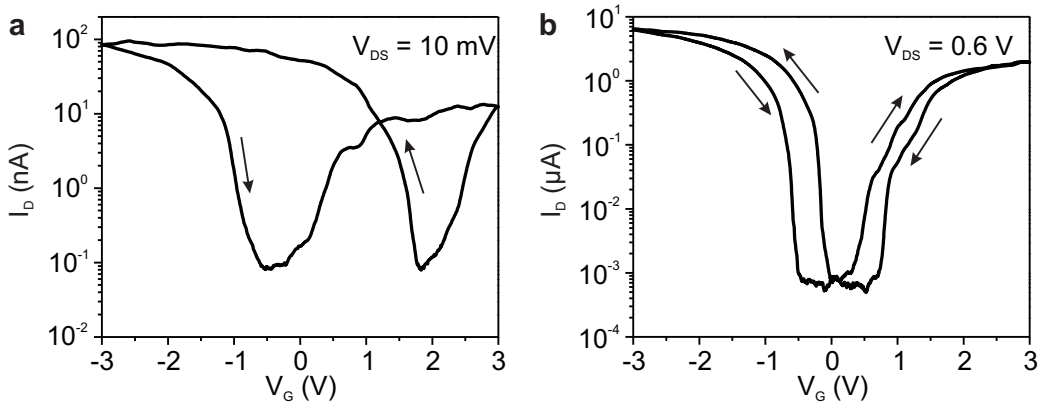

FIGURE 6.9 Hysteresis in the ALD island CNT-FETs. **a,** Transfer characteristics at room temperature with $V_{DS} = 10$ mV showing advanced hysteresis. The subthreshold slopes are for p-type ∼89 mV/dec and for n-type ∼161 mV/dec. **b,** Hysteresis at 4.2 K with $V_{DS} = 0.6$ V. The relative hysteresis decreases by 80% compared to the original room temperature hysteresis but it still remains strong. The corresponding subthreshold slopes are for p-type ∼17 mV/dec and for n-type ∼49 mV/dec.

In Chapter 5 was shown that ALD grown nanometer thick gate oxides of high-κ materials such as HfO_2, and layer structures such as $HfO_2 - TiO_2 - HfO_2$, are an efficient way to create controllable charge trapping in CNT devices. To further demonstrate that we have significant charge trapping in the ALD islands, we discuss results on the hysteresis seen in the measurements. We observe bipolar transconductance curves (Figure 6.9) for all the devices with the patterned gate oxide (ALD islands). This indicates that both the valence and conduction bands are contributing to the transconductance and makes band to band tunneling plausible [92]. In Figure 6.9b, the persistent advanced hysteresis at low temperatures shows that we have in these

devices very strong charge trapping within the oxide. For comparison, we also measured reference samples having uniform, *non-patterned* ALD grown triple layer of $HfO_2 - TiO_2 - HfO_2$ as gate oxide. The produced reproducible hysteresis loops are shown in Figure 6.10 and were measured at room temperature (Figure 6.10a) and at 4.2 K (Figure 6.10b). These hysteresis loops resemble those of the ALD island samples. At room temperature (Figure 6.10a) the relative hysteresis was 2.5 V/6 V. When measuring hysteresis at 4.2 K we used a higher (V_{DS}) voltage of 0.6 V to clearly see the hysteresis without any Coulomb blockade behavior visible in the measured traces. The triple ALD layer CNT-FET also displays strong advanced hysteresis at 4.2 K, with a relative hysteresis of 0.4 V/6 V, indicating that the triple layer gate oxide exhibits pronounced injected charge trapping "paper A.III and A.IV of this thesis".

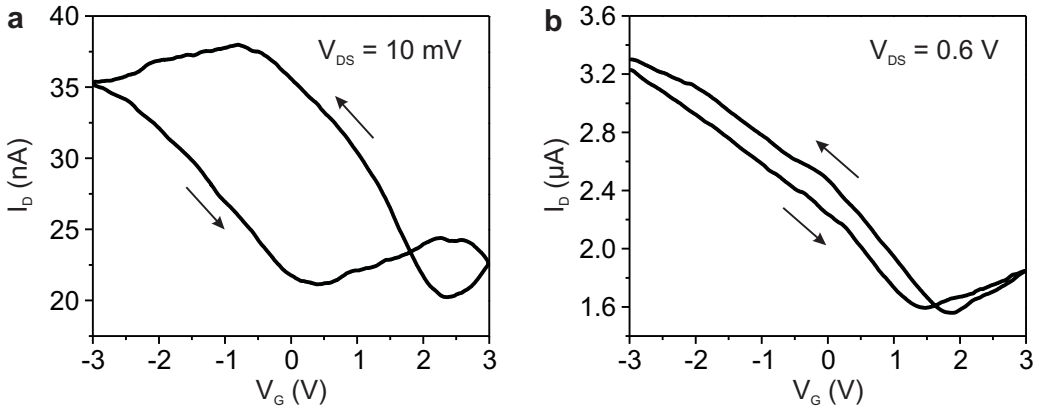

FIGURE 6.10 Hysteresis in CNT-FETs having ALD grown triple layer gate oxide. **a,** Transfer characteristics measured at room temperature with $V_{DS} = 10$ mV showing advanced hysteresis of a small band gap device RD1. **b,** Hysteresis at 4.2 K for the same device measured with $V_{DS} = 0.6$ V. The relative hysteresis decreases more than 80% compared to the original room temperature hysteresis but it still remains strong.

We measured also a reference device having more commonly used SiO_2 as its gate oxide. The transfer characteristics of the device with forward and reverse gate sweeps are shown in Figure 6.11. This device showed a strong unipolar behavior at room temperature with a relative hysteresis of 7.9 V/20 V as shown in Figure 6.11a. When taking the forward and reverse gate sweeps at 4.2 K, we do not see any hysteresis at all as shown in Figure 6.11b. This indicates that the main contribution to hysteresis at room temperature comes most likely from surface effects [136,147,149,160] e.g. water molecules adhered to the surface. At low temperatures these molecules are frozen and cannot be efficiently polarized with the gate voltage and the hysteresis diminishes [201].

We also measured at 4.2 K a differential conductance plot for the device having SiO_2 as its gate oxide, as shown in Figure 6.12. A wide band gap starts to open up

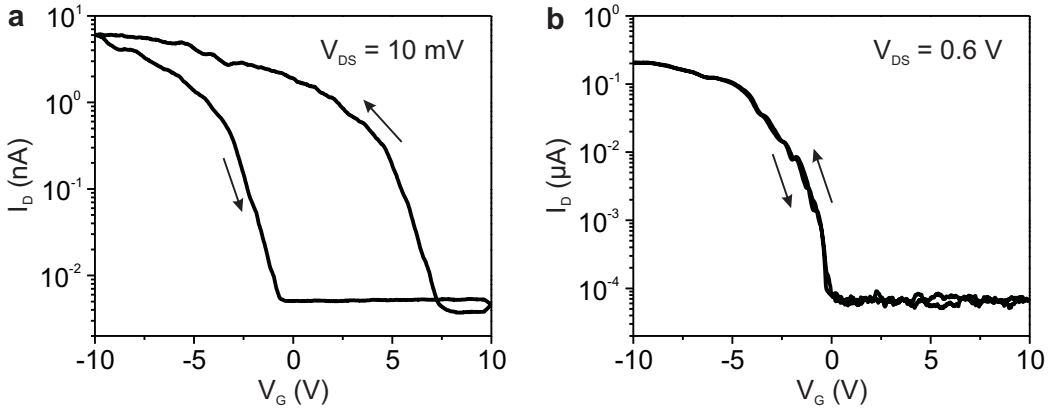

FIGURE 6.11 Hysteresis in CNT-FETs having commonly used SiO_2 as a gate oxide. **a,** Hysteresis measured at room temperature with $V_{DS} = 10$ mV showing strong advanced hysteresis of a large band gap device RD3. **b,** Transfer characteristics at 4.2 K for the same device measured with $V_{DS} = 0.6$ V. The hysteresis vanishes completely at low temperatures.

already at negative voltages, completely closing already at $V_G = 0$ V within our measured bias window. This illustrates the large band gap in this CNT. Also in this device, as in the devices having ALD grown continuous triple layer as a gate oxide, there was no evidence of NDR.

While these reference measurements either devices having ALD grown triple layer of $HfO_2 - TiO_2 - HfO_2$ and thermally grown SiO_2 as a gate dielectric showed similar results for hysteresis at room temperature and the triple layer reference sample also at 4.2 K, the SiO_2 reference sample did not show any hysteresis at 4.2 K. And most importantly, for both of these reference samples without the ALD island structure, we did not observe any NDR.

An earlier study found NDR in freely suspended nanotubes, and showed that it was induced at relatively large bias voltages due to self-heating and increased electron-phonon scattering [202]. This is not the case in our devices, since the nanotube rests on and is thermalized by the substrate. Also, the phenomenon observed here is different from multi-mode (multi-subband) effects observed in refs. [63,203], because multi-mode effects produce steps (or plateaus) in $I_D - V_{DS}$ and $I_D - V_G$ characteristics, not peaks and NDR as in Figure 6.7. Furthermore, in our case the separations between the subbands are hundreds of meV and not tens of meV that separates the NDR features. A more likely cause for the emergence of NDR is that a resonant tunneling level enters into the bias window. The phenomenon is related to band-to-band tunneling [92], where resonant tunneling from the valence into the conduction band and vice versa enables the flow of current through the device.

To quantitatively test the p-n junction and quantum dot model explaining the observed NDR, we estimate the expected energy level separation in the quantum dots formed by the ALD islands. From the AFM images shown in Figures 6.5b and c

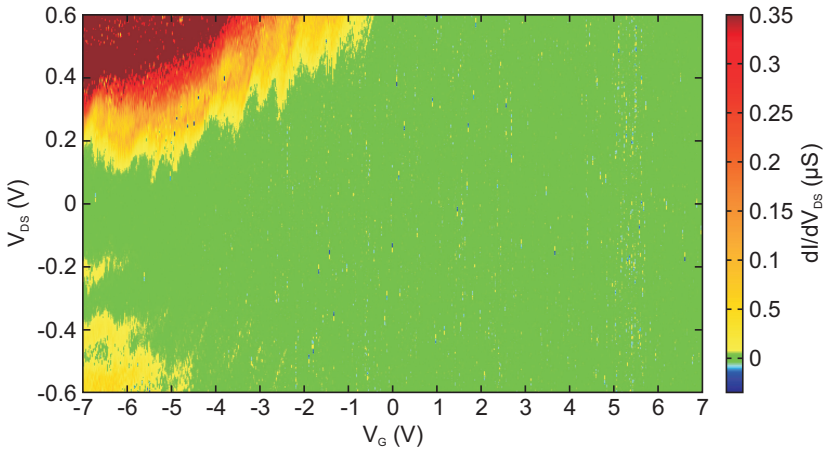

FIGURE 6.12 Stability diagram measured at 4.2 K for the device RD3 with non-patterned SiO_2 gate dielectric. A large band gap opens already at negative gate voltages. There was no evidence of NDR in this device.

we can estimate the quantum dot size to be ∼60 nm. We use the constant interaction model [187, 189] and the electrochemical potentials of transitions between successive resonant tunneling levels in the quantum dot to calculate the addition energy. The energy spacing in a simple particle-in-a-box picture is given by $\Delta E = h\nu_F/4L$, where ν_F is the Fermi velocity (8.1×10^5 m/s), h is Planck's constant, and L is the quantum confinement length. For the ∼60 nm quantum dot we obtain a level splitting of $\Delta E \approx 14$ meV. We use the Equation 2.13 to approximate the gate capacitance for our devices. Taking the HfO_2 dielectric constant of 25, and the thickness of 21 nm with the tube radius of 0.7 nm determined with AFM for D1, we can

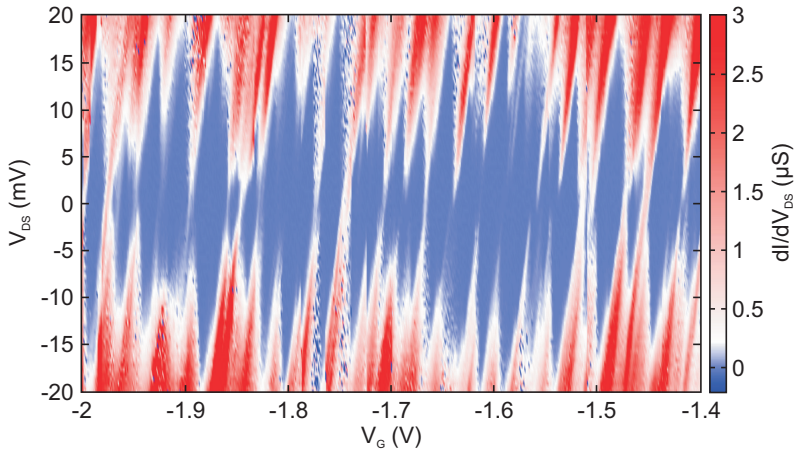

FIGURE 6.13 Stability diagram of the npn quantum dot. At 4.2 K, Coulomb blockade is visible in a series of diamonds and corresponds to a single electron charging of a quantum dot of the size ∼60 nm, having an addition energy ∼20 meV.

calculate the gate capacitance for the dot to be $C_G \approx 20$ aF. Using this, the total capacitance for the quantum dot can be extracted by measuring the ground-state lines forming the Coulomb diamonds in the stability diagram shown in Figure 6.13 as shown in Section 6.2.2. This yields $C_S \approx 2$ aF, $C_D \approx 3$ aF and $C \approx 25$ aF. For the charging energy this gives $E_C \approx 6$ meV, so the total addition energy would be $E_{add} = E_C + \Delta E \approx 20$ meV. This estimation of the addition energy fits remarkably well to our measured stability diagram in Figure 6.13 for D1, showing characteristic Coulomb blockade. Some of the diamonds are abruptly cut, supporting the conclusion that we have strong charging in these devices. In addition, we do not observe any modulation of the tunneling barriers as in the case of quantum dot formation by defects in CNT [204].

Chapter 7

Conclusions

In this thesis charging of the gate dielectric in CNT-FETs and the phenomena arising from the charging were studied. It was observed that CNT-FETs with SiO_2 gate dielectric sometimes exhibit hysteresis in their transfer characteristics. In contrast, if the gate dielectric is changed to Hf-based dielectric, hysteresis can be induced to *all* the CNT-FETs. If a gate stack of $HfO_2 - TiO_2 - HfO_2$ is used the distribution of their relative hysteresis gaps is narrow, and narrowing down further when the uppermost layer is changed from 3 nm to 1 nm. The CNT-FETs were operated in ambient conditions without any surface passivation. This indicates that there are stationary charge traps present beneath the upper layer that are dominating the electrostatic charging in the vicinity of the CNT so that the amount of hysteresis is relatively insensitive to the changes in the relative humidity. For example, if the relative humidity is lowered close to zero, the hysteresis in such a layered structure diminishes to $\sim$70% from the original, indicating that there is some contribution to the hysteresis from adsorbed water. In the same experiment, when having SiO_2 as a gate dielectric of CNT-FETs the reduction of hysteresis is much higher $\sim$50%. This observations support the conclusion of stationary charge traps in the layered dielectric. In the literature, there is still a debate about the magnitude of hysteresis induced by adsorbed water on the CNT-FETs having a gate dielectric of SiO_2 [136, 150, 160]. When different gate dielectrics are included to this field, new, more interesting questions are raised and possibly more insight to the mechanisms behind the different magnitude of induced hysteresis is gained. Nevertheless, the first results towards this goal and in inducing hysteresis to CNT-FETs with gate oxide design are presented. The Hf-based gate dielectrics are of particular interest for memory applications, providing to our knowledge the first proven route to 100% yield in single CNT-based memory elements.

When the properties of these CNT-FET-based memories were further studied, we showed that the memory elements made out of CNT-FETs can compete with commercial Flash-memories with 100 ns operation speed, largely exceeding the CNT-FET memory operation speeds reported previously. The endurance of these

memory elements is also good, exceeding 10^4 cycles. The findings are qualitatively explained by a charge trapping model, where HfO_2 has defect states situated above the CNT band gap in energy. The charge trapping in HfO_2 is known to be fast and efficient, and is likely to enable the high operation speed of our devices. While the operation speed and the endurance of these memories are outstanding, the retention time of $\sim 1.5 \times 10^4$ s leaves room for improvement. The charge trapping model suggests that it could be improved by adding a thin, defect-free tunneling oxide to separate the CNT and the charge traps. The CNT being a nanoscale ballistic conductor and that the essential features of the model, the defects in hafnium oxide together with the suitable location of the CNT band gap in energy are not dependent on detailed structure of the CNT indicates that the fast memory operation could potentially be realized also using other carbon materials such as double-wall CNTs, CNT bundles, or graphene ribbons.

In addition to the memory effects, charging of the gate dielectric can induce interesting and useful quantum mechanical effects, namely negative differential resistance at room temperature. By patterning the upper two layers of ALD grown $HfO_2 - TiO_2 - HfO_2$ triple layer gate oxide into separate islands, the charging within the gate oxide can be controlled. This in turn forms a quantum dot in the conduction channel of the CNT-FET, thus inducing NDR. The gate voltage can control the magnitude and the place where the NDR occurs in V_{DS}. This method is fully scalable and can be also used to generate NDR in other materials e.g. graphene ribbons and semiconducting nanowires. Most importantly, it enables a new class of low-cost nanoscale devices using NDR in their operation. For example, theoretical predictions of oscillations through CNT quantum dots having NDR suggests that they could reach tens of THz with output powers of several μW [205,206], surpassing the intrinsic limitations of state-of-the-art resonant tunneling diode oscillators made with conventional semiconductor technology with a record of 712 GHz in InAs/AlSb resonant-tunneling diode [207,208]. Our method could provide a way of making the first continuous wave oscillator that works well into the THz domain.

However, several challenges remain to be solved in order to make highly integrated carbon nanotube circuits. The direct production of single type CNT at large quantity is at the moment absent, although separation of single type CNTs from mixtures has been successful and shows a promise [24]. Also a challenge is the positioning the CNTs with nm precision on the integrated circuit. This has been pursued by either growing CNTs directly on the surface [104,209,210] or by placing them on the surface by means of electric fields [100,106] or self-assembly [105]. Yet another challenge is to provide each nanotube with a local, nanotube-specific gate that is wrapped around the tube. Progress towards this goal has also been done [211].

Bibliography

[1] Oberlin, A., Endo, M. & Koyama, T. Filamentous growth of carbon through benzene decomposition. J. Cryst. Growth 32 (1976) 335.

[2] Iijima, S. Direct observation of the tetrahedral bonding in graphitized carbon black by high resolution electron microscopy. J. Cryst. Growth 50 (1980) 675.

[3] Iijima, S. Helical microtubules of graphitic carbon. Nature 354 (1991) 56.

[4] Bethune, D. S., Klang, C. H., de Vries, M. S., Gorman, G., Savoy, R., Vazquez, J. & Beyers, R. Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls. Nature 363 (1993) 605.

[5] Iijima, S. & Ichihashi, T. Single-shell carbon nanotubes of 1-nm diameter. Nature 363 (1993) 603.

[6] Zheng, L. X., O'Connell, M. J., Doorn, S. K., Liao, X. Z., Zhao, Y. H., Akhadov, E. A., Hoffbauer, M. A.,Roop, B. J., Jia, Q. X., Dye, R. C., Peterson, D. E., Huang, S. M., Liu, J. & Zhu, Y. T. Ultralong single-wall carbon nanotubes. Nat. Mater. 3 (2004) 673.

[7] Avouris, Ph., Chen, Z. & Perebeinos, V. Carbon-based electronics. Nat. Nanotechnol. 2 (2007) 605.

[8] Dai, H., Javey, A., Pop, E., Mann, D. & Lu, Y. Electrical transport properties and field-effect transistors of carbon nanotubes. NANO: Brief Reports and Reviews 1 (2006) 1.

[9] Knoch, J. & Appenzeller, J. Tunneling phenomena in carbon nanotube field-effect transistors. Phys. Status Solidi A 205 (2008) 679.

[10] Journet, C., Maser, W., Bernier, P., Loiseau, A., Delachapelle, M., Lefrant, S., Deniard, P., Lee, R. & Fischer, J. Large-scale production of single-walled carbon nanotubes by the electric-arc technique. Nature 388 (1997) 756.

[11] Shi, Z., Lian, Y., Zhou, X., Gu, Z., Zhang, Y., Iijima, S., Zhou, L., Yue K. T. & Zhang, S. Mass-production of single-wall carbon nanotubes by arc discharge method. Carbon 37 (1999) 1449.

[12] Thess, A., Lee, R., Nikolaev, P., Dai, H., Petit, P., Robert, J., Xu, C., Lee, Y. H., Kim, S. G., Rinzler, A. G., Colbert, D. T., Scuseria, G. E., Tománek, D., Fischer, J. E. & Smalley, R. E. Crystalline ropes of metallic carbon nanotubes. Science 273 (1996) 483.

[13] Yudasaka, M., Komatsu, T., Ichihashi, T. & Iijima, S. Single-wall carbon nanotube formation by laser ablation using double-targets of carbon and metal. Chem. Phys. Lett. 278 (1997) 102.

[14] Scott, C. D., Arepalli, S., Nikolaev, P. & Smalley, R. E. Growth mechanisms for single-wall carbon nanotubes in a laser-ablation process. Appl. Phys. A 72 (2001) 573.

[15] Dai, H. Carbon nanotubes: synthesis, integration, and properties. Acc. Chem. Res. 35 (2002) 1035.

[16] Dai, H. Carbon nanotubes: opportunities and challenges. Surf. Sci. 500 (2002) 218.

[17] Murakami, Y., Chiashi, S., Miyauchi, Y., Hu, M., Ogura, M., Okubo, T. & Maruyama, S. Growth of vertically aligned single-walled carbon nanotube films on quartz substrates and their optical anisotropy. Chem. Phys. Lett. 385 (2004) 298.

[18] Hata, K., Futaba, D. N., Mizuno, K., Namai, T., Yumura, M. & Iijima, S. Water-assisted highly efficient synthesis of impurity-free single-walled carbon nanotubes. Science 306 (2004) 1362.

[19] Jorio, A., Dresselhaus, M. S. & Dresselhaus, G. Carbon nanotubes - Advanced topics in the synthesis, structure, properties and applications. Springer, Heidelberg, (2008), 13-163, 423-492.

[20] Charlier, J.-C., Blase, X. & Roche, S. Electronic and transport properties of nanotubes. Rev. Mod. Phys. 79 (2007) 677.

[21] Wallace, P. R. The band theory of graphite. Phys. Rev. 71 (1947) 622.

[22] Berber, S., Kwon, Y.-K. & Tománek, D. Unusually high thermal conductivity of carbon nanotubes. Phys. Rev. Lett. 84 (2000) 4613.

[23] Reich, S., Thomsen, C. & Maultzsch, J. Carbon nanotubes: Basic concepts and physical properties. Wiley-VCH, 2nd Edition (2004) 32.

[24] Hersam, M. C. Progress towards monodisperse single-walled carbon nanotubes. Nature Nanotechnol. 3 (2008) 387.

[25] Li, J.& Zhang, Q. Room-temperature negative differential conductance in carbon nanotubes. Carbon 43 (2005) 667.

[26] Wind, S. J., Appenzeller, J., Martel, R., Derycke, V. & Avouris, Ph. Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes. Appl. Phys. Lett. 80 (2002) 3817.

[27] Derycke, V., Martel, R., Appenzeller, J. & Avouris, Ph. Carbon nanotube inter- and intramolecular logic gates. Nano Lett. 1 (2001) 453.

[28] Baughman, R. H., Zakhidov, A. A. & de Heer, W. A. Carbon nanotubes-The route toward applications. Science 297 (2002) 787.

[29] Kane. C. J. & Mele, E. J. Size, shape, and low energy electronic structure of carbon nanotubes. Phys. Rev. Lett. 78 (1997) 1932.

[30] Delaney, P., Choi, H. J., Ihm, J., Louie, S. G. & Cohen, M. L. Broken symmetry and pseudogaps in ropes of carbon nanotubes. Nature 391 (1998) 466.

[31] O'Connell, M. J. Carbon nanotubes: Properties and applications. CRC Press (2006) 86-87.

[32] Saito, R., Dresselhaus, G. & Dresselhaus, M. S. Physical properties of carbon nanotubes. Imperial College Press (1998) 137-145.

[33] Burke, P. J. An RF circuit model for carbon nanotubes. IEEE Trans. Nanotechnol. 2 (2003) 55.

[34] Datta, S. Quantum transport: Atom to transistor. Cambridge University Press (2005) 139-174.

[35] Ilani, S., Donev, L. A. K., Kindermann, M. & McEuen, P. L. Measurement of the quantum capacitance of interacting electrons in carbon nanotubes. Nature Phys. 2 (2006) 687.

[36] John, D. L., Castro, L. C. & Pulfrey, D. L. Quantum capacitance in nanoscale device modeling. J. Appl. Phys. 96 (2004) 5180.

[37] Latessa, L., Pecchia, A., Di Carlo, A. & Lugli, P. Quantum capacitance effects in carbon nanotube field-effect devices. J. Comput. Electron. 4 (2005) 51.

[38] Akinwande, D., Nishi, Y. & Wong, H.-S. P. Carbon nanotube quantum capacitance for nonlinear terahertz circuits. IEEE Trans. Nanotechnol. 8 (2009) 31.

[39] Martel, R., Schmidt, T., Shea, H. R., Hertel, T. & Avouris, Ph. Single- and multi-wall carbon nanotube field-effect transistors. Appl. Phys. Lett. 73 (1998) 2447.

[40] Rosenblatt, S., Yaish, Y., Park, J., Gore, J., Sazonova, V. & McEuen, P. L. High performance electrolyte gated carbon nanotube transistors. Nano Lett. 2 (2002) 869.

[41] Carr, J. J. Secrets of RF circuit design. McGraw-Hill Professional (1996) 23-25.

[42] Tarkiainen, R., Ahlskog, M., Penttilä, J., Roschier, L., Hakonen, P., Paalanen, M. & Sonin, E. Multiwalled carbon nanotube: Luttinger versus Fermi liquid. Phys. Rev. B 64 (2001) 195412.

[43] Léonard, F. The physics of carbon nanotube devices. William Andrew (2008) 48-50.

[44] Javey, A. & Kong, J. Carbon nanotube electronics. Springer (2009) 164-166.

[45] Meservey R. & Tedrow P. M. Measurements of the kinetic inductance of superconducting linear structures. J. Appl. Phys. 40 (1969) 2028.

[46] Sonin, E. B. Tunneling into 1D and quasi-1D conductors and Luttinger-liquid behavior. J. Low Temp. Phys. 124 (2001) 321.

[47] Arns, R. G. The other transistor: early history of the metal-oxide-semiconductor field-effect transistor. Eng. Sci. Educ. J. 7 (1998) 233.

[48] Arden W., Cogez, P., Graef, M., Ishiuchi, H., Osada, T., Moon, J.T., Roh, J.S., Liang, M.-S., Diaz, C. H., Apte, P., Doering, B. & Gargini, P. International technology roadmap for semiconductors – Overview. (2008)

[49] Millman, J. & Grabel, A. Microelectronics. McGraw-Hill (1987) 144-149.

[50] Appenzeller, J., Knoch, J., Derycke, V., Martel, R. Wind, S. & Avouris, Ph. Field-modulated carrier transport in carbon nanotube transistors. Phys. Rev. Lett. 89, (2002) 126801.

[51] Dürkop, T., Getty, S. A., Cobas, E. & Fuhrer, M. S. Extraordinary mobility in semiconducting carbon nanotubes. Nano Lett. 4 (2004) 35.

[52] Fisher, J. E. Chemical doping of single-wall carbon nanotubes. Acc. Chem. Res. 35 (2002) 1079.

[53] Siddons, G. P., Merchin, D., Back, J. H., Jeong, J. K. & Shim, M. Highly efficient gating and doping of carbon nanotubes with polymer electrolytes. Nano Lett. 4 (2004) 927.

[54] Ago, H., Tanaka, I., Tsuji, M., Ikeda, K.-I. & Mizuno, S. Hole doping to aligned single-walled carbon nanotubes from sapphire substrate induced by heat treatment. J. Phys. Chem. C 112 (2008) 18350.

[55] Maiti, A. Carbon nanotubes: Bandgap engineering with strain. Nat. Mater. 2 (2003) 440.

[56] Fedorov, G., Tselev, A., Jimźnez, D., Latil, S., Kalugin, N. G., Barbara, P., Smirnov, D. & Roche, S. Magnetically induced field effect in carbon nanotube devices. Nano Lett. 7 (2007) 960.

[57] Tans, S. J., Verschueren, A. R. M. & Dekker, C. Room-temperature transistor based on a single carbon nanotube Nature 393 (1998) 4.

[58] Soh. H. T. Calvin F. Quate, C. F., Morpurgo, A. F., Marcus, C. M., Kong, J. & Dai, H. Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes. Appl. Phys. Lett. 75 (1999) 627.

[59] Bachtold, A., Hadley, P., Nakanishi, T. & Dekker, C. Logic circuits with carbon nanotube transistors. Science 294 (2001) 1317.

[60] Martel, R., Derycke, V., Lavoie, C., Appenzeller, J., Chan, K. K., Tersoff, J. & Avouris, Ph. Ambipolar electrical transport in semiconducting single-wall carbon nanotubes. Phys. Rev. Lett. 87 (2001) 256805.

[61] Heinze, S., Tersoff, J., Martel, R., Derycke, V., Appenzeller, J. & Avouris, Ph. Carbon nanotubes as Schottky barrier transistors. Phys. Rev. Lett. 89 (2002) 106801.

[62] Radosavljevic, M., Heinze, S., Tersoff, J. & Avouris, Ph. Drain voltage scaling in carbon nanotube transistors. Appl. Phys. Lett. 83 (2003) 2435.

[63] Appenzeller, J., Knoch, J., Radosavljevic, M. & Avouris, Ph. Multimode transport in schottky-barrier carbon-nanotube field-effect transistors. Phys. Rev. Lett. 92 (2004) 226802.

[64] Schottky, W. Abweichungen vom Ohmschen Gesets in Halbleitern. Phys. Z. 41 (1940) 570.

[65] Tung, R. T. Recent advances in Schottky barrier concepts. Mater. Sci. Eng., R 35 (2001) 1.

[66] Tersoff, J. Schottky barrier heights and the continuum of gap states. Phys. Rev. Lett. 52 (1984) 465.

[67] Léonard, F. & Talin, A. A. Size-dependent effects on electrical contacts to nanotubes and nanowires. Phys. Rev. Lett. 97 (2006) 026804.

[68] Léonard, F. & Tersoff, J. Role of Fermi-level pinning in nanotube schottky diodes. Phys. Rev. Lett. 84 (2000) 4693.

[69] Svensson, J., Sourab, A. A., Tarakanov, Y., Lee, D. S., Park, S. J., Baek, S. J., Park, Y.W. & Campbell, E. E. B. The dependence of the Schottky barrier height on carbon nanotube diameter for Pd-carbon nanotube contacts. Nanotechnology 20 (2009) 175204.

[70] Appenzeller, J., Radosavljevic, M., Knoch, J. & Avouris, Ph. Tunneling versus thermionic emission in one-dimensional semiconductors. Phys. Rev. Lett. 92 (2004) 048301.

[71] Chen, Z., Appenzeller, J. Knoch, J., Lin, Y.-M. and Avouris, P. The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. Nano Lett. 5 (2005) 1497.

[72] Javey, A., Guo, J., Wang, Q., Lundstrom M. & Dai, H. Ballistic carbon nanotube field-effect transistors. Nature 424 (2003) 654.

[73] Zhou, C., Kong, J. & Dai, H. Electrical measurements of individual semiconducting single-walled carbon nanotubes of various diameters. Appl. Phys. Lett. 76 (2000) 1597.

[74] Liang, W., Bockrath, M., Bozovic, D., Hafner, J. H., Tinkham, M. & Park, H. Fabry–Perot interference in a nanotube electron waveguide. Nature, 411 (2001) 665.

[75] Liang, W., Bockrath, M. & Park, H. Transport spectroscopy of chemical nanostructures: The case of metallic single-walled carbon nanotubes. Annu. Rev. Phys. Chem. 56 (2005) 475.

[76] Tersoff, J. Theory of semiconductor heterojunctions: The role of quantum dipoles. Phys. Rev. B 30 (1984) 4874.

[77] Mönch, W. Metal-semiconductor contacts: Electronic properties. Surf. sci. 300 (1994) 928.

[78] Robertson, J. Band offsets of wide-band-gap oxides and implications for future electronic devices. J. Vac. Sci. Technol. B 18 (2000) 1785.

[79] Robertson, J. Band offsets of high-κ gate oxides on high mobility semiconductors. Mater. Sci. Eng., B 135 (2006) 267.

[80] Tseng, Y.-C., Phoa, K., Carlton, D. & Bokor, J. Effect of diameter variation in a large set of carbon nanotube transistors. Nano Lett. 6 (2006) 1364.

[81] Sun, J. P. Zhang, Z. X., Hou, S. M., Zhang, G. M. Gu, Z. N., Zhao, X. Y., Liu, W. M. & Xue, Z. Q. Work function of single-walled carbon nanotubes determined by field emission microscopy. Appl. Phys. A 75 (2002) 479.

[82] Lide, D. R. CRC Handbook of chemistry and physics. 88th Edition. CRC Press (2008) 12-114.

[83] Palacios, J.J., P. Tarakeshwar, and Dae M. Kim. Metal contacts in carbon nanotube field-effect transistors: Beyond the Schottky barrier paradigm. Phys. Rev. B 77 (2008) 113403.

[84] Derycke, V., Martel, R., Appenzeller, J. & Avouris, Ph. Controlling doping and carrier injection in carbon nanotube transistors. Appl. Phys. Lett. 80 (2002) 2773.

[85] Javey, A., Wang, Q., Kim, W., Dai, H. Advancements in complementary carbon nanotube field-effect transistors. IEEE International Electron Devices Meeting, Technical Digest (2003) 31.2.1.

[86] Zhang, Z., Liang, X., Wang, S., Yao, K., Hu, Y., Zhu, Y., Chen, Q., Zhou, W., Li, Y., Yao, Y., Zhang, J. & Peng, L.-M. Doping-free fabrication of carbon nanotube based ballistic CMOS devices and circuits. Nano Lett. 7 (2007) 3603.

[87] Yang, M. H., Teo, K. B. K., Milne, W. I. & Hasko, D. G. Carbon nanotube Schottky diode and directionally dependent field-effect transistor using asymmetrical contacts. Appl. Phys. Lett. 87 (2005) 253116.

[88] Avouris, Ph. Molecular electronics with carbon nanotubes. Acc. Chem. Res. 35 (2002) 1026.

[89] Wind, S. J., Appenzeller, J., Martel, R., Derycke, V. & Avouris, Ph. Fabrication and electrical characterization of top gate single-wall carbon nanotube field-effect transistors. J. Vac. Sci. Technol. B 20 (2002) 2798.

[90] Wind, S. J., Appenzeller, j. & Avouris, Ph. Lateral scaling in carbon-nanotube field-effect transistors. Phys. Rev. Lett. 91 (2003) 058301.

[91] Lin, Y.-M., Appenzeller, J., Knoch, J. & Avouris, P. High-performance carbon nanotube field-effect transistor with tunable polarities. IEEE Trans. Nanotechnol. 4 (2005) 481.

[92] Appenzeller, J., Lin, Y.-M., Knoch, J. & Avouris, Ph. Band-to-band tunneling in carbon nanotube field-effect transistors, Phys. Rev. Lett. 93 (2004) 196805.

[93] Liu, X., Lee, C., Zhou, C. and Han, J. Carbon nanotube field-effect inverters. Appl. Phys. Lett. 79 (2001) 3329.

[94] Javey, A., Kim, H., Brink, M., Wang, Q., Ural, A., Guo, J., McIntyre, P., McEuen, P., Lundstrom M. & Dai, H. High-k dielectrics for advanced carbon nanotube transistors and logic gates. Nat. Mater. 1 (2002) 241.

[95] Javey, A., Wang, Q., Ural, A., Li, Y. & Dai, H. Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators. Nano Lett. 2 (2002) 929.

[96] Hasan, S., Salahuddin, S., Vaidyanathan, M., Alam, M. A. High-frequency performance projections for ballistic carbon-nanotube transistors. IEEE Trans. Nanotechnol. 5 (2006) 14.

[97] Chaste, J., Lechner, L., Morfin, P., Fève, G., Kontos, T., Berroir, J.-M., Glattli, D. C., Happy, H., Hakonen, P. & Plaçais, B. Single carbon nanotube transistor at GHz frequency. Nano Lett. 8 (2008) 525.

[98] Rueckes, T., Kim, K., Joselevich, E., Tseng, G. Y., Cheung, C.-L. & Lieber, C. M. Carbon nanotube-based nonvolatile random access memory for molecular computing. Science 289 (2000) 94.

[99] Zheng, M., Jagota, A., Semke, E. D., Diner, B. A., Mclean, R. S., Lustig, S. R., Richardson, R. E. & Tassi, N. G. DNA-assisted dispersion and separation of carbon nanotubes. Nat. Mater. 2 (2003) 338.

[100] Krupke, R., Hennrich, F., Kappes, M. M. & Lohneysen, H. V. Surface conductance induced dielectrophoresis of semiconducting single-walled carbon nanotubes. Nano Lett. 4 (2004) 1395.

[101] Krupke, R. & Hennrich, F. Separation techniques for carbon nanotubes. Adv. Engineer. Mat. 7 (2005) 111.

[102] Tu, X., Manohar, S., Jagota, A. & Zheng, M. DNA sequence motifs for structure-specific recognition and separation of carbon nanotubes. Nature 460 (2009) 250.

[103] Green, A. A., Duch, M. C., & Hersam, M. C. Isolation of single-walled carbon nanotube enantiomers by density differentiation. Nano Res. 2 (2009) 69.

[104] Zhang, Y., Chang, A., Cao, J., Wang, Q., Kim, W., Li, Y., Morris, N., Yenilmez, E., Kong, J. & Dai, H. Electric-field-directed growth of aligned single-walled carbon nanotubes. Appl. Phys. Lett. 79 (2001) 3155.

[105] Rao, S. G., Huang, L., Setyawan, W. & Hong, S. Nanotube electronics: Large-scale assembly of carbon nanotubes. Nature 425 (2003) 36.

[106] Vijayaraghavan, A., Blatt, S., Weissenberger, D., Oron-Carl, M., Hennrich, F., Gerthsen, D., Hahn, H. & Krupke, R. Ultra-large-scale directed assembly of single-walled carbon nanotube devices. Nano Lett. 7 (2007) 1556.

[107] Liu, Y., Hong, J., Zhang, Y., Cui, R., Wang, J., Tan, W. & Li, Y. Flexible orientation control of ultralong single-walled carbon nanotubes by gas flow. Nanotechnology 20 (2009) 185601.

[108] Ras, R. H. A., Kemell, M., de Wit, J., Ritala, M., ten Brinke, G., Leskelä, M. & Ikkala, O. Hollow inorganic nanospheres and nanotubes with tunable wall thicknesses by atomic layer deposition on self-assembled polymeric templates. Adv. Mater. 19 (2007) 102.

[109] Niinistö, J., Putkonen, M., Niinistö, L., Stoll, S. L., Kukli, K., Sajavaara, T., Ritala, M. & Leskelä, M. Controlled growth of HfO_2 thin films by atomic layer deposition from cyclopentadienyl-type precursor and water. J. Mater. Chem. 15 (2005) 2271.

[110] Niinistö, J., Kukli, K., Heikkilä, M., Ritala, M. & Leskelä, M. Atomic layer deposition of high-κ oxides of the group 4 metals for memory applications. Adv. Eng. Mater. 11 (2009) 223.

[111] Knez, M., Nielsch, K. & Niinistö, L. Synthesis and surface engineering of complex nanostructures by atomic layer deposition. Adv. Mater. 19 (2007) 3425.

[112] Suntola, T. & Antson, J. Method for producing compound thin films. US Patent 4 058 430, (1977).

[113] Mistry, K. *et al.* A 45 nm logic technology with high-κ+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging. Electron Devices Meeting, 2007. IEDM 2007. IEEE International. (2007) 247.

[114] Natarajan, S. *et al.* A 32 nm logic technology featuring 2^{nd}-generation high-κ + metal-gate transistors, enhanced channel strain and 0.171μm^2 SRAM cell size in a 291 Mb array. Electron Devices Meeting, 2008. IEDM 2008. IEEE International (2008) 1.

[115] Welnic, W & Wuttig, M. Reversible switching in phase-change materials. Mater. Today 11 (2008) 20.

[116] Atwood, G. Phase-change materials for electronic memories. Science 321 (2008) 210.

[117] Ritala, M., Pore, V., Hatanpää, T., Heikkilä, M., Leskelä, M., Mizohata, K., Schrott, A., Raoux, S. & Rossnagel, S. M. Atomic layer deposition of $Ge_2Sb_2Te_5$ thin films. Microelectron. Eng. 86 (2009) 1946.

[118] Leskelä, M., Pore, V., Hatanpää, T., Heikkilä, M., Ritala, M., Schrott, A., Raoux, S. & Rossnagel, S. M. Atomic layer deposition of materials for phase-change memories. ECS Trans. 25 (2009) 399.

[119] Rinkiö, M., Johansson, A., Paraoanu, G. S. & Törmä, P. High-speed memory from carbon nanotube field-effect transistors with high-κ gate dielectric. Nano Lett. 9 (2009) 643.

[120] Farmer, D. B. & Gordon, R. G. ALD of high-κ dielectrics on suspended functionalized SWNTs. Electrochem. Solid-State Lett. 8 (2005) G89.

[121] Lu, Y., Bangsaruntip, S., Wang, X., Zhang, L., Nishi, Y. & Dai, H. DNA functionalization of carbon nanotubes for ultrathin atomic layer deposition of high kappa dielectrics for nanotube transistors with 60 mV/decade switching. J. Am. Chem. Soc. 128 (2006) 3518.

[122] Javey, A., Guo, J., Farmer, D. B., Wang, Q., Yenilmez, E., Gordon, R. G., Lundstrom, M. & Dai, H. Self-aligned ballistic molecular transistors and electrically parallel nanotube arrays. Nano Lett. 4 (2004) 1319.

[123] Puurunen, R. L. Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/water process. J. Appl. Phys 97 (2005) 121301.

[124] Hermann, C. F., Fabreguette, F. H. & Finch, D. S. Multilayer and functional coatings on carbon nanotubes using atomic layer deposition. Appl. Phys. Lett. 87 (2005) 123110.

[125] Farmer, D. B. & Gordon, R. G. Atomic layer deposition on suspended single-walled carbon nanotubes via gas-phase noncovalent functionalization. Nano Lett. 6 (2006) 699.

[126] Raghu, P., Rana, N., Yim, C., Shero, E. & Shadmana, F. Adsorption of moisture and organic contaminants on hafnium oxide, zirconium oxide, and silicon oxide gate dielectrics. J. Electrochem. Soc. 50 (2003) 186.

[127] Nasibulin, A. G., Moisala, A., Brown, D. P., Jiang, H. and Kauppinen, E. I. A novel aerosol method for single walled carbon nanotube synthesis. Chem. Phys. Lett. 402 (2005) 227.

[128] Semiconductor industry association. Worldwide semiconductor revenues. <URL:http://www.sia-online.org/galleries/gsrfiles/GSR_0908.pdf> (read 28.10.2009)

[129] Bez, R., Camerlenghi, E., Modelli, A. & Visconti, A. Introduction to flash memory. Proceedings of the IEEE 91 (2003) 489.

[130] Lee, W.-S. Future memory technologies. 9th Int. Conf. Solid-State and Integrated-Circuit Technol. 2008 1.

[131] Kim, K. & Koh, G.-H. Future memory technology including emerging new memories. Proc. 24th Int. Conf. Microelectron. 1 (2004) 377.

[132] Kim, K. Future memory technology: Challenges and opportunities. Int. Symp. VLSI Technol., Syst. Appl. (2008) 5.

[133] Kuesters, K.-H., Ludwig, C., Mikolajick, T., Nagel, N., Specht, M., Pissors, V., Schulze, N., Stein, E. & Willer, J. Future trends in charge trapping memories. 8th Int. Conf. Solid-State Integr. Circuit Technol. (2006) 740.

[134] Sandhya, C., Singh, P. K., Gupta, S., Rohra, H., Shivatheja, M., Ganguly, U., Hofmann, R., Mukhopadhyay, G., Mahapatra, S. & Vasi, J. Recent advances in charge trap flash memories. 2nd Int. Workshop Electron Devices and Semicond. Technol. (2009) 1.

[135] Weitz, R. T., Zschieschang, U., Effenberger, F., Klauk, H., Burghard, M., & Kern, K. High-performance carbon nanotube field effect transistors with a thin gate dielectric based on a self-assembled monolayer. Nano Lett. 7 (2007) 22.

[136] Kim, W., Javey, A., Vermesh, O., Wang, Q., Li, Y. & Dai, H. Hysteresis caused by water molecules in carbon nanotube field-effect transistors. Nano Lett. 3 (2003) 193.

[137] Ozel, T., Gaur, A., Rogers, J. A. & Shim, M. Polymer electrolyte gating of carbon nanotube network transistors. Nano Lett. 5 (2005) 905.

[138] Wang, S., Sellin, P., Zhang, Q. & Yang, D. Nonvolatile memory from single-walled carbon nanotube-based field effect transistors. Current Nanoscience 1 (2005) 43.

[139] McGill, S. A., Rao, S. G., Manandhar, P., Xiong, P. & Hong, S. High-performance, hysteresis-free carbon nanotube field-effect transistors via directed assembly. Appl. Phys. Lett. 89 (2006) 163123.

[140] Pavan, P., Bez, R., Olivo, P. & Zanoni, E. Flash memory cells – An overview. Proc. IEEE 85 (1997) 1248.

[141] Fazio, A. Solid state storage, limits of Flash memory. IEEE Int. Magn. Conf. (2006) 101.

[142] Fuhrer, M. S., Kim, B. M., Durkop, T. & Britlinger, T. High-mobility nanotube transistor memory. Nano Lett. 2 (2002) 755.

[143] Radosavljevic, M., Freitag, M., Thadani, K. V. & Johnson, A. T. Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors. Nano Lett. 2 (2002) 761.

[144] Cui, J. B., Sordan, R., Burghard, M. & Kern, K. Carbon nanotube memory devices of high charge storage stability. Appl. Phys. Lett. 81 (2002) 3260.

[145] Choi, W. B., Chae, S., Bae, E., Lee, J.-W., Cheong, B.-H., Kim, J.-R. & Kim, J.-J. Carbon-nanotube-based nonvolatile memory with oxide-nitride-oxide film and nanoscale channel. Appl. Phys. Lett. 82 (2003) 275.

[146] Marty, L., Naud, C., Chaumont, M., Bonnot, A. M., Fournier, T. & Bouchiat, V. Self-assembled single wall carbon nanotube field effect transistors. IEEE-Nano 1 (2003) 240.

[147] Wang, S. & Sellin, P. Pronounced hysteresis and high charge storage stability of single-walled carbon nanotube-based field-effect transistors. Appl. Phys. Lett. 87 (2005) 133117.

[148] Ganguly, U., Kan, E. C. & Zhangb, Y. Carbon nanotube-based nonvolatile memory with charge storage in metal nanocrystals. Appl. Phys. Lett. 87 (2005) 043108.

[149] Rinkiö, M., Zavodchikova, M. Y., Törmä, P. & Johansson, A. Effect of humidity on the hysteresis of single walled carbon nanotube field-effect transistors. Phys. Status Solidi B 245 (2008) 2315.

[150] Rinkiö, M., Johansson, A., Zavodchikova, M. Y., Toppari, J. J., Nasibulin, A. G., Kauppinen, E. I. & Törmä, P. High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric. New J. Phys. 10 (2008) 103019.

[151] Bradley, K., Cumings, J., Star, A., Gabriel, J.-C. P. & Gruner, G. Influence of mobile ions on nanotube based FET devices. Nano Lett. 3 (2003) 639.

[152] Vijayaraghavan, A., Kar, S., Soldano, C., Talapatra, S., Nalamasu, O. & Ajayan, P. M. Charge-injection-induced dynamic screening and origin of hysteresis in field-modulated transport in single-wall carbon nanotubes. Appl. Phys. Lett. 89 (2006) 162108.

[153] Robert-Peillard, A. & Rotkin, S. V. Modeling hysteresis phenomena in nanotube field-effect transistors. IEEE Trans. Nanotechnol. 4 (2005) 284.

[154] Freitag, M., Johnson, A. T., Kalinin, S. V. & Bonnell, D. A. Role of single defects in electronic transport through carbon nanotube field-effect transistors. Phys. Rev. Lett. 89 (2002) 216801.

[155] Park, J.-Y. Electrically tunable defects in metallic single-walled carbon nanotubes. Appl. Phys. Lett. 90 (2007) 023112.

[156] Kim, Y., Oh, Y. M., Park, J.-Y. & Kahng, S.-J. Mapping potential landscapes of semiconducting carbon nanotubes with scanning gate microscopy. Nanotechnology 18 (2007) 475712.

[157] Kar, S., Vijayaraghavan, A., Soldano, C., Talapatra, S., Vajtai, R., Nalamasu, O., & Ajayan, P. M. Quantitative analysis of hysteresis in carbon nanotube field-effect devices. Appl. Phys. Lett. 89 (2006) 132118.

[158] Purewal, M. S., Hong, B. H., Ravi, A., Chandra, B., Hone, J. & Kim, P. Scaling of resistance and electron mean free path of single-walled carbon nanotubes Phys. Rev. Lett. 98 (2007) 186808.

[159] Vanheusden, K., Warren, W. L., Devine, R. A. B., Fleetwood, D. M., Schwank, J. R., Shaneyfelt, M. R., Winokur, P. S. & Lemmios, Z. J. Non-volatile memory device based on mobile protons in SiO_2 thin films. Nature 386 (1997) 587.

[160] Lee, J. S., Ryu, S., Yoo, K., Choi, I. S., Yun, W. S. & Kim, J. Origin of gate hysteresis in carbon nanotube field-effect transistors. J. Phys. Chem. C 111 (2007) 12504.

[161] Zhuravlev, L. T. The surface chemistry of amorphous silica. Zhuravlev model. Colloids Surf. A 173 (2000) 1.

[162] Marty, L., Bonnot, A. M., Bonhomme, A., Iaia, A. Naud, C, André, E. and Bouchiat, V. Self-Assembly of Carbon-Nanotube-Based Single-Electron Memories. Small 2 (2006) 110.

[163] Gruneis, A., Esplandiu, M. J., Garcia-Sanchez, D. & Bachtold, A. Detecting individual electrons using a carbon nanotube field-effect transistor. Nano Lett. 7 (2007) 3766.

[164] Shim, S. I., Yeh, F. C., Wang, X. W. & Ma, T. P. SONOS-type flash memory cell with metal/Al_2O_3/SiN/Si_3N_4/Si structure for low-voltage high-speed program/erase operation. IEEE Electron Device Lett. 29 (2008) 512.

[165] Lin, H. & Tiwari, S. Localized charge trapping due to adsorption in nanotube field-effect transistor and its field-mediated transport. Appl. Phys. Lett. 89 (2006) 073507.

[166] Ribes, G., Mitard, J., Denais, M., Bruyere, S., Monsieur, F., Parthasarathy, C., Vincent, E. & Ghibaudo, G. Review on high-k dielectrics reliability issues. IEEE Trans. Device Mater. Reliab. 5 (2005) 5.

[167] Zafar, S., Callegari, A., Gusev, E. & Fischetti, M. V. Charge trapping in high k gate dielectric stacks. Int. Electron Devices Meeting 1 (2002) 517.

[168] Young, C. D., Bersuker, G., Brown, G. A., Lim, C., Lysaght, P., Zeitzoff, P., Murto, R. W. & Huff, H. R. Charge trapping in MOCVD hafnium-based gate field dielectric stack structures and its impact on device performance. IEEE Int. Integrated Reliab. Workshop 1 (2003) 28.

[169] Sim, J. H., Song, S. C., Kirsch, P. D., Young, C. D., Choi, R., Kwong, D. L., Lee, B. H. & Bersuker, G. Effects of ALD HfO_2 thickness on charge trapping and mobility. Microelectron. Eng. 80 (2005) 218.

[170] Kerber, A., Cartier, E., Pantisano, L., Degraeve, R., Kauerauf, T., Kim, Y., Hou, A., Groeseneken, G., Maes, H. E. & Schwalke, U. Origin of the threshold voltage instability in SiO_2/HfO_2 dual layer gate dielectrics. IEEE Electron Device Lett. 24 (2003) 87.

[171] Takeuchi, H., Ha, D. & King, T.-J. Observation of bulk HfO_2 defects by spectroscopic ellipsometry. J. Vac. Sci. Technol. A 22 (2004) 1337.

[172] Foster, A. S., Lopez Gejo, F., Shluger, A. L. & Nieminen, R. M. Vacancy and interstitial defects in hafnia. Phys. Rev. B 65 (2002) 174117.

[173] Esaki, L. & Tsu, R. Superlattice and negative differential conductivity in semiconductors. IBM J. Res. Dev. 14 (1970) 61.

[174] Tsu, R. & Esaki, L. Tunneling in a finite superlattice. Appl. Phys. Lett. 22 (1973) 562.

[175] Chang, L. L., Esaki, L. & Tsu, R. Resonant tunneling in semiconductor double barriers. Appl. Phys. Lett. 24 (1974) 593.

[176] Xue, Y., Datta, S., Hong, S., Reifenberger, R., Henderson, J. I. & Kubiak, C. P. Negative differential resistance in the scanning-tunneling spectroscopy of organic molecules. Phys. Rev. B 59 (1999) R7852.

[177] Chen, J., Reed, M. A., Rawlett, A. M. & Tour, J. M. Large on-off ratios and negative differential resistance in a molecular electronic device. Science 286 (1999) 1550.

[178] Zeng, C., Wang, H., Wang, B., Yang, J. & Hou, J. G. Negative differential-resistance device involving two C_{60} molecules. Appl. Phys. Lett. 77 (2000) 3595.

[179] Zhou, C., Kong, J., Yenilmez, E. & Dai, H. Modulated chemical doping of individual carbon nanotubes. Science 290 (2000) 1552.

[180] Buchs, G., Ruffieux, P., Groning, P. & Groning, O. Defect-induced negative differential resistance in single-walled carbon nanotubes. Appl. Phys. Lett. 93 (2008) 073115.

[181] Biswas, S. K., Schowalter, L. J., Jung,Y. J., Vijayaraghavan, A., Ajayan, P. M. & Vajtai, R. Room-temperature resonant tunneling of electrons in carbon nanotube junction quantum wells. Appl. Phys. Lett. 86 (2005) 183101.

[182] Chandra, B., Bhattacharjee, J., Purewal, M., Son, Y.-W., Wu, Y., Huang, M., Yan, H., Heinz, T. F., Kim, P., Neaton, J. B. & Hone, J. Molecular-scale quantum dots from carbon nanotube heterojunctions. Nano Lett. 9 (2009) 1544.

[183] Ahlskog, M., Herranen, O., Johansson, A., Leppäniemi, J., & Mtsuko, D. Electronic transport in intermediate sized carbon nanotubes. Phys. Rev. B 79 (2009) 155408.

[184] Lee, S. W., Kornblit, A., Lopez, D., Rotkin, S. V., Sirenko, A. A. & Grebel, H. Negative differential resistance: Gate controlled and photoconductance enhancement in carbon nanotube intraconnects. Nano Lett. 9 (2009) 1369.

[185] Haddad, G. I. & Mazmunder, P. Tunneling devices and applications in high functionality/speed digital circuits. Solid-State Electron. 41 (1997) 1515.

[186] Laskar, J. Ketterson, A. A., Baillargeon, J. N. Brock, T., Adesida, I., Cheng, K. Y. & Kolodzey, J. Gate-controlled negative differential resistance in drain current characteristics of AlGaAs/InGaAs/GaAs pseudomorphic MODFETs. IEEE Electron Device Lett. 10 (1989) 528.

[187] Kouwenhoven, L. P., Austing, D. G. & Tarucha, S. Few-electron quantum dots. Rep. Prog. Phys. 64 (2001) 701.

[188] Reimann, S. M. & Manninen, M. Electronic structure of quantum dots. Rev. Mod. Phys. 74 (2002) 1283.

[189] Hanson, R., Kouwenhoven, L. P., Petta, J. R., Tarucha, S. & Vandersypen, L. M. K. Spins in few-electron quantum dots. Rev. Mod. Phys. 79 (2007) 1217.

[190] Grabert, H. Single charge tunneling: A brief introduction. Z. Phys. B: Condens. Matter. 85 (1991) 319.

[191] van Houten, H., Beenakker, C. W. J. & Staring, A. A. M. Single charge tunneling: Coulomb blockade phenomena in nanostructures. Edited: Grabert, H. & Devoret, M. H. NATO Science Series: B: Springer, Plenum, New York, (1992) 294.

[192] Ashoori, R. C. Electrons in artificial atoms. Nature 379 (1996) 413.

[193] Gotz, G., Steele, G. A. Vos, W.-J. & Kouwenhoven, L. P. Real time electron tunneling and pulse spectroscopy in carbon nanotube quantum dots. Nano Lett. 8 (2008) 4039.

[194] Andresen, S. E. S., Wu, F., Danneau, R., Gunnarsson, D. & Hakonen, P. J. Highly sensitive and broadband carbon nanotube radio-frequency single-electron transistor. J. Appl. Phys. 104 (2008) 033715.

[195] Churchill, H. O. H., Kuemmeth, F., Harlow, J. W., Bestwick, A. J., Rashba, E. I., Flensberg, K., Stwertka, C. H., Taychatanapat, T., Watson, S. K. & Marcus, C. M. Relaxation and dephasing in a two-electron ^{13}C nanotube double quantum dot. Phys. Rev. Lett. 102 (2009) 166802.

[196] Field, M., Smith, C. G., Pepper, M., Ritchie, D. A., Frost, J. E. F., Jones, G. A. C. & Hasko, D. G. Measurements of Coulomb blockade with a noninvasive voltage probe. Phys. Rev. Lett. 70 (1993) 1311.

[197] Steele, G. A., Gotz, G. & Kouwenhoven, L. P. Tunable few-electron double quantum dots and Klein tunnelling in ultraclean carbon nanotubes. Nat. Nanotechnol. 4 (2009) 363.

[198] Léonard, F. & Tersoff, J. Multiple functionality in nanotube transistors. Phys. Rev. Lett. 88 (2002) 258302.

[199] Sollner, T. C. L. G., Goodhue, W. D., Tannenwald, P. E., Parker, C. D. & Peck, D. D. Resonant tunneling through quantum wells at frequencies up to 2.5 THz. Appl. Phys. Lett. 43 (1983) 588.

[200] Reed, M. A., Randall, J. N., Aggarwal, R. J., Matyi, R. J., Moore, T. M. & Wetsel, A. E. Observation of discrete electronic states in a zero-dimensional semiconductor nanostructure. Phys. Rev. Lett. 60 (1988) 535.

[201] Cowin, J. P., Tsekouras, A. A., Iedema, M. J., Wu, K. & Ellison, G. B. Immobility of protons in ice from 30 to 190 K. Nature 398 (1999) 405.

[202] Pop, E., Mann, D., Cao, J., Wang, Q., Goodson, K. & Dai, H. Negative differential conductance and hot phonons in suspended nanotube molecular wires. Phys. Rev. Lett. 95 (2005) 155505.

[203] Antonov, R. D. & Johnson, A. T. Subband population in a single-wall carbon nanotube diode. Phys. Rev. Lett. 83 (1999) 3274.

[204] Bockrath, M., Liang, W., Bozovic, D., Hafner, J. H., Lieber, C. M., Tinkham, M. & Park, H. Resonant electron scattering by defects in single-walled carbon nanotubes. Science 291 (2001) 283.

[205] Dragoman, D. & Dragoman, M. Terahertz oscillations in semiconducting carbon nanotube resonant-tunneling diodes. Physica E 24 (2004) 282.

[206] Dragoman, D. & Dragoman, M. Voltage-controlled high-frequency oscillations based on suspended semiconducting carbon nanotubes. Phys. Rev. B 73 (2006) 125417.

[207] Nishizawa, J., Potka, P. & Kurabayashi, T. Ballistic and tunneling GaAs static induction transistors: Nano-devices for THz electronics. IEEE Trans. Electron Devices 49 (2002) 1102.

[208] Brown, E. R., Söderström, J. R., Parker, C. D., Mahoney, L. J. & Molvar, K. M. Oscillations up to 712 GHz in InAs/AlSb resonant-tunneling diodes. Appl. Phys. Lett. 58 (1991) 2291.

[209] Ismach, A. & Joselevich, E. Orthogonal self-assembly of carbon nanotube crossbar architectures by simultaneous graphoepitaxy and field-directed growth. Nano Lett. 6 (2006) 1706.

[210] Marty, L., Bonhomme, A., Iaia, A., André, E., Rauwel E., Dubourdieu C., Toffoli, A., Ducroquet, F., Bonnot, A. M. & Bouchiat, V. Integration of self-assembled carbon nanotube transistors: statistics and gate engineering at the wafer scale. Nanotechnology 17 (2006) 5038.

[211] Chen, Z., Farmer, D., Xu, S., Gordon, R., Avouris, Ph. & Appenzeller, J. Externally assembled gate-all-around carbon nanotube field-effect transistor. IEEE Electron Device Lett. 29 (2008) 183.

A.I

phys. stat. sol. (b) **244**, No. 11, 4188–4192 (2007) / **DOI** 10.1002/pssb.200776187

Fabrication of carbon nanotube-based field-effect transistors for studies of their memory effects

M. Y. Zavodchikova[*, 1], **A. Johansson**[1], **M. Rinkiö**[1], **J. J. Toppari**[1], **A. G. Nasibulin**[2], **E. I. Kauppinen**[2, 3], and **P. Törmä**[1]

[1] NanoScience Center, Department of Physics, University of Jyväskylä, Finland
[2] NanoMaterials Group, Center for New Materials and Laboratory of Physics, Helsinki University of Technology, Finland
[3] VTT Biotechnology, Espoo, Finland

Received 30 April 2007, revised 20 August 2007, accepted 20 August 2007
Published online 8 October 2007

PACS 73.23.–b, 73.40.Sx, 73.63.Fg, 85.30.Tv, 85.35.Kt

Carbon nanotube-based field-effect transistors (CNTFETs) have been fabricated using nanometer thin dielectric material as the gate insulator film. The demonstrated fabrication technique is highly suitable for preparing devices with low contact resistances between the electrodes and the carbon nanotube, down to 14 kΩ. Electronic transport measurements of the fabricated devices have been conducted on more than 70 FETs. Hysteretic behavior in the transfer characteristics of some CNTFETs was observed.

© 2007 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

1 Introduction

Due to the variety of unique electrical and mechanical properties, CNTs have emerged as highly promising building blocks for future molecular nanodevices. Rapid progress has been done in the exploration of the device potential of CNT-based field-effect transistors (CNTFETs). CNTFETs are known to frequently display undesirable hysteresis in their transfer characteristics between the forward and reverse sweeps of the gate potential (see for example [1–3]). The hysteresis allows the device to function as a memory cell. That makes hysteretic behaviour of CNTFETs a favourable feature, which could be utilized in the fabrication of memory elements. To date, there is no method to control the reproducibility of the hysteresis phenomenon in CNTFETs. Here, we report the details of a high-yield fabrication technique of CNTFETs that we have developed with the intention to further study their memory effects.

2 Fabrication technique

CNTFETs were fabricated in a bottom-up approach on top of a highly boron-doped silicon substrate, used as a back gate, which was covered with a thin dielectric layer. In our study, the emphasis was made on developing a fabrication technique which is compatible with the use of a nanometer thin dielectric material as the gate insulator film, grown by atomic layer deposition (ALD) technique (e.g. Al_2O_3 or HfO_2 with a thickness of at most 40 nm). ALD film coating was provided by our research project collaborators at Planar Systems Inc (Espoo, Finland), using Planar P400A ALD deposition tool. In addition, reference devices on a Si substrate, covered with a thermally grown SiO_2 layer with the thickness of ~300 nm, have been fabricated.

* Corresponding author: e-mail: marina.zavodchikova@hut.fi

© 2007 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

Two positive resist layers were used in our experiments for covering the substrate as a mask. First the wafer was uniformly coated with polymethylmethacrylate-co-methacrylic acid (PMMA-MMA EL 3%) with the rotation speed of 3000 rpm for the time period of 50 sec. Then the second resist layer of polymethylmethacrylate dissolved in anisole (PMMA A 2%) was spun on top with a rotation speed of 6000 rpm during 50 sec. The resist was soft baked on a hot plate at 160 °C for 3 min after each layer deposition.

Standard electron beam lithography and subsequent evaporation of Ti/Pd was used in order to fabricate a 6 × 6 alignment mark matrix surrounded by 28 electrodes, as seen in Fig. 1. In total, the patterned structure measures 2.5 × 2.5 mm. The alignment marks were around 650 nm long with a separation of 7 μm between them (see Fig. 1(d)).

Patterning of this structure was carried out with a new Raith e-line electron-beam writer (equipped with Elphy Quantum 4.0-lithography software) with an acceleration voltage of 20 kV and a dose of ~220 μA/cm^2. The patterned structure was exposed using two different working areas (WA). The smaller features (alignment marks and inner electrodes) had a WA of 500 μm and exposure was carried out with a beam aperture size of 30 μm. For the larger structural elements (outer electrodes and bonding pads) 2500 μm WA and 120 μm beam aperture size were used. For all exposures the write field was 500 μm. The working distance was near 6 mm. The spot size of the focused electron beam was estimated to be in the range of 10–40 nm, which allows to perform an accurate exposure with a good linewidth control.

After exposing the desired pattern with the electron beam, the resist was developed in a 1:3 solution of methylisobutylketone:isopropyl alcohol (MIBK:IPA) for 40 sec and then in 2:1 solution of methanol:methoxyethanol for 5 sec, followed by washing the chip with IPA and drying under a nitrogen flow. A bilayer technique of depositing two layers of resist was applied for creating a so-called undercut profile, which is due to an increased developing of the more sensitive bottom layer (PMMA-MMA EL 3% in our case), helpful during the lift-off process.

After the development process, two metal layers, 5 nm Ti (evaporation rate ~0.15 nm/s) and 25 nm Pd (evaporation rate ~0.12 nm/s) were thermally evaporated using Balzers Evaporator System. The Ti layer was evaporated below the Pd layer in order to improve adhesion of the latter. Lift-off was carried out in acetone for about 15 min without ultrasonic agitation. The sample was washed with IPA and dried under a nitrogen flow. Figure 1(a)–(d) shows an overview of the patterned design, giving a close-up look at the smaller structural elements.

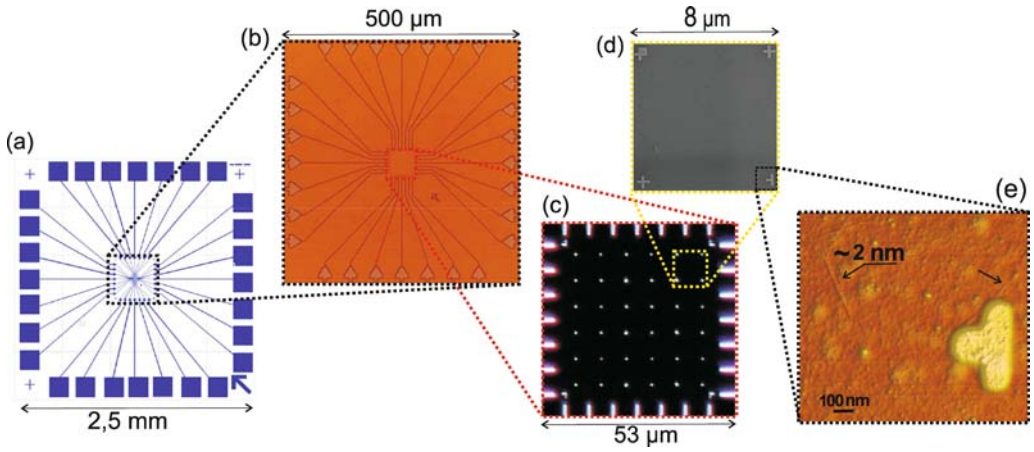

Fig. 1 (online colour at: www.pss-b.com) (a) Overview of the pattern design (2.5 × 2.5 mm). (b) Enlarged optical microscope image of the fabricated structure, including inner electrodes and a matrix of alignment marks (500 × 500 μm area). (c) Enlarged optical microscope image of a 6 × 6 alignment mark matrix in the middle of a structure (53 × 53 μm area). (d) Enlarged SEM image of the four alignment marks (8 × 8 μm area). (e) Enlarged AFM image of two SWCNTs located close to an alignment mark.

© 2007 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

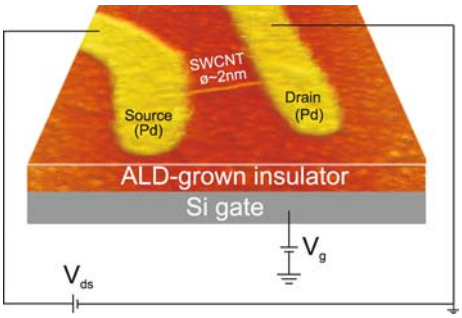

Fig. 2 (online colour at: www.pss-b.com) AFM image of an individual SWCNT device contacted by Pd electrodes in its schematic three-terminal FET configuration (SWCNT colored for better visibility). The scanning area is 2 × 2 μm.

Subsequently deposited CNTs were precisely located with respect to the alignment mark matrix using atomic force microscopy (AFM). Figure 1(e) shows two CNTs mapped in the vicinity of one of the alignment marks. In our studies, either commercial SWCNTs (purchased from a CNT producing company – NanoCyl, Sambreville, Belgium) or SWCNTs produced by a hot wire generator (HWG) method (from Helsinki University of Technology (HUT), NanoMaterials group) were used. The original powder like NanoCyl SWCNTs (with an average diameter of 2 nm), produced via catalytic carbon vapor deposition process, were first dispersed in a 1,2-dichloroethane suspension and then deposited onto the substrate after a mild sonication for 10–15 min. SWCNTs from HUT were produced by an aerosol method by means of introducing catalyst particles, formed by a hot wire generator, into a laminar flow reactor where suitable conditions for the nanotube formation were maintained. An electrostatic filter was used for the separation of individual (electrically neutral) CNTs from bundled ones (charged). SWCNTs of an average diameter of 1.4 nm were deposited onto the substrate, directly from the reactor without any suspension [4].

After mapping the locations of CNTs with an AFM, Pd source and drain electrodes (25 nm thick) were fabricated on top of the selected SWCNTs by a second e-beam lithography step with the processing parameters similar to the ones used for the primary pattern. An AFM image of a typical fabricated device can be observed in Fig. 2.

Since the sample processing incorporates two steps of electron beam lithography, a nanometer scale accuracy in spatial alignment between the consecutive layers is important. We have achieved an alignment precision of a few tens of nanometers. Finally, thin Au wires were carefully bonded to the contact pads at the end of each electrode in order to electrically connect the device terminals and the chip carrier.

3 Measurements

Electronic transport measurements of the fabricated devices have been conducted on more than 70 FETs (21 of which were made with thermally grown SiO_2 as the gate insulator layer and the rest with different types of ALD materials, e.g. Al_2O_3 or HfO_2). When measuring their I–V characteristics, both metallic and semiconducting nanotubes were found in close agreement with the expected ratio of 1:2. Figure 3 shows that metallic nanotubes had no response to the gate voltage variations (Fig. 3(a)), while in the case of semiconducting nanotubes, the conductance was significantly varied with changes in the back-gate voltage (Fig. 3(b), (c)). Most of the semiconducting nanotubes displayed strongly suppressed conductance at larger positive gate voltages, in accordance with the expected p-type unipolar behavior [5, 6] (see Fig. 3(b)). A few of the measured semiconducting devices showed finite conductance at both positive and negative gate voltages, separated by a non-conducting gap. That is attributed to ambipolar behavior, typical for semiconducting nanotubes with a small band gap [7, 8] (see Fig. 3(c)).

It was demonstrated that Pd contacts, used in this study, greatly reduce the energy barriers for transport through the valence band of the nanotube due to their high work function and good wetting interactions with nanotubes [9, 10]. Our measurements of the two-terminal resistance of metallic nanotubes, connected with Pd electrodes, gave resistance values in the range of 14–160 kΩ (close to the minimum

© 2007 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

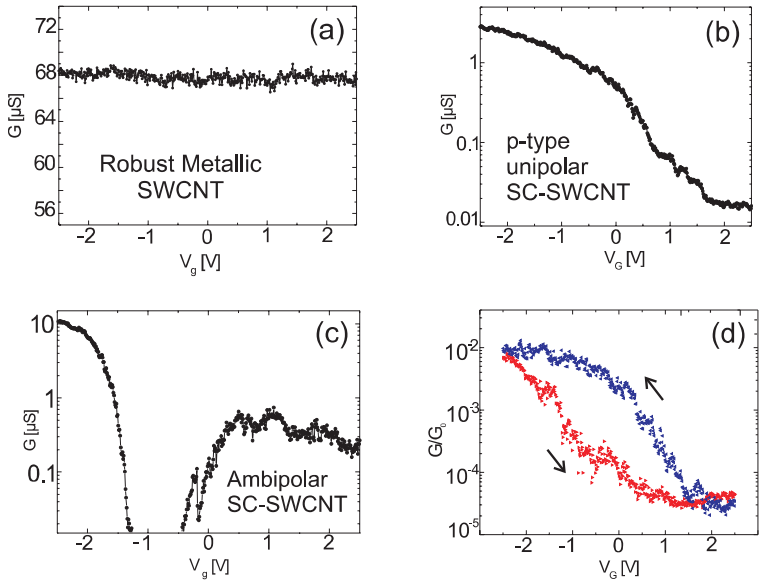

Fig. 3 (online colour at: www.pss-b.com) Representative transfer characteristics (observed in both SiO_2-based and ALD-based samples) of (a) robust metallic nanotube exhibiting no conductance variation with V_g; (b) p-type unipolar nanotube showing strongly suppressed conductance for larger positive voltages; (c) ambipolar nanotube demonstrating finite conductance for positive and negative voltages (V_{ds} = 0.3 V for (a, b and c)). (d) Hysteresis behavior of conductance as a function of gate voltage. Gate voltage was swept from –2.5 V to 2.5 V and back (as shown by the arrows), V_{ds} was kept 1 mV.

theoretical contact resistance of 6.45 kΩ). This assures that the presented fabrication technique is well suitable for preparing nearly ohmic contacts to the nanotubes.

Hysteretic behavior of CNTFETs was observed in conductance versus gate voltage characteristics, when the back gate voltage was swept from negative to positive direction and back. A representative example of transfer characteristics at V_{ds} = 1 mV is shown in Fig. 3(d). The measurements were taken at room temperature from a typical CNTFET, based on an individual SWCNT with a diameter of ~2 nm. A schematics of the measurement setup is shown in Fig. 2. The gate voltage was swept from –2.5 V to 2.5 V and back, as shown by the arrows in Fig. 3(d). Voltage bias was kept constant when sweeping the gate voltage. The hysteresis behavior in the transfer characteritics reveals a clear memory effect, demonstrating different conductance values at zero gate voltage depending on the sweep direction. The hysteresis loops were found to be reproducible.

4 Conclusions

We have presented a technique for the fabrication of FETs based on individual semiconducting SWCNTs. Two-terminal measurements revealed low contact resistances between electrodes and the CNT, showing that the demonstrated technique is highly suitable for preparing nearly ohmic contacts to the nanotube. Electronic transport measurements of the fabricated devices have been carried out. Both p-type unipolar and ambipolar semiconducting CNTs have been measured. Reproducible hysteretic behavior of as-fabricated devices was observed for some CNTFETs. High production yield of 85% of successfully working devices has been achieved.

Acknowledgements We acknowledge our research project collaborators: Prof. M. Ahlskog's and Prof. K. Rissanen's groups from the University of Jyväskylä, as well as companies Planar Inc (Olli Jylhä, ALD processing) and Nokia Oyj, who have supported this research work. We thank Finnish Funding Agency for Technology and Innovation (TEKES) for financial support (project number 40309/05).

© 2007 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

References

[1] J. Cui, R. Sordan, M. Burghard, and K. Kern, Appl. Phys. Lett. **81**, 3260 (2002).
[2] M. Fuhrer, B. Kim, T. Durkop, and T. Brintlinger, Nano Lett. **2**, 755 (2002).
[3] M. Radosavljevic, K. Thadani, A. Johnson, and P. Ajayan, Nano Lett. **2**, 761 (2002).
[4] A. Nasibulin, A. Moisala, D. Brown, H. Jiang, and E. Kauppinen, Chem. Phys. Lett. **402**, 227 (2005).
[5] S. Tans, C. Dekker, and A. Verschueren, Nature **393**, 49 (1998).
[6] R. Martel, T. Schmidt, H. Shea, T. Hertel, and P. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[7] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. Chan, J. Tersoff, and P. Avouris, Phys. Rev. Lett. **87**, 256805 (2001).
[8] P. Avouris, Acc. Chem. Res. **35**, 1026 (2002).
[9] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature **424**, 654 (2003).
[10] Z. Chen, J. Appenzeller, J. Knoch, Y. Lin, and P. Avouris, Nano Lett. **5**, 1497 (2005).

© 2007 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

A.II

phys. stat. sol. (b) **245**, No. 10, 2315–2318 (2008) / **DOI** 10.1002/pssb.200879596

physica status solidi b
www.pss-b.com
basic solid state physics

Effect of humidity on the hysteresis of single walled carbon nanotube field-effect transistors

Marcus Rinkiö[1,*], Marina Y. Zavodchikova[2], Päivi Törmä[3], and Andreas Johansson[1]

[1] Department of Physics, Nanoscience Center, P.O. Box 35, 40014 University of Jyväskylä, Finland
[2] Laboratory of Physics and Center for New Materials, Helsinki University of Technology, P.O. Box 5100, 02015 HUT, Finland
[3] Department of Engineering Physics, Helsinki University of Technology, P.O. Box 5100, 02015 HUT, Finland

Received 30 April 2008, revised 16 June 2008, accepted 19 June 2008
Published online 26 August 2008

PACS 68.43.–h, 73.40.Sx, 73.63.Fg, 81.07.De, 85.30.Tv, 85.35.Kt

* Corresponding author: e-mail marcus.rinkio@phys.jyu.fi, Phone: +358-14-2604725, Fax: +358-14-2604756

Single walled carbon nanotube field-effect transistors (SWCNT FETs) are attributed as possible building blocks for future molecular electronics. But often these transistors seem to randomly display hysteresis in their transfer characteristics. One reason for this is suggested to be water molecules adsorbed to the surface of the gate dielectric. In this study we investigate the hysteresis of SWCNT FETs at different relative humidities. We find that SWCNT FETs having atomic layer deposited (ALD) $HfO_2 - TiO_2 - HfO_2$ as a gate dielectric retain their ambient condition hysteresis better in dry N_2 environment than the more commonly used SiO_2 gate oxide.

© 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

1 Introduction Molecular electronics is suggested to extend the down-scaling of electronic components beyond the limitations of present Si-based technology. One of the candidates is the single walled carbon nanotube (SWCNT) [1–4], featuring either semiconducting or metallic transport properties. This in principle allows SWCNTs to replace both active components as well as their interconnects. One of the most studied components are field-effect transistors made out of carbon nanotubes. These SWCNT-FETs display often some degree of hysteresis in their transfer characteristics. For a transistor this is an unwanted attribute but it opens up new possible applications. Several studies have shown that by utilizing the hysteresis, CNT FETs can be used as a memory element or sensors [5–12]. Nevertheless, the hysteresis so far has been reported as a more or less random property among the studied CNT FETs [7,9,13] and the challenge still is to be able to control the presence of hysteresis [14].

Previously, several different models have been suggested to explain the hysteresis in the transfer characteristics of a SWCNT FET. The models include mobile ions or charges within the dielectric layer that can be relocated by gate voltage [5,6,9], defects in the nanotube itself behaving as charging centers or stationary charge traps located in the vicinity of the CNT that can be filled or emptied by charge carriers from the CNT in response to the gate voltage [5,15,16]. In this study we are focusing on the suggested model that surface chemistry plays an important role in the hysteresis of SWCNT FETs. Water molecules adhered to the surface have been shown to give a large contribution to the hysteresis of some CNT FETs [17,18]. We present the first results on how the ambient humidity changes the hysteresis in SWCNT FETs having Hf-based gate dielectric and compare it to the more conventional SiO_2.

2 Fabrication and measurement methods The samples used were fabricated in a bottom up approach described in detail in ref. [19]. As a basis of the device a highly boron-doped Si wafer was used, acting as a backgate. The backgate was covered with either thermally grown SiO_2 (nominal thickness 300 nm) or $HfO_2 - TiO_2 - HfO_2$ (nominal thickness 40-0.5-1 nm). The ALD deposition was done by Beneq Oy (Vantaa, Finland), using a Beneq P400A ALD deposition tool. The precursors used were $HfCl_4$ and H_2O for HfO_2, and $TiCl_4$ and H_2O for TiO_2. The deposition temperature was 300 °C, which produces amorphous HfO_2 films [20]. On

WILEY InterScience DISCOVER SOMETHING GREAT

© 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

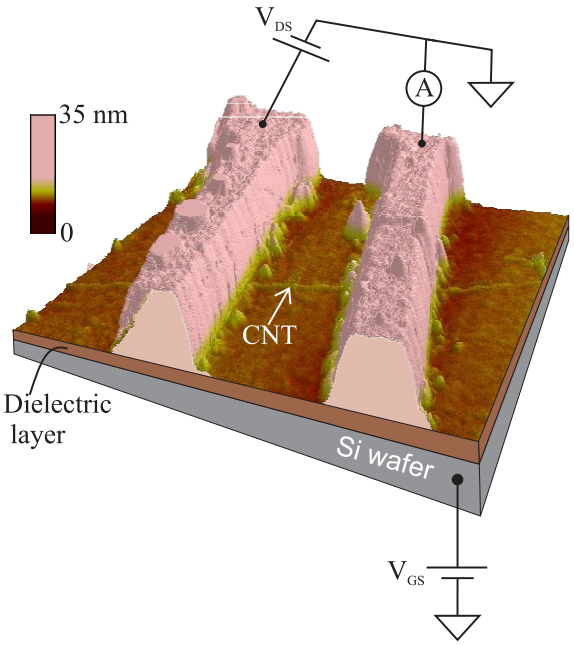

Figure 1 AFM image of a typical device, covering an area of 1 μm^2. The SWCNT is resting on the dielectric layer, and has Pd source and drain electrodes with a spacing of 260 nm. The measurement setup is schematically drawn with voltage applied to the Si wafer, acting as a backgate, and voltage applied between the drain and source electrodes while measuring the current response through the CNT.

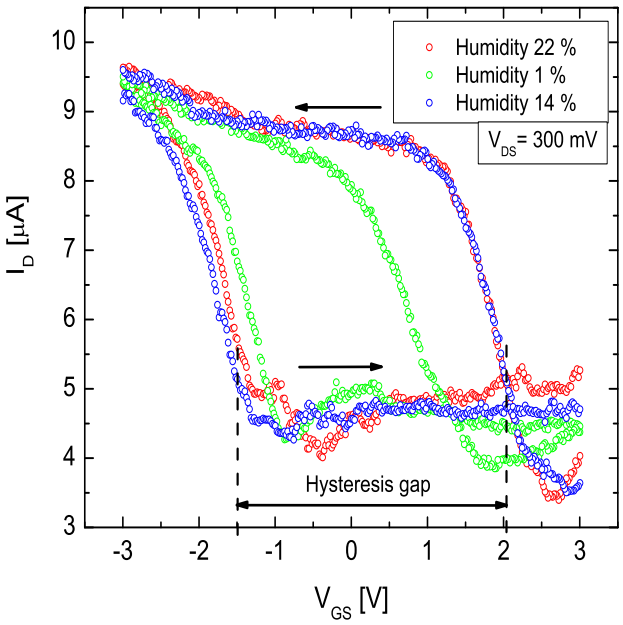

Figure 2 Hysteresis loops of SWCNT FET in different relative humidities. Drain current versus backgate voltage for a typical device with a gate dielectric of $HfO_2 - TiO_2 - HfO_2$. The arrows mark the scan direction to produce the loop. This loop is shown for three different relative humidity values; red trace for 22 %, green trace for 1 % and blue trace for 14 %. The hysteresis gap is presented for the humidity value of 14 % and is given by the difference in threshold voltages between reverse and forward scan directions.

top of this gate insulator a matrix of alignment markers was deposited, using e-beam lithography and metallization of Pd with an adhesion layer of Ti. Commercial SWCNTs produced by NanoCyl S.A. (Sambreville, BELGIUM) were suspended in a solvent by ultra-sonication. A few droplets of the nanotube suspension were then deposited onto the sample. After deposition the SWCNTs were left at random places on the oxide surface. Their locations were then precisely mapped in relation to the alignment marker matrix, using an atomic force microscope (AFM). Finally, a second e-beam lithography and subsequent metallization step was done to connect the CNTs with Pd source and drain electrodes. Here palladium was chosen for achieving a low contact resistance between electrodes and the carbon nanotube [21,22]. Also our previous work shows that Pd gives low contact resistance to our SWCNT FETs [14,19].

An AFM image of as prepared device with a schematic of the measurement setup is shown in Fig. 1. All the 12 devices measured in this study were biased with 0.3 V using a home-made voltage distribution box powered by batteries and computer controlled via a data acquisition card. The current through the tube was monitored while sweeping the backgate voltage. All measurements were carried out at room temperature in an electrically shielded room. For controlling the humidity, a measurement chamber specially made for this study was used. The chamber contains a gas inlet for dry nitrogen gas flow. A Honeywell relative humidity sensor (HIH-3602-A) with a $\pm$ 2 % total accuracy was incorporated for monitoring the relative humidity and temperature.

3 Results and discussion The focus of this study is on the influence of humidity on hysteresis in the transfer characteristics of a CNT FET [16,17]. A typical example is shown in Fig. 2 for a SWCNT resting on a backgate dielectric of $HfO_2 - TiO_2 - HfO_2$ (nominal thickness 40-0.5-1 nm) with 300 mV applied between the drain and source electrodes. All of the measured SWCNT FETs displayed a typical unipolar p-type behaviour [23,24], with suppressed conductance at positive gate voltages and a transition into a highly conducting state at negative gate voltages. While scanning the backgate from positive to negative voltages and back, the threshold voltage attains a higher value for reverse than forward sweep direction. This results in a highly reproducible hysteresis loop with different conductance values at zero backgate voltage depending on the sweep direction.

We quantify this hysteresis loop in each device in terms of the shift in threshold voltage, called the hysteresis gap (see Fig. 2). This measure relates directly to the recon-

© 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

Table 1 Hysteresis gap in dry N_2 flow (in % of hysteresis gap in ambient conditions). The accuracy used here is $\pm$ 2 %

Sample	Gate dielectric $HfO_2 - TiO_2 - HfO_2$	Gate dielectric SiO_2
1	51 %	67 %
2	61 %	28 %
3	91 %	77 %
4	68 %	47 %
5	71 %	56 %
6	67 %	
7	85 %	
Average	71 %	55 %
Sd	14 %	19 %

figuration of charges trapped in the close vicinity of the SWCNT, and is sensitive to the gate voltage scan range, the scan rate, as well as the hold time at the turning points of the scanning interval before starting the next scan in the opposite direction. While the scan rate was kept at 10 mV/s and the hold time at the turning points was close to 1 second throughout the study, the gate voltage scan range was altered between the samples due to differing gate insulator thicknesses. The samples with 300 nm thick SiO_2 dielectric were measured with a gate voltage scan range of $\pm$ 10 V, while the ALD based samples with gate insulator thickness of 41.5 nm had a gate voltage scan range of $\pm$ 3 V.

For studying the effects of humidity on these transfer characteristics, the hysteresis loop was taken at different relative humidity values. The hysteresis loops presented in Fig. 2 are taken consecutively as follows: the first trace (red) was recorded under ambient conditions with a relative humidity of 22 %. Then a dry nitrogen flow was introduced to the chamber and the humidity was monitored until it was below 1 %, which is below the lower sensing limit of our humidity sensor. The samples were kept at this point under N_2 flow for 0.5 - 18 hours, after which a second hysteresis loop trace (green) was measured. Finally the chamber was opened to ambient air. When the relative humidity reached 14 % the third trace (blue) was measured. Figure 2 shows that when relative humidity is lowered close to zero the hysteresis diminishes but does not vanish. In this case the hysteresis gap is 68 % of the original value. One sample from each dielectric was held in N_2 for longer than 0.5 hours. The development of the hysteresis gap was followed, and no noticeable change was observed. After the SWCNT FET was exposed to ambient conditions again the hysteresis loop quickly attains the original shape. The shift of threshold voltage to lower gate voltage for the reverse gate sweep in low humidity compared to higher humidity is observed. This can be attributed to the desorption of water molecules around the SWCNT FET, including surface-bound water in the vicinity of the nanotube [16, 17].

The described measurements were repeated for 7 SWCNT FETs with $HfO_2 - TiO_2 - HfO_2$ as a gate dielectric. For the 5 SWCNT FETs with SiO_2 as a gate dielectric, the hysteresis loop was measured in ambient conditions and in dry nitrogen flow to make a good comparison between these devices. Only devices showing hysteresis in ambient conditions were chosen. Our results are presented in Table 1, displaying the change in hysteresis gap in dry N_2 flow compared to the original value under ambient conditions for different samples having ALD-based triple-stack or SiO_2 gate dielectrics. Table 1 shows that in dry N_2 flow the hysteresis gap of SWCNT FETs having gate dielectric of $HfO_2 - TiO_2 - HfO_2$ decreases less than that of SWCNT FETs having SiO_2 gate dielectric when compared to original gap size. The mean of hysteresis gaps of the devices having gate dielectric of $HfO_2 - TiO_2 - HfO_2$ at low humidity is at 71 %, while the mean of devices having SiO_2 as a gate dielectric is at 55 %. The standard deviations are 14 % and 19 %, respectively. This indicates that the devices having an ALD-based gate dielectric retain their hysteresis gap better and have smaller distribution than devices on SiO_2.

It is known that water molecules can bind on the hydroxylated silica surface [25]. J. S. Lee *et al.* have shown that surface-bound water on SiO_2 alone is not the only cause of gate hysteresis in SWCNT FETs [16] contradicting the earlier finding of W. Kim *et al.* [17]. On HfO_2 this specific surface chemistry is absent but P. Raghu *et al.* have shown that moisture adsorbs better on HfO_2 than on SiO_2 due to the polar nature of amorphous HfO_2. In the same study it is also shown that water desorbs slower from HfO_2 than from SiO_2 but in both cases almost all adsorbed water could be removed after a 300 °C bake-out [20]. This is one possibility of explaining our findings, that more moisture is desorbed from the SiO_2 than from the $HfO_2 - TiO_2 - HfO_2$ gate dielectric. On the other hand we have previously shown that the hysteresis gap can be controlled by carefully designing the gate dielectric in nm-thin layers. By using the same ALD grown $HfO_2 - TiO_2 - HfO_2$ gate oxide used here we achieved the first CNT FETs with consistent and narrowly distributed hysteresis gap in their transfer characteristics [14]. ALD is known to produce a very conformal coating, while the preparation of themally grown SiO_2 may produce a more porous film. This could have an influence on the adsorption/desorption behavior of water. The effect and magnitude of adsorbed water on SWCNT FET gate dielectrics is still under debate. This study gives the first results on the effect of humidity on hysteresis of SWCNT FETs on $HfO_2 - TiO_2 - HfO_2$ gate dielectric.

4 Conclusions We have fabricated and investigated the influence of relative humidity on hysteresis in the transfer characteristics of SWCNT FETs with gate dielectrics of either $HfO_2 - TiO_2 - HfO_2$ or SiO_2. We have shown

© 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

that reduction in relative humidity decreases the hysteresis on SWCNT FETs having $HfO_2 - TiO_2 - HfO_2$ gate dielectric but this decrease is even larger in SWCNT FETs having a more conventional SiO_2 as a gate oxide. The role of humidity on CNT FETs is important for their possible memory and sensor applications and it needs to be studied further to improve the reliability and operation of these devices.

Acknowledgements We acknowledge valuable discussions with our research project collaborators: Prof. M. Ahlskog's and Prof. K. Rissanen's groups at University of Jyväskylä, Esko Kauppinen's group at Helsinki University of Technology, as well as the companies Vaisala Oyj and Nokia Oyj. We thank Beneq Oy, Olli Jylhä for ALD processing and suggesting the materials used. This work was supported by the Finnish Funding Agency for Technology and Innovation (TEKES), project number 40309/05, and the Academy of Finland. M. R. would like to acknowledge support from the Magnus Ehrnrooth Foundation and the Finnish Foundation for Technology Promotion (TES).

References

[1] C. Dekker, Phys. Today **52**, 22 (1999).
[2] H. Dai, Surf. Sci. **500**, 218 (2002).
[3] P. L. McEuen, M. S. Fuhrer, and H. K. Park, IEEE Trans. Nanotechnol. **1**, 78 (2003).
[4] W. Lu and C. M. Lieber, Nature Mater. **6**, 841 (2007).
[5] M. S. Fuhrer, B. M. Kim, T. Durkop, and T. Britlinger, Nano Lett. **2**, 755 (2002).
[6] M. Radosavljevic, M. Freitag, K. V. Thadani, and A. T. Johnson, Nano Lett. **2**, 761 (2002).
[7] J. B. Cui, R. Sordan, M. Burghard, and K. Kern, Appl. Phys. Lett. **81**, 3260 (2002).
[8] W. B. Choi, S. Chae, E. Bae, J.-W. Lee, B.-H. Cheong, J.-R. Kim, and J.-J. Kim, Appl. Phys. Lett. **82**, 275 (2003).
[9] K. Bradley, J. Cumings, A. Star, J.-C. P. Gabriel, and G. Gruner, Nano Lett. **3**, 639 (2003).
[10] S. Wang and P. Sellin, Appl. Phys. Lett. **87**, 133117 (2005).
[11] B. Mahar, C. Laslau, R. Yip, and Y. Sun, IEEE Sens. J. **7**, 266 (2007).
[12] J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, and H. Dai, Science **287**, 622 (2000).
[13] A. Vijayaraghavan, S. Kar, C. Soldano, S. Talapatra, O. Nalamasu, and P. M. Ajayan, Appl. Phys. Lett. **89**, 162108 (2006).
[14] M. Rinkiö, A. Johansson, M. Y. Zavodchikova, J. J. Toppari, A. G. Nasibulin, E. I. Kauppinen, and P. Törmä, arXiv:0801.2359v2 [cond-mat.mes-hall].
[15] S. Kar, A. Vijayaraghavan, C. Soldano, S. Talapatra, R. Vajtai, O. Nalamasu, and P. M. Ajayan, Appl. Phys. Lett. **89**, 132118 (2006).
[16] J. S. Lee, S. Ryu, K. Yoo, I. S. Choi, W. S. Yun, and J. Kim, J. Phys. Chem. Lett. C **111**, 12504 (2007).
[17] W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, and H. Dai, Nano Lett. **3**, 193 (2003).
[18] S. Wang, P. Sellin, Q. Zhang, and D. Yang, Current Nanoscience **1**, 43 (2005).
[19] M. Y. Zavodchikova, A. Johansson, M. Rinkiö, J. J. Toppari, A. G. Nasibulin, E. I. Kauppinen, and P. Törmä, phys. stat. sol. (b) **244**, 4188 (2007).
[20] P. Raghu, N. Rana, C. Yim, E. Shero, and F. Shadmana, J. Electrochem. Soc **50**, 186 (2003).
[21] Z. Chen, J. Appenzeller, J. Knoch, Y. Lin, and Ph. Avouris, Nano Lett. **5**, 1497 (2005).
[22] J. J. Palacios, P. Tarakeshwar, and D. M. Kim, Phys. Rev. B **77**, 113403 (2008).
[23] S. J. Tans, A. R. M. Verschueren, and C. Dekker, Nature **393**, 49 (1998).
[24] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[25] L. T. Zhuravlev, Colloids Surf. A **173**, 1 (2000).

© 2008 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

A.III

New Journal of Physics
The open-access journal for physics

High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric

Marcus Rinkiö[1], Andreas Johansson[1,5], Marina Y Zavodchikova[1,3], J Jussi Toppari[1], Albert G Nasibulin[2], Esko I Kauppinen[2] and Päivi Törmä[1,4]

[1] Department of Physics, Nanoscience Center, PO Box 35, 40014 University of Jyväskylä, Finland
[2] Center for New Materials and Laboratory of Physics, Helsinki University of Technology, PO Box 1602, 02044 Espoo, Finland
E-mail: andreas.johansson@phys.jyu.fi

New Journal of Physics **10** (2008) 103019 (16pp)
Received 23 June 2008
Published 16 October 2008
Online at http://www.njp.org/
doi:10.1088/1367-2630/10/10/103019

Abstract. Carbon nanotube field-effect transistors (CNT FETs) have been proposed as possible building blocks for future nano-electronics. But a challenge with CNT FETs is that they appear to randomly display varying amounts of hysteresis in their transfer characteristics. The hysteresis is often attributed to charge trapping in the dielectric layer between the nanotube and the gate. We find that the memory effect can be controlled by carefully designing the gate dielectric in nm-thin layers. By using atomic layer depositions (ALD) of HfO_2 and TiO_2 in a triple-layer configuration, we achieve to our knowledge the first CNT FETs with consistent and narrowly distributed memory effects in their transfer characteristics. The study includes 94 CNT FET samples, providing a good basis for statistics on the hysteresis seen in five different CNT-gate configurations.

[3] Present address: Center for New Materials and Laboratory of Physics, Helsinki University of Technology, PO Box 5100, 02015 HUT, Finland.
[4] Present address: Department of Applied Physics, Helsinki University of Technology, PO Box 5100, 02015 HUT, Finland.
[5] Author to whom any correspondence should be addressed.

© IOP Publishing Ltd and Deutsche Physikalische Gesellschaft

Contents

1. Introduction

The quasi-one-dimensional, nearly perfect, crystalline structures of carbon nanotubes (CNTs) make them promising candidates [1]–[4] to extend the down-scaling of electronic components beyond the limitations of present Si-based technology. Featuring either semiconducting or metallic transport properties, they can in principle replace both active components as well as their interconnects. It was suggested that CNT-based devices could be mounted with an integration level of up to $10^{12}\,\mathrm{cm}^{-2}$ [5], which is about four orders of magnitude higher density than in current technology. Field-effect transistors (FETs) have been made out of CNTs with impressive device parameters, e.g. subthreshold slopes close to $60\,\mathrm{mV\,decade}^{-1}$ [6], and field-effect mobilities of up to $79\,000\,\mathrm{cm}^2\,\mathrm{V}^{-1}\mathrm{s}^{-1}$ [7]. But there are many challenges with incorporating CNTs into logic devices, such as being able to separate the semiconducting CNTs from the metallic ones, or to control their placement with nanometre accuracy. Another challenge with CNT FETs is that often they display some degree of hysteresis in their transfer characteristics. For a CNT FET this is an unwanted feature, rendering it unpredictable in its output, and it has motivated several studies to find ways to prevent or remove these tendencies [6], [8]–[11]. On the other hand, the presence of hysteresis opens up the possibility to utilize the device as a memory element instead. This has been pointed out by several studies [12]–[17], demonstrating CNT FETs with ON and OFF states which are well separated and addressable with positive or negative gate voltage pulses. However, the challenge is to be able to control the presence of hysteresis, which so far has been reported as a widely varying property among the studied CNT FETs [14, 16, 18]. In this paper, we use Hf-based atomic layer deposition (ALD)-grown gate dielectric to control hysteresis and achieve a 100% yield in memory effect, as well as study the origin of the hysteresis in our devices. This is to our knowledge the first report on CNT FETs featuring memory effects that are *consistent* from sample to sample.

Several different models, which all can explain hysteresis in the transfer characteristics of a CNT FET, have been suggested. First it was pointed out that, especially for CNT FETs with a gate insulator of SiO_2, it may have the same origin as the hysteresis sometimes seen in

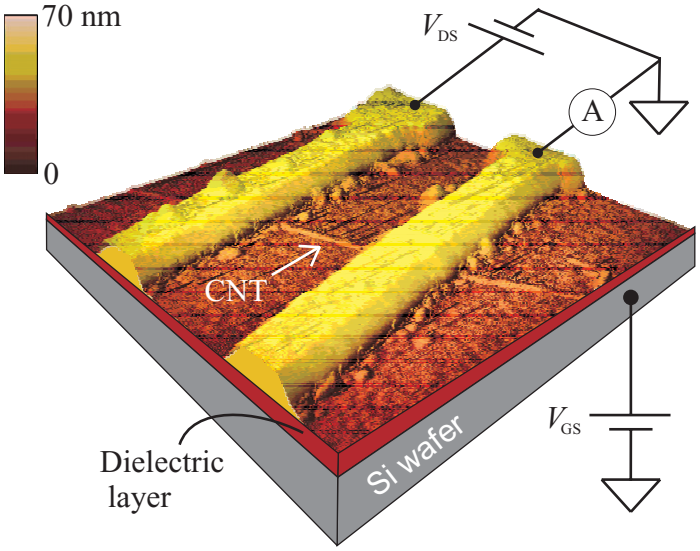

Figure 1. AFM image of a typical device, covering an area of 1 μm^2. The SWCNT is resting on a dielectric layer, and has source and drain electrodes of Pd deposited on top with a spacing of 260 nm. The measurement setup is schematically drawn with voltage applied to the Si wafer, acting as a backgate, and voltage applied between the drain and source electrodes while measuring the current response through the CNT.

conventional Si-MOSFETs [12, 13, 16]. There it is known that mobile ions or charges within the SiO_2 layer can relocate in response to the applied gate voltage, and as a result modify the local electric field sensed by the charge carriers in the conduction channel. But this is not the only proposed mechanism. It has also been suggested [12, 19, 20] that the charge traps may not be mobile, but located stationary in the near vicinity of the CNT. An applied gate voltage could then assist in filling or emptying the charge traps with charge carriers moving in the CNT, which in turn screens the applied electric field and causes hysteresis to appear in the gate voltage response. Yet another possibility is that surface chemistry plays an important role. For example water molecules adhered to the surface have been shown [8, 10] to give a large contribution to the hysteresis of some CNT FETs. A fourth model suggests that defects in the nanotube itself could provide charging centers, which can be filled or emptied in response to the gate modulation. A charging center in this case may be a carbon atom substituted with a different atom or molecule, which can donate or accept electrons from the conduction channel. All four models may contribute in varying degree to hysteresis in the transfer characteristics of a CNT FET. One way of controlling the memory response would be to tailor one mechanism to dominate the electrostatic charging around the CNT conduction channel.

2. Experiment

2.1. Sample preparation

This study includes in total 94 single-walled carbon nanotube (SWCNT) FETs with varying gate insulator, which by far exceeds the number of samples included in earlier studies of hysteresis in CNT FETs [8, 10, 12, 13, 15, 16, 19, 20]. An atomic force microscope (AFM) image of a

typical sample is shown in figure 1. The samples were built in a bottom-up approach, described in detail in [21], starting from a highly boron-doped Si wafer which acts as a backgate. While there are many possible device parameters to vary, we chose here to study the influence of two of them; the first is the composition of the dielectric material and the second is variation of the thickness of the same. The backgate was covered with an ALD layer of either Al_2O_3 (nominal thickness: 20 nm), HfO_2 (20 nm), or HfO_2–TiO_2–HfO_2 (40–0.5–3 or 40–0.5–1 nm). All ALD depositions were done at Beneq Oy. (Espoo, Finland), using a Beneq P400A ALD deposition tool. The idea motivating the triple-layer structure is to create, in a controlled way, charge traps in the close vicinity of the CNT FET [15]. The interface between two different ALD layers may serve that purpose, and thereby dominate the local electrostatic charging effects. We also prepared reference samples with gate insulator of the more commonly used thermally grown SiO_2 (300 nm). On top of the gate insulator a matrix of alignment markers was deposited, using e-beam lithography and metallization of Pd with an adhesion layer of Ti. CNTs were then deposited in two different ways, depending on their origin. Our primary source was commercial SWCNTs produced by NanoCyl S.A. (Sambreville, Belgium), bought in the form of black powder, which was suspended in dichloroethane by ultra-sonication for about 30 min. Typically 5–15 droplets of the nanotube suspension were then deposited onto the sample while it was spun at 1500 rpm. We also prepared, as a reference, 11 samples with SWCNTs from a hot wire generator reactor on to substrates with the HfO_2–TiO_2–HfO_2 (40–0.5–1 nm) triple-layer. The hot wire generator reactor is based on aerosol (floating catalyst) synthesis of CNTs. Iron particles and carbon monoxide were utilized as the catalyst and the carbon source, respectively [22]. Individual CNTs were filtered out from the bundled tubes in the gas phase as described in [23] and deposited onto the sample surface at room temperature using a thermophoretic precipitator [24]. In both methods CNTs were left at random places on the surface. Their locations were then mapped in relation to the matrix of alignment markers, using an AFM. The AFM images allowed us to select what appeared to be non-bundled and clean CNTs for the remaining fabrication steps, but some of the devices may also consist of a small bundle of semiconducting CNTs. Finally, electrodes of Pd were deposited onto the ends of the CNTs, with the help of e-beam lithography and subsequent metallization. The CNT diameters and FET channel lengths were then determined from AFM images of the devices, and can be found in appendix A.

2.2. Measurements

All measurements in this study were carried out at room temperature in an electrically shielded room, either under ambient conditions or in a chamber under dry nitrogen gas flow, which reduced the relative humidity to below 1% (below the resolution of our humidity sensor). Two-terminal measurements were performed, with the substrate acting as a backgate. Dc measurements were used with the applied voltage given by a home-built voltage distribution box, powered by batteries and computer controlled via a data acquisition card, while measuring the current response through the nanotube. I–V characteristics and conductance response to an applied backgate voltage were collected from all samples. A schematic of the measurement setup is drawn in figure 1. The samples with linear I–V characteristics and conductance not sensitive to an applied backgate voltage were considered to have metallic CNTs. The study includes in total 94 semiconducting SWCNTs, featuring a clear backgate dependence. These comprise about 82% of all the samples made, which is somewhat higher than the expected

67% for randomly picked CNT chiralities. Surprisingly, eight of the eleven devices made with SWCNTs from the hot wire generator reactor show clear metallic behavior. Of the three remaining semiconducting SWCNTs, one had a malfunctioning backgate, leaving only two CNT FETs of this kind added to the study. As will be seen in figure 3, these two CNT FETs do not deviate notably in performance compared to the other 25 devices with the same gate dielectric.

2.3. Contact resistance

An often problematic part of CNT sample processing is to achieve low contact resistance between electrode and nanotube [25]. As an upper limit measure of the contact resistances in our devices, we sampled the total two-terminal resistances of the metallic CNTs. These were found to be in the range of 14–160 kΩ, which is close to the theoretical minimum resistance for SWCNTs of $1/2G_0 = h/4e^2 \approx 6.45\,\mathrm{k\Omega}$. Here G_0 is the quantum unit of conductance, e is the charge of the electron and h is Planck's constant.

3. Results

The focus of this study is on the appearance of hysteresis in the transfer characteristics of our CNT FETs in relation to the gate dielectric used. Seven of the 94 samples had the backgate covered with ALD of Al_2O_3 (nominal thickness: 20 nm), 14 with ALD of HfO_2 (20 nm), 11 with ALD of HfO_2–TiO_2–HfO_2 (40–0.5–3 nm), 27 with ALD of HfO_2–TiO_2–HfO_2 (40–0.5–1 nm), and the remaining 25 with thermally grown SiO_2 (300 nm). A typical example of a CNT FET exhibiting hysteresis is shown in figure 2(a), for a SWCNT resting on a backgate dielectric of 20 nm thick HfO_2 with 10 mV applied between the drain and source electrodes. Most SWCNT FETs displayed typical unipolar p-type behavior [26, 27], with strongly suppressed conductance at positive gate voltages and a transition into a highly conducting state at negative gate voltages. A few devices showed ambipolar dependence with a somewhat increased conductance at high positive backgate voltages, which has been attributed to semiconducting nanotubes with a small bandgap [28, 29]. From these data, estimates of field-effect mobility and subthreshold slope have been made, which are presented in appendix C. Upon scanning the backgate voltage back and forth, the threshold voltage attains in some, but not all, of the CNT FETs a higher value for the reverse sweep than for the forward sweep, resulting in a highly reproducible hysteresis loop with different conductance values at zero backgate voltage depending on the sweep direction. In figure 2(b), it is demonstrated how the current response of such a CNT FET can be switched between the two states by sending either a positive or negative voltage pulse to the backgate.

The working memory devices included in this study have so far been subjected to slow switching frequencies of up to 10 Hz. Some of the devices show charge stability with no change in ON or OFF state for several days, while others have a retention time of down to a few hours. Durability has been tested for a few of the CNT memories, with no significant change in ON/OFF states after switching 10^4 times or more. We are currently studying these aspects, but would like to add they should not be compared to single device characteristics of state-of-the-art commercial memories before the gate configuration is changed from a backgate to a local gate for each CNT. That work is also in progress.

All mass-fabricated electronic devices have a natural variation of characteristic parameters, which is acceptable as long as the parameter distribution is narrow enough not to interfere

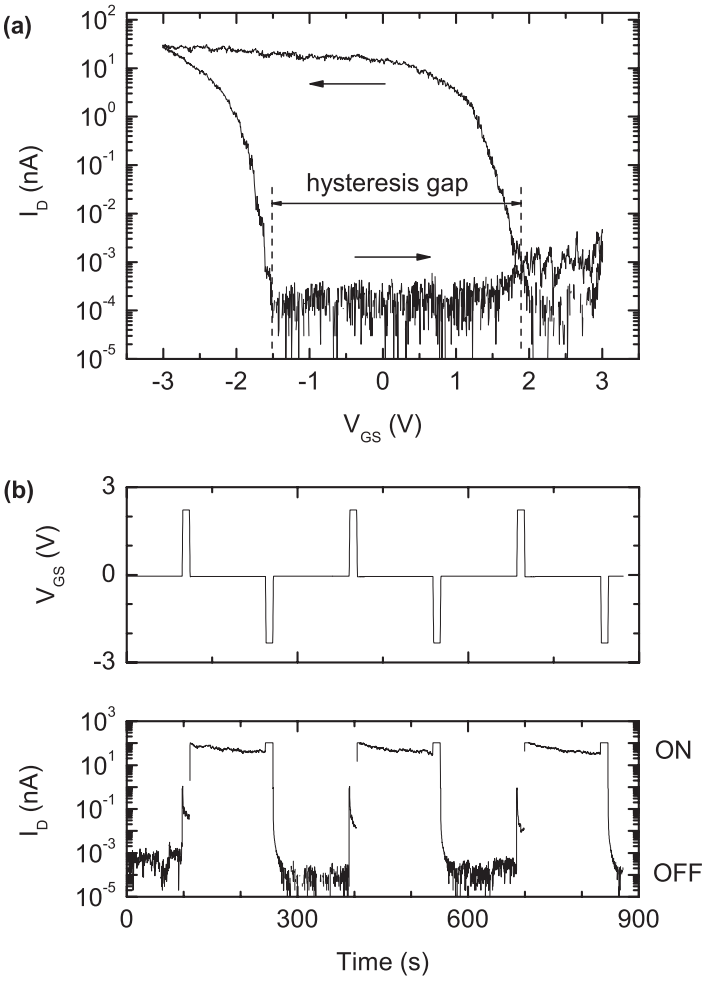

Figure 2. Memory effect for a typical SWCNT FET with a gate dielectric of HfO_2. (a) Drain current versus backgate voltage at a constant drain–source voltage of 10 mV. The arrows mark the scan direction within the loop. The hysteresis gap is given by the difference in threshold voltage between the reverse and the forward scan direction. (b) Demonstration of its memory function. The upper panel displays the voltage applied to the backgate as a function of time. The lower panel shows how at a constant V_{DS} of 0.1 V, the current response through the CNT switches to an ON state or an OFF state in response to a positive or negative voltage pulse on the backgate, respectively.

with its intended function. The large number of devices in this study allows us to estimate the distribution of hysteresis response seen for differing gate dielectrics. We quantify the memory effect in each device in terms of the shift in threshold voltage, called the hysteresis gap (see figure 2(a)). This measure relates directly to the reconfiguration of charges trapped in the close vicinity of the SWCNT, and is sensitive to the gate voltage scan rate, the scan range, as well as the hold time at the turning points of the scanning interval before starting the next scan. While the scan rate was kept at 10 mV s^{-1} and the hold time at the turning points was close to 1 s throughout the study, the gate voltage scan range was altered between the samples

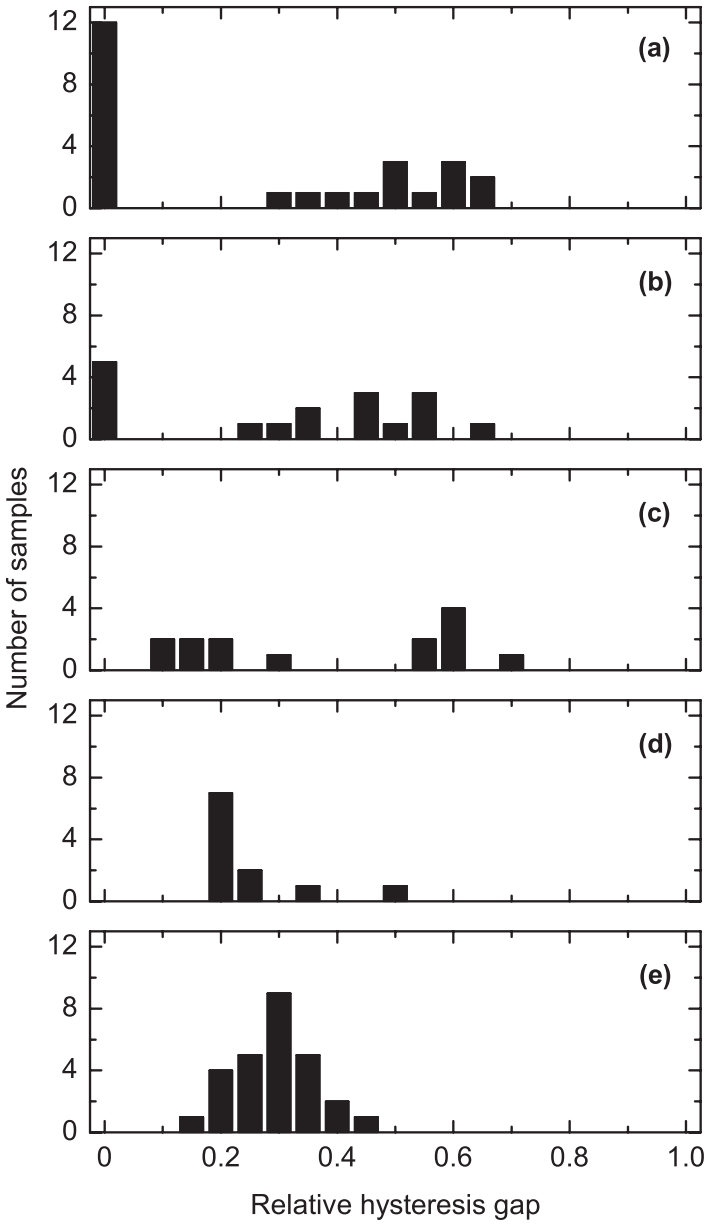

Figure 3. Statistics of the relative hysteresis gap from 94 devices with varying gate dielectric. Each column represents a 5% interval of the full scale. The gate dielectric is in (a) SiO_2 (300 nm), (b) Al_2O_3 (20 nm), (c) HfO_2 (20 nm), (d) HfO_2–TiO_2–HfO_2 (40–0.5–3 nm) and (e) HfO_2–TiO_2–HfO_2 (40–0.5–1 nm).

due to differing gate insulator thicknesses. The samples with 300 nm thick SiO_2 dielectric were measured with a gate voltage scan range of ± 10 V, while the ALD based samples with gate insulator thicknesses of 20–43.5 nm had gate voltage scan ranges of ± 2–3 V. To allow comparison between these different cases, we calculated the relative hysteresis gap, where the hysteresis gap is normalized by the gate scan range. The measured threshold voltages together with ON and OFF conductance values for the CNT devices are presented in appendix B.

Our results are plotted in figure 3. Each column represents a 5% interval of the relative hysteresis gap along the x-axis. We show in figure 3(a) that from 25 SiO_2-based CNT FETs, 12

Table 1. Statistics taken from data in figure 3, with the lettering of gate dielectric in the first column according to that of the panels. The following columns display the total number of samples, the mean relative hysteresis gap, and its standard deviation.

Gate dielectric	Number of samples	Mean relative hysteresis gap	Standard deviation
a	25	0.27	0.27
b	17	0.32	0.24
c	14	0.38	0.22
d	11	0.26	0.09
e	27	0.29	0.06

devices do not exhibit hysteresis at all. The remaining 13 display a relative hysteresis gap almost evenly spread within the interval 30–65%. The results are in agreement with earlier reports [14, 16] on SiO_2-based SWCNT FETs, finding that only a fraction of the produced devices show hysteresis in their transfer characteristics. The picture is very similar in figure 3(b), where the SWCNT FETs have a gate dielectric of 20 nm thick ALD grown Al_2O_3. Five devices show no hysteresis, whereas 12 devices have their relative hysteresis gap within the interval 25–65%.

For the remaining three panels of figure 3, there is a distinct difference in that *all* the fabricated devices display a clear relative hysteresis gap. With memory devices in mind, this translates into a 100% fabrication yield. In figure 3(c), the gate dielectric is 20 nm thick ALD grown HfO_2. The 14 devices made have their relative hysteresis gaps spread from 10% up to 70% of the total gate scan range. While all CNT FETs in this set show a memory effect, the distribution of the relative hysteresis gaps is very wide, having a standard deviation of 22%. The following two panels of figure 3 show data from a specially designed three-layered ALD structure. It was made in order to study the hypothesis that the lower interface of the top most HfO_2 layer could play an important role in controlling the amount of charge traps available. The first deposited layer is a 40 nm thick buffer layer of HfO_2 with the purpose of providing a stable dielectric which can withstand the physical stress of sample processing. Next a 0.5 nm thick layer of TiO_2 was deposited with the intent of creating an interface to the top most layer. Finally another layer of HfO_2 was deposited, with a thickness of 3 nm in figure 3(d) and 1 nm in figure 3(e). While the total thicknesses of the ALD dielectrics in figures 3(d) and (e) are about twice the thickness in figure 3(c), the lower interface of the top HfO_2 layers are moved considerably closer to the CNT. The resulting relative hysteresis gap distributions show strongly decreased standard deviations of 0.09 and 0.06 for figures 3(d) and (e), respectively. More so, the latter panel with a top layer of only 1 nm thickness displays a distribution of relative hysteresis gap values that closely resembles the normal distribution. This indicates that the distribution is not likely to change noticeably if we were to add more samples to the study.

Our results are summarized in table 1, displaying the number of samples, the mean of the relative hysteresis gap, and its standard deviation for each type of gate dielectric according to the lettering in figure 3. Clearly, the triple layer with thinner upper HfO_2 layer is the better choice as gate insulator when preparing a memory storage device. More importantly, we show here that memory effects in a CNT FET can be controlled in ambient conditions, even without applying any kind of surface passivation layer onto the device. To test the influence of surface

chemistry (e.g. adhered H_2O molecules) on the memory effects seen for CNT FETs with the thinner triple-layer ALD dielectric, 12 of these samples were measured in a chamber with dry nitrogen gas flow, reducing the relative humidity to less than 1%. The samples were kept at these conditions from 30 min up to 18 h, while repeatedly measuring the transfer characteristics [30]. The relative hysteresis gap decreased somewhat during the first 30 min, on average 12% with a standard deviation of $\pm 8.6\%$, and was thereafter stable. The ON and OFF states remained almost unaffected. It is therefore reasonable to assume that while the water molecules adhered to the surface of the CNT and the dielectric somewhat affect the hysteresis, they play a minor role in the memory effects seen. In addition, the fact that changes in memory effects follow changes in gate dielectric, with relatively narrow distributions in two cases, discredit the model that defects in the SWCNTs are providing the charge traps responsible for the hysteresis. The reason for the differences seen between single layer dielectrics of SiO_2, Al_2O_3 and HfO_2 is difficult to discern, but may be related to differing charge trap densities, or even types of charge traps. While we have not made direct measurements of the charge trap densities, this could possibly be done for charge traps close to the surface using either scanning probe microscopy or conductive AFM.

Turning our attention to the rapidly narrowing distribution in hysteresis gap when going from single layer HfO_2 to a triple-layered dielectric structure, the most significant difference in the surrounding of the CNT is the closely located interface between the HfO_2 and the TiO_2 layer. It is commonly known that the interface between two different materials may carry defects or charge traps. An alternative explanation could be that as the top-layer of HfO_2 becomes thinner, its surface becomes rougher and hosts an increasing number of defects, e.g. oxygen vacancies. The defects may act as charge traps and cause the increased hysteresis. But here we would like to point out two opposing observations. Firstly, surface defects are likely to interact with or be screened by adhered water molecules, which then would decrease the relative hysteresis gap in ambient conditions. We see the opposite trend, a slight decrease of the relative hysteresis gap in dry nitrogen flow. Secondly, our AFM measurements show no quantitative difference in surface roughness between the samples with different layer thicknesses. Here should be added though that the AFM is working close to its limit of resolution, measuring roughnesses of the order of 0.1 nm. From Si MOSFETs it is known that mobile charge traps within the gate dielectric cause retarded hysteresis [31]. Here we see the opposite, advanced hysteresis, which is the case for charging of stationary charge traps close to the CNT. While mobile charge traps also may be present within the dielectric, and could possibly be a minor contributor to memory effects seen in the single layer dielectrics, it is reasonable to assume on the basis of these data that moving the lower interface of the upper HfO_2 layer closer to the CNT provides a layer of stationary charge traps at a well-calibrated distance from the CNT. This is supported by the notion that a layer of stationary charge traps in the vicinity of the CNT will screen the action from mobile charge carriers, thus creating a well-defined device geometry with a narrow hysteresis gap distribution. We therefore conclude that the most probable dominating charge storage mechanism in the triple layer structure is due to stationary charge traps at the lower interface of the uppermost HfO_2 layer, which are filled and emptied by charge carriers from the CNT in response to application of a negative or a positive gate voltage.

Here, we would like to end with a short discussion of the response time of the memory devices. As was mentioned earlier in the measurements section, the shortest write and erase pulses that were used for switching the CNT memories in this study had a duration of 0.1 s. From earlier studies by others we have found working frequencies for CNT FET memories of at most 100 Hz [12, 13, 32]. This is a number that needs to be improved to be able to compete

with, e.g. commercial flash memories, which currently have write and erase times approaching 100 μs [33] and readout performed in tens of nanoseconds [34]. It has been shown that the CNT FET itself can have a working frequency of tens of GHz [35], making the readout competitive. Hence, the limiting factor is the response time for write and erase operations. Here the charge trapping mechanism is of fundamental importance. Naturally, mobile ions or charges within the dielectric layer as well as molecules adhered to the surface have, due to their size, a slower response time compared to stationary charge traps, where electrons are responsible for the charge redistribution. Thus, stationary charge traps should provide the more competitive charge storage mechanism. We are currently investigating these aspects.

4. Summary

We have investigated 94 SWCNT FETs with different gate insulators, giving us unprecedented statistics on the presence of hysteresis in their transfer characteristics. We find that by using a gate dielectric composed by consecutive ALD layers of HfO_2, TiO_2, and then HfO_2 again, all SWCNT FETs display hysteresis with a narrow distribution of their relative hysteresis gaps, which narrows down further when the upper most layer is changed from 3 nm to 1 nm. The study shows that these SWCNT FETs can be fabricated and operated in ambient conditions without any surface passivation. This points toward having stationary charge traps beneath the upper layer that are dominating the electrostatic charging in the vicinity of the CNT such that the memory effect is insensitive to changes in the relative humidity. Such a layered gate dielectric is of particular interest for memory applications, providing to our knowledge the first proven route to 100% yield in single CNT-based memory elements. However, several challenges remain to be solved in order to make highly integrated CNT memory cells, such as positioning the CNTs with nm precision and providing each of them with a local, nanotube-specific gate.

Acknowledgments

We acknowledge valuable discussions with Professor H Häkkinen, and our research project collaborators: Professor M Ahlskog's and Professor K Rissanen's groups at University of Jyväskylä, as well as the companies Vaisala Oyj and Nokia Oyj. We thank Beneq Oy and Olli Jylhä for ALD processing and suggesting the materials used. This work was supported by the Finnish Funding Agency for Technology and Innovation (TEKES), project number 40309/05, and the Academy of Finland. MR acknowledges support from the Magnus Ehrnrooth Foundation and the Finnish Foundation for Technology Promotion (TES).

Appendix A. Nanotube diameters and FET channel lengths

The physical dimensions of each CNT FET was determined through AFM imaging. A pie chart of nanotube diameters used in this study is presented in figure A.1. Most of the nanotubes have diameters between 0.8 nm and 3 nm (all together 73 nanotubes, or 78%) and are interpreted as single-walled nanotubes. The rest of the tubes fall between 3 nm and 10 nm and are probably comprised of large diameter single-walled and/or multi-walled carbon nanotubes and nanotube bundles.

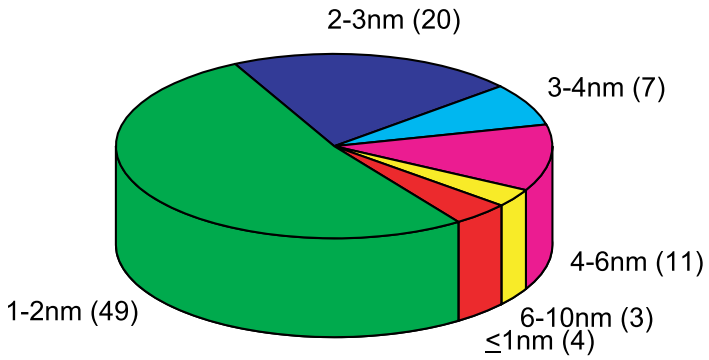

Figure A.1. Distribution of the conduction channel diameter for the CNT devices, with the interval displayed in nanometres followed by the number of CNTs within that range. The CNT diameter was determined from AFM images.

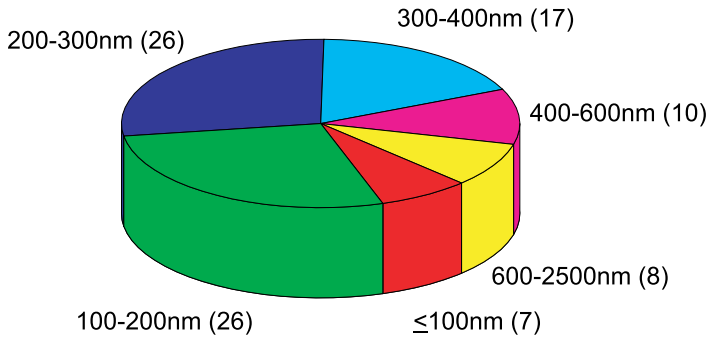

Figure A.2. Distribution of CNT lengths between the source and drain electrodes. The channel length interval is displayed followed by the number of devices in that range.

A pie chart of transistor channel lengths is presented in figure A.2. Most of the channel lengths fall in between 70 nm and 600 nm (all together 86 nanotubes, or 91%), leaving only eight devices in the range from 600 nm to 2.5 μm.

Appendix B. Threshold voltages and ON and OFF conductances

In this section, the threshold voltages from all samples in the study are presented, see figure B.1. The values are extracted from the drain current versus backgate voltage data taken at ambient conditions. When sweeping the backgate voltage in forward and reverse directions, different threshold voltages are seen for some of the samples, as explained in the measurements section and shown in figure 2(a). Both forward (blue) and reverse (red) sweep threshold voltage values are displayed, and divided into different panels according to the dielectric layer used. The last 12 samples in panel (a) and the last five samples in panel (b) show no shift in threshold voltage. The remaining samples have a shift in threshold voltage between forward and reverse scan directions, which depends on the scan rate, the scan range and the hold time when changing the scan direction. Therefore the scan rate was kept at 10 mV s^{-1} and the hold time at about 1 s throughout the study. Due to the significantly thicker (300 nm) dielectric of SiO_2 compared to

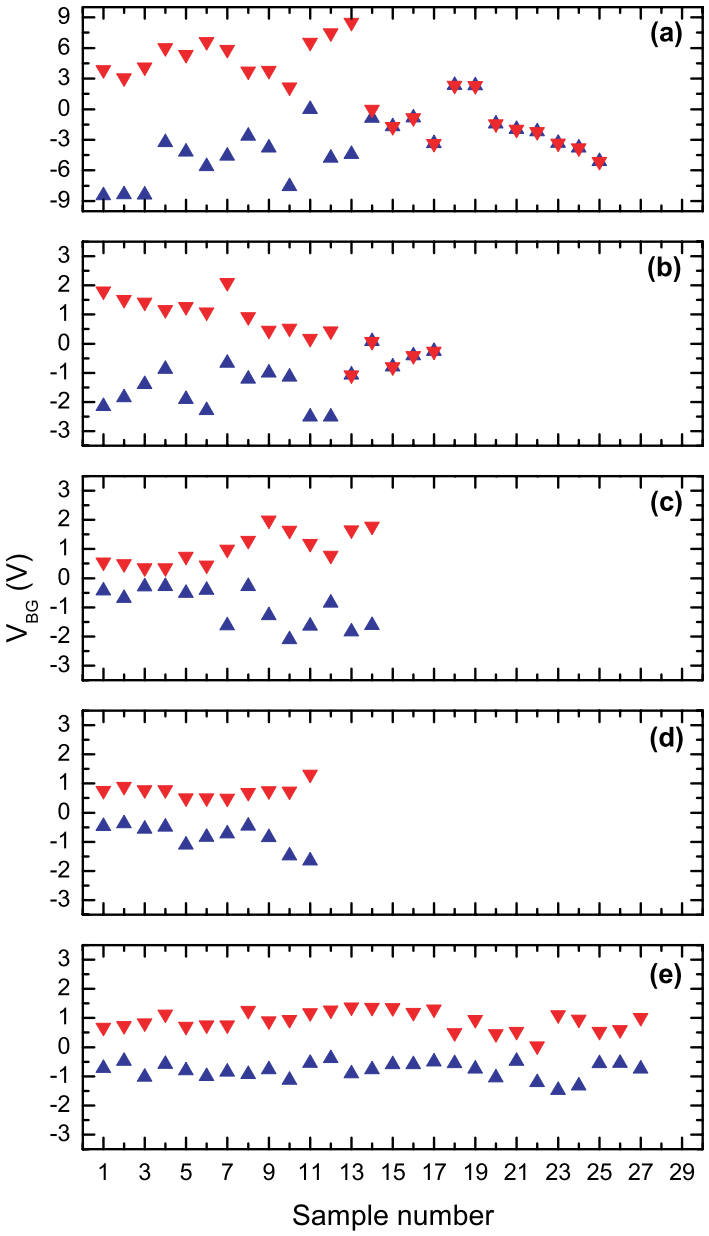

Figure B.1. Threshold voltages for forward (blue) and reverse (red) scan directions for all samples. The voltage scan range was in (a) ±10 V and in the rest of the panels ±2–3 V. The gate dielectric is in (a) SiO_2 (300 nm), (b) Al_2O_3 (20 nm), (c) HfO_2 (20 nm), (d) HfO_2–TiO_2–HfO_2 (40–0.5–3 nm) and (e) HfO_2–TiO_2–HfO_2 (40–0.5–1 nm).

the other gate dielectrics (20–43.5 nm), a higher backgate voltage range was used to produce the electric field strength required for reaching the saturation plateau in the ON state. All the SiO_2 based CNT FETs in figure B.1(a) have a scan range of ±10 V. All the samples in the remaining panels have a scan range of ±3 V, except for a few exceptions. The exceptions are samples 11 in panel (c) and 17, 25 and 26 in panel (e), which have a scan range of ±2.5 V and sample 12 in

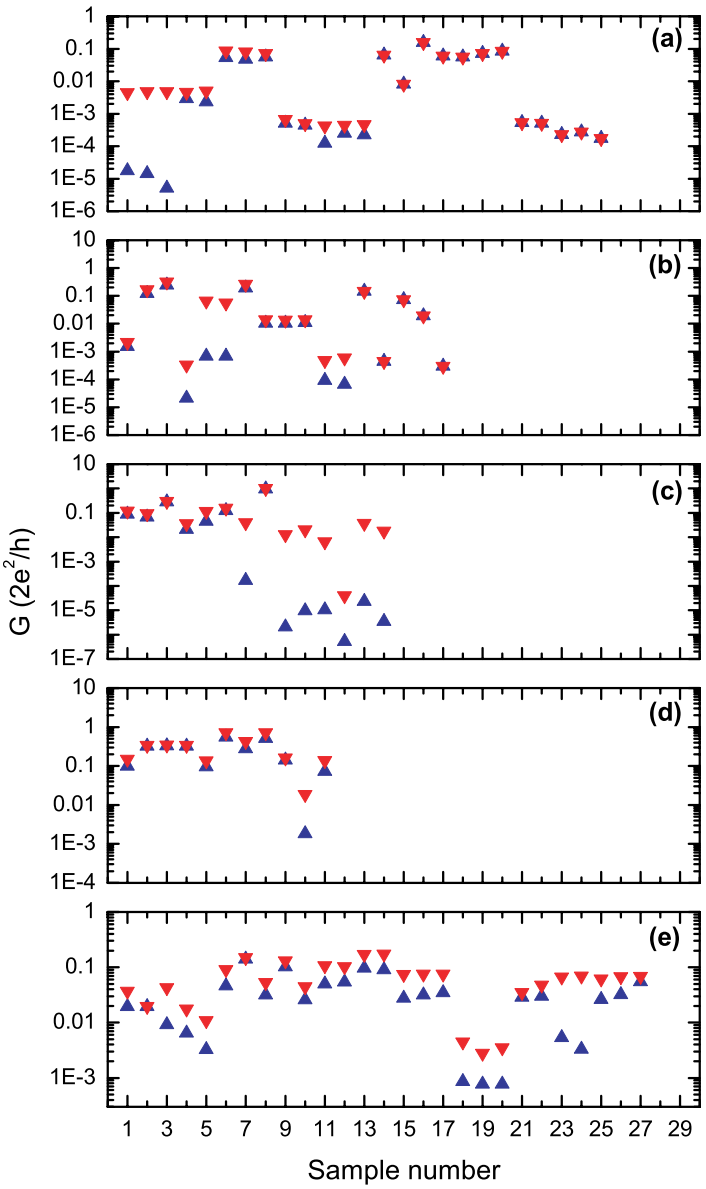

Figure B.2. ON (red) and OFF (blue) conductances for the CNT memories at zero gate voltage. The gate dielectric is in (a) SiO_2 (300 nm), (b) Al_2O_3 (20 nm), (c) HfO_2 (20 nm), (d) HfO_2–TiO_2–HfO_2 (40–0.5–3 nm) and (e) HfO_2–TiO_2–HfO_2 (40–0.5–1 nm).

panel (c) which has a scan range of ±2 V. It has been shown that for CNT FETs with hysteresis, the threshold voltage value scales roughly linearly with the scan range for quite large voltage ranges [10, 18]. Therefore we calculate the hysteresis gap and normalize it with the scan range to include the samples with a differing scan range. The normalization also makes comparison of the hysteresis gap distribution between different samples sets easier, as seen in figure 3.

The corresponding ON and OFF conductance values for the memory devices are displayed in figure B.2. The ON and OFF values are taken at zero gate voltage, as appropriate for nonvolatile memory readout. The last 12 samples in panel (a) and the last five samples in

panel (b) have no shift in threshold voltage, and thus show the same conductance value for both forward and reverse scan directions. The best memory devices have an ON/OFF ratio of about four orders of magnitude, while some of the others have a value just above 1. We would like to point out that in these cases the ON and OFF states were clearly separated and reproducible in the data. The small ON/OFF ratios in some of the samples are caused by a 'bad' or highly conducting OFF state, which could be explained by these devices consisting of either a small band gap CNT or a bundle of several CNTs instead of a single tube. But for memory applications, a large ON/OFF ratio is of much smaller importance than having a narrowly distributed hysteresis gap. We therefore also valued these samples and included them in the study.

Appendix C. Mobility and subthreshold swing

For determining mobilities for our devices we first calculated the nanotube capacitances per unit length with respect to the backgate given by $C_{bg}/L \approx 2\pi\varepsilon\varepsilon_0/ln(2h/r)$, where r and L are the nanotube radius and the length of the device, and h and ε_0 the thickness and the average dielectric constant of the dielectric [27]. For the SiO_2 samples the calculated capacitances were around $C_{bg}/L \sim 0.33\,\mathrm{pF\,cm^{-1}}$ and for the Al_2O_3 samples $C_{bg}/L \sim 1.1\,\mathrm{pF\,cm^{-1}}$. In the capacitance calculation, we used average dielectric constant values of 3.95 for thermally grown SiO_2 and 7.5 for the ALD grown Al_2O_3 gate dielectric. For the ALD grown HfO_2-based gate dielectrics we used an ε_0 value of 25 for all. The corresponding capacitances are $C_{bg}/L \sim 4.0\,\mathrm{pF\,cm^{-1}}$ for the HfO_2 (20 nm) samples and for the HfO_2–TiO_2–HfO_2 (40–0.5–3 nm) and (40–0.5–1 nm) samples $C_{bg}/L \sim 3.2\,\mathrm{pF\,cm^{-1}}$, and $C_{bg}/L \sim 3.7\,\mathrm{pF\,cm^{-1}}$, respectively. As most of the calculated capacitances are close to the quantum capacitance of a carbon nanotube having a value in the order of $C_q/L = 4e^2/\pi\hbar v_F \sim 4\,\mathrm{pF\,cm^{-1}}$, we need to take C_q into account. Here v_F is the Fermi velocity. The C_{bg} and the C_q add inversely, so that the total capacitance is $C = (1/C_{bg} + 1/C_q)^{-1}$ [36]. For devices having SiO_2 as a gate dielectric the contribution from the gate capacitance clearly dominates over the quantum capacitance.

For calculating the mobility of our devices we used the so-called 'field-effect mobility' μ_{fe}, which is often used to compare device properties. It is device specific and includes e.g. surface effects, contact resistances, etc. The field-effect mobility of a SWCNT FET can be calculated by [7]

$$\mu_{fe} = \frac{L^2}{C}\frac{\partial G}{\partial V_{bg}}, \quad \text{where } V_{bg} \text{ is the backgate voltage.} \tag{C.1}$$

Purewal *et al* [37] reported electron mean free paths for semiconducting SWCNTs ranging from ~250 nm to ~800 nm at room temperature. The majority of our CNT devices have lengths that fall between 70 nm and 600 nm, and are thus in the ballistic limit where the field-effect mobility does not apply. We therefore calculated the mobility for our longest device of 2.5 μm, which has HfO_2–TiO_2–HfO_2 (40–0.5–1 nm) as its gate dielectric. Using equation (C.1), we extracted a value of $200\,\mathrm{cm^2\,V^{-1}s^{-1}}$, which corresponds well to previously reported mobilities for similar devices [12, 13, 27, 38, 39].

We also calculated the subthreshold swing S, which is given by $(\mathrm{d}(\log G)/\mathrm{d}V_{bg})^{-1}$. We found for our SWCNT FETs values as small as $100\,\mathrm{mV\,decade^{-1}}$, e.g. from the data shown in figure 2(a). This is close to the theoretical limit of $60\,\mathrm{mV\,decade^{-1}}$ [6].

References

[1] Dekker C 1999 Carbon nanotubes as molecular quantum wires *Phys. Today* **52** 22–8

[2] Dai H 2002 Carbon nanotubes: opportunities and challenges *Surf. Sci.* **500** 218–41

[3] McEuen P L, Fuhrer M S and Park H K 2003 Single-walled carbon nanotube electronics *IEEE Trans. Nanotechnol.* **1** 78–85

[4] Lu W and Lieber C M 2007 Nanoelectronics from the bottom up *Nat. Mater.* **6** 841–50

[5] Rueckes T, Kim K, Joselevich E, Tseng G Y, Cheung C and Lieber C M 2000 Carbon nanotube-based nonvolatile random access memory for molecular computing *Science* **289** 94

[6] Weitz R T, Zschieschang U, Effenberger F, Klauk H, Burghard M and Kern K 2007 High-performance carbon nanotube field effect transistors with a thin gate dielectric based on a self-assembled monolayer *Nano Lett.* **7** 22–7

[7] Dürkop T, Getty S A, Cobas E and Fuhrer M S 2004 Extraordinary mobility in semiconducting carbon nanotubes *Nano Lett.* **4** 35

[8] Kim W, Javey A, Vermesh O, Wang Q, Li Y and Dai H 2003 Hysteresis caused by water molecules in carbon nanotube field-effect transistors *Nano Lett.* **3** 193

[9] Ozel T, Gaur A, Rogers J A and Shim M 2005 Polymer electrolyte gating of carbon nanotube network transistors *Nano Lett.* **5** 905

[10] Wang S, Sellin P, Zhang Q and Yang D 2005 Nonvolatile memory from single-walled carbon nanotube-based field effect transistors *Curr. Nanosci.* **1** 43

[11] McGill S A, Rao S G, Manandhar P, Xiong P and Hong S 2006 High-performance, hysteresis-free carbon nanotube field-effect transistors via directed assembly *Appl. Phys. Lett.* **89** 163123

[12] Fuhrer M S, Kim B M, Durkop T and Britlinger T 2002 High-mobility nanotube transistor memory *Nano Lett.* **2** 755

[13] Radosavljevic M, Freitag M, Thadani K V and Johnson A T 2002 Nonvolatile molecular memory elements based on ambipolar nanotube field effect transistors *Nano Lett.* **2** 761

[14] Cui J B, Sordan R, Burghard M and Kern K 2002 Carbon nanotube memory devices of high charge storage stability *Appl. Phys. Lett.* **81** 3260–2

[15] Choi W B, Chae S, Bae E, Lee J, Cheong B, Kim J and Kim J 2003 Carbon-nanotube-based nonvolatile memory with oxide-nitride-oxide film and nanoscale channel *Appl. Phys. Lett.* **82** 275

[16] Bradley K, Cumings J, Star A, Gabriel J-C P and Gruner G 2003 Influence of mobile ions on nanotube based FET devices *Nano Lett.* **3** 639

[17] Wang S and Sellin P 2005 Pronounced hysteresis and high charge storage stability of single-walled carbon nanotube-based field-effect transistors *Appl. Phys. Lett.* **87** 133117

[18] Vijayaraghavan A, Kar S, Soldano C, Talapatra S, Nalamasu O and Ajayan P M 2006 Charge-injection-induced dynamic screening and origin of hysteresis in field-modulated transport in single-wall carbon nanotubes *Appl. Phys. Lett.* **89** 162108

[19] Robert-Peillard A and Rotkin S V 2005 Modeling hysteresis phenomena in nanotube field-effect transistors *IEEE Trans. Nanotechnol.* **4** 284

[20] Kar S, Vijayaraghavan A, Soldano C, Talapatra S, Vajtai R, Nalamasu O and Ajayan P M 2006 Quantitative analysis of hysteresis in carbon nanotube field-effect devices *Appl. Phys. Lett.* **89** 132118

[21] Zavodchikova M Y, Johansson A, Rinkiö M, Toppari J J, Nasibulin A G, Kauppinen E I and Törmä P 2007 Fabrication of carbon nanotube-based field-effect transistors for studies of their memory effects *Phys. Status Solidi* b **244** 4188

[22] Nasibulin A G, Moisala A, Brown D P, Jiang H and Kauppinen E I 2005 A novel aerosol method for single walled carbon nanotube synthesis *Chem. Phys. Lett.* **402** 227

[23] Gonzalez D, Nasibulin A G, Shandakov S D, Jiang H, Queipo P, Anisimov A S, Tsuneta T and Kauppinen E I 2006 Spontaneous charging of single-walled carbon nanotubes: a novel strategy for the selective substrate deposition of individual tubes at ambient temperature *Chem. Mater.* **18** 5052

[24] Gonzalez D, Nasibulin A G, Baklanov A G, Shandakov S D, Queipo P, Brown D P and Kauppinen E I 2005 A new thermophoretic precipitator for collection of nanometer-sized aerosol particles *Aerosol Sci. Technol.* **39** 1064

[25] Chen Z, Appenzeller J, Knoch J, Lin Y and Avouris P 2005 The role of metal–nanotube contact in the performance of carbon nanotube field-effect transistors *Nano Lett.* **5** 1497–502

[26] Tans S, Dekker C and Verschueren A 1998 Room-temperature transistor based on a single carbon nanotube *Nature* **393** 49

[27] Martel R, Schmidt T, Shea H, Hertel T and Avouris P 1998 Single- and multi-wall carbon nanotube field-effect transistors *Appl. Phys. Lett.* **73** 2447

[28] Martel R, Derycke V, Lavoie C, Appenzeller J, Chan K, Tersoff J and Avouris P 2001 Ambipolar electrical transport in semiconducting single-wall carbon nanotubes *Phys. Rev. Lett.* **87** 256805

[29] Avouris P 2002 Molecular electronics with carbon nanotubes *Acc. Chem. Res.* **35** 1026

[30] Rinkiö M, Zavodchikova M Y, Törmä P and Johansson A 2008 Effect of humidity on the hysteresis of single walled carbon nanotube field-effect transistors *Phys. Status Solidi* b **245** 2315

[31] Vanheusden K, Warren W L, Devine R A B, Fleetwood D M, Schwank J R, Shaneyfelt M R, Winokur P S and Lemmios Z J 1997 Non-volatile memory device based on mobile protons in SiO_2 thin films *Nature* **386** 587–9

[32] Marty L, Naud C, Chaumont M, Bonnot A M, Fournier T and Bouchiat V 2003 Self-assembled single wall carbon nanotube field effect transistors *Third IEEE Conf. Nanotechnol.* **1** 240

[33] Shim S I, Yeh F C, Wang X W and Ma T P 2008 SONOS-type flash memory cell with metal/Al_2O_3/SiN/Si_3N_4/Si structure for low-voltage high-speed program/erase operation *IEEE Electron Device Lett.* **29** 512

[34] Micron Technology, Inc. 2008 *Micron High-Speed NAND Flash Memory*

[35] Chaste J, Lechner L, Morfin P, Fève G, Kontos T, Berroir J-M, Glattli D C, Happy H, Hakonen P and Plaçais B 2008 Single carbon nanotube transistor at GHz frequency *Nano Lett.* **8** 525

[36] Rosenblatt S, Yaish Y, Park J, Gore J, Sazonova V and McEuen P L 2002 High performance electrolyte gated carbon nanotube transistors *Nano Lett.* **2** 869

[37] Purewal M S, Hong B H, Ravi A, Chandra B, Hone J and Kim P 2007 Scaling of resistance and electron mean free path of single-walled carbon nanotubes *Phys. Rev. Lett.* **98** 186808

[38] Javey A, Guo J, Wang Q, Lundstrom M and Dai H 2003 Ballistic carbon nanotube field-effect transistors *Nature* **424** 654

[39] Wanga S and Sellin P 2005 Pronounced hysteresis and high charge storage stability of single-walled carbon nanotube-based field-effect transistors *Appl. Phys. Lett.* **87** 133117

A.IV

NANO LETTERS

2009
Vol. 9, No. 2
643-647

High-Speed Memory from Carbon Nanotube Field-Effect Transistors with High-κ Gate Dielectric

Marcus Rinkiö,[†] Andreas Johansson,[†] G. S. Paraoanu,[‡] and Päivi Törmä*[,§]

Department of Physics, Nanoscience Center, University of Jyväskylä, P.O. Box 35, 40014 Jyväskylä, Finland, and Low Temperature Laboratory and Department of Applied Physics, Helsinki University of Technology, P.O. Box 5100, 02015 Helsinki, Finland

Received October 2, 2008; Revised Manuscript Received December 21, 2008

ABSTRACT

We demonstrate 100 ns write/erase speed of single-walled carbon nanotube field-effect transistor (SWCNT-FET) memory elements. With this high operation speed, SWCNT-FET memory elements can compete with state of the art commercial Flash memories in this figure of merit. The endurance of the memory elements is shown to exceed 10^4 cycles. The SWCNT-FETs have atomic layer deposited hafnium oxide as a gate dielectric, and the devices are passivated by another hafnium oxide layer in order to reduce surface chemistry effects. We discuss a model where the hafnium oxide has defect states situated above, but close in energy to, the band gap of the SWCNT. The fast and efficient charging and discharging of these defects is a likely explanation for the observed operation speed of 100 ns which greatly exceeds the SWCNT-FET memory speeds of 10 ms observed earlier for devices with conventional gate oxides.

In the past few years, there has been steady progress in demonstrating electrical components made of carbon nanotubes, such as electron field emitters, switches, sensors, and field-effect transistors.[1] Especially the performance of the latter has shown great potential. The single-walled carbon nanotube field-effect transistors (SWCNT-FETs) have been shown to be very fast, with transit frequency as high as 50 GHz,[2] and could theoretically approach a maximum value of $v_F/2\pi L \sim 130\ \text{GHz}/L\ (\mu\text{m})$.[3] The high sensitivity of CNT-FETs have been also demonstrated by monitoring single-electron tunneling events between a gold particle and a nearby nanotube.[4] Since the first demonstration of an electromechanical carbon nanotube memory,[5] there have also been reports of CNT-FETs showing memory effects.[6−13] While the mobility of these devices is excellent (79000 $\text{cm}^2/(\text{V s})$),[14] the charge storage stability of at best 14 days[11] for CNT-FET memories leaves room for improvement. Another key property for a high-performance nonvolatile memory is the speed with which the write and erase operations are executed. To date the operation frequency in CNT-FET memories is reported to be in the order of 10 ms.[7,10] This figure of merit needs to be improved before a SWCNT-FET memory can compete with conventional silicon-based memories with write and erase times of 100 μs.[15]

In this Letter we demonstrate a SWCNT-FET memory having write and erase operations with 100 ns long pulses. This operation speed is $\sim 10^5$ times higher than that previously reported in the literature for CNT-FET memories. Such high speed is achieved by using hafnium oxide (HfO_2) as gate and passivation oxide. We also show results for SWCNT-FET memory operation speed on more commonly used silicon oxide (SiO_2) gate dielectric for comparison. Results on endurance under continuous operation and retention times are also shown. While we can conclude the surface chemistry effects, mobile charges in the dielectric, and defects in the CNT to have a minimal role in the observed hysteresis, trapping of charges in the defects of the hafnium oxide remains a plausible explanation. Band offsets are calculated within a simple model to show that fast charging and recharging of the hafnium oxide defects by charge carriers from the CNT is likely.

The devices were built on a highly boron-doped Si wafer, which also served as a backgate. Without removing the native SiO_2 layer from the surface, an atomic layer deposition (ALD) of HfO_2 was carried out on top of the wafer by Beneq Oy (Vantaa, Finland), using a Beneq P400A ALD deposition tool. Precursors used were hafnium tetrachloride ($HfCl_4$) and water at a deposition temperature of 300 °C. The thickness of this layer, 197 ± 10 Å, and its refractive index of 2.05 ±

* Corresponding author: tel, +358 94518490; fax, +358 94513517; e-mail paivi.torma@hut.fi.
[†] University of Jyväskylä.
[‡] Low Temperature Laboratory, HUT.
[§] Department of Applied Physics, HUT.

10.1021/nl8029916 CCC: $40.75 © 2009 American Chemical Society
Published on Web 01/16/2009

0.01, were measured with Rudolph Research AutoEL III ellipsometer having an excitation wavelength of 632.8 nm. Then a matrix of alignment markers was deposited, using e-beam lithography and metallization of Pd with an adhesion layer of Ti. Commercial SWCNTs bought from NanoCyl S.A. (Sambreville, Belgium) were suspended in 1,2-dichloroethane by ultrasonication. A few droplets of the nanotube suspension were deposited onto the sample, and the locations of SWCNTs were precisely mapped in relation to the alignment marker matrix, using an atomic force microscope (AFM). Suitable CNTs were then contacted with Pd source and drain electrodes through a second step of e-beam lithography and subsequent metallization. The sample fabrication is described in detail in ref 16. The diameters of the CNTs used in this study ranged from 1.2 to 1.5 nm and FET channel lengths from 100 to 360 nm, which was determined from AFM images. Finally, another ALD layer of HfO_2, having a nominal thickness of 20 nm, was deposited by Beneq Oy on top of the devices using tetrakis(ethylmethylamino)hafnium (TEMA-Hf) and water as precursors at a process temperature of 100 °C. The fabricated devices are illustrated together with grown ALD layers in Figure 1a.

An AFM image of a device taken before the second ALD deposition with a schematic of the measurement setup is shown in Figure 1b. The drain−source and gate−source voltage bias was supplied by a computer-controlled homemade voltage distribution box powered by batteries. A drain−source bias of 10 mV was used for all the SWCNT-FET measurements. The current response through the tube was monitored while changing the voltage on the gate. The backgate was operated in two different ways. The transfer characteristics of SWCNT-FETs were measured while the backgate was scanned from positive to negative voltages and back. The high-speed memory operation was performed with voltage pulses applied to the backgate by manually triggering either a positive or negative voltage pulse from an Agilent 33250A 80 MHz function generator with a duration of 100 ns and an amplitude of ±4 V. All measurements were carried out at room temperature in an electrically shielded room.

The focus of this study is on the write/erase speed of memory elements made out of SWCNT-FET operated with a backgate, and we consider also other device parameters such as operation endurance and retention time. A typical example of transfer characteristics for such a memory is presented in Figure 2. Here the threshold voltage where the current response starts to rise attains a higher value for reverse than forward sweep. This results in a highly reproducible hysteresis loop that has different current response (indicated as I_{ON} and I_{OFF}) at zero backgate voltage depending on the sweep direction. We define these two states as the ON and the OFF states of the memory device. In this device, they are separated by more than 3 orders of magnitude. In the inset of Figure 2, an $I-V$ curve taken at $V_{GS} = 0$ in the OFF-state is shown.

Having a stable hysteresis loop with well-separated states at zero gate voltage enables us to use this device as a memory element. Similar devices have previously been studied with different gate insulators, device geometries, and varying

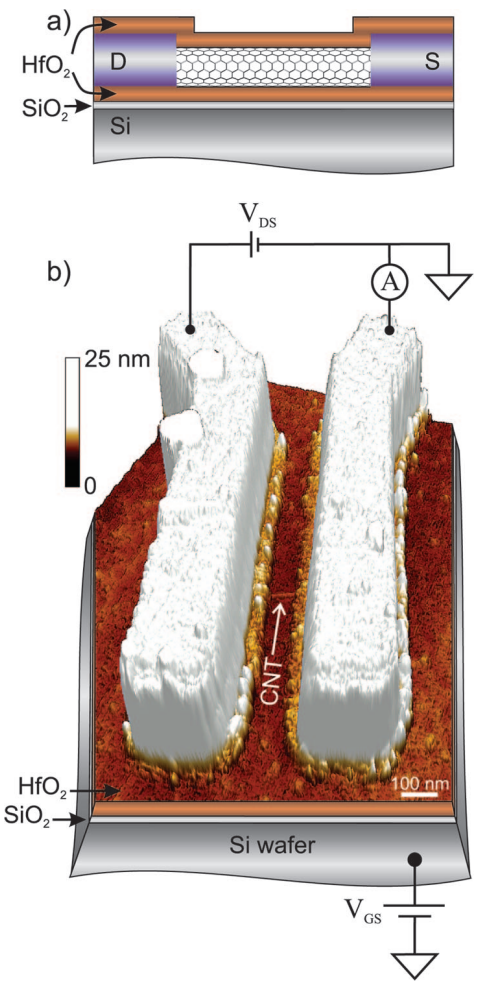

Figure 1. (a) Side view of a SWCNT-FET having an ALD grown HfO_2 gate and passivation layers together with drain (D) and source (S) electrodes. The nominal thicknesses of both HfO_2 layers were 20 nm. (b) AFM image of a typical device where a SWCNT is resting on a HfO_2 layer and connected with Pd source and drain electrodes having a spacing of 140 nm. The measurement setup is also schematically illustrated. The bias voltage is applied between the drain and source electrodes and the gate voltage to the Si wafer, acting as a backgate, while measuring the current response through the CNT.

parameters.[6−13] So far these SWCNT-FET memory elements have been subjected to slow write and erase times, the fastest being 10 ms.[7,10] The write pulse sent to the backgate is shown in the inset of Figure 3. The ON and OFF states are separated by more than 2 orders of magnitude and monitored for ∼25 s before switching to the other state. This 100 ns operation speed is at the moment limited by our measurement setup; therefore the SWCNT device itself may allow even higher speeds. As a comparison we also performed similar operation speed measurements for SWCNT-FET memories having more commonly used SiO_2 as a gate oxide shown in Figure S1 in the Supporting Information. We found that with 1 ms long pulses we can still operate the SiO_2 based memory but with shorter pulses the ON and OFF states are no longer distinguishable.

We also investigated how the fast memory devices perform under continuous operation. The endurance of another device (that also showed 100 ns operation speed) is presented in

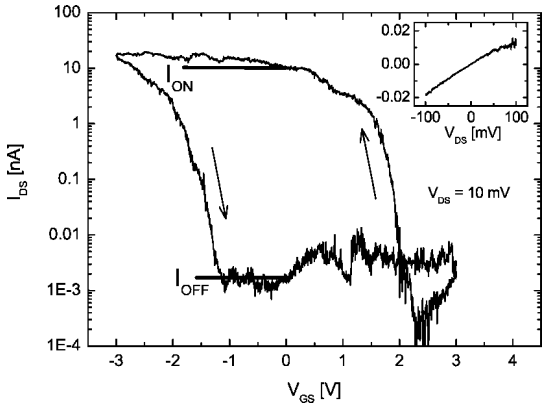

Figure 2. Hysteresis loop of a typical SWCNT-FET used in this study with $V_{DS} = 10$ mV. The device has a hysteresis gap of 3.2 V, subtreshold slope of 120 mV/dec, and an ON/OFF ratio more than 10^3. The arrows mark the backgate scan direction within the loop. The inset shows the $I-V$ curve of the device in the OFF-state.

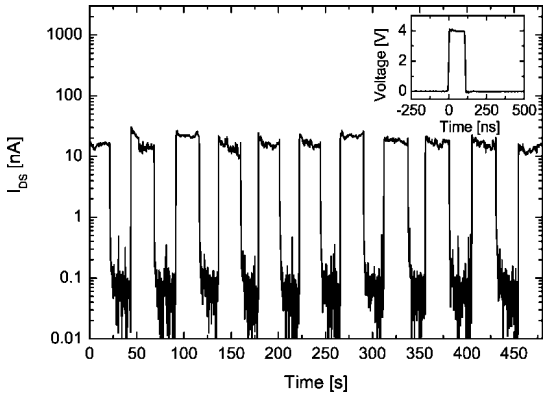

Figure 3. Memory operation of the SWCNT-FET. Writing and erasing the memory was done with 100 ns pulsing to the gate, and the state was recorded between the pulsing with $V_{GS} = 0$ V. In the inset is shown the write pulse for high current state.

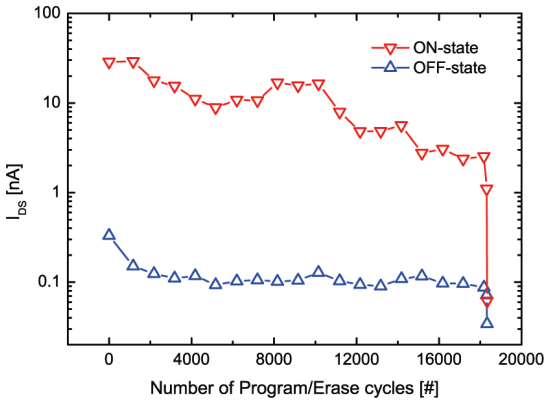

Figure 4. Memory operation endurance of a SWCNT-FET. Write and erase cycles operated with ±3 V and 10 ms pulses. The memory can be operated for more than 18000 cycles before a failure. The OFF state stays unchanged while the ON state is lowered by about a decade before a failure of operation.

Figure 4, where 10 ms long write and erase pulses with an amplitude of ±3 V and rise and fall times of 3 μs were used. The state readout time was 0.5 s. The states stayed well separated for more than 10^4 cycles, until after 18000 cycles a failure of operation was observed and the device was

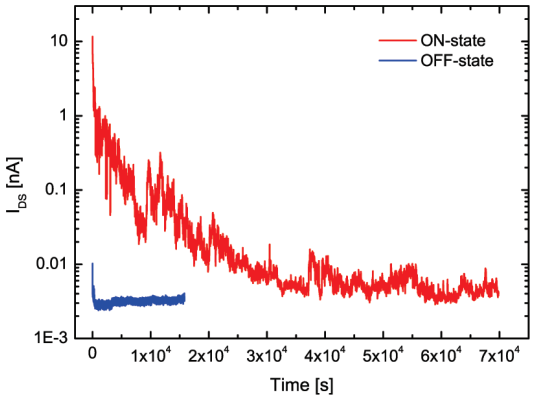

Figure 5. Retention time for the ON and OFF states of a SWCNT-FET memory device. The ON state has an exponential decay to the OFF state with a retention time of about ~1.5 × 10^4 s. The OFF state stays relatively unchanged throughout the measurement.

broken. For more detailed development of the states, a histogram of more than 13000 cycles is presented in Figure S2 in the Supporting Information. The pulse duration in this endurance measurement is 100000 times longer (for reasons explained in the Supporting Information) than the fastest operation speed achieved. Compared to the 100 ns operation, this adds an extra static stress on the gate oxide that is also contributing to the aging of the device. In addition, breaking of the nanotube is likely to be caused by the backgate operation since due to large parasitic capacitances and small rise and fall times of the pulses, a transient pulse is induced in the source and drain electrodes. To ensure that this transient response is not seen in our measurements, a 10 Hz lowpass filter was placed between the SWCNT-FET and the current amplifier. This response also sets the higher limit for our readout speed and the readout needed to be done below the lowpass filter's cutoff frequency of 10 Hz. Previously, it has been demonstrated by others that the SWCNT is capable of giving accurate readout response in the gigahertz regime when gated with a local gate[2] which could probably be attainable with SWCNT-FET memory devices on HfO_2 having a top-gated device configuration.

To investigate the volatility of the memories, the retention times of both ON and OFF states were recorded after the hysteresis loop sweep shown in Figure 2. The OFF state does not change remarkably during the measurement, as seen in Figure 5. In contrast to the OFF state, the ON state has an exponential decay, with fast relaxation in the beginning and a slower tail, until it reaches the OFF state. Here we considered the two states to be separated as long as they differed by more than a factor of 10, and with this threshold the retention time of the device was ~1.5 × 10^4 s (>4 h). This relaxation time is not sufficient for a nonvolatile memory element, but it could be improved by an additional insulator layer as will be discussed below.

Finally, we discuss the origin of the extremely fast operation speeds observed. The hysteresis in the transfer characteristics of SWCNT-FETs has previously been explained by several different models. (1) Surface chemistry effects, where for instance water molecules adhered to the surface of the dielectric have been shown to give a large

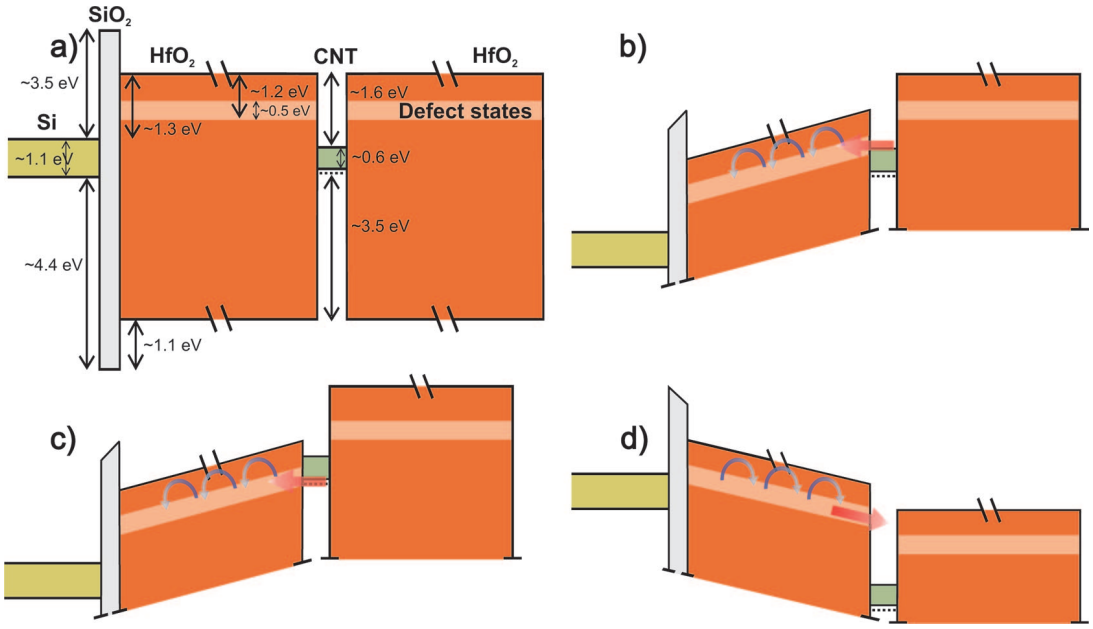

Figure 6. Schematic energy band diagram for a $Si/SiO_2/HfO_2/CNT/HfO_2$ gate stack containing defect states in the HfO_2 layers. (a) The flat band condition without taking into account voltage drops within the dielectric. The CNT band gap is calculated for a 1.4 nm diameter tube. (b and c) Band profile when writing with positive gate voltage. The electrons tunnel from the conduction and the valence band of CNT to the defect states in HfO_2. (d) Band profile with the stored electrons erased from the HfO_2 by applying a negative gate voltage. The band bending induced by the gate operation in (b), (c) and (d) is omitted for clarity, and the diagram represents the positions of bands away from the interface.

contribution to the hysteresis for some CNT-FETs.[17−19] Our studied devices have on top of the CNT a 20 nm passivation layer of HfO_2 to reduce the surface chemistry effects to a minimum. Also, screening of the applied gate voltage by adsorbed water molecules is a relatively slow process and already 500 μs pulsing was shown to remove completely the hysteresis induced by surface effects.[20] In summary, the passivation layer and the fast operation speed in our experiments make significant contribution of surface effects unlikely. (2) Mobile charges or ions that can be relocated within the dielectric layer by modulating the gate voltage are known from Si MOSFETS to cause retarded hysteresis.[21] Here we see advanced hysteresis, which indicates that this mechanism is not the main reason for the memory effect. (3) Charging centers like defects in the nanotube itself could cause hysteresis when filled or emptied with the applied gate voltage.[22−24] However, using several different layer structures of oxides as gate insulators, we have recently shown that the amount of hysteresis in SWCNT-FETs can be controlled by the design of the gate dielectric.[13] That study thus indicates that defects in the nanotube are a minor contributor in the hysteresis. (4) Therefore, in the present case, the most likely explanation remains a model where stationary charge traps within the dielectric are dominating the hysteresis. An applied gate voltage could fill these charge traps with charge carriers moving in the CNT.

As high-κ dielectrics are being introduced to increase the physical thickness of the Si-MOSFET gate dielectric, a lot of recent research has focused on studying charge trapping, particularly in HfO_2.[25] It has been shown that HfO_2 has fast, significant charge trapping[26] and thicker oxide layers exhibit stronger charge trapping.[27,28] This indicates that the traps are located at the bulk of the HfO_2. The fast charge trapping and detrapping we observe could be due to charging and discharging of pre-existing bulk defects since no defect generation has been observed in measurements.[29] On the basis of their measurements, Kerber et al. suggested a defect states model to explain the experimental data.[29] The model is also supported by spectroscopic ellipsometry measurements, where an additional absorption peak exists in the range 0.7−1.2 eV below the bottom of the conduction band of HfO_2.[30] These states available within the band gap of HfO_2 can function as electron traps.[30] These defect states are attributed to oxygen vacancies which have a large electron affinity.[30,31]

To show that charge trapping in the HfO_2 defects is a likely process in our case for the high-speed operation, we estimated the band alignments for our devices; see Figure 6. The flat band case for the $Si/SiO_2/HfO_2/CNT/HfO_2$ energy band diagram together with the defect states in HfO_2 layers is depicted in Figure 6a. We calculated the semiconductor band alignments using the Schottky barrier theory presented in ref 32. The oxides were considered as wide-band gap semiconductors and their conduction band offsets determined by matching the charge neutrality levels of each semiconductor, modified by the Schottky pinning parameter. For the CNT, we took into account that it is in contact with electrodes made of palladium which has the work function of 5.12 eV. Note that we used the values for intrinsic Si, although in our experiment the substrate was p-type Si; the result for p-type Si would be modified only slightly and, especially, does not affect the CNT−HfO_2 alignment which is the main point here. Also, for HfO_2 we used the experimentally determined band gap of 5.7 eV,[30] which is slightly smaller than the theoretical band gap of 6 eV. The location and width of the HfO_2 defect states are also taken from the experiment in ref 30. The charge traps located above

the CNT can be efficiently charged with positive gate bias by electron tunneling from the conduction and valence bands of the CNT as shown in panels b and c of Figure 6, even for rather small gate voltages. This corresponds to the write sequence of the memory. During the erase sequence, depicted in Figure 6d, the defect states can be discharged by tunneling to the CNT. This model can also explain qualitatively the observed short ON state retention time. When the memory is programmed to ON state with a positive gate voltage, the HfO_2 layer stores negative charge. As there is no additional tunneling oxide between the CNT and trapped charges in the HfO_2 layer, the electrons have only a small barrier to cross in order to tunnel back to the CNT. The thermal energy could assist this tunneling process. The retention time could possibly be made longer by having a thin, large band gap, and defect-free tunneling oxide between the CNT and HfO_2 charge trap layer.

In summary, we have shown for the first time a high-speed (100 ns) operation of charge trap SWCNT-FET memory elements having ALD grown HfO_2 as a gate dielectric. The results show that memory elements made out of SWCNT-FETs can compete with commercial Flash memories in this figure of merit. The endurance of these memory elements is shown to exceed 10^4 cycles. We can qualitatively explain our findings within a charge trapping model where HfO_2 has defect states situated above the CNT band gap in energy. The charge trapping in HfO_2 is known to be fast and efficient and is likely to enable the high operation speed of our devices, which is largely exceeding the CNT-FET memory operation speeds reported so far. The charge trapping model also suggests that the observed retention time of $\sim 1.5 \times 10^4$ s could be improved by adding a thin, defect-free tunneling oxide to separate the CNT and the charge traps. Note that the essential features of the model, and therefore the origin of the fast memory operation, are not dependent on detailed structure of the SWCNT: the key issues are the defects in hafnium oxide as well as the existence and suitable location of the CNT band gap in energy and the fact that the CNT is a nanoscale, nearly ballistic conductor. Therefore, the fast memory operation demonstrated here could potentially be realized also using other carbon materials such as CNT bundles or graphene with a band gap engineered by layer structure or reduced dimension.

Acknowledgment. We acknowledge valuable discussions with our research project collaborators: Professor M. Ahlskog, Professor K. Rissanen, and Dr. J. J. Toppari's groups at University of Jyväskylä, E. I. Kauppinen's group at Helsinki University of Technology, as well as the companies Nokia Oyj and Vaisala Oyj. We thank Beneq Oy, Olli Jylhä, for ALD processing. This work was supported by the Finnish Funding Agency for Technology and Innovation (TEKES), Project Number 40309/05, and the Academy of Finland, Project Numbers 00857, 118122, 129896, 207935, 210147, and 210308, and conducted as part of a EURYI scheme award, see www.esf.org/euryi. M.R. acknowledges support from the Magnus Ehrnrooth Foundation and the Finnish Foundation for Technology Promotion (TES).

Supporting Information Available: Results for SWCNT-FET memory operation speed on more commonly used SiO_2 gate dielectric and statistical distributions of the ON and OFF states in the endurance test. This material is available free of charge via the Internet at http://pubs.acs.org.

References

(1) Jorio, A.; Dresselhaus, M. S.; Dresselhaus, G. *Carbon Nanotubes - Advanced Topics in the Synthesis, Structure, Properties and Applications*; Springer: Heidelberg 2008; Vol. 1, pp 3−61.
(2) Chaste, J.; Lechner, L.; Morfin, P.; Fève, G.; Kontos, T.; Berroir, J.-M.; Glattli, D. C.; Happy, H.; Hakonen, P.; Plaçais, B. *Nano Lett.* **2008**, *8* (2), 525–528.
(3) Hasan, S.; Salahuddin, S.; Vaidyanathan, M.; Alam, M. A. *IEEE Trans. Nanotechnol.* **2006**, *5* (1), 14–22.
(4) Gruneis, A.; Esplandiu, M. J.; Garcia-Sanchez, D.; Bachtold, A. *Nano Lett.* **2007**, *7* (12), 3766–3769.
(5) Rueckes, T.; Kim, K.; Joselevich, E.; Tseng, G. Y.; Cheung, C.-L.; Lieber, C. M. *Science* **2000**, *289* (5476), 94–97.
(6) Fuhrer, M. S.; Kim, B. M.; Durkop, T.; Britlinger, T. *Nano Lett.* **2002**, *2* (7), 755–759.
(7) Radosavljevic, M.; Freitag, M.; Thadani, K. V.; Johnson, A. T. *Nano Lett.* **2002**, *2* (7), 761–764.
(8) Cui, J. B.; Sordan, R.; Burghard, M.; Kern, K. *Appl. Phys. Lett.* **2002**, *81* (17), 3260–3262.
(9) Choi, W. B.; Chae, S.; Bae, E.; Lee, J.-W.; Cheong, B.-H.; Kim, J.-R.; Kim, J.-J. *Appl. Phys. Lett.* **2003**, *82* (2), 275–277.
(10) Marty, L.; Naud, C.; Chaumont, M.; Bonnot, A. M.; Fournier, T.; Bouchiat, V. *IEEE-Nano 2003* **2003**, *1*, 240–243.
(11) Wang, S.; Sellin, P. *Appl. Phys. Lett.* **2005**, *87*, 133117.
(12) Ganguly, U.; Kan, E. C.; Zhangb, Y. *Appl. Phys. Lett.* **2005**, *87*, 043108.
(13) Rinkiö, M.; Johansson, A.; Zavodchikova, M. Y.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törmä, P. *New J. Phys* **2008**, *10* (10), 103019.
(14) Dürkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. *Nano Lett.* **2004**, *4* (1), 35–39.
(15) Shim, S. I.; Yeh, F. C.; Wang, X. W.; Ma, T. P. *IEEE Electron Device Lett.* **2008**, *29* (5), 512–514.
(16) Zavodchikova, M. Y.; Johansson, A.; Rinkiö, M.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törmä, P. *Phys. Status Solidi B* **2007**, *244* (11), 4188–4192.
(17) Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. *Nano Lett.* **2003**, *3* (2), 193–198.
(18) Wang, S.; Sellin, P.; Zhang, Q.; Yang, D. *Curr. Nanosci.* **2005**, *1*, 43–46.
(19) Rinkiö, M.; Zavodchikova, M. Y.; Törmä, P.; Johansson, A. *Phys. Status Solidi B* **2008**, *245* (10), 2315–2318.
(20) Lin, H.; Tiwari, S. *Appl. Phys. Lett.* **2006**, *89*, 073507.
(21) Vanheusden, K.; Warren, W. L.; Devine, R. A. B.; Fleetwood, D. M.; Schwank, J. R.; Shaneyfelt, M. R.; Winokur, P. S.; Lemmios, Z. J. *Nature* **1997**, *386*, 587–589.
(22) Freitag, M.; Johnson, A. T.; Kalinin, S. V.; Bonnell, D. A. *Phys. Rev. Lett.* **2002**, *89* (21), 216801.
(23) Park, J.-Y. *Appl. Phys. Lett.* **2007**, *90*, 023112.
(24) Kim, Y.; Oh, Y. M.; Park, J.-Y.; Kahng, S.-J. *Nanotechnology* **2007**, *18*, 475712.
(25) Ribes, G.; Mitard, J.; Denais, M.; Bruyere, S.; Monsieur, F.; Parthasarathy, C.; Vincent, E.; Ghibaudo, G. *IEEE Trans. Device Mater. Reliab.* **2005**, *5* (1), 5–19.
(26) Zafar, S.; Callegari, A.; Gusev, E.; Fischetti, M. V. *Int. Electron Devices Meet.* **2002**, *1*, 517–520.
(27) Young, C. D.; Bersuker, G.; Brown, G. A.; Lim, C.; Lysaght, P.; Zeitzoff, P.; Murto, R. W.; Huff, H. R. *IEEE Int. Integr. Reliab. Workshop* **2003**, *1*, 28–35.
(28) Sim, J. H.; Song, S. C.; Kirsch, P. D.; Young, C. D.; Choi, R.; Kwong, D. L.; Lee, B. H.; Bersuker, G. *Microelectron. Eng.* **2005**, *80*, 218–221.
(29) Kerber, A.; Cartier, E.; Pantisano, L.; Degraeve, R.; Kauerauf, T.; Kim, Y.; Hou, A.; Groeseneken, G.; Maes, H. E.; Schwalke, U. *IEEE Electron Device Lett.* **2003**, *24* (2), 87–89.
(30) Takeuchi, H.; Ha, D.; King, T.-J. *J. Vac. Sci. Technol., A* **2004**, *22* (4), 1337–1341.
(31) Foster, A. S.; Lopez Gejo, F.; Shluger, A. L.; Nieminen, R. M. *Phys. Rev. B* **2002**, *65* (17), 174117.
(32) Robertson, J. *J. Vac. Sci. Technol., B* **2000**, *18* (3), 1785–1791.

NL8029916

Supporting information

High Speed Memory from Carbon Nanotube Field-Effect Transistors with High-κ Gate Dielectric

Marcus Rinkiö[†], Andreas Johansson[†], G.S. Paraoanu[‡], and Päivi Törmä[§,*]

Department of Physics, Nanoscience Center, P.O. Box 35, 40014 University of Jyväskylä, FINLAND

Low Temperature Laboratory, P.O.Box 5100, 02015 Helsinki University of Technology, FINLAND

Department of Applied Physics, P.O.Box 5100, 02015 Helsinki University of Technology, FINLAND

Memory response of SWCNT-FETs on SiO_2 to pulse-gating

As a reference for our high speed SWCNT-FET memory devices on HfO_2, we also carried out investigation of similar devices on SiO_2. These devices were fabricated on thermally grown SiO_2 having thickness of about 300 nm. The used SWCNTs were produced by arc-discharge and spin coated onto the wafer. The field-effect transistors were then fabricated in the same manner as described in the manuscript. Results on memory operation speed for these SWCNT-FETs are shown in Figure S1. The device has an I_{ON}/I_{OFF} ratio (referred as ON/OFF ratio from now on) of about 10 at $V_{GS} = 0$ V, as shown in the inset of Figure S1 **a)**. The 1 s pulsing is writing well to these states but already at 1 ms pulsing these states deviate distinctly from the original. As the pulse length is still lowered to 100 μs the states cannot be anymore resolved as shown in Figure S1 **b)**. The drain-source bias voltage was 10 mV and the pulse amplitude was $\pm$ 10 V in all the measurements done with SWCNT-FET memory devices having SiO_2 as gate dielectric.

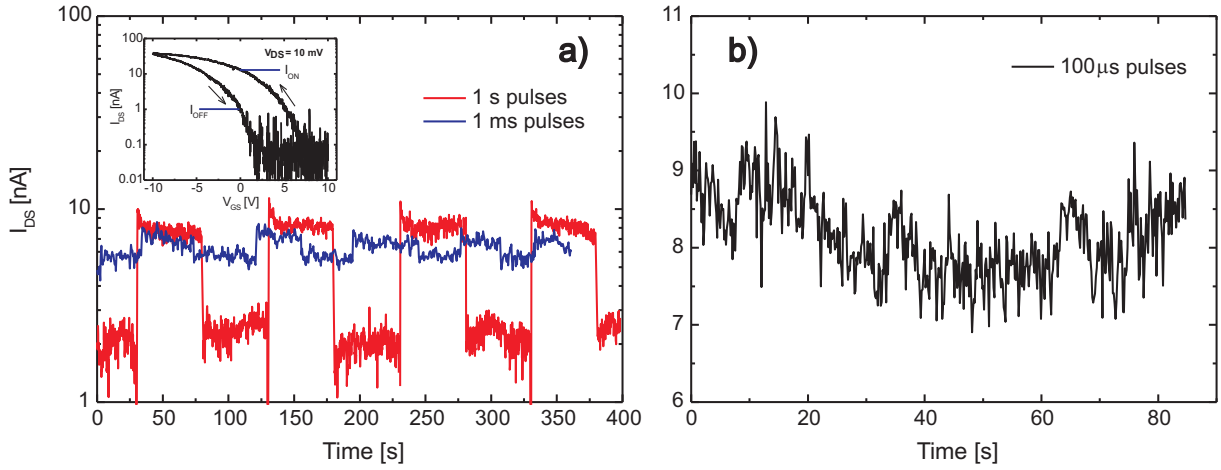

Figure S1: Memory operation of the SWCNT-FET on SiO_2 with different pulsing speeds. **a)** Writing and erasing the memory was done with 1 s pulsing (red) and with 1 ms pulsing (blue) to the gate, both having an amplitude of $\pm$ 10 V. After a pulse the state was recorded with $V_{GS} = 0$ V. The timescale in 1 ms data is multiplied by three to allow better comparison with 1 s data, which expands longer in time. In the inset is shown the hysteresis loop for the same device with $V_{DS} = 10$ mV. The arrows mark the scan directions. The device has an ON/OFF ratio of about 10 at $V_{GS} = 0$ V, which the 1 s pulsing is still keeping but when having 1 ms pulsing the ON/OFF ratio is almost vanished. **b)** Trial of memory operation of the SWCNT-FET on SiO_2 with 100 μs pulsing speed and $\pm$ 10 V amplitude. As seen from the graph the states are no longer resolved.

*Corresponding author. Tel.: +358 94518490. Fax: +358 94513517. E-mail address: paivi.torma@hut.fi

[†]University of Jyväskylä

[‡]Low Temperature Laboratory, HUT

[§]Department of Applied Physics, HUT

Statistical distributions of the ON and OFF states in the endurance test

In the endurance test, 10 ms pulses were used for the following reasons. During the backgate operation, due to parasitic capacitances and small rise and fall times of the pulses, a transient pulse is induced in the source and drain electrodes. This transient response was filtered away by a 10 Hz lowpass filter. This response also sets the higher limit for the readout speed and readout was done below the lowpass filters cutoff frequency of 10 Hz. This also affected the choices for our pulse duration and readout time of a state in the endurance test. Since in our function generator the pulse width and waiting period before the next pulse are related through a finite number of points in an arbitrary wave function, for us to be able to get 0.5 s readout period we used 10 ms pulses in the endurance test. When studying the fast memory operation, we obtained the 100 ns pulse width combined with a long readout time by triggering the pulses manually, which was not feasible in the endurance test consisting of a large number (18 000) pulses.

To represent the development of the memory endurance data we constructed a histogram containing more than 13 000 cycles shown in Figure S2. We considered the ON and OFF state plateaus in each cycle, and to show single state with one value, we calculated averages from the ON and OFF states in each cycle. From this data we constructed the histogram shown in Figure S2. Since the endurance data is logarithmic in nature, the bin intervals in this histogram are also logarithmic. This way we can produce equal size bins in logarithmic I_{DS} scale and do not distort the number of counts in each bin. In Figure S2 two distinct peaks are observed. These peaks correspond to the ON-state (red) centered at 4.80 nA with a standard deviation of 4.47 and to the OFF-state (blue) centered at 0.14 nA with a standard deviation of 0.11. In between these two peaks is a valley which contains a few counts that overlap with each other. These are indicated by purple bins around 1 nA and they occur as the device is aging.

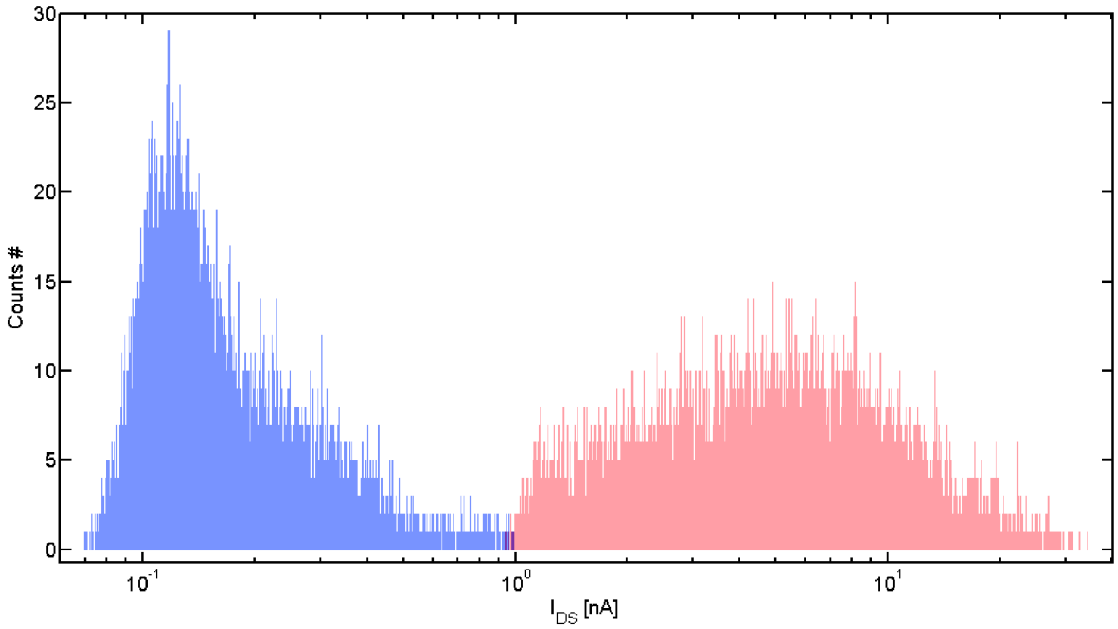

Figure S2: A histogram showing variation in the ON-state (red) and OFF-state (blue) when testing the endurance of SWCNT-FET memory device. The ON-state is centered at 4.80 nA with a standard deviation of 4.47 and the OFF-state is centered at 0.14 nA with a standard deviation of 0.11. In the valley between these two peaks bins that contain counts from both states are shown in purple. These occur due to aging of the device.

A.V

Room Temperature Negative Differential Resistance in Carbon Nanotube Field-Effect Transistors with Novel Gate Oxide Design

Marcus Rinkiö[†,‡], Andreas Johansson[†,*], Ville Kotimäki[†], and Päivi Törmä[‡,*]

Department of Physics, Nanoscience Center, P.O. Box 35, 40014 University of Jyväskylä, FINLAND

Department of Applied Physics, P.O.Box 5100, 02015 Helsinki University of Technology, FINLAND

November 2, 2009

Abstract

We demonstrate controllable and gate-tunable negative differential resistance in carbon nanotube field-effect transistors, at room temperature and at 4.2 K. This is achieved by effectively creating quantum dots along the carbon nanotube channel by patterning of the underlying, high-κ gate oxide. The negative differential resistance feature can be modulated by both the gate and the drain-source voltage, which leads to more than 20% change of the current peak-to-valley ratio. Our approach is fully scalable and opens up a possibility for a new class of nanoscale electronic devices using negative differential resistance in their operation.

The first demonstration of negative differential resistance (NDR) was in a GaAs double barrier structure [1]. Since then NDR has been observed in a variety of devices all the way down to molecular scale [2,3]. Recently, there have been emerging carbon nanotube [4] (CNT) devices that exhibit NDR in their electrical characteristics due to many different phenomena, e.g. chemical doping [5], defects [6], heterojunctions [7], quantum dots between the metal contact and the CNT [8], and bundled or multi-walled CNTs [9,10]. So far the NDR in these devices has been uncontrolled and not suitable for mass production.

In this work, we observe reproducible negative differential resistance in carbon nanotube field-effect transistors (CNT-FETs) at room temperature and also at 4.2 K. We induce NDR to the CNT-FETs by patterning the atomic layer deposited (ALD) gate oxide of the device, resulting in strong charge trapping at specific places within the gate oxide. With sufficient gate voltages the charge trapping induces p-n junctions along the channel of the CNT-FET. This shows up as NDR in the vicinity of the CNT band gap. Further evidence of this p-n junction confinement and band-to-band tunneling [11] in our devices is the bipolar behavior in the transfer characteristics of all our CNT-FETs at room temperature, as well as a specific quantum dot behavior at 4.2 K. Our approach opens a possibility for a new class of nanoscale electronic devices using NDR: fast switching elements [12], nanoscale amplifiers [13], and high frequency oscillators working well into the THz domain.

A cross-section of our devices together with the patterned profile of the grown ALD layers is illustrated in Figure 1a. The devices were built on a highly boron-doped Si wafer, which also served as a backgate. Without removing the native SiO_2 layer from the surface, an ALD deposition of the first HfO_2 layer was carried out on top of the wafer by Beneq Oy (Vantaa, Finland), using a Beneq P400A ALD deposition tool. Precursors of hafnium tetrachloride ($HfCl_4$) and water were used at a deposition temperature of 300 °C. The thickness of this layer, 20 ± 1 nm, and its refractive index of 2.05 ± 0.01, was measured with Rudolph Research AutoEL III ellipsometer with an excitation wavelength of 632.8 nm. Next a matrix of alignment markers of Pd (25 nm) with an adhesion layer of Ti (5 nm) was deposited, using e-beam lithography and metallization. Subsequently a second e-beam lithography step was done to open squares in poly(methyl methacrylate) (PMMA) with nominal dimensions of 150×150 nm. Then another ALD deposition together with a lift off procedure was performed to produce more than 20 000 ALD islands comprising of $TiO_2 - HfO_2$, having nominal thicknesses of 0.5 nm and 1 nm, re-

[†]Department of Physics, Nanoscience Center, P.O. Box 35, 40014 University of Jyväskylä, FINLAND

[‡]Department of Applied Physics, P.O.Box 5100, 02015 Helsinki University of Technology, FINLAND

[*]Corresponding authors. E-mail addresses: paivi.torma@hut.fi, andreas.johansson@jyu.fi

spectively. The total thickness of this oxide stack is measured with AFM to be ∼0.5 nm. Precursors used were titanium tetrachloride ($TiCl_4$) and water for TiO_2 growth and tetrakis(ethylmethylamino)hafnium (TEMA–Hf) and water for HfO_2 growth, both done at a deposition temperature of 100 °C. We use the patterned, ALD grown, high-κ gate oxide to influence the local electrical properties of our transistors. An atomic force microscope (AFM) image of the ALD structure together with a cross shaped AFM marker is shown in Figure 1b. In the dark grooves, there is only a layer of HfO_2 (20 nm) on top of the silicon wafer. Between the lines, ALD islands (AI) comprising of $TiO_2 - HfO_2$ (nominal thickness 0.5–1 nm) are grown.

A few droplets of nanotube suspension made in 1,2-dichloroethane by ultrasonication, containing commercial single walled carbon nanotubes (SWCNTs) bought from NanoCyl S.A. (Sambreville, Belgium), was then deposited onto the sample. Using an atomic force microscope, the locations of the CNTs were precisely mapped in relation to the alignment marker matrix. Chosen CNTs were then contacted with Pd (30 nm) drain (D) and source (S) electrodes through a third e-beam lithography step and subsequent metalization. The FET channel lengths in this study were 400 ± 10 nm and the diameters of the CNTs ranged from 1.3 – 3.4 nm, based on AFM images. An AFM image of device D1 together with a schematic of the measurement setup and the ALD islands is shown in Figure 1c, where a SWCNT is connected with Pd electrodes. The silicon wafer is used as a backgate for three terminal operation. The drain-source and gate-source voltage bias was supplied for all the measurements from a home-made voltage distribution box powered by batteries and computer-controlled via a data acquisition card. The room temperature measurements were done at ambient conditions as well as in vacuum for reducing surface chemistry effects, e.g. adsorbed water. Vacuum measurements were done in a home-made vacuum chamber at a pressure of 1.3×10^{-2} mbar. The liquid helium measurements at 4.2 K were done with a home-made dip-stick where the sample was situated in a helium atmosphere of a few mbar, isolated from the liquid helium. All measurements were carried out in an electrically shielded room.

An earlier study found NDR in freely suspended nanotubes, and showed that it was induced at relatively large bias voltages due to self-heating and increased electron-phonon scattering[14]. This is not the case in our devices, since the nanotube rests on and is thermalized by the substrate. A more likely cause for the emergence of NDR is that a resonant tunneling level enters into the drain-source bias window. This is illustrated in detail in the form of a differential conductance plot in Figure 2a measured for device D2, at 4.2

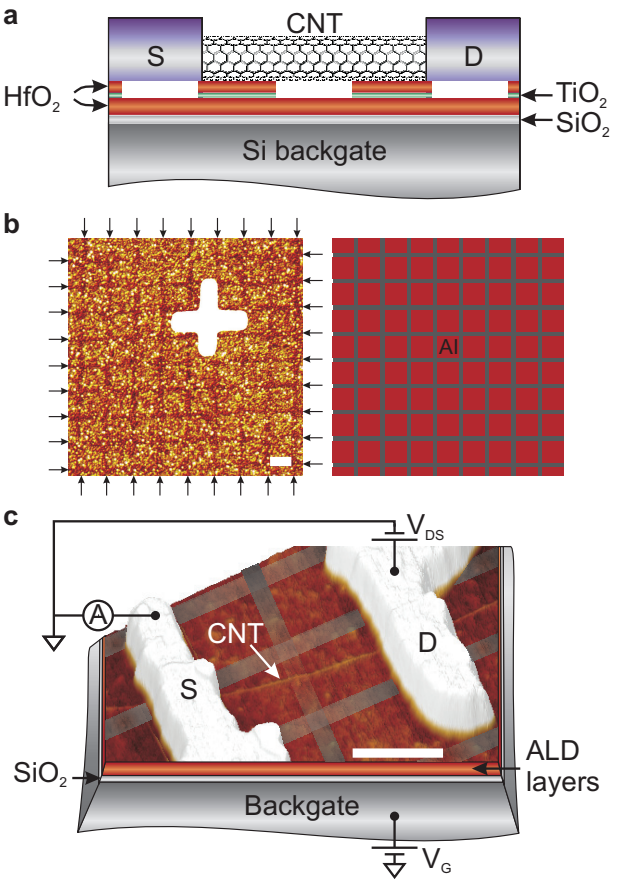

Figure 1: Integrating patterned gate oxide with CNT-FETs. (a) A schematic cross-section of our CNT-FETs having ALD grown triple layer of $HfO_2 - TiO_2 - HfO_2$ with patterned upper two layers of $TiO_2 - HfO_2$. The nanotube is contacted with palladium (30 nm) drain (D) and source (S) electrodes. (b) An AFM image together with a schematic of ALD grown $TiO_2 - HfO_2$ islands. In the grooves highlighted with arrows, there is a single layer of HfO_2 (20 nm) and between these grooves are additional layers of $TiO_2 - HfO_2$ (0.5–1 nm) forming squares of $\sim 200 \times 200$ nm (called ALD islands in the following). The width of the groove between the islands is measured with AFM to be ~ 50 nm. Also an AFM marker is visible in the image. (c) An AFM image of device D1 where a SWCNT is connected to drain (D) and source (S) electrodes having channel length of ~ 400 nm. Also the measurement setup is schematically illustrated. Between the CNT and the gate we have the ALD island structure. Scale bars are 200 nm.

K. The NDR is visible with both positive and negative drain-source voltages as diagonal lines that occur after a resonant level enters to the bias window, as highlighted with arrows. For positive drain-source bias we observe strong NDR peaks related to two resonant lev-

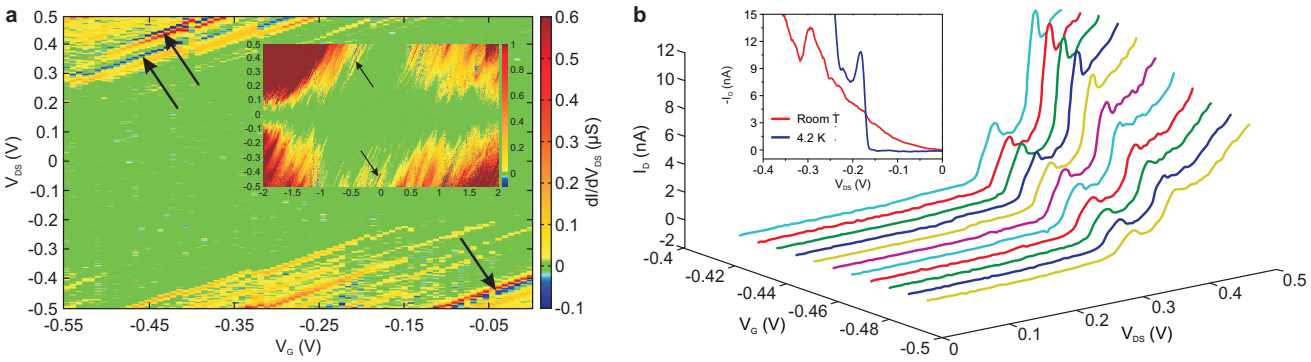

Figure 2: Negative differential resistance in gate-oxide designed CNT-FETs. (a) Differential conductance for device D2 measured at 4.2 K. The NDR regions are shown with blue and indicated with arrows. NDR is visible at both positive and negative drain-source bias voltages. At positive bias the NDR is related to two different resonant tunneling levels. In the inset is shown a larger parameter space from the same device. The NDR occurs in the vicinity of the CNTs band gap as indicated by arrows. (b) The development of the NDR related to the two resonant levels. When sweeping the gate to more positive voltages, the NDR corresponding to the first resonant level increases only slightly while the NDR related to the second localized level has a twenty-fold increase. Inset: Current vs voltage curves for the device D1 measured at room temperature (red) and at 4.2 K (blue). Clear NDR peaks are visible for both, situated at around -0.3 V at room temperature and around -0.18 V at 4.2 K. The peak to valley ratio is 1.38 for room temperature and 1.45 at 4.2 K. The gate voltage sweep direction was from negative to positive.

els. Also the charging of the gate oxide is visible in the images as abrupt horizontal displacements of the slopes while sweeping the gate voltage. The inset of Figure 2a shows that the NDR emerges in the vicinity of the band gap edge of the CNT. In Figure 2b, the first NDR feature is increased only slightly while changing the gate to more positive voltages, whereas the second NDR feature has a twenty-fold increase. These results show that the place of the NDR and more importantly its magnitude are tunable with the gate voltage. Moreover, our approach to induce NDR to CNT-FETs is fully scalable and the islands providing the effect can be accurately positioned at any desired location on the underlying wafer. In the inset of Figure 2b two typical current vs. drain-source voltage curves are shown, measured on device D1 in 1.3×10^{-2} mbar vacuum at room temperature and at 4.2 K. Clear NDR peaks are visible in both traces, situated at around -0.3 V at room temperature and around -0.18 V at 4.2 K. The difference between the peak and the valley current is ~ 3.5 nA at room temperature and ~ 4 nA for the same device measured in cold. In this study, we measured three large-band-gap CNT-FETs, all showing NDR. The phenomenon observed here is different from multi-mode (multi-subband) effects observed in refs.[15,16], because multi-mode effects produce steps (or plateaus) in $I_D - V_{DS}$ and $I_D - V_G$ characteristics, not peaks and NDR as in Figure 2. The phenomenon is rather related to band-to-band tunneling[11], where resonant tunneling from the valence into the conduction band and vice versa enables the flow of current through the device as described below.

We explain the observations by the formation of p-n junctions in the middle of the CNT due to specific and efficient charging of the ALD islands, effectively forming quantum dots[17] whose resonant tunneling levels enable the NDR phenomenon[18]. This is schematically illustrated in Figure 3. With zero gate voltage, the ALD islands are neutral (Figure 3a), corresponding to the flat band case. When the gate voltage is increased, electrons from the CNT tunnel to the ALD islands, making them charged (Figure 3b). The charge stored within the islands screens the applied gate voltage. Thus, the sections of the CNT above these regions, forming the CNT drain and source sections, see a smaller electric field. On the other hand, the region between the islands stays uncharged and in this region the positive gate voltage can lower the bands in energy. When a sufficiently high voltage is applied to the gate, the CNT band gap descends below the Fermi level (E_F) and forms an n-type quantum dot with discrete electronic states. At a fixed gate voltage, with increasing amplitude of the drain voltage, the current increases at first, until a resonant tunneling level aligns with the Fermi level and the current reaches a local maximum. When further increasing the amplitude of the drain voltage, the resonant level moves below the Fermi level of the p-type CNT drain section and the current drops, until the next resonant level enters to the bias window. This is analogous to the negative differential resistance observed in double barrier structures like GaAs quantum dots[1,19,20]. Similarly, we can

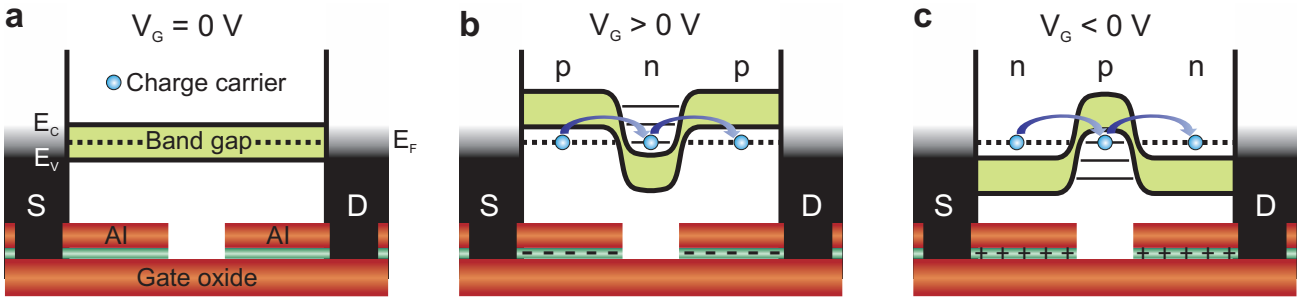

Figure 3: Quantum dots defined by charging the ALD island structure. (a) The flat band case at zero gate voltage. The Fermi level (E_F) within the band gap of the CNT is aligned with the drain (D) and source (S) electrodes and the ALD islands (AI) are neutral. (b) A positive gate voltage pulls electrons from the CNT to the ALD islands which in turn screens the applied V_G. Between the islands, the oxide stays uncharged and the conductance band (E_C) is pulled below the Fermi level. The resulting p-n junctions define a quantum dot with discrete electronic states. When a resonant level is aligned with the Fermi level the charge carriers can flow. (c) The electrons are ejected from the ALD islands by applying a negative gate voltage and the remaining positive charge screens the V_G above these sections. Between these islands, the valence band (E_V) is pulled above the Fermi level and the resulting p-n junctions form a quantum dot.

have a p-type quantum dot (Figure 3c).

In our earlier work[21,22], we have shown that ALD grown nanometer thick gate oxides of high-κ materials such as HfO_2, and layer structures such as $HfO_2 - TiO_2 - HfO_2$, are an efficient way to create controllable charge trapping in CNT devices. To further demonstrate that we have significant charge trapping here, we will point out a few observations from gate dependence measurements. We observe bipolar transconductance curves (Figure 4) for all the devices with the patterned gate oxide (ALD islands). This indicates that both the valence and conduction bands are contributing to the transconductance and makes band-to-band tunneling plausible[11]. The devices have very steep subthreshold slopes, down to 89 mV/dec at room temperature and 17 mV/dec at 4.2 K. While not reaching below the thermal limit, which has been shown possible when having band-to-band tunneling[11], these values are well comparable with other studies where band-to-band tunneling was attributed to highly performing CNT transistors[23]. On the other hand, the apparent temperature behavior does not follow the theoretical prediction of almost flat response for band-to-band tunneling[11]. But a straightforward application of the theoretical prediction is not either expected, since also temperature dependent charging within the dielectric, which strongly affects the subthreshold slope, has to be considered. In Figure 4b, the persistent advanced hysteresis at low temperatures shows that we have in these devices very strong charge trapping within the oxide (for more discussion, see Supporting Information). For comparison, we also measured reference samples having uniform, *non-patterned* conventional SiO_2 and an ALD grown triple layer of $HfO_2 - TiO_2 - HfO_2$ as their gate oxides (see Supporting Information). While they showed similar results for hysteresis at room temperature and the triple layer reference sample also at 4.2 K, the SiO_2 reference sample did not show any hysteresis at 4.2 K. And most importantly, for both of these reference samples without the ALD island structure, we did not observe any NDR (see Supporting Information).

To quantitatively test how well the p-n junction and quantum dot model can explain the observed NDR, we estimate the expected energy level separation in the quantum dots formed by the ALD islands. From the AFM images shown in Figures 1b and c we can estimate the quantum dot size for D1 to be ~ 60 nm. In the constant interaction model[24], the electrochemical potentials of transitions between successive resonant tunneling levels in a quantum dot are spaced by the so-called addition energy $E_{add} = \Delta E + E_C$ where E_C is the charging energy and ΔE is the energy spacing between two discrete quantum levels. For our system we obtain a level splitting of $\Delta E \approx 14$ meV and a charging energy of $E_C \approx 6$ meV (see Supporting Information), i.e. $E_{add} \approx 20$ meV. This estimation of the addition energy fits remarkably well to our measured stability diagram for D1 in Figure 5, showing characteristic Coulomb blockade. These values are also significantly lower than the CNT subband separations of several hundreds of meV based on our CNT diameter range of 1.3 – 3.4 nm[25], which is speaking against the involvement of multi-mode effects. In addition, we do not observe the tunneling barriers to tune to transparency at any backgate voltage in any of the three devices, as was shown in the case of quantum dot formation by defects in CNTs[26]. Some of the diamonds are abruptly cut, supporting the conclusion that we

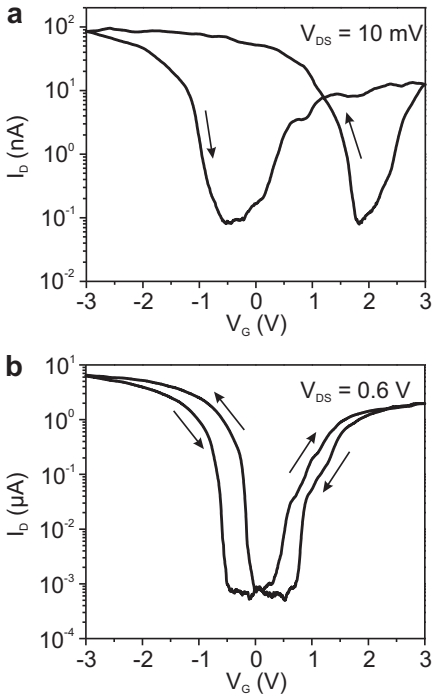

Figure 4: Hysteresis in the ALD island CNT-FETs. (a) Transfer characteristics at room temperature with V_{DS} = 10 mV showing advanced hysteresis. The subthreshold slopes are for p-type ∼89 mV/dec and for n-type ∼161 mV/dec. (b) Hysteresis at 4.2 K with V_{DS} = 0.6 V. The relative hysteresis decreases by 80% compared to the original room temperature hysteresis but it still remains strong. The corresponding subthreshold slopes are for p-type ∼17 mV/dec and for n-type ∼49 mV/dec.

have strong charging within the dielectric in these devices.

In summary, we have presented a new technique to induce negative differential resistance in carbon nanotube field-effect transistors at room temperature. By patterning the upper two layers of ALD grown $HfO_2 - TiO_2 - HfO_2$ triple layer gate oxide into separate islands, we can control the charging within the gate oxide and induce NDR by forming a quantum dot in the conduction channel of the CNT-FET. With gate voltage we can control the magnitude and the place where the NDR occurs in V_{DS}. The method is fully scalable and can also be used to generate NDR in other materials e.g. graphene ribbons and semiconducting nanowires. Our novel technique enables a new class of low-cost nanoscale devices using NDR in their operation. Theoretical predictions of oscillations through CNT quantum dots with NDR suggest they could reach tens of THz with output powers of several μW[27]. Both parameters supersede the intrinsic limi-

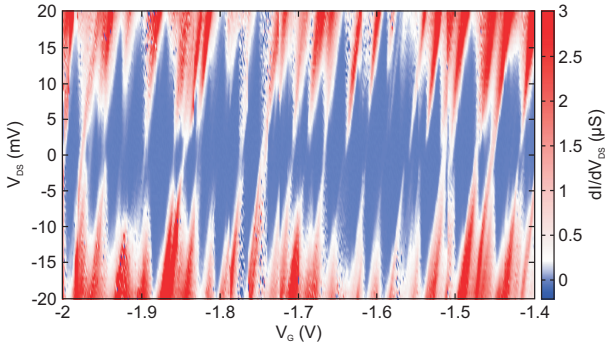

Figure 5: Stability diagram of the npn quantum dot. At 4.2 K, Coulomb blockade is visible in a series of diamonds and corresponds to a single electron charging of a quantum dot of the size ∼ 60 nm, having an addition energy ∼ 20 meV. The gate voltage sweep direction was from negative to positive.

tations of state-of-the-art RTD oscillators made with conventional semiconductor technology, with current record of 712 GHz by an InAs/AlSb resonant-tunneling diode with an output power of 0.3 μW[28,29]. While our presented prototypes have resistance values that limit the upper frequency to around 50 GHz, with a by all means realistic reduction of the CNT to electrode contact resistance to below 10 kΩ and the NDR resistance to below 100 kΩ, the THz mark would be reached (see Supporting Information). It has also been suggested that the output power of high frequency oscillators could be increased into the mW range, by combining several devices either in series[30] or parallel[27] configuration, depending on how the signal is coupled out. Our method of inducing NDR in CNT-FETs is suitable for both configurations, in particular the series integration which can be done along one single CNT, and may provide a path to making the first continuous wave oscillator that works well into the THz domain.

Acknowledgements We acknowledge valuable discussions with our research project collaborators: Prof. M. Ahlskog's, Prof. K. Rissanen's and Dr. J. J. Toppari's groups at University of Jyväskylä, E. I. Kauppinen's group at Helsinki University of Technology, as well as the companies Nokia Oyj and Vaisala Oyj. We thank Beneq Oy, Olli Jylhä for ALD processing. This work was supported by the Finnish Funding Agency for Technology and Innovation (TEKES), project number 40309/05, and by the Academy of Finland (Project Nos. 213362, 217045, 217041) and conducted as part of a EURYI scheme award. See www.esf.org/euryi. M. R. would like to acknowledge support from the Magnus Ehrnrooth Foundation and the Finnish Foundation for Technology Promotion (TES).

Supporting Information Available: Re-

sults on reference samples having either SiO_2 or $HfO_2 - TiO_2 - HfO_2$ triple layer gate oxide. Estimation of the energy level separation in the quantum dots together with estimations of the cutoff frequency and the output power of NDR-based oscillators are given. Also the controlled modulation of the NDR feature is shown. This material is available free of charge via the Internet at http://pubs.acs.org.

References

[1] Chang, L. L.; Esaki, L.; Tsu, R. *Appl. Phys. Lett.*, **1974**, *24*, (12), 593-595.

[2] Chen, J.; Reed, M. A.; Rawlett, A. M.; Tour, J. M. *Science*, **1999**, *286*, (5444), 1550-1552.

[3] Zeng, C.; Wang, H.; Wang, B.; Yang, J.; Hou, J. G. *Appl. Phys. Lett.*, **2000**, *77*, (22), 3595-3597.

[4] Charlier, J.-C.; Blase, X.; Roche, S. *Rev. Mod. Phys.*, **2007**, *79*, (2), 677-732.

[5] Zhou, C.; Kong, J.; Yenilmez, E.; Dai, H. *Science*, **2000**, *290*, (5496), 1552-1555.

[6] Buchs, G.; Ruffieux, P.; Groning, P.; Groning, O. *Appl. Phys. Lett.*, **2008**, *93*, (7), 073115.

[7] Chandra, B.; Bhattacharjee, J.; Purewal, M.; Son, Y.-W.; Wu, Y.; Huang, M.; Yan, H.; Heinz, T. F.; Kim, P.; Neaton, J. B.; Hone, J. *Nano Lett.*, **2009**, *9*, (4), 1544-1548.

[8] Lee, S. W.; Kornblit, A.; Lopez, D.; Rotkin, S. V.; Sirenko, A. A.; Grebel, H. *Nano Lett.*, **2009**, *9*, (4), 1369-1373.

[9] Li, J.; Zhang, Q. *Carbon*, **2005**, *43*, 667-670.

[10] Ahlskog, M.; Herranen, O.; Johansson, A.; Leppäniemi, J.; Mtsuko, D. *Phys. Rev. B*, **2009** *79*, (15), 155408.

[11] Appenzeller, J.; Lin, Y.-M.; Knoch, J.; Avouris, Ph. *Phys. Rev. Lett.*, **2004**, *93*, (19), 196805.

[12] Haddad, G. I.; Mazmunder, P. *Solid-State Electron.*, **1997**, *41*, (10), 1515-1524.

[13] Laskar, J.; Ketterson, A. A.; Baillargeon, J. N.; Brock, T.; Adesida, I.; Cheng, K. Y.; Kolodzey, J. *IEEE Electron Device Lett.*, **1989**, *10*, (12), 528-530.

[14] Pop, E.; Mann, D.; Cao, J.; Wang, Q.; Goodson, K.; Dai, H. *Phys. Rev. Lett.*, **2005**, *95*, (15), 155505.

[15] Antonov, R. D.; Johnson, A. T. *Phys. Rev. Lett.*, **1999**, *83*, (16), 3274-3276.

[16] Appenzeller, J.; Knoch, J.; Radosavljević, M.; Avouris, Ph. *Phys. Rev. Lett.*, **2004**, *92*, (22), 226802.

[17] Steele, G. A.; Gotz, G.; Kouwenhoven, L. P. *Nat. Nanotechnol.*, **2009**, *4*, 363-367.

[18] Léonard, F.; Tersoff, J. *Phys. Rev. Lett.*, **2002**, *88*, (25), 258302.

[19] Sollner, T. C. L. G.; Goodhue, W. D.; Tannenwald, P. E.; Parker, C. D.; Peck, D. D. *Appl. Phys. Lett.*, **1983**, *43*, (6), 588-590.

[20] Reed, M. A.; Randall, J. N.; Aggarwal, R. J.; matyi, R. J.; Moore, T. M.; Wetsel, A. E. *Phys. Rev. Lett.*, **1988**, *60*, (6), 535-537.

[21] Rinkiö, M.; Johansson, A.; Zavodchikova, M. Y.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törmä, P. *New J. Phys.*, **2008**, *10*, (10), 103019.

[22] Rinkiö, M.; Johansson, A.; Paraoanu, G. S.; Törmä, P. *Nano Lett.*, **2009**, *9*, (2), 643-647.

[23] Javey, A.; Tu, R.; Farmer, D. B.; Guo, J.; Gordon, R. G.; Dai, H. *Nano Lett.*, **2005**, *5*, (2), 345-348.

[24] Hanson, R.; Kouwenhoven, L. P.; Petta, J. R.; Tarucha, S.; Vandersypen, L. M. K. *Rev. Mod. Phys.*, **2007**, *79*, (4), 12171265.

[25] Saito, R.; Dresselhaus, G.; Dresselhaus, M. S. *Phys. Rev. B*, **2000**, *61*, (4), 2981.

[26] Bockrath, M.; Liang, W.; Bozovic, D.; Hafner, J. H.; Lieber, C. M.; Tinkham, M.; Park, H. *Science*, **2001**, *291*, (5502), 283-285 (2001).

[27] Dragoman, D.; Dragoman, M. *Physica E*, **2004**, *24*, (3), 282-289.

[28] Nishizawa, J.; Potka, P.; Kurabayashi, T. *IEEE Trans. Electron Devices*, **2002**, *49*, (7), 1102-1111.

[29] Brown, E. R. *et al. Appl. Phys. Lett.*, **1991**, *58*, (20), 2291-2293.

[30] Yang, C. C.; Pan, D. *IEEE Trans. Microwave Theory and Techniques*, **1992**, *40*, (3), 434-441 (1992).

Supporting information

Room Temperature Negative Differential Resistance in Carbon Nanotube Field-Effect Transistors with Novel Gate Oxide Design

Marcus Rinkiö[1,2], Andreas Johansson[1,*], Ville Kotimäki[1], and Päivi Törmä[2,*]
[1] Department of Physics, Nanoscience Center, P.O. Box 35, 40014 University of Jyväskylä, FINLAND
[2] Department of Applied Physics, P.O.Box 5100, 02015 Helsinki University of Technology, FINLAND

S1 Reference on $HfO_2 - TiO_2 - HfO_2$ triple layer gate oxide

For further evidence that the engineered structures within the gate oxide are causing the negative differential resistance (NDR) in our devices, we also measured reference devices on a continuous $HfO_2 - TiO_2 - HfO_2$ gate oxide, without the atomic layer deposition (ALD) island patterning. The devices were built similarly as the devices having the ALD islands as a gate oxide. The triple layer gate oxide was grown on top of a highly boron-doped Si wafer, without removing the native SiO_2. The gate oxide deposition was carried out by Beneq Oy (Vantaa, Finland), using a Beneq P400A ALD deposition tool. Precursors used for HfO_2 deposition were hafnium tetrachloride ($HfCl_4$) and water, and for TiO_2 deposition the precursors were titanium tetrachloride ($TiCl_4$) and water. The triple layer gate oxide deposition temperature was 300 °C and the layers had a nominal thickness of HfO_2(40 nm) − TiO_2(0.5 nm) − HfO_2(1 nm).

After the gate oxide deposition, a matrix of alignment markers of Pd(25 nm) with an adhesion layer of Ti(5 nm) was deposited onto the sample, using an e-beam lithography and metalization. A nanotube suspension containing commercial SWCNTs bought from NanoCyl S.A. (Sambreville, Belgium) was made in 1,2-dichloroethane by ultrasonication and a few droplets of the suspension was deposited onto the sample. Using an atomic force microscope, the locations of CNTs were precisely mapped in relation to the predefined alignment marker matrix. Chosen CNTs were then contacted with Pd (30nm) drain (D) and source (S) electrodes through a second e-beam lithography step and subsequent metalization. The sample fabrication is described in more detail in ref[1].

We characterized the charge trapping in these triple ALD layer CNT-FETs by measuring the transconductance with forward and reverse gate sweeps[2]. Using the silicon wafer as a backgate, we sweep the gate voltage from negative to positive voltages and back. This produced reproducible hysteresis loops shown for device RD1 in Figure S1. Hysteresis loops were measured at room temperature (Figure S1a) and at 4.2 K (Figure S1b). These hysteresis loops resemble the hysteresis loops of the ALD island samples. At room temperature (Figure S1a) the relative hysteresis was 2.5 V/6 V. When measuring hysteresis at 4.2 K we used a higher (V_{DS}) voltage of 0.6 V to clearly

*Corresponding authors. E-mail addresses: paivi.torma@hut.fi, andreas.johansson@jyu.fi
[1]University of Jyväskylä
[2]Helsinki University of Technology

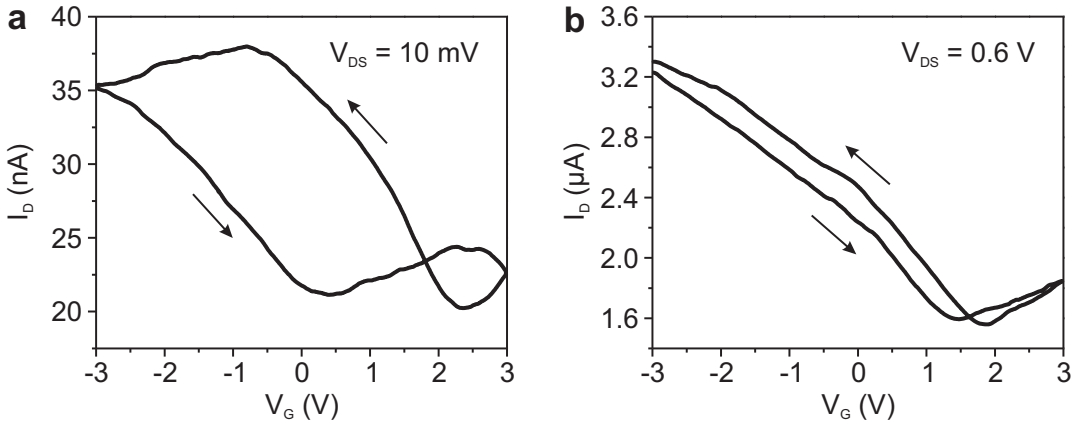

Figure S1: Hysteresis in CNT-FETs having ALD grown triple layer gate oxide. (a) Transfer characteristics measured at room temperature with $V_{DS} = 10$ mV showing advanced hysteresis of a small band gap device RD1. (b) Hysteresis at 4.2 K for the same device measured with $V_{DS} = 0.6$ V. The relative hysteresis decreases more than 80% compared to the original room temperature hysteresis but it still remains strong.

see the hysteresis without any Coulomb blockade behavior visible in the measured traces. The triple ALD layer CNT-FETs also displays strong advanced hysteresis at 4.2 K, with a relative hysteresis of 0.4 V/6 V, indicating that the triple layer gate oxide exhibit pronounced injected charge trapping[3] (See section S3).

When searching for NDR, we performed the same measurements for these reference devices as for the ALD island samples. The results at 4.2 K are shown in Figure S2 in the form of differential conductance plots. For RD1 (Figure S2a), there is no wide band gap visible which is in agreement with the small ON/OFF ratio in of the transconductance measurements in Figure S1. This demonstrates the small band gap nature of the CNT. For the device RD2 (Figure S2b), the band gap gradually opens up at positive gate voltages, resulting in a completely closed structure for $V_G > 2$ V, illustrating the large band gap nature of the CNT. All together we measured three devices having the unpatterned triple layer gate oxide and in these reference devices we did not see any evidence of negative differential resistance (NDR).

S2 Reference on SiO_2 gate oxide

We measured also a reference device (RD3) having more commonly used SiO_2 as its gate oxide. The transfer characteristics of the device with forward and reverse gate sweeps are shown in Figure S3. This device showed a strong unipolar behavior at room temperature with a relative hysteresis of 7.9 V/20 V as shown in Figure S3a. When taking the forward and reverse gate sweeps at 4.2 K, we do not see any hysteresis at all as shown in Figure S3b. This indicates that the main contribution to hysteresis of RD3 at room temperature comes most likely from surface effects[4–7] e.g. water molecules adhered to the surface. At low temperatures these molecules are frozen and cannot be efficiently polarized with the gate voltage and the hysteresis diminishes[8] (See section S3).

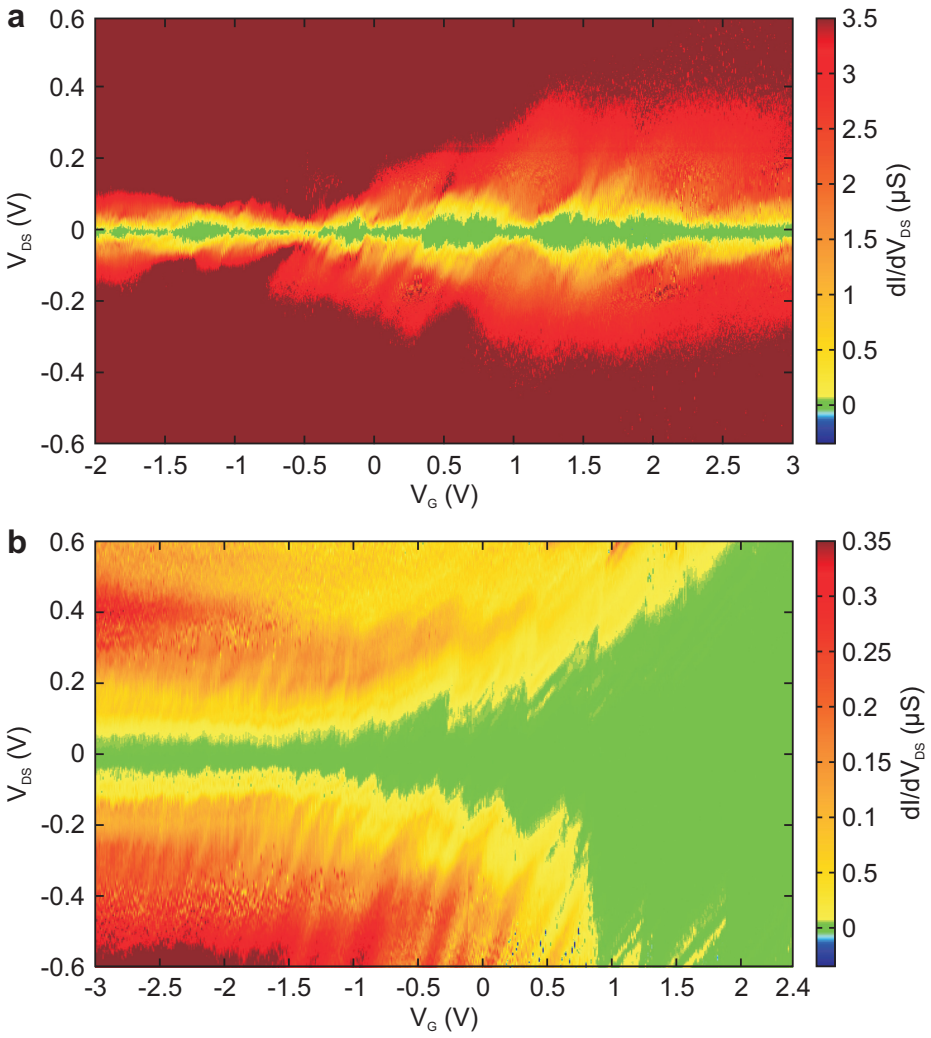

Figure S2: Differential conductance plots measured at 4.2 K for RD1 and RD2. (a) No clear band gap is visible for the device RD1, showing the small band gap nature of the CNT. (b) For the device RD2 band gap opens up at positive gate voltages, illustrating the large band gap nature of the CNT. There was no evidence of NDR in these devices.

We also measured a stability diagram for this device at 4.2 K as shown in Figure S4 in the form of a differential conductance plot. For this device a wide band gap starts to open up already at negative voltages, completely closing already at $V_G = 0$ V within our measured bias window. This illustrates the large bad gap of this CNT. Also in this device there was no evidence of NDR.

S3 Origin of hysteresis in ALD island samples

In this chapter we will discuss the origin of hysteresis in our ALD island samples and the reference samples. We observe bipolar transconductance curves for all the devices having the patterned gate oxide (ALD islands), as shown for device D1 in Figure S5. The transfer characteristics at room temperature are shown in Figure S5a. The gate

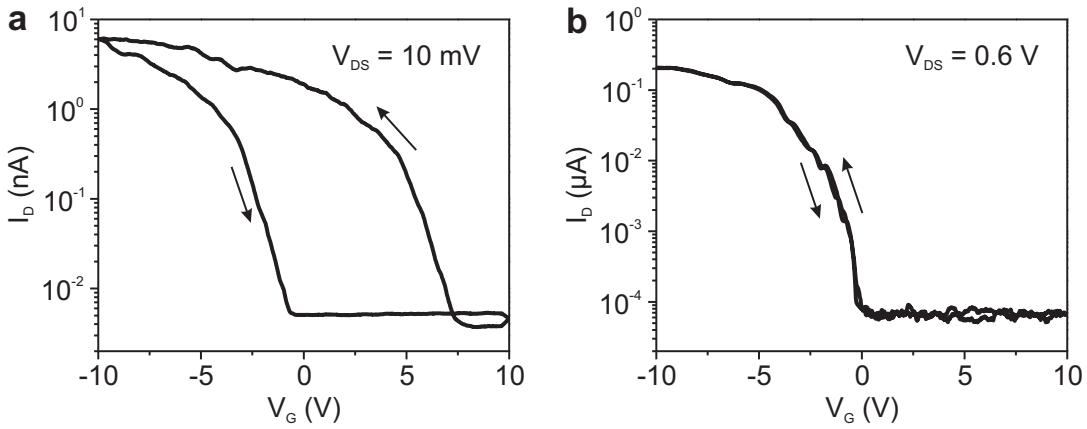

Figure S3: Hysteresis in CNT-FETs having commonly used SiO_2 as a gate oxide. (a) Hysteresis measured at room temperature with V_{DS} = 10 mV showing strong advanced hysteresis of a large band gap device RD3. (b) Transfer characteristics at 4.2 K for the same device measured with V_{DS} = 0.6 V. The hysteresis vanishes completely at low temperatures.

voltage is swept from negative to positive voltages and back, while the drain-source voltage (V_{DS}) is kept at 10 mV. The threshold for current increase attains a higher value for reverse than forward sweep. This produces a highly reproducible hysteresis loop with relative hysteresis of 2.5 V/6 V. A similar hysteresis loop measured at 4.2 K is shown in Figure S5b. Again the current increases at higher gate voltage for reverse sweep. Here we used a higher (V_{DS}) voltage of 0.6 V to clearly see the hysteresis without any Coulomb blockade behavior visible in the measured traces. The produced hysteresis loop has a relative hysteresis of 0.5 V/6 V.

Previously, several different models have been presented for explaining hysteresis in CNT-FETs. (1) Especially,

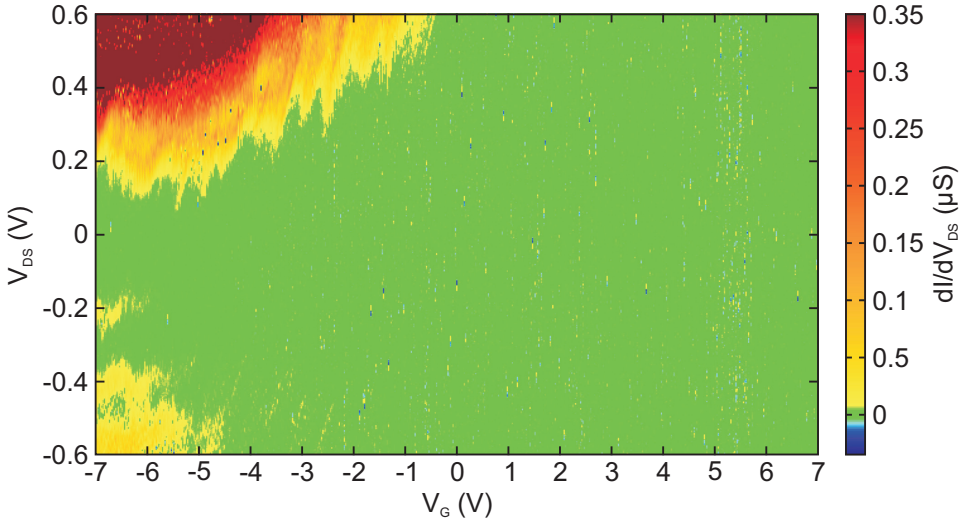

Figure S4: Stability diagram measured at 4.2 K for RD3. A large band gap opens already at negative gate voltages. There was no evidence of NDR in this device.

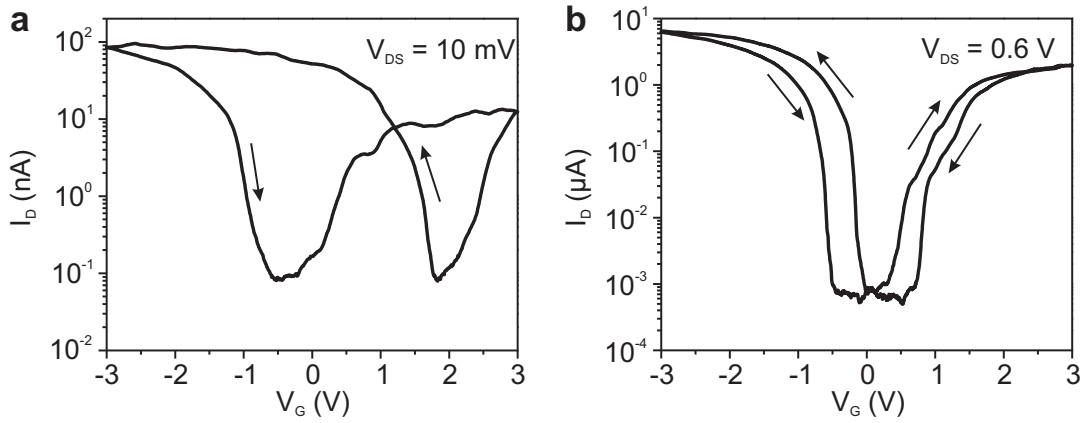

Figure S5: Hysteresis in the ALD island CNT-FETs. (a) Transfer characteristics at room temperature with V_{DS} = 10 mV showing advanced hysteresis. (b) Hysteresis at 4.2 K with V_{DS} = 0.6 V. The relative hysteresis decreases by 80% compared to the original room temperature hysteresis but it still remains signifigant.

in the case of CNT-FETs having SiO_2 as a gate dielectric[9–11], mobile charges or ions within the dielectric can be relocated by altering the gate voltage and as a result they modify the local electric field sensed by the CNT. This is known from Si-MOSFETs to cause retarded hysteresis[12]. Here we see in all our devices advanced hysteresis, which indicates that this is not the main reason for the hysteresis. Also the fact that hysteresis is still present at 4.2 K when having ALD grown gate dielectric rules out mobile charge carriers within the insulator as the main contributors to the hysteresis. (2) Surface chemistry effects, where for instance water molecules adhered to the surface of the dielectric, have been shown to play an important role in some CNT-FETs[4–7]. On the other hand, J. S. Lee *et al.* have shown that surface bound water at 56 K did not significantly change the hysteresis of CNT-FETs having SiO_2 as their gate dielectric. This also indicates that at low temperatures these molecules are frozen and cannot be efficiently polarized with the gate voltage[8]. (3) Defects in the nanotube itself could behave as charging centers. When filled or emptied in response to the gate modulation, these centers could cause hysteresis[13–15]. In a recent study we have shown that using tripple layer ALD $HfO_2 - TiO_2 - HfO_2$ we can control the amount of hysteresis in CNT-FETs[2]. That study thus indicates that defects in the nanotube and the surface chemistry effects are minor contributors to the hysteresis in our case.(4) From the persistent advanced hysteresis at room temperature and at 4.2 K, and from our earlier studies with the triple layer ALD of $HfO_2 - TiO_2 - HfO_2$, it can be concluded that the dominant mechanism behind the hysteresis in the CNT FETs with the patterned layered high-κ dielectric structure is due to tunneling of charge carriers from the nanotube to stationary charge traps induced by the TiO_2 middle layer at a narrowly calibrated distance from the CNT.

S4 Estimation of the expected energy level separation in the quantum dots formed by the ALD islands

To quantitatively test the p-n junction confined quantum dot model we use to explain the observed NDR, we estimate the expected energy level separation in the CNT quantum dots induced by the ALD islands. From the AFM images shown in Figures 1b and c we can estimate the quantum dot size. Taking into account a small angle of the CNT ($\sim 30\,^\circ$) in respect to the groove between the ALD islands and the ~ 50 nm width of the groove, we can estimate the size of our CNT quantum dot induced by the ALD islands for D1 to be ~ 60 nm. In the constant interaction model[16], the electrochemical potentials of transitions between successive resonant tunneling levels in a quantum dot are spaced by the so-called addition energy $E_{add} = \Delta E + E_C$ where E_C is the charging energy and ΔE is the energy spacing between two discrete quantum levels. The level splitting in a simple particle-in-a-box picture is given by $\Delta E = h\nu_F/4L$, where ν_F is the Fermi velocity (8.1×10^5 m/s), h is Planck's constant, and L is the quantum confinement length. For the ~ 60 nm quantum dot we obtain a level splitting of $\Delta E \approx 14$ meV.

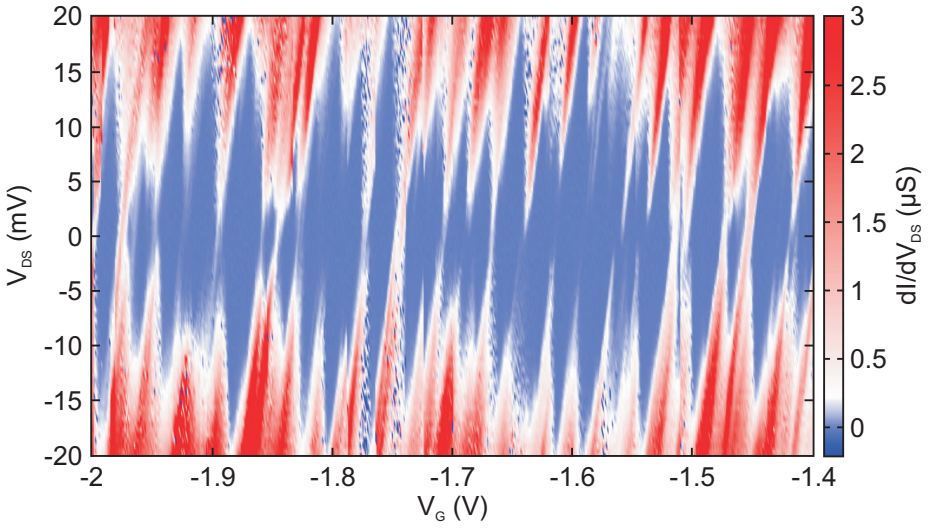

Figure S6: Stability diagram of the npn quantum dot. At 4.2 K, Coulomb blockade is visible in a series of diamonds and corresponds to a single electron charging of a quantum dot of the size ~ 60 nm, having an addition energy ~ 20 meV.

The charging energy is given by $E_C = e^2/C_E$, where e is the electron charge and C_E is the electrical capacitance of the quantum dot. Here C_E is the sum of three capacitances, $C_E = C_{source} + C_{drain} + C_{gate}$. The gate capacitance for a CNT is given by $C_{gate} \approx 2\pi\varepsilon\varepsilon_0 L/ln(2h/r)$, where ε_0 is the permittivity constant, r is the nanotube radius, L is the quantum confinement length and h and ε are the thickness and the average dielectric constant of the dielectric[17]. Taking the HfO_2 dielectric constant of 25, and the thickness of 21 nm with the tube radius of 0.7 nm determined with AFM for D1, we can calculate the gate capacitance for the dot to be $C_{gate} \approx 20$ aF. Using this, the electrical capacitance for the quantum dot can be extracted by measuring the ground-state lines forming the Coulomb diamonds

in the stability diagram shown in Figure S6, with the positive and negative slopes given by $C_{gate}/(C_E - C_{source})$ and $-C_{gate}/C_{source}$. This yields $C_{source} \approx 2$ aF, $C_{drain} \approx 3$ aF and $C_E \approx 25$ aF. For the charging energy this gives $E_C \approx 6$ meV, so the total addition energy would be $E_{add} = \Delta E + E_C \approx 20$ meV. This estimation of the addition energy fits remarkably well to our measured stability diagram in Figure S6 for D1, showing characteristic Coulomb blockade.

These measurements strongly support our model of creating negative differential resistance in CNT-FETs by strong charge trapping in specific places due to designed structures within the gate dielectric, namely the patterning of ALD grown $HfO_2 - TiO_2 - HfO_2$ oxide. Although we have strong hysteresis in the reference devices at ambient conditions and also at 4.2 K in the case of $HfO_2 - TiO_2 - HfO_2$ triple layer gate oxide, we do not see any NDR in the measurements. This indicates that the spatially inhomogeneous electric field caused by the charges trapped within the ALD islands results in band to band tunneling and p-n junction confined quantum dot behavior.

S5 Controlled modulation of the NDR feature

The characteristics of the NDR features are modified by both gate voltage and drain-source voltage, as can be seen in Figure 2c for two different cases (referred here to as NDR 1 and NDR 2). Both show the same qualitative behavior while the modulation is smaller for the NDR feature appearing at lower drain-source voltage (NDR 1). The modulation can be quantified by extracting the peak and valley positions of both current and drain-source voltage as a function of gate voltage. In Figure S7a, the peak and valley drain-source voltage values shift linearly versus gate voltage while maintaining a constant spacing between themselves. This correlates well with the described quantum dot model, for which an external electric field shifts level positions within the dot. The two NDR features could likely be due to two consecutive levels within the dot, considering the roughly 60 mV separation between the two. The peak and valley current responses have on the other hand a non-linear dependence on gate voltage with a strongly varying spacing, as seen in Figure S7b. This leads to more than 20% change of the current peak-to-valley ratio. It may be understood as modulation of the transmission coefficient for transport through the dot by a shift of the dot resonant tunneling levels, tuning of the tunneling barriers and the modulation of the Fermi level. All of these affect to the peak-to-valley ratio and give a direct tuning of the NDR, see Figure S7c.

S6 Estimation of the cutoff frequency and the output power of NDR-based CNT oscillators

One can estimate the ultimate frequency of oscillation that a device of length L could provide by calculating the ideal average passage time of electrons through the channel, i.e. $\tau \sim L/v_F$, where v_F is the Fermi velocity[18]. In the previous section S4, we extracted the value of the level spacing of the quantum dot, $\Delta E = hv_F/(4L) \approx 14$ meV. Using the value given by this to L/v_F, we end up with the frequency $1/\tau \sim 10$ THz. This simple estimate indicates

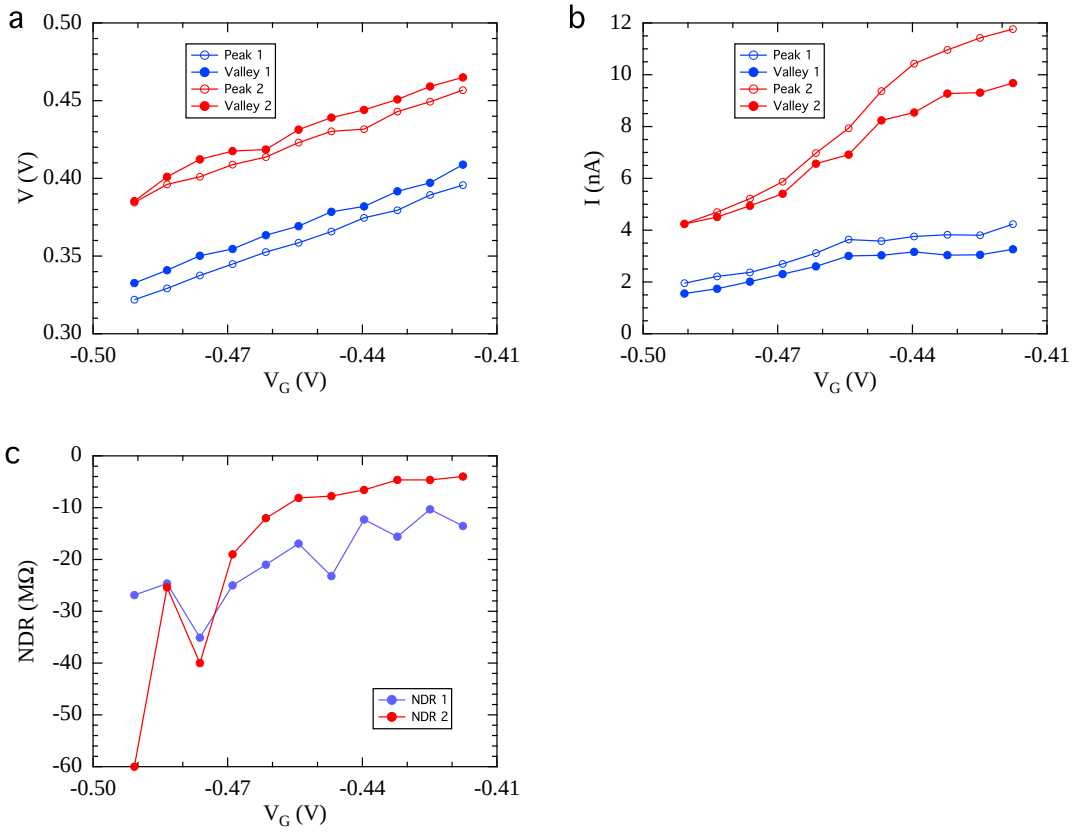

Figure S7: Modulation of NDR characteristics for two NDR features (NDR 1 and NDR 2) in Figure 2b. (a) Drain-source voltage peak and valley values versus gate voltage. Peak and valley values shift linearly with gate voltage but retain a constant spacing between themselves. (b) Current peak and valley values versus gate voltage. The difference between peak and valley current is strongly dependent on the gate voltage. (c) NDR versus gate voltage. The magnitude of NDR can be tuned by the gate voltage, and exceeds here more than one order of magnitude for the 2nd NDR feature. All data are taken from NDR features in Fig. 2b.

that extremely high frequencies should be possible if the device is optimized, that is, has very low contact resistances. For our present non-optimized device we can use the estimate for the cutoff frequency given in [19]. One possible way to couple the potential THz oscillation frequency to propagating waves is by using a bowtie antenna formed with the source and drain electrodes. This gives a condition for having oscillations in a device utilizing NDR of [19]

$$R_{NDR} < -(R_C + R_A), \tag{1}$$

where R_{NDR} is the negative resistance of the NDR feature, R_C is the contact resistance and R_A is the radiation resistance of the bowtie antenna. From Figure S5 we determined the contact resistance of ~ 100 kΩ in our devices. The negative resistance ranges between -60 MΩ to -4 MΩ as shown in Figure S7. Using these values together with the radiation resistance of 80 Ω [19], the relation for oscillations in Equation 1 is satisfied for our device. Assuming

that the inductance of the element is negligible, the cutoff frequency for these oscillations is [19]

$$f_{RC} = \frac{1}{2\pi C_{tot}} \left(-\frac{G}{R_C + R_A} - G^2 \right)^{\frac{1}{2}}, \tag{2}$$

where C_{tot} is the total capacitance and G is total conductance of the CNT quantum dot oscillator. There are two independent parts contributing to the total capacitance $C_{tot} = \left(\frac{1}{C_E} + \frac{1}{C_Q} \right)^{-1}$, where C_Q is the quantum capacitance and has a value in the order of 10^{-16} $\frac{\mathrm{F}}{\mu\mathrm{m}}$ [20] and C_E is the electrical capacitance of the quantum dot calculated in section S4. This gives for our ~ 60 nm CNT quantum dot a quantum capacitance value of $C_Q \sim 6$ aF and the total capacitance of $C_{tot} \approx 5$ aF. For the G_{NDR} we used a value of $(-4\ M\Omega)^{-1}$. Using these values, the maximum cutoff frequency for our current device is $f_{RC} \simeq 50$ GHz.

In order to reach a maximum cutoff frequency above 1 THz, it would be sufficient to reduce R_C below 10 kΩ and R_{NDR} below 100 kΩ. The former is often observed and may be achieved by a post-process annealing step [21]. The latter may a require that also the quantum dot size is reduced, which is easily done with this technique. A smaller quantum dot has a larger level spacing, which is likely to suppress the tunneling probability in the valley region and can enhance the NDR current peak-to-valley ratio. Furthermore, a strength of the method is that the device can be optimized through tuning of the gate induced electrostatic doping of the CNT, which modifies the resistance of the CNT drain and source sections as well as the tunneling barriers surrounding the quantum dot.

References

[1] Zavodchikova, M. Y.; Johansson, A.; Rinkiö, M.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törmä, P. *phys. stat. sol. (b)*, **2007**, *244*, (10), 4188-4192.

[2] Rinkiö, M.; Johansson, A.; Zavodchikova, M. Y.; Toppari, J. J.; Nasibulin, A. G.; Kauppinen, E. I.; Törmä, P. *New J. Phys.*, **2008**, *10*, (10), 103019.

[3] Rinkiö, M.; Johansson, A.; Paraoanu, G. S.; Törmä, P. *Nano Lett.*, **2009**, *9*, (2), 643-647.

[4] Kim, W.; Javey, A.; Vermesh, O.; Wang, Q.; Li, Y.; Dai, H. *Nano Lett.*, **2003**, *3*,, (2), 193-198.

[5] Wang, S.; Sellin, P.; Zhang, Q.; Yang, D. *Curr. Nanosci.*, **2005**, *1*, (1), 43-46.

[6] Lee., J. S.; Ryu, S.; Yoo, K.; Choi, I. S.; Yun, W. S.; Kim, j. *J. Phys. Chem. C*, **2007**, *111*, (34), 12504-12507.

[7] Rinkiö, M.; Zavodchikova, M. Y.; Törmä, P.; Johansson, A. *phys. stat. sol. (b)*, **2008**, *245*, (10), 2315-2318.

[8] Cowin, J. P.; Tsekouras, A. A.; Iedema, M. J.; Wu, K.; Ellison, G. B. *Nature*, **1999**, *398*, 405-407.

[9] Fuhrer, M. S.; Kim, B. M.; Dürkop, T.; Britlinger, T. *Nano Lett.*, **2002**, *2*, (7), 755-759.

[10] Radosavljevic, M.; Freitag, M.; Thadani, K. V.; Johnson, A. T. *Nano Lett.*, **2002**, *2*, (7), 761-764.

[11] Bradley, K.; Cumings, J.; Star, A.; Gabriel, J.-C. P.; Gruner G. *Nano Lett.*, **2003**, *3*, (5), 639-641.

[12] Vanheusden, K.; Warren, W. L.; Devine, R. A. B.; Fleetwood, D. M.; Schwank, J. R.; Shaneyfelt, M. R.; Winokur, P. S.; Lemnios, Z. J. *Nature*, **1997**, *386*, 587-589.

[13] Freitag, M.; Johnson, A. T.; Kalinin, S. V.; Bonnell, D. A. *Phys. Rev. Lett.*, **2002**, *89*, (21), 216801.

[14] Park, J.-Y. *Appl. Phys. Lett.*, **2007**, *90*, 023112.

[15] Kim, Y.; Oh, Y. M.; Park, J.-Y.; Kahng, S.-J. *Nanotechnology*, **2007**, *18*, (47), 475712.

[16] Hanson, R.; Kouwenhoven, L. P.; Petta, J. R.; Tarucha, S.; Vandersypen, L. M. K. *Rev. Mod. Phys.*, **2007**, *79*, (4), 12171265.

[17] Martel, R.; Schmidt, T.; Shea, H.; Hertel, T.; Avouris, P. *Appl. Phys. Lett.*, **1998**, *73*, (17), 2447-2449.

[18] Dragoman, D.; Dragoman, M. *Phys. Rev. B*, **2006**, *73*, (12), 125417-125420.

[19] Dragoman, D.; Dragoman, M. *Physica E*, **2004**, *24*, 282-289.

[20] Ilani, S.; Donev, L. A. K.; Kindermann, M.; McEuen, P. L. *Nature Phys.*, **2006**, *2*, 687-691.

[21] Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M; Dai, H. *Nature*, **2003**, *424*, 654-657.