Graphene phononic crystals fabricated with electron-beam lithography

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Abstract

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Graphene, as a true 2D material, presents the possibility of studying in practice many theoretical models for the behaviour of such systems. One area of particular interest is the suppression of thermal conductance resulting from the introduction of a periodic array of holes into a material, known as a phononic crystal (PnC).

In this thesis work, an electron-beam lithography based process for fabricating PnCs of varying lattice parameters in graphene was developed. Additionally, a method for cleaning carbon contamination off graphene surfaces by reactive ion etching (RIE) was tested. The resulting graphene PnC (GPnC) devices were imaged through optical, scanning electron, helium ion and atomic force microscopy, as well as electrically characterized through differential conductance measurements at temperatures ranging from liquid nitrogen 75 K to liquid helium 4 K. The fabrication method was demonstrated to be capable of producing stable structures with feature sizes down to tens of nanometers, and the RIE cleaning method showed qualitative improvement of the graphene surfaces. Differential conductance of GPnC devices displayed a significant decrease at zero voltage bias with decreasing temperature, which provides a way for local thermometry of graphene in future work. Further research is required to measure the thermal conductance of such devices at temperatures below 4 K.

Keywords: phononic crystal, graphene, electron-beam lithography

Tiivistelmä

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Grafeenifononikiteiden valmistus elektronisuihkulitografian avulla
Pro gradu -tutkielma
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Koska grafeeni on aito kaksiulotteinen materiaali, sen avulla voidaan tutkia käytännössä teorioiden ennustamaa käyttäytymistä sellaisissa järjestelmissä. Yksi erityisen kiinnostava ilmiö on lämmönjohtavuuden lasku kun materiaaliin luodaan säännöllinen reikien joukko. Tällöin puhutaan fononikiteestä.

Tässä pro gradu -tutkielmassa kehitettiin elektronisuihkulitografiaan pohjautuva prosessi, jolla voidaan valmistaa fononikiteitä useilla eri hilan parametreillä. Lisäksi kokeiltiin grafeenipinnan puhdistusta reaktiivisen ionietsauksen (RIE) avulla. Valmiit grafeenifononikidelaitteet kuvannettiin optisen, elektronisuihku-, heliumioni- ja atomivoimamikroskopian keinoin, sekä karakterisoitiin sähköisesti differentiaalikonduktanssin mittauksilla nestetypen lämpötilasta 75 K nesteheliumin läpötilaan 4 K. Työssä näytettiin, että valmistusmenetelmällä voidaan tuottaa vakaita rakenteita, joissa pienimmät kohdat ovat kymmenien nanometrien luokkaa, ja RIE-puhdistus paransi grafeenipinnan laatua kvalitatiivisesti. Grafeenifononikidelaitteiden differentiaalikonduktanssissa nähtiin huomattava aleneminen, kun jännitebias oli nolla alhaisemmilla lämpötiloilla. Tämä mahdollistaa tulevissa mittauksissa grafeenin lämmönmittauksen lokaalisti. Lisää tutkimusta tarvitaan, jotta tällaisten laitteiden lämmönjohtavuus saadaan mitattua alle 4 K:n lämpötiloissa.

Avainsanat: fononikide, grafeeni, elektronisuihkulitografia

Preface

Ever since my bachelor's thesis on the applications of focused ion beam techniques, I have been steadily falling down the proverbial nanofabrication rabbit hole. Some 2.5 years later, about to make my own small contribution to this rapidly growing field, I remain convinced that we can expect ever greater insight into the nature of matter at the smallest of scales moving forward into the future. Now, I would like to take this opportunity to offer thanks to the people who made my work possible.

First, I would like to thank Prof. Ilari Maasilta for the opportunity of working with his thermal nanophysics group on this project since my induction as a summer trainee in 2020. For his continued guidance on all things practical during this thesis work, I would especially like to thank Mr. Jaakko Mastomäki. For providing the graphene used in this work, I wish to thank laboratory technician Mr. Olli Rissanen. Staff scientist Dr. Kimmo Kinnunen and laboratory engineer Mr. Tarmo Suppula have my gratitude for ensuring the smooth operation of the laboratory equipment at the Nanoscience Center. Also, I would like to thank the rest of our research group members, especially Mr. Aki Ruhtinas and Mr. Tatu Korkiamäki for their general assistance and insightful discussions, as well as Mr. Geng Zhuoran for his help with the electrical measurements.

Finally, I wish to thank my parents and brother for their ongoing support during this process. The support from my friends is also greatly appreciated.

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Aaro Lankinen

Contents

1 Introduction

Phononics is a rapidly emerging field of study of quantized crystal lattice vibrations called phonons. Low-dimensional systems are of particular interest, with graphene, a one-atom-thick layer of carbon, being an archetypal 2D material. Along with electrons, phonons show widely different behaviour in 2D materials as compared to bulk. In the case of graphene the primary factors are the number of carbon layers and the presence or absence of a regular lattice of holes, then referred to as a graphene phononic crystal (GPnC) or graphene nanomesh (GNM) [1], [2].

While graphene has only recently experienced what could be described as a blooming into public consciousness, the study of this material goes back for some 70 years, with the earliest works being from the 1940s [3]–[5]. At this point, graphene was thought of more as a theoretical tool to explain the behaviour seen in bulk graphite, rather than a physical material in and of itself. This base was further expanded during the 1980s to utilize graphene as a condensed matter analogue for the study of (2+1)D quantum electrodynamics [6]–[8]. Still, graphene was thought to not be able to exist by itself in a free state until just such a discovery was made after the turn of the millennium by Novoselov et al. [9], [10] and the charge carriers were identified as massles Dirac fermions [11], [12]. This discovery also paved the way for graphene analogues, such as single-layer boron nitride [10], [13].

Although the existence of graphene as a standalone material might be taken for granted these days, the prevailing ideology before the time of Novoselov et al. that graphene cannot exist on its own at least without a crystalline base [14], [15] was supported by theoretical work [16] which suggested that low-dimensional crystal lattices should indeed decompose at finite temperatures due to thermal fluctuation. Experiments have since confirmed that graphene can indeed be isolated not only on top of noncrystalline surfaces [10]–[12] and suspended in a liquid [9], [17] but also across an air gap [18]. After the experimental proof for the existence of the free state of graphene was obtained, the theory can be made to reconcile with these findings by positing that graphene sheets are metastable after being extracted from bulk material [16]. Another way in which graphene can be though to stabilize is

by crumpling into the third dimension on the scale of 10 nm [18]. This process can suppress the propagation of thermal vibrations through the material [13], [19].

Due to its compatibility with the existing semiconductor industry processes, graphene has long been considered a viable candidate to overtake silicon as the material for the next generation of electronic devices [20]. As with all electronics though, heat dissipation will ultimately set a boundary for the performance that can realistically be expected. Hence, if graphene is to be integrated into electronics, particularly microprocessors, its novel thermal transport properties have to be thoroughly understood.

Previous research has shown that introducing a tightly packed 2D lattice of similarly sized holes into a sheet of graphene greatly enhances boundary scattering and leads to strong diffusive behaviour [1], [2]. This can strongly suppress thermal conductivity, the majority of which in graphene at room temperature is due to phonons with a mean free path longer than 100 nm and a wavelength shorter than 5 nm, if the diameter of the holes is engineered to fall in between these two values [21].

While a GPnC with a high filling factor (porosity), that is to say lots of air in the finished sheet, is often desirable, various geometries for the pores themselves can be implemented. These range from the simple circle [22] and square [23] to more elaborate cross [24] and snowflake patterns [25]. Another key point in understanding GPnCs is the formation of a phononic band gap (PBG) [22], [26], when introducing holes into the sheet. The exact frequency of this PBG is highly tunable from MHz to THz regimes by varying the lattice parameters [22], [25]. Molecular dynamics simulations suggest that by changing porosity from 21% to 65% we can expect the thermal conductivity of a GPnC to drop by and order of magnitude when compared to a plain graphene sheet [27]. Moreover, due to its relative ruggedness, graphene also presents the possibility of further changing the bandgap and the thermal transport properties of a GPnC by up to 350% by strain engineering through electrostatic gating of freestanding GPnC [22].

A novel way of non-invasively tuning a phononic crystal in graphene is through the use of a periodic array of electrodes held away from a suspended graphene sheet. Upon application of a DC voltage to the electrodes, the electrostatic stress on the graphene sheet simulates a phononic crystal of periodic "bumps" without the need to make any permanent modifications to the graphene [28].

As for fabrication methods, reactive ion etching (RIE) with a hard mask has been shown to be able to produce consistent pores of the order of tens of nanometers [1], while helium ion microscopy (HIM) [25] and bottom up chemical synthesis [29] can go down to single nanometers. Thus far, HIM is ill suited for industrial scale production due to its low throughput, while RIE and bottom-up synthesis could potentially be scaled up. Of course, another hurdle before ever getting to PnC patterning is to find a commercially viable and fast method of producing high purity graphene monolayers.

Beyond mere heat-resistant electronics, GPnCs have a number of other potential applications, such as: superlenses with negative refractive index for studying sound waves below the diffraction limit [30], phonon nanocapacitors for storing terahertz acoustic radiation [31], [32], micro-electromechanical system (MEMS) resonators [23], mechanical qubits [22], mass and force sensors [22], molecular sensors [29], acoustic waveguides and filters [25], acoustic and thermal cloaking [24], and thermal diodes [24].

In this thesis work, an electron beam lithography (EBL) based process for fabricating phononic crystals in graphene is developed.

2 Theoretical Background

2.1 Phonons

Phonons can be understood as quanta of sound waves, similarly to how photons are the quanta of electromagnetic (EM) waves. Unlike EM waves though, phonons can only propagate through a medium, such as condensed matter or liquid. Phonons are also responsible for heat transport in such media. Heat transport in a solid can be conceptualized as an arrangement of hard atoms connected by "springy" interatomic forces, where a displacement in the position of some of these atoms from equilibrium is propagated through the lattice by nearest neighbour interactions. However, such a model proves insufficient to explain many phenomena outside of everyday observations, like the high thermal conductivity of diamond [33].

For a more robust handling of phonons, we must consider that the collective vibration of the whole atomic lattice has characteristic normal modes, among which the thermal energy is distributed. These normal modes can classically be thought of as being composed of travelling waves moving in opposite directions giving rise to a standing wave. When longitudinally polarized, we know these travelling waves as sound waves as opposed to the transverse waves of EM radiation [33].

Now, a classical harmonic system with normal mode of frequency ω corresponds to a quantum system with eigenstates of energy

$$E_n = \hbar\omega \left(n + \frac{1}{2} \right). \tag{1}$$

Keeping in mind that such a harmonic oscillator can represent the collective normal mode of an entire crystal's vibration rather than that of a single particle within, we can define the phonon as a quantum of vibration. We also note that many phonons can occupy the same state, as evidenced by the fact that that n in equation 1 is a positive real number [34].

The number of thermal phonons occupying a given state is described by the Bose

occupation factor

$$n_B(\beta\hbar\omega) = \frac{1}{e^{\beta\hbar\omega} - 1}, \tag{2}$$

where $\beta = (k_B T)^{-1}$, $\hbar$ is the reduced Planck's constant, ω the frequency of the phonon mode, k_b the Boltzmann constant and T the temperature [34]. Now, the expectation value for energy of a single mode corresponding to the wavevector $\vec{k}$ is given by

$$E_{\vec{k},s} = \hbar\omega_s(\vec{k}) \left(n_B(\beta\hbar\omega_s(\vec{k})) + \frac{1}{2} \right), \tag{3}$$

and the total energy of such a system is the sum over all normal modes

$$U = \sum_{\vec{k},s} E_{\vec{k},s} \tag{4}$$

$$\tag{5}$$

where $\vec{k}$ runs over the first Brillouin zone and s over the three allowed (two transverse and one longitudal) phonon polarization modes [34]. For any real system, the number of normal modes is going to be large and the distance between individual points in k-space is small. Hence, the sum can be taken as an integral instead, giving the total internal energy of the system as

$$U = \sum_s \int \frac{d\vec{k}}{(2\pi)^3} E_s(\vec{k}). \tag{6}$$

The heat capacity is then obtained as dU/dT [34].

2.2 Phononic crystals

As the name implies, phononic crystals (PnCs) are similar to photonic crystals in many ways. While photonic crystals can be defined as artificial materials with periodic modulation of the dielectric constant on the scale of optical wavelengths [35], phononic crystals are similarly artificial materials with periodic modulation of the speed of sound [36]. This can be understood as periodic scattering centers in photonic or phononic crystal changing the ease at which photons (electromagnetic waves) or phonons (elastic waves) propagate though the material. While the definition merely requires periodic arrangement of scatterers, the most common PnC structure is an array of holes filled with air or vacuum in a thin film. In such a structure, the

interfaces between air or vacuum and graphene serve as the scattering centres for phonons. This is exactly the approach taken in this work when it comes to patterning graphene.

In order to characterize a PnC, we will use parameters such as periodicity, filling factor and band gap. For the simple square lattice considered in this study, we can take think of the periodicity a PnC as the distance from the centre of one hole to the centre of its nearest neighbour. Alternatively, we can think of the periodicity as being equivalent to the lattice constant of the structure. Filling factor is the ratio of the surface area of the periodic disturbance to the overall surface area of the unit cell. A phononic band gap is a range of prohibited frequencies for acoustic waves in a material, such as a PnC. It forms when interference takes place between multiple scattered waves and the frequencies for which destructive interference occurs can not propagate through the material. The presence of this band gap is one of the defining features of a phononic crystal and of great interest where applications are considered [37]. Phononic crystals with periodicities on the order of 1 µm have been successfully fabricated in our group using suspended silicon nitride [38]. An example of such a PnC is shown in Figure 1.

While the exact mechanisms by which phonon mobility in a PnC is altered are varied, they can be roughly divided into coherent and incoherent regimes, where phonons display wave- and particle-like behaviour, respectively. These are strongly temperature dependent, with incoherent mechanisms mostly dominating at temperatures above $\approx 10\,\mathrm{K}$. Here, incoherent mechanisms refer to those that destroy phonon phase after successive scatterings and prevent wave interference from occurring. Examples of incoherent scattering mechanisms are phonons scattering diffusely off material interfaces, off impurities in the crystal or off one-another. With ever-greater portion of the phonons travelling through a material being backscattered, this can lead to suppression of thermal conductivity [39].

Conversely, at temperatures below $\approx 10\,\mathrm{K}$, phonon transport is best described by coherent mechanisms which preserve phonon phase information and allow for wave-like interference to take place. The suppression of thermal conductance here is due to the periodicity inherent in a PnC causing modification to the phonon dispersion relation, which leads to lower group velocities [39].

For an isotropic insulator, the heat capacity in two dimensions can be obtained

with the Debye approximation as

$$C_{\mathrm{2D}} = \frac{3\zeta(3)}{\pi}\frac{k_B^3}{\hbar^2}\left(\frac{2}{c_t^2}+\frac{1}{c_l^2}\right)T^2, \tag{7}$$

where ζ is the Riemann zeta function, k_B the Boltzmann constant, $\hbar$ the reduced Planck's constant, c_t and c_l the velocities of the transversal and longitudal bulk phonon modes respectively and T is the temperature [40].

While a phononic crystal can equally be realized in 1, 2 or 3 dimensions, this work considers the case in 2D only as we aim to demonstrate that such a structure can be implemented in graphene, an archetypical 2D material.

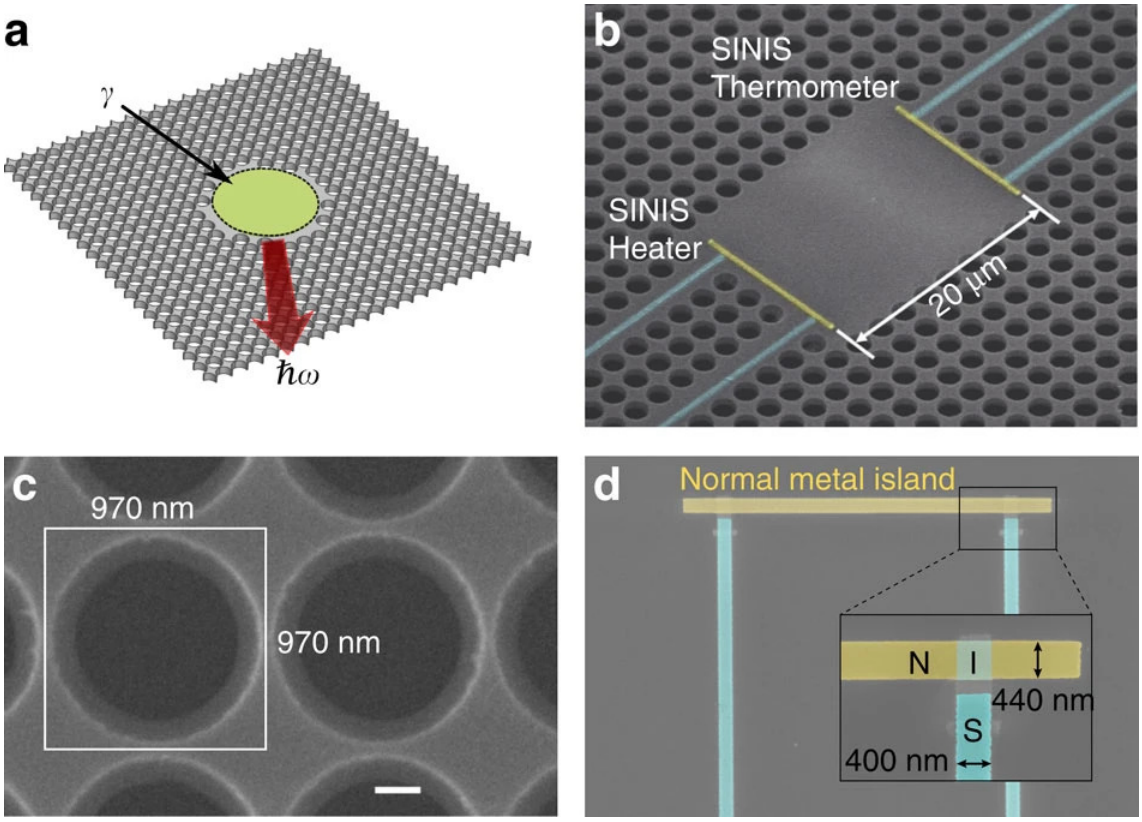


Figure 1. **(a)** Theoretical structure of a PnC device that can be fabricated with e-beam lithography. A heater is included in the centre as part of the design, shown here radiating phonons into the crystal lattice. **(b)** A SEM image of the central region of an actual PnC device with lattice constant $a = 2425\,\text{nm}$. The silicon nitride membrane is shown in light grey, while the dark regions are holes in the membrane. False colors are further applied to highlight the heater and thermometer elements. Aluminium wires are shown in blue and copper wires in yellow. This wiring scheme carries over between different samples. The overall size of the PnC is $100\,\mu\text{m} \times 100\,\mu\text{m}$. **(c)** A SEM closeup of the holes in a PnC with smaller lattice constant, showcasing the $970\,\text{nm} \times 970\,\text{nm}$ unit cell and the $\sim 60\,\text{nm}$ neck width between individual holes. The sidewalls for each hole are slightly angled inwards, so that the holes have a slightly smaller diameter at the bottom than at the top. The white scale bar here is 200 nm in length. **(d)** A SEM closeup of the structure of a heater or thermometer element with false colors applied as above. Superconducting aluminium leads connect from the measurement circuit to two normal metal-insulator-superconductor (NIS) tunnel junctions, which are in turn connected by a normal metal copper wire. Figure reprinted from [38], under the Creative Commons Attribution-NonCommercial-NoDerivs 3.0 Unported License.

2.3 Graphene

Graphene consists of a two-dimensional monolayer of carbon atoms arranged in a regular hexagonal "honeycomb" lattice. This structure arises from the fact that carbon has 4 valence electrons in orbitals $2s$, $2p_x$, $2p_y$ and $2p_z$, which can hybridize. One possible hybridization, as seen in graphene, produces 3 identical sp^2 orbitals which lie 120° apart on the xy-plane, and the single unhybridized $2p_z$ orbital is left over on the z-axis. The sp^2 hybrid orbitals can then form a honeycomb lattice through σ-bonding, while the electron on the $2p_z$ orbital is weakly bonded and can roam through the lattice by π-bonding, leading to conductivity [41][42].

Figure 2 shows the graphene honeycomb lattice in real and reciprocal space. The honeycomb lattice itself consists of two triangular Bravais sublattices named A and B according to the atom used as their base. The unit cell for the lattice is a rhomboidal in shape and encompasses the two atoms for the sublattices A and B. The lattice is defined in real space by the basis vectors $\boldsymbol{a_1} = a\left[\frac{\sqrt{3}}{2}, \frac{1}{2}\right]$ and $\boldsymbol{a_2} = a\left[\frac{\sqrt{3}}{2}, -\frac{1}{2}\right]$ and in reciprocal space by $\boldsymbol{b_1} = \frac{2\pi}{3}a\left[1, \sqrt{3}\right]$ and $\boldsymbol{b_2} = \frac{2\pi}{3}a\left[1, -\sqrt{3}\right]$ respectively. The K and K' points are mirror images of one another in terms of their geometry in reciprocal space [43].

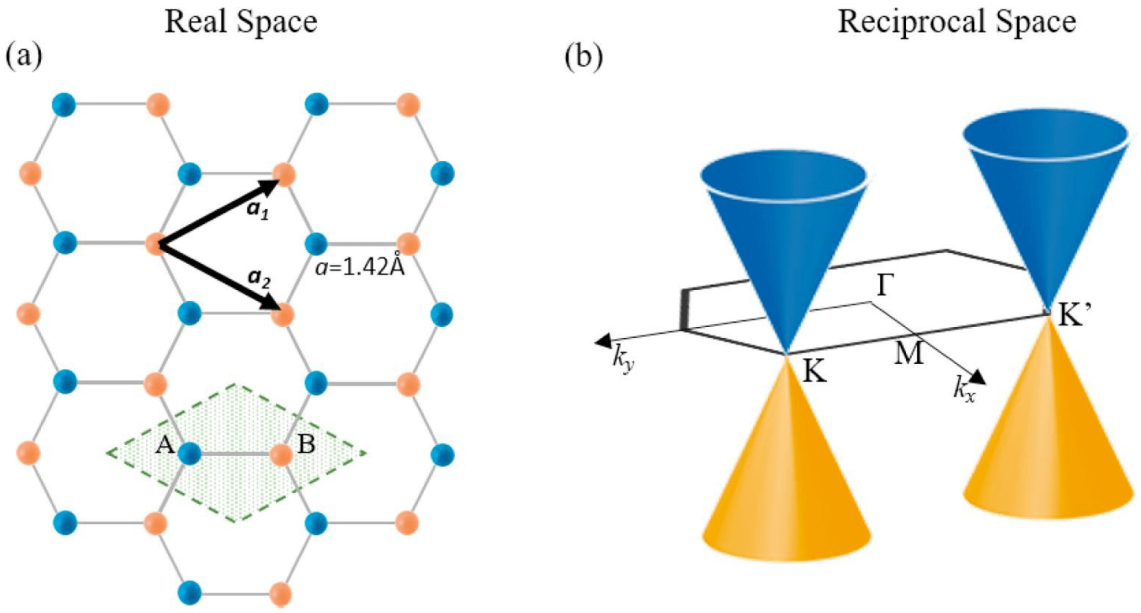


Figure 2. (a) The honeycomb lattice of graphene in real space, as defined by the basis vectors $\boldsymbol{a_1}$ and $\boldsymbol{a_2}$ and basis atoms A and B. $a = 1.42$ Å is the nearest neighbour distance. (b) A single Brillouin zone for the same lattice in reciprocal space. The Dirac cones at K and K' points are due to the unique dispersion relation in graphene. Figure reprinted from [43], with permission from Elsevier.

As an allotrope of carbon, graphene can be though of as a single sheet of three-dimensional graphite, whereby it acts as building block for the whole family of graphitic materials. Apart from graphene, these include 3D graphite, 1D carbon nanotubes and 0D fullerenes, all of which can be constructed from graphene by stacking, rolling and wrapping up a single sheet in on itself, respectively [13]. With high purity fabrication methods, close to defect-free graphene can be obtained, allowing the charge carriers therein a mean free path of up to thousands of interatomic distances even at room temperature [9]–[13].

Considering graphene is but a sheet of atoms, it is interesting to consider what happens if one was to keep adding on layers. Both single-layer and bilayer graphene are electrically similar in that they can both be considered zero-gap semiconductors where, depending on doping and gating, the charge carriers can be electrons or holes. From 3 to 10 layers we can observe multiple types of charge carriers as the conduction and valence bands start to overlap [9], [44], [45]. Beyond 10 layers, stacked graphene is electrically (if not mechanically) similar to bulk graphite [44]. Hence we can comfortably talk about single-, double- and "few"(3-10)-layer graphene as their own structures distinct from bulk graphite. However, due to the relatively short

screening length of less than two graphene layers in graphite, it becomes possible to differentiate surface from bulk in stacked graphene as thin as five layers [13], [45], [46].

2.3.1 Graphene Fabrication

Methods to fabricate graphene range from mechanical and chemical exfoliation to supported growth and chemical vapor deposition (CVD) epitaxial growth, which is the method used to grow the graphene sheets used in this thesis.

Mechanical exfoliation is perhaps the simplest of all these methods, and requires little more than the repeated folding of a thin sheet of graphite between to pieces of adhesive tape [9], or rubbing a graphite block against a solid surface [10]. Specifically, the latter technique can produce single-layer graphene sheet up to 100 µm in size [10]. A problem arises when trying to identify those precious flakes of single-layer graphene from among the considerably larger volume of graphite leftovers. However, it turns out that graphene can be made visible under optical microscope by placing it on top of a silicon substrate with approximately 300 nm of SiO_2 [10]. Raman spectroscopy can also be used to analyse the thickness of graphene due to it possessing a fingerprint [13], [47], [48].

Chemical exfoliation is another way to obtain graphene from bulk graphite. In this process, also called intercalation, graphite is exposed to chemicals which tend to embed themselves in between individual graphene layers [49]. The goal here is to create enough separation between the layers to overcome the van der Waals interaction inherent in graphite. The tricky part is to then dissolve away the intercalated molecules while preventing the graphene layers from stacking back into graphite. Traditionally, this method tends to produce a sort of graphitic sludge consisting of re-stacked and scrolled graphene sheets [50]–[52]. Where the properties of individual graphene sheets are to be studied, this method is less than ideal. However, it does have comparatively high throughput and could prove useful in producing larger quantities of few-layer graphene [53] and graphene oxide [54]. Following research shows some promise of obtaining defect-free single sheet graphene [13], [55].

Chemical vapor deposition can be used to grow epitaxial graphene directly from hydrocarbons onto a metal substrate [56], [57]. Rather than hydrocarbons, silicon carbide SiC can also be thermally decomposed to provide carbon atoms for graphene

growth. This technique tends to produce few-layer graphene with high mobility charge carriers [58], [59]. So far CVD growth of epitaxial graphene seems to posses a balance of throughput that may be one day suitable for industrial scale production and an acceptable quality for the individual graphene sheets [13].

The modern process for CVD growth of graphene is largely based on the use of a flexible copper foil as substrate on which the graphene is grown. The Cu foil is wrapped around a quartz (glass) tube and inserted into a cylindrical CVD reactor (furnace). Before the CVD growth, the copper film is annealed in high temperature ≈1000 °C to allow for the formation of grains in the film of the order of 100 µm. Methane is then introduced into the furnace at 3 : 1 ratio to hydrogen for approximately 30 min after which the chamber is quickly cooled down to room temperature. Generally, one can expect higher quality graphene to form with higher reactor temperature as thermal motion cleans up the less stable contamination from the forming graphene. This technique can potentially produce single-crystal graphene flakes up to 0.5 mm in size [60], [61].

2.3.2 Electrical properties of graphene

Contrary to "normal" charge carriers as seen in metals and semiconductors which are described by the Schrödinger equation, the charge carriers in graphene mimic relativistic behaviour and are effectively described by the massless Dirac equation instead [6]–[8], [62]–[66]. The Dirac equation for a relativistic particle is given by

$$i\hbar\frac{\partial \mathbf{\Psi}}{\partial t} = \left[-i\hbar\left(\sigma_x\frac{\partial}{\partial x} + \sigma_y\frac{\partial}{\partial y}\right)\right]\mathbf{\Psi}, \tag{8}$$

where the Pauli matrices are

$$\sigma_x = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \sigma_y = \begin{bmatrix} 0 & -i \\ i & 0 \end{bmatrix}, \sigma_z = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}, \mathbf{\Psi} = \begin{bmatrix} \Psi_\uparrow \\ \Psi_\downarrow, \end{bmatrix} \tag{9}$$

where $\Psi_\uparrow$ and $\Psi_\downarrow$ are the wavefunctions for the up and down spins respectively.

As discussed before, the motion of electrons through the periodic potential of the honeycomb lattice gives rise to linear dispersion for the electron bands, thus leading to massless Dirac fermions. These quasiparticles are described by the Hamiltonian

$$\hat{H} = \hbar v_F \boldsymbol{\sigma}\cdot\vec{k} = \hbar v_F \begin{bmatrix} 0 & k_x - ik_y \\ k_x + ik_y & 0 \end{bmatrix}, \tag{10}$$

where $\hbar$ is the reduced Planck's constant, v_F is the Fermi velocity instead of the speed of light c, $\boldsymbol{\sigma}$ is the 2D Pauli matrix and $\vec{k}$ is the wavevector of the quasiparticle. This Dirac-like Hamiltonian comes about to the fact that the graphene lattice consists of two sublattices, whose energy bands intersect near the edges of the Brillouin zone. These sublattices are correspond to the "spins" of the relativistic Dirac equation and are thus known as pseudospins. Noteworthy is the fact that many quantum electrodynamic phenomena tend to be inversely proportional to the speed of light. As lightspeed is vastly larger than the Fermi velocity of charge carriers ($c/v_F \approx 300$) in graphene, relativistic effects are also more pronounced [13], [41].

The property that first sparked a real interest in graphene was its linear energy dispersion relation near the Fermi-energy, shown in Figure 2b, which leads to an unusually high charge carrier mobility [2], [9], [13]. Electronic mobility in graphene deposited onto a substrate can exceed $2 \times 10^3\,\mathrm{cm}^2\,\mathrm{V}^{-1}$ at room temperature while suspended and annealed graphene can reach $2 \times 10^5\,\mathrm{cm}^2\,\mathrm{V}^{-1}$ [67].

The dispersion relation for graphene near the $\bar{K}$ and $\bar{K}^{(\prime)}$ points is given by [41]

$$E = \pm\hbar v_F \left|\bar{k} - \bar{K}^{(\prime)}\right|. \tag{11}$$

To begin to assess the electrical behaviour of a 2D system such as graphene, we need the density of states (DOS) in such a material. In general, the DOS of an n-dimensional system as a function of its energy E is

$$\mathrm{DOS}_n(E) = \rho(E) = \frac{d\Omega_n(E)}{dE} = \frac{nc_n}{pc_k{}^{n/p}} \left(E - E_0\right)^{n/p-1}, \tag{12}$$

where $\Omega_n(E)$ is the k-space volume enclosed by the surface E, $\Omega_n(E) = c_n k^n(E)$ so that $c_2 = \pi$, c_k is the prefactor of the dispersion relation and p is the power law exponent of the dispersion relation ($p = 1$ for single-layer graphene and $p = 2$ for bilayer graphene respectively) [41]. Plugging the linear dispersion relation of graphene into equation 12 with $E_0 = 0$ gives us the density of states per unit cell for graphene as

$$\rho(E) = \frac{2A_c}{\pi}\frac{|E|}{v_F^2}, \tag{13}$$

where $A_c = 3\sqrt{3}a^2/2$ is the area of a single unit cell [68].

Graphene also displays a property called chirality, which is to say that for

an electron in graphene its propagation direction and phase are not independent. Chirality can be thought to arise from the fact that the Pauli matrix for massless Dirac fermions in graphene, $\boldsymbol{\sigma}$, does not describe real spins but rather pseudospins due to contributions from both of the sublattices in the structure of graphene. Chirality in graphene can also be understood in terms of the Berry's phase [12], [68], [69]. This describes the additional phase π that is added to the electron wavefunction in single layer graphene or 2π for bilayer graphene. Many of the QED phenomena in graphene, such as Klein tunnelling [65], [70], [71] can be understood in terms of the conservation of chirality and pseudospin [41].

This behaviour is due to the interaction of electrons with the periodic potential of the graphene lattice, which produces these quasiparticles known as massless Dirac fermions. While not fundamentally such, a helpful shorthand can be to think of these quasiparticles as either electrons that have lost their rest mass or as neutrinos that have acquired a charge equal to that of the electron [13].

Another interesting electrical feature of graphene is the tendency for its charge carriers to undergo ambipolar diffusion when placed in an external electric field. Depending on field strength, the concentration of electrons or holes can be made as high as $1 \times 10^{13}\,\mathrm{cm}^{-2}$ and charge carrier mobility can exceed $1.5 \times 10^{4}\,\mathrm{cm}^{2}\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ under ambient conditions [9]–[12]. This exceptional charge carrier mobility combined with the fact that graphene can display the quantum Hall effect at room temperature [72] makes the material ripe for electrical studies [13].

Graphene also retains some conductivity undoped and in the absence of gate potential when the charge carrier density approaches zero. More specifically conductivity tends towards the conductance quantum q^2/h per carrier type [11]. For normal materials in a similar situation, a metal-insulator transition is expected to occur with decreasing temperature, but graphene does not display this even at liquid helium temperatures. Both of these observations hint at the theorized [7], [64], [66], [73]–[78] minimum quantum conductivity for Dirac fermions. Bilayer graphene in the absence of gate potential and with vanishing carrier density also shows minimum conductivity of q^2/h per carrier type [79], [80], which suggests that chirality is the main source for such an effect and not the linear energy spectrum of graphene [13].

Graphene does not display significant low field ($B < 1\,\mathrm{T}$) magnetoresistance near the Dirac point down to liquid helium temperatures [81]. On the other hand, graphene shows universal conductance fluctuations in line with the normal metallic behaviour

when away from the Dirac point [81]. While early theories predicted that graphene could show both positive, negative, as well as zero magnetoresistance due to weak localization, more recent work posits that one should expect zero magnetoresistance for sufficiently large carrier density and where no inter-valley scattering takes place [82]. This is explained by the breaking of time-reversal symmetry within the valleys of the Fermi surface of graphene due to triangular warping of those surfaces [82]. As more and more inter-valley scattering occurs, one would expect to see negative weak localization as in a normal material. In experimental work [81], magnetoresistance due to weak localization has varied from sample to sample likely due to the fabrication processes affecting inter-valley scattering rates in each sample. Theory [83] and experiments [81] do agree on universal conductance fluctuations at high carrier densities [13].

Apart from its many exciting experimentally verified qualities, graphene could present viable means of testing two of the QED effects unobservable in particle physics, namely the Klein paradox and *zitterbewegung*. Klein paradox is the seeming ability of relativistic electrons to escape from the pull of an atomic nucleus by simply tunnelling out of its potential well. A graphene nanoribbon with gates attached to tune the potential barrier could be used to implement such a tunnelling experiment [65]. *Zitterbewegung* or "jittery motion" is observed for relativistic electrons as a result of the interference that occurs when the energy of a single wavepacket is split between electron and positron energy states. This effect may be partly or wholly responsible for the finite conductivity seen in ballistic devices [66], [73]. It may be possible to study this effect by directly imaging Dirac quasiparticle trajectories [84], [85]. Here graphene, with its electronic states directly accessible for scanning probes on the surface, is uniquely suited as a basis for constructing such an experiment. By bending a graphene sheet under observation, QED could also be studied in curved space. This is of particular interest to cosmological studies [13], [86].

To perform electrical measurements on the finished GPnC devices, we need a contact between the graphene sheet and a metal wire leading from the sample out to the macro-world. The contact resistance R_C is obtained from the Landauer-Buttiker linear response theory as the inverse of conductance

$$G = R_C^{-1} = \frac{2q^2}{h} \int -T(E) \frac{\partial f(E,T)}{\partial E}, \tag{14}$$

where q is the elementary charge, h is Planck's constant, $T(E)$ is the transmission coefficient, and $f(E,T)$ is the Fermi-Dirac function. Usually, contact resistance between graphene and metal contributes the majority of resistance when measuring a graphene sample [87]–[89].

2.3.3 Electron-Phonon Coupling in Graphene

In general, there are two mechanisms responsible for heat dissipation in thin film devices connected to metal electrodes. Joule heating due to externally applied voltage bias generates a gas of hot electrons in the graphene. Heat is then transferred from this hot gas of electrons to the crystal lattice via electron-phonon scattering. Diffusion is in turn responsible for transferring heat from the electron gas to the metal contacts, where it is dissipated to the environment. For a disordered graphene device, heat dissipation can be dominated by electron-phonon scattering [90].

When a graphene device is free of defects and operating well below the Bloch-Gruneisen temperature [91]

$$T_{\mathrm{BG}} = 2s\frac{\sqrt{\pi n}}{k_B}, \tag{15}$$

where $s = 2 \times 10^4\,\mathrm{m\,s^{-1}}$ is the average speed of sound in graphene, and n is the carrier density, the cooling power is given by

$$P = A\Sigma_1(T^4 - T_0^4), \tag{16}$$

where T and T_0 are the temperatures of the electron gas and the crystal lattice respectively, and A is the area of the graphene sheet [92]. Here, the electron-phonon coupling constant (EPCC) is of the form

$$\Sigma_1 = \frac{\pi^2 D^2 |E_F| k_B^4}{15\rho_M \hbar^5 v_F^3 s^3}, \tag{17}$$

where $E_F = \hbar v_F \sqrt{\pi n}$ is the Fermi energy, v_F the Fermi velocity, D the deformation potential of graphene and ρ_M the mass density of graphene [92].

On the other hand, for a disordered graphene device, the cooling power becomes

$$P = A\Sigma_2(T^3 - T_0^3), \tag{18}$$

where EPCC is in turn

$$\Sigma_2 = \frac{2\zeta(3)D^2|E_F|k_B^3}{\pi^2\rho_M\hbar^4 v_F^3 s^2 l}, \tag{19}$$

$\zeta(3) \approx 1.2$ is the Riemann zeta function and l the mean free path [92].

2.3.4 Diffusion Cooling Model (DCM)

For the diffusive cooling mechanism, we model the electrical conductivity of graphene according to the Wiedemann-Franz law

$$\kappa = \mathcal{L}\sigma(T)T, \tag{20}$$

where $\mathcal{L} = \pi^2 k_B^2/(3e^2) = 2.44 \times 10^{-8}\,\mathrm{W\,\Omega\,K^{-2}}$ is the Lorentz number and $\sigma(T)$ is the temperature dependent conductivity [93]. This model accounts for the transport of heat from graphene into the metal-contacts. The temperature dependent conductivity has been shown experimentally [93] to obey a logarithmic equation in the range $T = 0.2\,\mathrm{K}$ to $50\,\mathrm{K}$

$$\sigma(T) = \sigma_0 + \sigma_1 \ln\left(\frac{T}{1\,\mathrm{K}}\right). \tag{21}$$

For fitting the differential conductance measurements in section 4.3 we will use a a slightly altered form of equation 21, such that the conductance is

$$G = \left(G_0 + G_1 \ln\left(\frac{T}{1\,\mathrm{K}}\right)\right) G_Q, \tag{22}$$

where G_0 and G_1 are dimensioneless parameters and $G_Q = e^2/h \approx 3.874 \times 10^{-5}\,\Omega^{-1}$ is half the conductance quantum.

If diffusion cooling dominates over electron cooling in graphene at low temperatures, we can use the Wiedemann-Franz law to write the one-dimensional heat balance equation inside the graphene sheet as

$$\frac{I_{\mathrm{dc}}^2 + I_{\mathrm{ac}}^2}{W^2\sigma(T)} + \frac{\partial}{\partial x}\left(\kappa(T)\frac{\partial T}{\partial x}\right) = 0, \tag{23}$$

where I_{DC} is the current due to the externally applied voltage bias, I_{ac} the AC current induced perpendicular to the current flow by a possible source of external radiation, W the width of the graphene sheet, and x the coordinate in a direction parallel to the current flow [93]. The heat balance equation above can be solved for Dirichlet

boundary conditions

$$T_0 = T(-\frac{L}{2}) = T(\frac{L}{2}), \tag{24}$$

where T_0 is the temperature of the metal contacts located at $\pm L/2$ along the x-axis and L is the overall length of the graphene sheet [93].

The I/V curve for a graphene device of the above description can then be derived as [93]

$$I(V) = G(T_0)V = G_1 V \left(\frac{\sqrt{1+u^2}}{u} \ln(\sqrt{1+u^2} + u) - 1 \right), \tag{25}$$

where $G(T_0) = \sigma(T_0)W/L$ is the conductance of the device at zero voltage bias and base temperature T_0 with no external radiation applied, $G_1 = \sigma_1 W/L$, and u is by definition

$$u = \frac{V}{V_T}\sqrt{1 + \frac{I_{\text{ac}}^2}{I^2}} = \frac{1}{V_T}\sqrt{V^2 + \frac{V}{I}P_{\text{ac}}}. \tag{26}$$

In the above expression, V_T is the characteristic thermal voltage [93]

$$V_T = 2\sqrt{\mathcal{L}}T_0 = \frac{2\pi}{\sqrt{3}}\frac{k_B T_0}{e}. \tag{27}$$

2.3.5 Applications for Graphene

Graphene looks to have potentially innumerable applications, but let us start from perhaps the most urgent one, a potential replacement for silicon as the basis of current and future electronics. Out of the qualities discussed before, the intrinsically high charge carrier mobility as well as graphene's ability to maintain it as such in spite of ambient electric fields or chemical doping of the material itself [94]. Specifically for transistors, the large Fermi velocity and lack of a Schottky barrier [9] in graphene may translate to faster switching time and therefore higher clock speeds. Devices operating at THz frequencies could become achievable with graphene-based components [13].

In its free state, graphene maintains a zero semiconductor gap at the neutrality point, making it unusable for some current electronics engineering paradigms. Semiconductor gaps can still be artificially introduced into mono- and bilayer graphene via lateral superlattice potential, and by applying a gate potential respectively. Research suggests that a band gap will form into single-layer graphene grown epitaxially on top of a crystalline substrate with a lattice structure matching that of graphene, such as boron nitride or silicon carbide [13], [58], [59], [95]–[97].

Compared with other semiconductors, the energy gap in graphene due to confinement perpendicular to current flow (ribbon geometry) is relatively large thanks to its large Fermi velocity and linear energy dispersion [98]–[100]. This translates to devices designed to operate at room temperature requiring graphene nanoribbons of approximately 10 nm in width. Fortunately, these feature sizes are already achievable with current lithographic processes in use in the semiconductor industry, and applying the same workflows to graphene that have already been proven for silicon processing should significantly speed up development. Still a further hurdle is to develop a process to produce graphene nanoribbons with uniform edges. With irregular edges, sample dependent conductance becomes a problem for graphene in short conductive channels [98]–[100]. Irregular edges on long conductive graphene channels may instead lead to additional scattering effectively ruining ballistic transport. As zigzag and armchair edges in graphene have distinct chemical reactivity, it might be possible to develop an anisotropic etching technique to guarantee uniform edges [13].

Due to its excellent conductivity, graphene is well suited to serve the role of the conductive channel in a field effect-transistor (FET) architecture. This high conductivity is a double-edged sword, however. While excellent from the point of view of energy efficiency in the ON-state of a transistor, a pure graphene sheet has a harder time producing an OFF-state with a sufficiently high resistance. Innovative changes in the design geometry can get around this, such as using two parallel sheets of graphene acting as the source and drain respectively on an oxidized silicon substrate. As this arrangement lacks an actual conductive channel, current is instead carried parallel to the graphene edges by electrons tunnelling across the barrier [61], [101].

While simply substituting graphene for silicon with current design paradigms is the most readily achievable solution, graphene can also offer a way to evolve from the current field-effect transistor into a genuine single electron transistor (SET). This is made possible by graphene's exceptional stability and mechanical strength, allowing a sheet to be patterned directly with SETs and all the necessary circuitry to support them. While the SET architecture is maturing fast [102], [103], the problem thus far has been the inability of traditional materials such as silicon to remain stable down to the sizes required [13].

Yet another way of incorporating graphene into electronics is through its use in organic field effect transistors (OFETs). While a traditional OFET consists of a

pentacene conductive channel and a gold gate, the gate can be readily replaced with graphene [61], [104].

Whichever avenue of approach is selected, however, these wondrous new devices will not progress beyond prototyping and eventually into the hands of consumers if the dual problems of scalable production and reproducible feature size pushing single nanometers can not be effectively solved. As of now, epitaxial CVD growth of graphene on a metal substrate shows the greatest promise toward industrial applications [13], [59], [97].

In the modern world, especially in the field of electronics, we can consistently expect a high fraction of total energy used to be dissipated as waste heat. Thermoelectric conversion refers to the process of directly converting this waste heat into electricity and is sure to become a widely explored avenue for mitigating energy losses and protecting temperature sensitive devices. The efficiency of this process in a material is measured by the dimensionless quantity ZT, defined as

$$ZT = S^2 \frac{\sigma}{k} T, \tag{28}$$

where S is the Seebeck coefficient, σ is the electrical conductivity, T is the absolute temperature and k is the thermal conductivity. Increasing either S or $\frac{\sigma}{k}$ for a material will lead to an increase in the ZT value, but this has been difficult to achieve due to the two parameters being coupled [105]–[107]. Where bulk graphene has a relatively low ZT value of 1×10^{-4} to 1×10^{-3}, fabricating graphene into suspended nanoribbons of approximately 250 nm in length and 40 nm in width has been shown to enhance σ/k-ratio by up to 2 orders of magnitude and also increase the Seebeck coefficient several times over, resulting in a ZT value of around 0.1 [108].

Apart from electronics, graphene could see greater adoption in the production of various composite materials, such as conductive plastics. Battery technology could also see the adoption of cheaply produced graphene powder to enhance the performance. Graphene powder may also be able to enhance the emission qualities for displays [17].

Being able to absorb large quantities of hydrogen [109], [110], graphene could become a vital part of new infrastructure if the switch to hydrogen economy is ever made. In fact, monolayer graphene has the highest surface area per mass of any of the currently known materials [61]. The stored hydrogen can be released from the

few-layer graphene by heating it up to around 500 °C, making for a relatively simple and reusable way to store hydrogen [61], [110].

While not photovoltaic as such, graphene can nonetheless play an important role in solar cells, as an absorbing material could potentially be sandwiched between graphene sheets and the two materials oppositely doped to place the absorber in an electric field and to increase the conductivity of the cell. In this role, graphene can offer increased rigidity to the cell while being transparent to allow for applications such as photovoltaic windows [61].

Another field where transparent electrodes are in demand is the touch-screen market, where indium tin oxide (ITO) is traditionally used [111]. However indium as a rare metal is in ever shorter supply, and prices for such devices are expected to rise. If a commercially viable way to cheaply produce large quantities of graphene can be developed, it could find a place as a more flexible material alternative to ITO. Few-layer stacked graphene on top of polyethylene terephthalate (PET) can produce a flexible conductor with up to 90% optical transmission [60], [61].

Yeat another potential application for graphene is in supercapacitors. Here, cheaper chemically exfoliated graphene can be used [112], [113]. These sorts of devices can compete with current nickel metal hybride batteries in terms of energy density (85.6 $\mathrm{W\,h\,kg^{-1}}$ at room temperature and 136 $\mathrm{W\,h\,kg^{-1}}$ at 80 °C with 1 $\mathrm{A\,g^{-1}}$ current density), and offer a noticeable improvement in charging/discharging times down to a minutes or even seconds [113]. A commercially scalable process based on microwave heating induced exfoliation of graphite oxide has also been developed with a projected 75 $\mathrm{kW\,kg^{-1}}$ power density for a finished supercapacitor device [61], [114].

Not only supercapacitors, but traditional lithium-ion batteries can also see an improvement in efficiency from incorporating graphene. Using the same process of intercalation described earlier, a cell made of $LiCoO_2$ and graphene can have Li ions reversibly stored between graphene layers. The charge capacity of such a device is dependent on the amount of Li ions that can be accommodated in the graphene, and the charge rate depends on the ease at which ions can move in and out of the intercalated sites. Combining the common graphite intercalation compound C_6Li with graphene produces a charge capacity of 372 $\mathrm{mA\,h\,g^{-1}}$. As an alternative to this, different anode materials such as pure crystalline graphite (320 $\mathrm{mA\,h\,g^{-1}}$), graphene nanosheets 6 to 15 layers thick (540 $\mathrm{mA\,h\,g^{-1}}$) can be used [115]. The

performance of graphene nanosheets can further be improved by introducing carbon nanotubes or fullerenes to the structure, resulting in significantly higher charge capacities at $730\,\mathrm{mA\,h\,g^{-1}}$ and $784\,\mathrm{mA\,h\,g^{-1}}$ respectively [115]. In general, increasing the separation between carbon layers allows for grater accommodation of Li ions into the structure [61].

As a transparent conductor, graphene is also suited for use in the construction of LEDs. Both organic [116] and inorganic [117] construction for LEDs incorporating graphene has been demonstrated. This could pave the way for graphene supplanting ITO as the dominant material used for LED back-lit displays as they continue to become more common. Due to its flexibility, graphene is also uniquely suited for flexible transparent displays for use in wearable electronics [61].

Table 1. A general overview of the fabrication steps and equipment used. The whole process consists roughly of 3 subsequent EBL runs, separated here by the horizontal lines.

Step	**Equipment**
Spin resist + copolymer	PMMA spinner
Pattern markers	SEM
Develop resist	Fume hood
O_2 plasma etch	RIE
Evaporate Au + Ti	UHV evaporator
Lift-off	Fume hood
Transfer graphene	Fume hood
Strip resist	Fume hood
Bake graphene	Hot plate
Spin resist	PMMA spinner
Pattern PnC and paths	SEM
Develop resist	Fume hood
O_2 plasma clean	RIE
Strip resist	Fume hood
Spin resist + copolymer	PMMA spinner
Pattern pads and leads	SEM
Develop resist	Fume hood
O_2 plasma etch	RIE
Evaporate Au + Ti	UHV evaporator
Lift-off	Fume hood

3 Methods and Equipment

This section goes over the design and fabrication of the phononic crystals step by step. Note that what is presented here is a general overview of the steps involved while the following sections outline some of the changes that were implemented in an effort to improve the quality of the produced GPnCs. Table 1 lists all the steps of the fabrication process and the equipment used. What follows is a more in depth look at each of the individual steps and the various challenges that can arise in the course of fabrication.

3.1 Sample design

Before fabrication can begin, the 2D design geometry of the finished sample is designed and implemented with Raith ELPHY Multibeam software. While the work in this thesis includes much iteration on the best parameters to be used, in general, all of the samples follow a unified design based on previous research by Jaakko Mastomäki. The design template is shown in Figure 3, and a closeup of the grid to be covered up by graphene in Figure 4, while Figure 5 shows the design of individual PnC devices with different filling factors. Markers of varying sizes allow the patterning of subsequent layers to be aligned with one another. The outer edges are encircled by larger pads that can be bonded to a dipstick sample stage and hence connected to external measurement apparatus. The pads in turn connect down to the actual GPnC via leads. Again, a single chip will have multiple devices to try out PnCs of varying lattice constants and hole diameters, and to account for the inevitable breaking of some devices during fabrication.

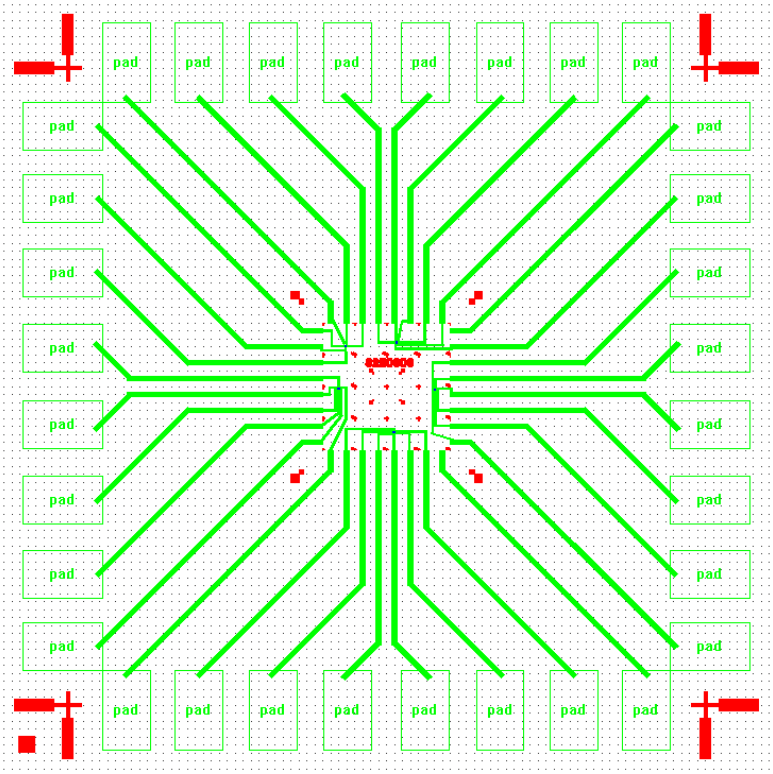


Figure 3. General design of the samples, see text above for details. The whole design is 5.5 mm by 5.5 mm in size, while the smaller central grid is 800 µm by 800 µm. The areas patterned on the first EBL run are shown in red, the second run in blue and the third run in green.

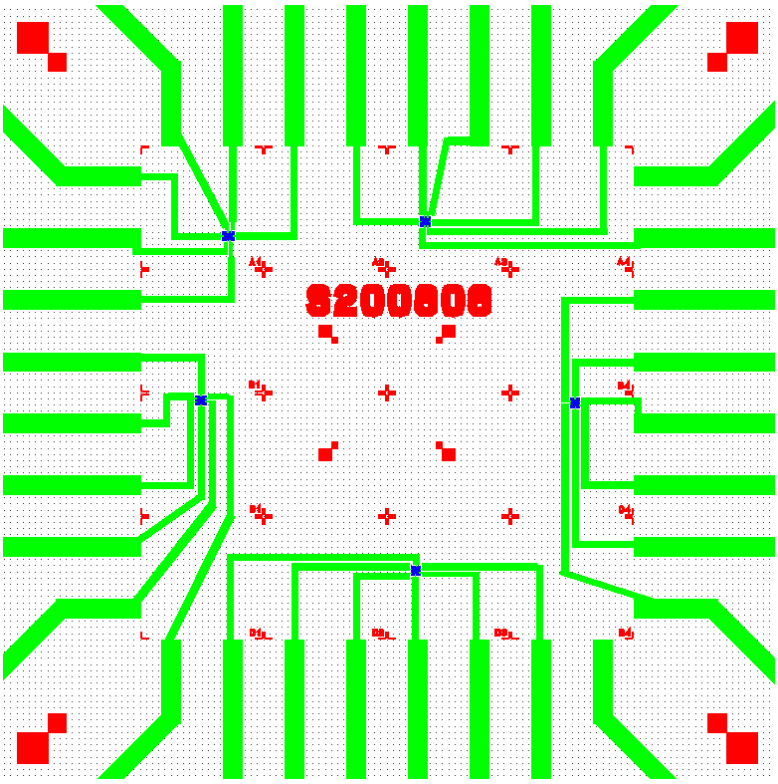
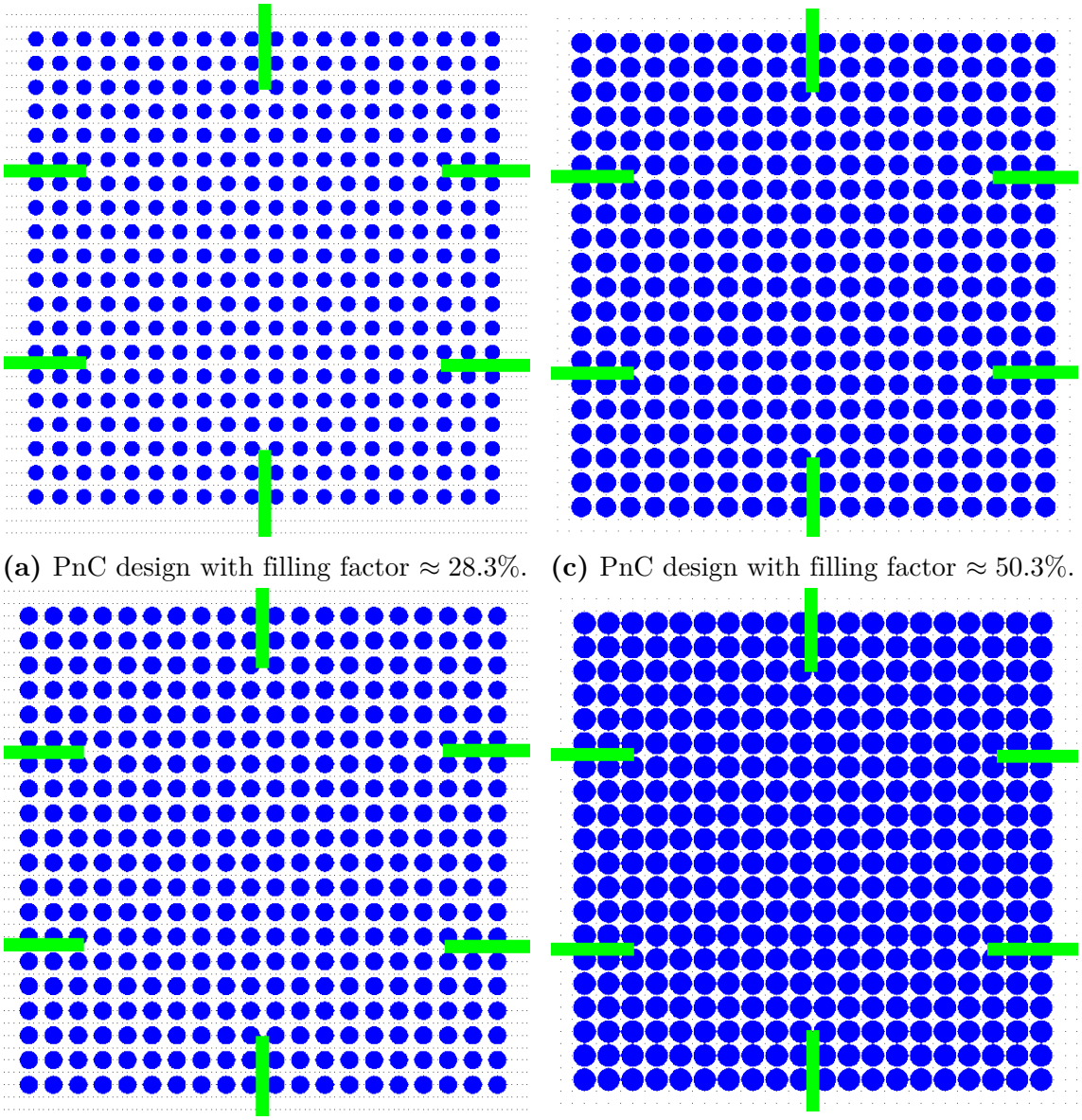


Figure 4. An example of the central grid on the samples. GPnC devices can be found in the square spaces where the thin leads converge. The placement and shape of the thin leads varies from sample to sample. Seen at the outer corners of the figure are square-shaped markers to help with alignment. The areas patterned on the first EBL run are shown in red, the second run in blue and the third run in green.



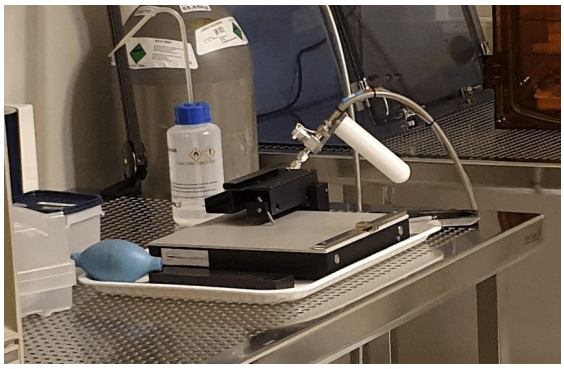
(a) PnC design with filling factor ≈ 28.3%.

(c) PnC design with filling factor ≈ 50.3%.

(b) PnC design with filling factor ≈ 38.5%.

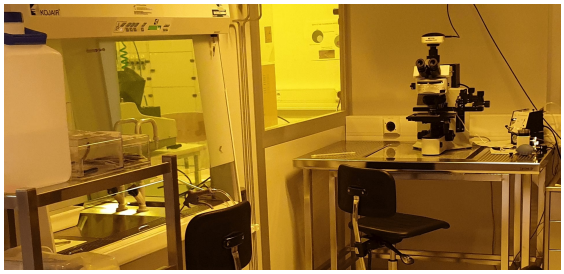
(d) PnC design with filling factor ≈ 63.6%.

Figure 5. PnC designs with different filling factors. The six thin fingers spaced around the perimeter connect to the measurement leads. The areas patterned on the second EBL run are shown in blue and the third run in green.

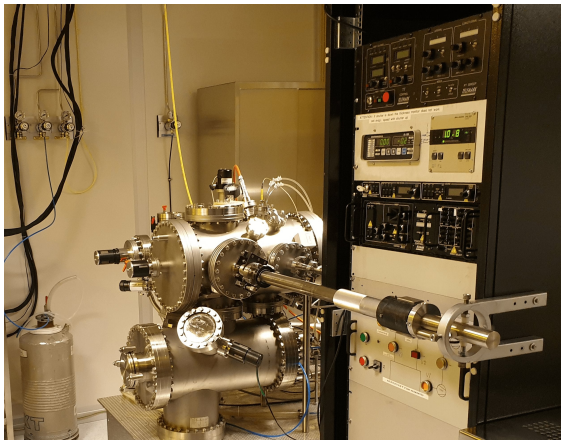


(a) Diamond-tipped silicon cutter.

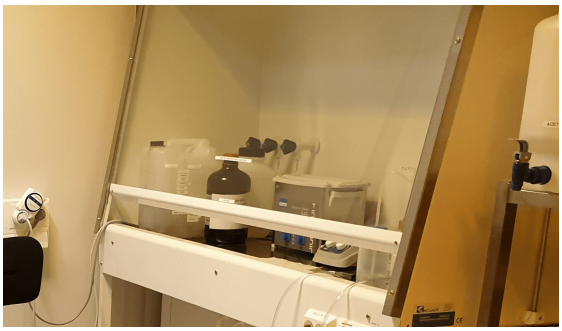
(b) Spinner cabinets and hotplates for baking resists.



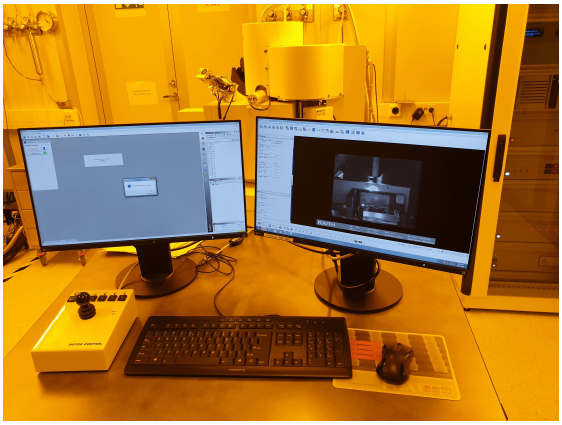
(c) Fume hood used for development and optical microscope.



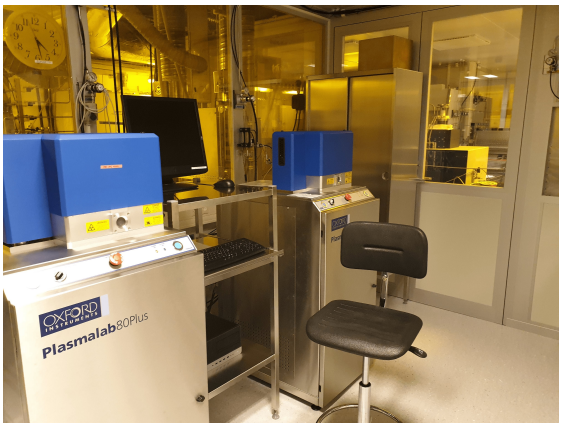
(d) Ultra-high vacuum evaporator.



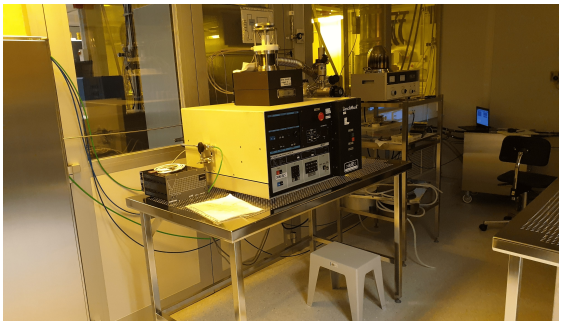
(e) Fume hood used for lift-off with sonicator.



(f) Scanning electron microscope.



(g) Reactive ion etcher (Oxford).



(h) Reactive ion etcher (AXIC).

Figure 6. The workstations used during fabrication.

3.2 First EBL run

Figure 6 shows the workstations in the cleanroom of the University of Jyväskylä Nanoscience Center used during the fabrication process. The fabrication of each sample started with a wafer of Si substrate with 300 nm of SiO_2 on top. Considering the design takes up an area of approximately 6 mm by 6 mm, chips of approximately 8 mm by 8 mm were cut from the wafer using a diamond-tipped cutter shown in Figure 6a. The new chips were cleaned in the lift-off cabinet with IPA wash at 23 °C, followed by an acetone wash at 56 °C, sonication for 5 min, IPA wash at 23 °C, and blow-drying with N_2 gas.

The resists and copolymer as well as the development solution used during this work were sourced from Allresist GmbH. In preparation for the first lift-off, a 400 nm thick layer of EL9 copolymer was spun at 2500 rpm in the PMMA spinner and baked at 160 °C for 2 min. This comparatively thick layer of additional material was to allow the solvent in the lift-off step to easily permeate the whole design. On top of the copolymer, a 200 nm thick layer of 950k PMMA A4 resist was spun at 4000 rpm and baked at 160 °C for 2 min.

Scanning electron microscope (SEM), shown in Figure 6f, was then used to pattern the big and small markers on the sample. To aid with focusing and write field alignment, a small collection of polystyrene spheres was deposited on each sample before loading by gently tapping on unoccupied space on the sample with a wooden tip containing the spheres. The sample holder for the SEM has room to comfortably secure three chips at a time, and this capacity was used whenever possible to process the samples in greater batches. In this work, the SEM working distance was always set to 6 mm, and an acceleration voltage of 20 kV and an area dose of 160 µC cm^{-2} was used when working with the A4 resist. For comparatively large features, such as the big markers in this step, a write field of 1000 µm, with a 120 µm aperture and 100× magnification was used, while smaller features, such as the small markers here, warrant the use of a smaller 200 µm write field with 30 µm aperture and 500× magnification.

Following the electron exposure, the sample was taken to be developed in the fume hood, shown in Figure 6c. The development was done by immersion in a 1:3 mixture of MIBK:IPA (Developer 1) for 40 s and subsequently halted by immersion in IPA bath. Samples were then blow-dried with N_2 and inspected for flaws under

optical microscope. This development step will be the same for subsequent runs, only the development time changes according to the resist used.

Next, the exposed areas were cleaned with O_2 plasma in Oxford Plasmalab 80 Plus RIE, as seen in Figure 6g, in preparation for metal evaporation. The recipe used (O2 soft clean PMMA) has the following parameters: time 15 s, RF power 20 W, gas flow 50 sccm.

The evaporation was done under ultra-high ($<5 \times 10^{-8}$ m) vacuum with the e-beam evaporator shown in Figure 6d. A 5 nm layer of Ti was evaporated first to act as a bond with the underlying SiO_2, with a further Au layer of 30 nm thickness on top for better visibility under subsequent resist layers. Titanium was evaporated at a rate of $0.03\,\mathrm{nm\,s^{-1}}$ and gold at $0.07\,\mathrm{nm\,s^{-1}}$.

Lift-off was performed in the fume hood shown in Figure 6e. The chip underwent the following steps: IPA wash at 23 °C, acetone wash at 23 °C, acetone wash at 56 °C where flaking of the excess metal was aided by circulating the acetone over the chip with a syringe, acetone wash at 23 °C to remove any remaining flakes. The result was inspected under an optical microscope, while keeping the chip immersed in acetone. If no excess metal remained, the chip was washed with IPA at 23 °C and blow dried with N_2, otherwise washing with acetone would continue.

The chip was now ready for graphene transfer. Both the CVD growth of graphene and the transfer onto the chip was done by Olli Rissanen. Following the transfer procedure, the graphene sheet now covers the small grid in the centre of the sample but a layer of PMMA resist remains on top of the sheet. This resist was removed with the same procedure as described earlier in lift-off. To aid the graphene adhering to the underlying layers, the sample was baked at 120 °C for 5 min. The sheet was then inspected under optical microscope for greater flaws in the graphene.

3.3 Second EBL run

After the first EBL run we are left with a sample with metallized markers and a graphene sheet covering the centre grid. Next, the actual PnC will be patterned and excess graphene removed to make way for the metallized leads in the third EBL run. As this run includes no lift-off, we can use a thinner layer of resist to hopefully produce finer features.

A 50 nm thick layer of 950k PMMA A2 resist was spun at 4000 rpm and baked at 160 °C for 2 min. The sample was then patterned in SEM using 10 kV acceleration

voltage and 40 µC cm^{-2} area dose to account for the thinner layer of more lightweight resist. 1000 µm write field with 120 µm aperture and 100× magnification was used for the larger areas, such as when creating trenches for the metallic leads to avoid any possible short-circuits forming between neighbouring leads in the subsequent metallization step. The patterning of the actual PnCs and the cleaning of excess graphene on the central grid was done with the smaller 200 µm write field, 30 µm aperture and 500× magnification. The patterned resist was developed in Developer 1 for 10 s and inspected under optical microscope, taking particular care to look for over-development, to which a thinner layer of light resist is particularly susceptible.

To transfer the pattern from the developed resist onto the graphene sheet, "O2 soft clean PMMA" was again used in RIE and the leftover resist is removed as per the procedure during lift-off.

3.4 Third EBL run

Following the second EBL run, we have a graphene sheet patterned with the PnCs and excess graphene removed. Now all that remains is to pattern the metallized contacts, so we can measure the behaviour of these devices.

A "sandwich" of 400 nm EL9 with 200 nm 950k PMMA A4 on top was spun with the PMMA spinner and baked for 2 min at 160 °C as in the first run. Next, the sample was patterned using a 20 kV acceleration voltage and 160 µC cm^{-2} area dose. The larger pads were done using 1000 µm write field, 120 µm aperture and 100× magnification, while the smaller leads interfacing with the PnCs over the central grid used 200 µm write field, 30 µm aperture and 500× magnification.

Resist was then developed for 40 s in Developer 1 and inspected for flaws under optical microscope, before the exposed areas were cleaned with RIE in preparation for metal evaporation, using the recipe "O2 extrasoft clean PMMA" with the parameters: time 10 s, RF power 15 W, gas flow 50 sccm. Evaporation with the UHV apparatus and lift-off was done the same as in the first run. The sample was now ready for rough resistance measurement with a multimeter to identify functioning devices, after which it was transferred out of the cleanroom for AFM imaging and IV-characterization at 4 K.

3.5 Recipe permutations and challenges

Due to a desire to find the limits of EBL in terms of the smallest GPnC that could be reliably fabricated with the individual holes remaining distinct, as well as changing availability of equipment in the cleanroom, many variations of the general recipe described in the previous sections 3.2, 3.3 and 3.4 was tried out.

While the first samples used 950k PMMA A4 resist both for the lift-off and PnC patterning runs, the smallest feature size achievable seemed dependent on the thickness of the resist layer. As the A4 spin curve dictates that the thinnest layer for such a resist is 200 nm when spun at 4000 rpm, a move to a process with the lighter A2 resist was necessary as finer features were desired. However, while the use of this lighter resist did indeed allow for thin layers down to 50 nm at 4000 rpm to be spun, the delicate nature of this layer soon became apparent. Namely, the acceleration voltage, area dose and development time used in SEM patterning for the thicker A4 resist turned out to greatly overexpose/overdevelop the intended design, resulting in rounded edges and blooming being visible under light microscope after development. These values were tuned from 20 kV, 160 µC cm^{-2} and 40 s down to 10 kV, 40 µC cm^{-2} and 20 s respectively. Through trial runs these parameters struck a balance avoiding blooming due to overexposure while still allowing for complete development of the exposed areas.

The Oxford Instruments RIE machine (Figure 6g) was temporarily unavailable during parts of this work so a comparable setup with Axic Benchmark RFX-600 PC-5100 (AXICRIE), shown in Figure 6h was used instead for some samples. To replicate the recipe "O2 soft clean PMMA" in this machine, power was set to $0.05 \times 600\,\mathrm{W} = 30\,\mathrm{W}$, O_2 gas flow to $0.35 \times 150\,\mathrm{sccm} = 52.5\,\mathrm{sccm}$ and time to 30 s. This was confirmed with SEM and AFM imaging to be sufficient to etch away graphene from the exposed areas in the pattern. An experiment was also conducted as to whether AXICRIE could be used at lower power to clean away some of the contamination observed on top of the graphene sheets. For this purpose, power was gradually lowered to $0.025 \times 600\,\mathrm{W} = 15\,\mathrm{W}$ where the plasma could still consistently ignite while keeping the other two parameters the same. The results of graphene cleaning with AXICRIE are discussed in section 4.2.

3.6 Imaging

While the fabrication process could be monitored with optical microscope (OM) and SEM imaging, both come with their own limitations, and we ultimately want to use AFM to inspect the finished product. For OM, the diffraction limit prevents us from directly observing structures smaller than approximately 400 nm. However, it is also the fastest and least destructive method and hence ideal for periodic monitoring of the quality of the developed pattern in the resist layer as well as locating greater tears and imperfections in the graphene sheet so that the actual GPnC devices might be patterned onto pristine areas. OM therefore served as a quick check at regular intervals to ensure no undue effort was given to areas where relatively large microscopic flaws popped up.

SEM offers a clear advantage in resolution over OM, down to tens of nm. However, because the technique requires vacuum to operate, it is also slower to rotate out samples to be inspected. The act of irradiating an image area with the electron beam also tends to leave behind a layer of deposited carbon contamination on graphene with each pass. Hence, a great quality image can be obtained from a site with GPnC in less time than with AFM, but that spot on the sample will be left dirty afterwards. Where SEM imaging was used for expediency's sake, care was taken to avoid irradiating the whole site for a possible GPnC device.

AFM imaging of the finished samples is done outside of the cleanroom with Bruker Dimension Icon AFM shown in Figure 7. The software associated with this machine comes with many preloaded measurement setups, and out of these Quantum Nanomechanical Mapping in Air, a tapping Mode derivative is used in this work to obtain high quality images of features down to sub nanometer scale with minimal damage to the sample. Adjustment of the measurement parameters is left up to the automation in the software, except for Peak Force Setpoint which is locked at 1 nN to protect the delicate graphene surface. Section 4.1 discusses the images obtained with AFM.

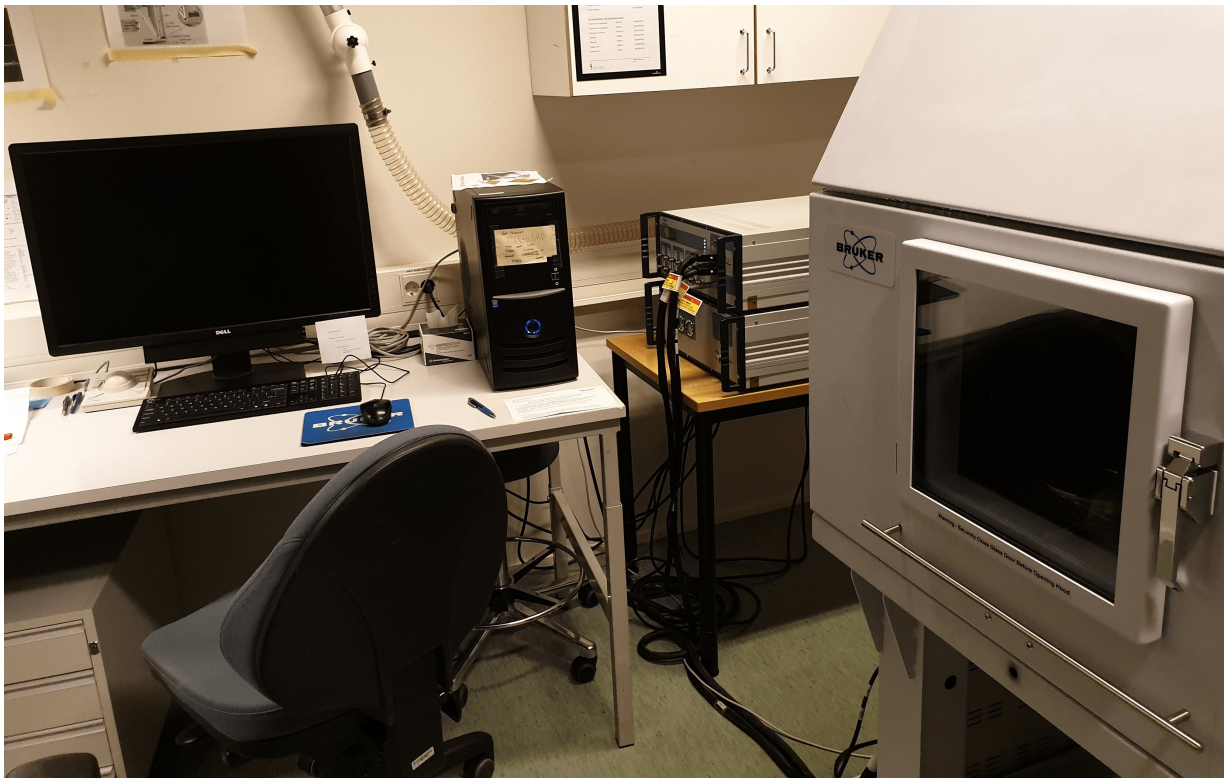


Figure 7. The AFM workstation.

Figure 8. Wirebonder used to join the chips to the dipstick sample holder.

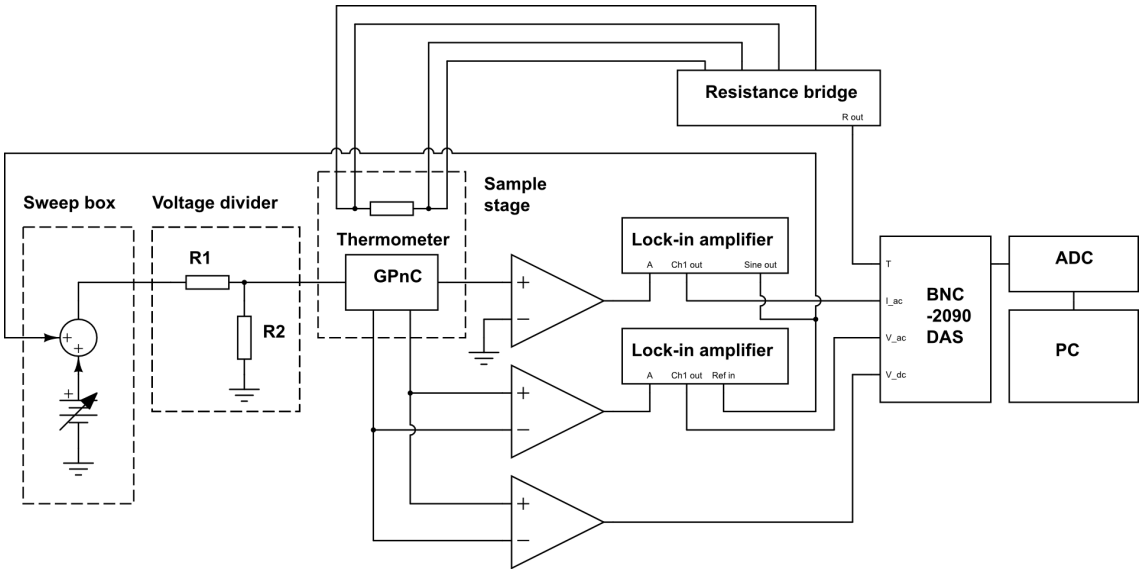


Figure 9. Circuit diagram of the measurement for four-probe setup. Voltage sweep is provided by a battery powered sweep box.

3.7 Differential Conductance Measurement at Low Temperatures

In preparation for the dipstick measurement, a chip with individual device resistance values in the single to tens of kΩ range was selected based on the rough measurements with a multimeter. This is about what we would expect for for a thin film device, and greater measured resistances pushing MΩs likely indicate a broken device. The best device on the chip was then bonded to the pads on a dipstick sample holder in such a way that four pads of the total six leads on the chip connected to two different pads on the sample holder, for redundancy and the possibility of doing two- and four-probe measurements. The wirebonder used for this is shown in Figure 8.

As a curiosity, it has also been demonstrated that graphene can be electrically characterised in atmosphere and vacuum with micro four-point probes when working with pieces of the order of 10 µm without the need to pattern permanent electrodes onto the device with E-beam lithography [118].

After a successful bonding, the sample holder is screwed onto the dipstick and the measurement leads are connected to the external measurement apparatus. The dipstick offers us access to a temperature range from 300 K down to 4.2 K. The differential conductance of the device was measured at different temperatures ranging from liquid nitrogen at 77 K to liquid helium at 4.2 K as a function of bias voltage.

Graphene displays the dependence of conductance on temperature strongly in this range. Furthermore, at temperatures above that of liquid nitrogen, thermal noise begins to overpower the signal extracted from the measurement apparatus. To this end, we can construct a four-probe measurement circuit, shown in Figure 9.

Four signals were collected from the measurement: temperature of the sample stage, current through the device as well as AC and DC voltage across the device. Using Figure 9 as reference, we can trace the paths of the electrical signals. The sweep box generates a triangular DC-voltage waveform to which an AC-signal is added in the form of the reference sine wave produced by one of the lock-in amplifiers. The voltage sweep is then passed through a voltage divider before going through the GPnC device. The voltage division ratio was tuned throughout the experiments to obtain sizable signals without damaging the GPnC devices, with the most common values used being 1/50 and 1/100. Current and AC-voltage signals are collected with a standard 4-probe setup and preamplified with DL Instruments 1211 current amplifier and 1201 voltage amplifier respectively before being sent to the lock-in amplifiers. The sweep DC voltage is also collected with a DL Instruments 1201 voltage amplifier operating in the DC-mode. The three signals are then recorded by National Instruments BNC-2090 Data Acquisition System (DAS) along with the sample stage temperature signal from RV-Elektroniikka Picowatt AV47 resistance bridge. The analog signals are finally converted to digital with National Instruments PXI-6251 Analog-to-Digital Converter (ADC), passed optically out of the Faraday cage and logged on a computer.

The resistance of the measurement leads at room temperature were approximately $67\,\Omega$, which is irrelevant when compared to the (tens) of kilo-ohms measured for the GPnC devices. The cooldown procedure consisted of gradually lowering the dipstick into the dewar, whereby the sample stage is first cooled by helium vapor and eventually fully submerged in liquid helium. After a settling period of approximately 20 minutes, the measurement at liquid helium temperature would be carried out. Further data points were acquired by gradually raising the dipstick closer to the top of the dewar, where it is cooled by progressively less dense helium vapors.

Figure 10. Dipstick measurement setup. The sample holder with the bonded chip resides in the cylinder at the bottom. The white dewar is filled with liquid helium, where the dipstick is immersed. The measurements were carried out in an electronically shielded Faraday cage.

4 Results and Discussion

This section will present data on both the quality of the finished GPnC devices, as seen through AFM imaging, and their electrical characterization at temperatures ranging from liquid nitrogen to liquid helium temperatures. While original goal for this project was to measure the thermal conductance of the GPnC devices at liquid helium temperatures, this will be left for further research due to time constraints.

4.1 Analysis of GPnC Quality

This contains examples of the kind of finished GPnCs one can expect to obtain with the process described in sections 3.2, 3.3 and 3.4. An overview of a typical site with a GPnC device as seen through OM is shown in Figure 11. Figure 12a shows a typical result using the thicker 950k PMMA A4 resist, while Figure 12b shows the same datapoints in 3D view. Figures 12c and 12d show the 2D and 3D representations of a different sample with larger lattice parameters and less contamination. Unless otherwise stated, all of the AFM images have been post-processed with the Flatten function of the z-direction, so the actual height of of the brightest peaks does not conform to the z-scale displayed. After trial and error using 50 nm increments in the fabrication process, it was determined that a neck width of 150 nm is desirable in the design to obtain a a uniform result where the holes remain distinct. The periodic arrangement of holes is shown here with the darker colored circles while the interweaving lighter-colored material is graphene.

These pictures also demonstrate the different kinds of contamination that can be expected on the graphene. Randomly distributed throughout the area are spherical and linear bumps, with width and height on the order of 1 to 10 nm. Of these, the spherical contamination is suspected to be stray carbon species adhered to the surface, and the linear defects are likely wrinkles and fold in the graphene sheet. Of particular note is the fact that we observe both kinds of contamination both on top of the graphene but also on the exposed silicon substrate. This suggests that while sufficient to etch away graphene, the RIE programs used are not powerful enough

to remove such contamination. As graphene growth is still a lengthy process and the material is in high demand at the laboratories, a primary concern in this work was to preserve even the thinnest resist layers and the graphene underneath and avoid wasting the material. This fear was motivated by the fact that 50 nm layer of 950k PMMA A2 resist shows a clear color change in optical microscope after being subjected to the RIE process step, indicative of the resist layer having lost some of its thickness. Further research can be conducted however to find the precise parameters for a given resist that allow for maximum removal of material only in the exposed regions.

The third distinct type of contamination is seen as the brightly colored ribbons encircling the edges of the holes in figures 12a and 12b. Curiously, this deposition seems to be concentrated mainly on one side of each hole, here the left edges specifically. Little explanation can be given for such behaviour except for the fact that graphene edges etched away by RIE processing offer greater adhesion than a flat graphene sheet. Hence, this type of contamination is likely PMMA residues from the etch mask.

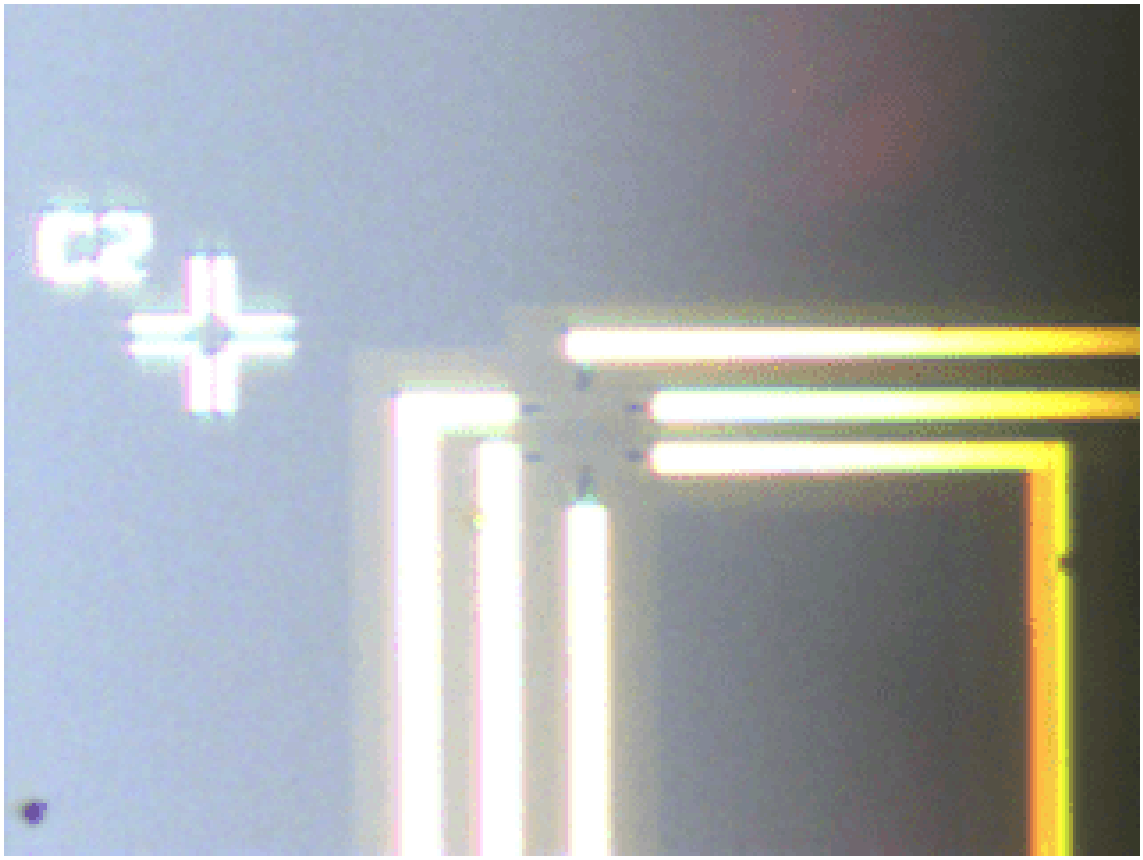
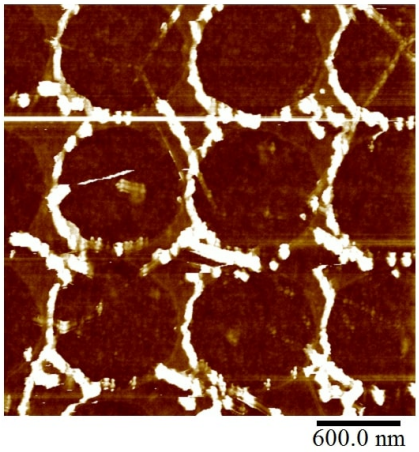
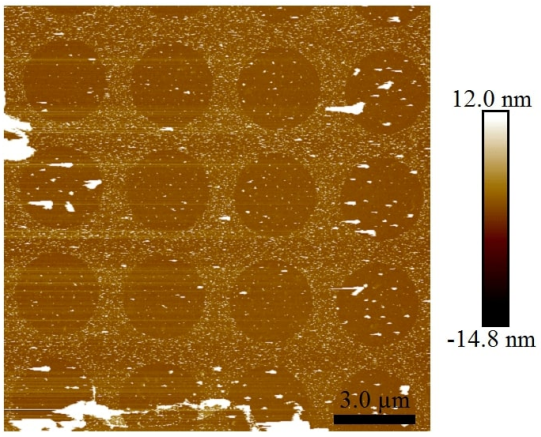


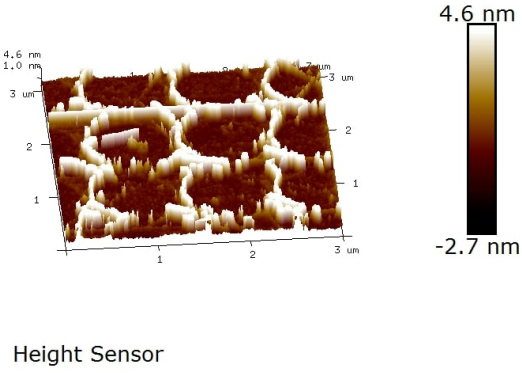
Figure 11. Optical microscope image of a finished GPnC device. The graphene sheet here is seen as a slightly darker shade of blue as opposed to the lighter coloring around the measurement leads, which denotes the exposed substrate.



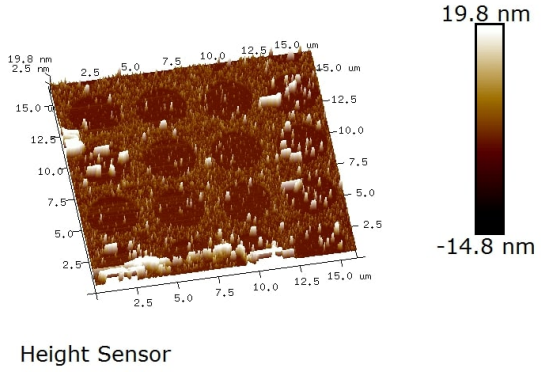
(a) 2D AFM image of a GPnC with $a = 1\,\mu\text{m}$ and $d = 850\,\text{nm}$.



(c) 2D AFM image of a GPnC with $a = 3.5\,\mu\text{m}$ and $d = 3\,\mu\text{m}$.

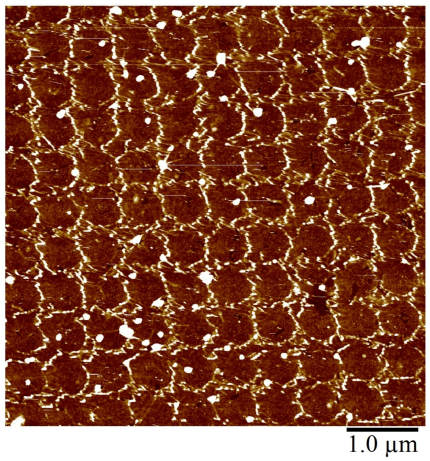


(b) 3D representation of the region in the image above.

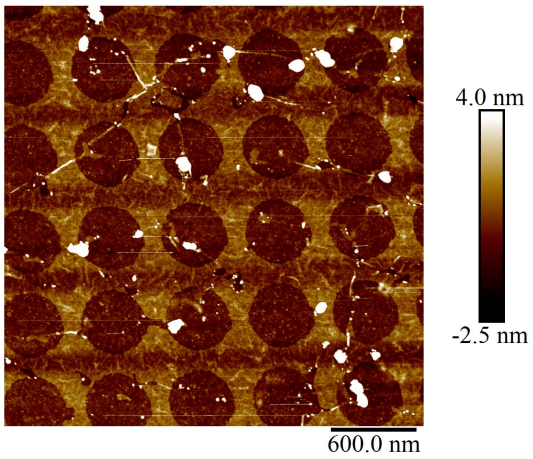


(d) 3D representation of the region in the image above.

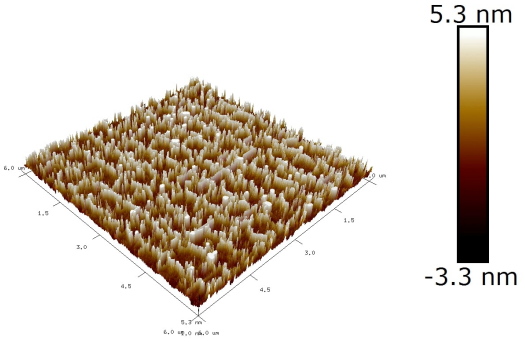
Figure 12. AFM images of GPnCs with different periodicities.



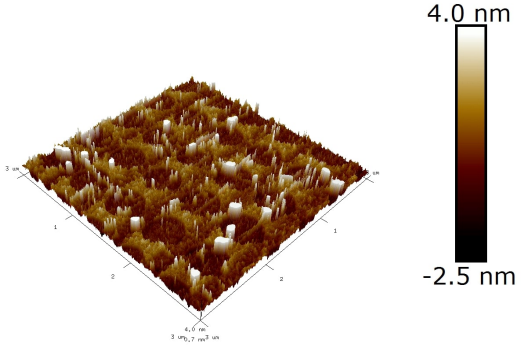
(a) 2D AFM image of a GPnC, $a = 600\,\text{nm}$ and $d = 420\,\text{nm}$, before AXICRIE cleaning.



(c) 2D AFM image of a GPnC, $a = 600\,\text{nm}$ and $d = 420\,\text{nm}$, after AXICRIE cleaning.



(b) 3D AFM image of a GPnC, $a = 600\,\text{nm}$ and $d = 420\,\text{nm}$, before AXICRIE cleaning.

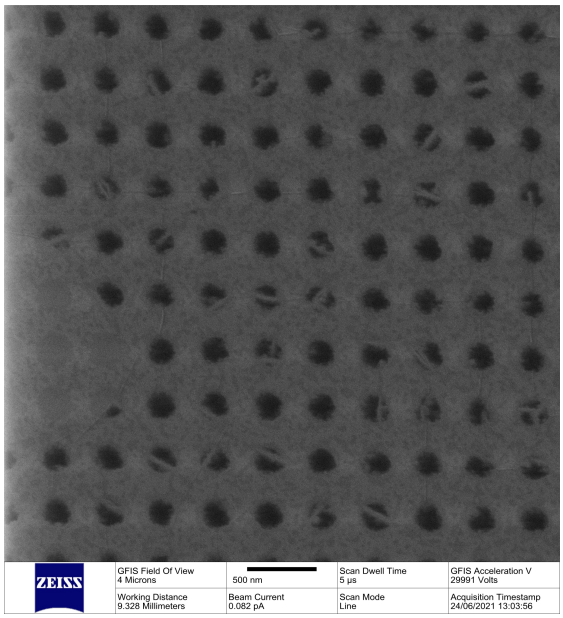


(d) 3D AFM image of a GPnC, $a = 600\,\text{nm}$ and $d = 420\,\text{nm}$, after AXICRIE cleaning.

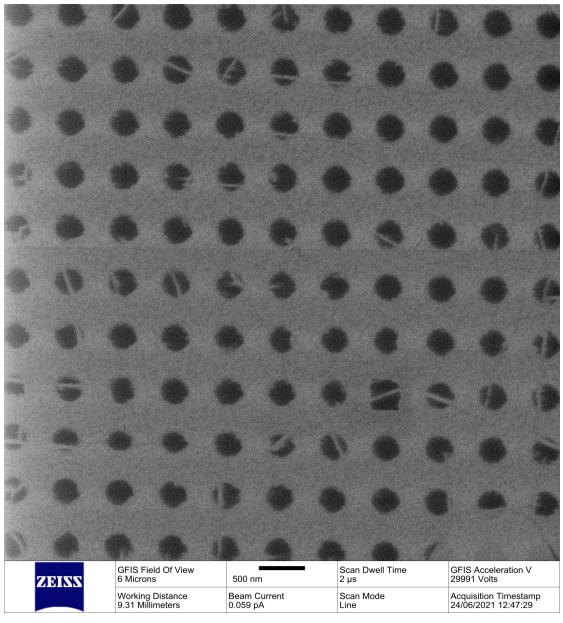
Figure 13. AFM images of GPnCs before and after cleaning with AXICRIE.

4.2 AXICRIE cleaning

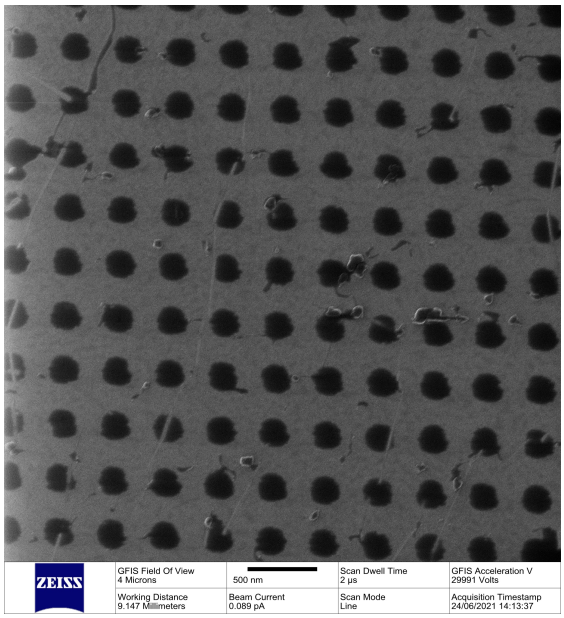
Figures 13 and 14 show AFM and HIM images respectively of GPnCs before and after cleaning with AXICRIE. From the images, we note that while there exists both types of contamination before and after cleaning, the procedure shows qualitative improvement of graphene cleanliness, especially when it comes to removing the spherical contamination. As the contamination is assumed to be mostly made of amorphous carbon, finding parameters to use with RIE that only attack the contamination presents a challenge. Further research is required into this procedure.



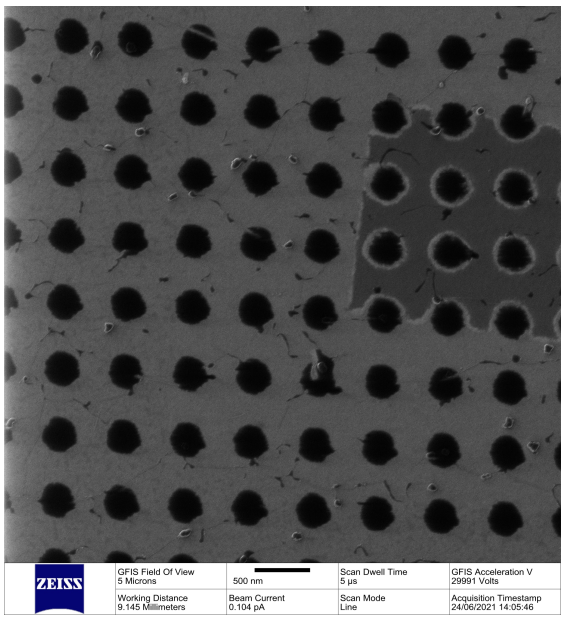
(a) HIM image of a GPnC, $a = 400\,\text{nm}$ and $d = 200\,\text{nm}$, before AXICRIE cleaning.



(b) HIM image of a GPnC, $a = 600\,\text{nm}$ and $d = 300\,\text{nm}$, before AXICRIE cleaning.



(c) HIM image of a GPnC, $a = 400\,\text{nm}$ and $d = 200\,\text{nm}$, after AXICRIE cleaning.



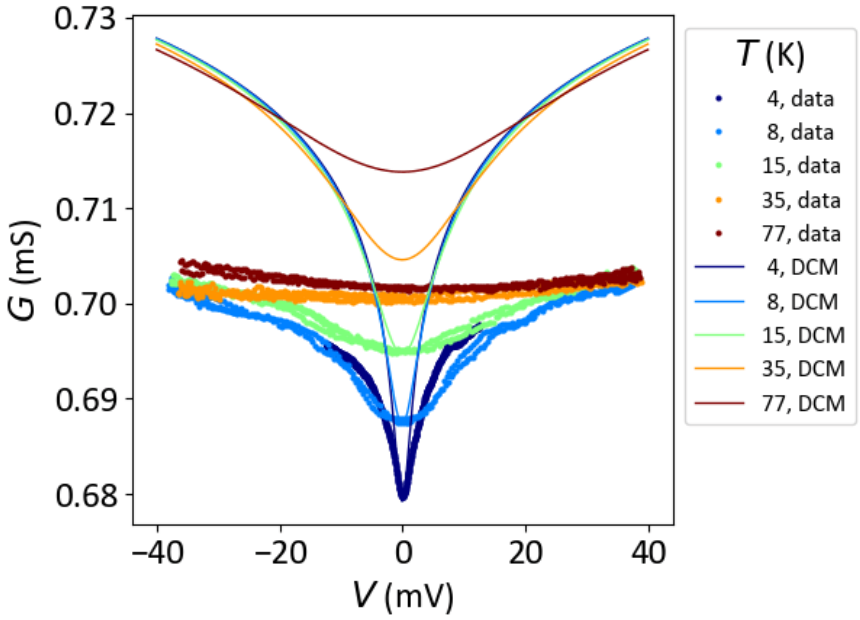
(d) HIM image of a GPnC, $a = 600\,\text{nm}$ and $d = 300\,\text{nm}$, after AXICRIE cleaning. The darker area in the upper-right quadrant of the image is likely due to previous exposure by SEM.

Figure 14. HIM images of GPnCs before and after cleaning with AXICRIE.

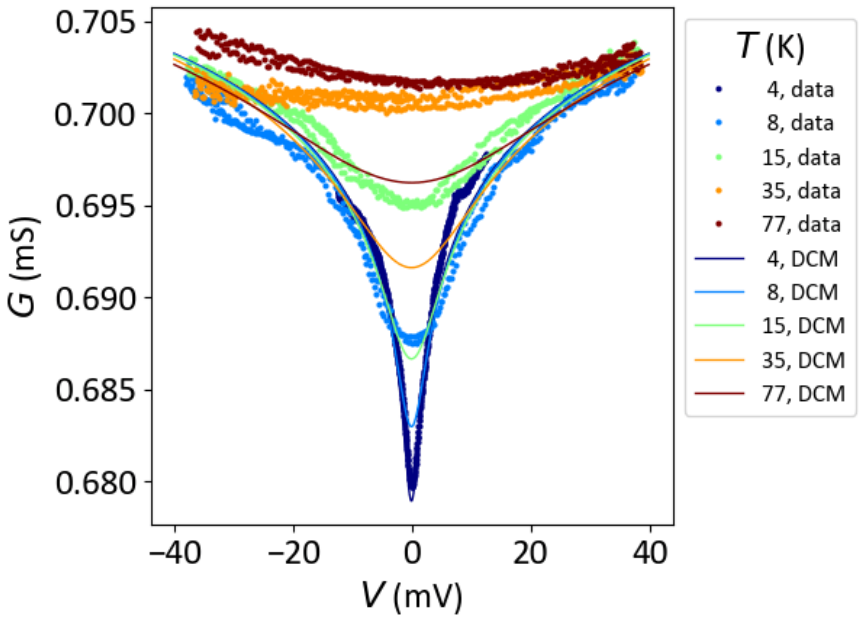
4.3 Analysis of Electrical Measurements

The differential conductance of a GPnC with $a = 1\,\mu\text{m}, d = 400\,\text{nm}$ device as a function of bias voltage is shown in Figure 15 at temperatures ranging from that of liquid nitrogen at 75 K to liquid helium at 4 K. Fitted to the data is the simple DCM model introduced in section 2.3.4 using 2 sets of parameters. We note that the differential conductance displays a significant decrease in value around zero bias voltage at the lowest temperatures, with the effect becoming less and less pronounced with higher bias voltage and increasing temperature. The effect is due to the relatively small heat capacity of graphene, so even a minute amount of current through the device, as induced by increasing voltage bias, leads to the system heating up. This combined with the fact that increasing temperature also increases the conductance of the graphene leads to the behaviour we observe in Figure 15. Hence, the actual conductance of a graphene device at the temperature of the surrounding helium bath can be observed with zero voltage bias [93]. We also see that the model tends to agree with experimental results better with decreasing temperature. Similar results are obtained for pristine graphene [93].

Figure 16 shows the conductance at zero voltage bias as a function of temperature with linear fitting according to DCM theory in Equation 22. We note that our model tends to agree well with experimental results up to a temperature of about 15 K, beyond which the results deviate noticeably from the linear fit. Considering, that the eventual aim of this research is to measure thermal conductivity of similar GPnC devices at temperatures below 4 K and the model has been shown to be valid down to 0.2 K [93], DCM model will likely remain relevant for those measurements as well.



(a) Differential conductance of a GPnC device as a function of bias voltage at different temperatures with fitting according to DCM theory, using equation 25, and parameters $G_0 = 17G_Q$ and $G_1 = 0.3G_Q$, extracted from the fit in Figure 16.



(b) Differential conductance of a GPnC device as a function of bias voltage at different temperatures with fitting according to DCM theory, using equation 25, and best fit parameters $G_0 = 17.2G_Q$ and $G_1 = 0.15G_Q$.

Figure 15. Differential conductance measurement results, fitted with DCM theory using 2 sets of parameters.

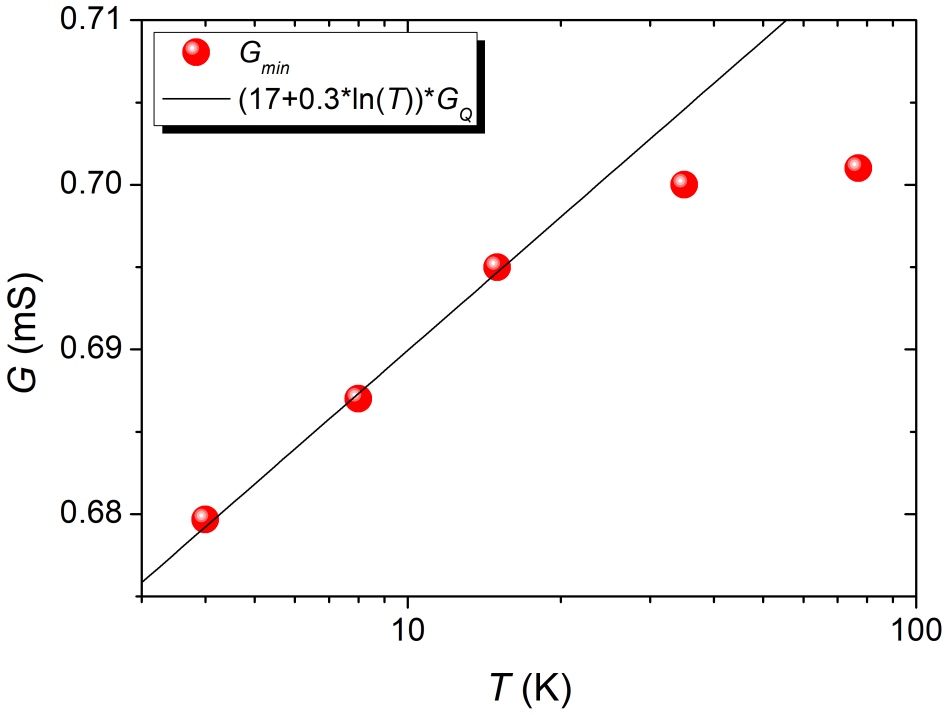


Figure 16. Conductance at zero bias as a function of temperature, with linear fitting according to equation 22. The values are extracted from Figure 15a.

In addition to differential conductance measurements at fixed temperatures, the behaviour of zero bias resistance/conductance of the GPnCs was also studied as a function of temperature for the whole temperature range. These results are plotted in Figures 17 and 18 respectively for a different sample than what was used for the differential conductance measurement. The parameters for this sample were $a = 400\,\text{nm}$,$d = 200\,\text{nm}$ We note that, with increasing temperature from 4 K to 75 K, the conductance of the device increases by about an order of magnitude.

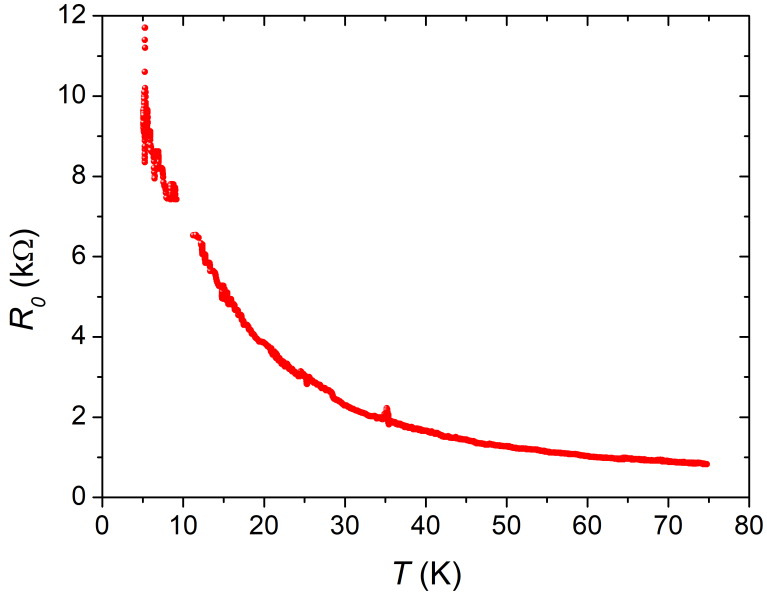


Figure 17. Resistance at zero bias as a function of temperature.

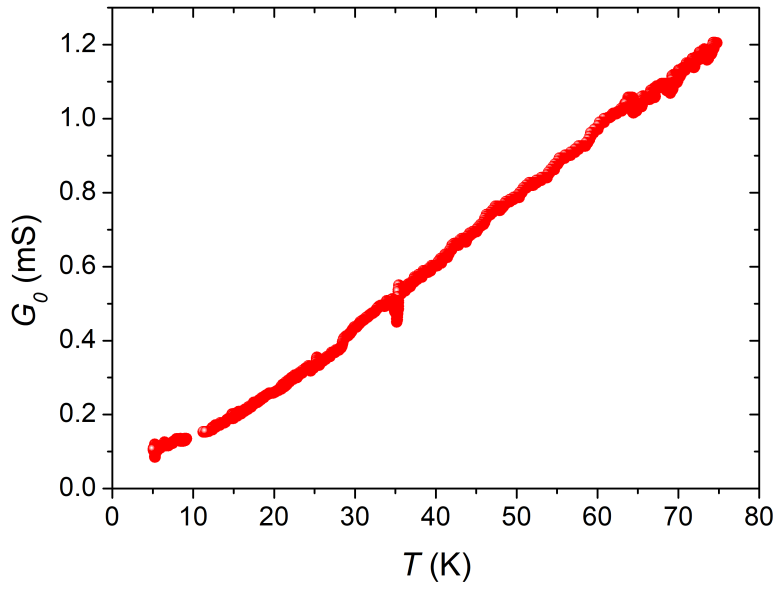


Figure 18. Conductance at zero bias as a function of temperature.

5 Conclusions

In this thesis work, an EBL based method for producing phononic crystals in graphene was developed. Various parameters from design feature size, resist thickness, exposure speed, area dose, development time and RIE power were optimized for two different PMMA resists and RIE machines to reliably fabricate graphene phononic crystals, with individual holes of diameter down to 120 nm. The resulting devices were imaged with AFM to obtain qualitative data as to the robustness of the fabrication method. Motivated by the fact that, depending on sample, large amounts of carbon or resist contamination was found to be present on the graphene sheets, a method for cleaning off contamination with low-power RIE treatment was also attempted. This showed some qualitative improvement in the cleanliness of the graphene surface when imaged with HIM and AFM. Further research is required to perfect such a method for use with future graphene device fabrication using a similar process as in this thesis work.

The GPnC devices were also electrically characterized at temperatures ranging from that of liquid nitrogen to liquid helium by differential conductance measurement with a dipstick. A distinct dip in differential conductance was observed for the devices at zero voltage bias. This effect became more pronounced at lower temperatures, confirming that the electrical properties of graphene are not significantly changed by the presence of a PnC. This presents the possibility of creating local thermometers on a GPnC device using the fabrication process described in this thesis. Yet further research is required to measure the thermal conductance of similar devices at liquid helium temperatures and below.

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