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Efficient techniques for fault detection and location of multiple controlled Toffoli-based reversible circuit

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Abstract
It is very important to detect and correct faults for ensuring the validity and reliability of these circuits. In this regard, a comparative study with related existing techniques is undertaken. Two techniques to achieve the testability of reversible circuits are introduced that have been improved in terms of quantum cost and fault coverage rate. Considering this aspect, the main focus of these techniques is on the efficient detection and location of faults with 100% accuracy. These techniques for fault detection in reversible circuit design, in addition to being able to produce the correct outputs, can also provide information for fault location that has already been done at a higher cost. Proposed approaches have been successfully tested for all types of SMGF, MMGF, PMGF, RGF, and SBF. In order to verify the functional correctness of the proposed scheme, it also has executed the testing over a reversible full adder circuit, and findings are checked. In the following, the proposed approach of reversible sequential circuits is presented for the first time so far. The cost metrics are evaluated for all the proposed designs and compared the estimated results against some existing design approaches of reversible circuits for better understanding.

Keywords Reversible circuit · Fault detection · Fault location · Test · Fault models · Cost metrics

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1 Introduction

Power dissipation and therewith heat generation is a serious problem for today's computer chips. One such technology that can address this challenge is reversible logic which is an alternative technology to design various digital circuits with almost zero power dissipation, whereby the function of reversible logic is performed faster with minimum power consumption requirements and reduced heat generation [1]. Hence, reversible logic has become a promising technology in the implementation of digital design [2].

One of the most important challenges of any future technology is high failure rates. Therefore, the design of reversible circuits should be considered fault detection and correction [3]. Overall, the concept of fault tolerance is very important in the development process of a system. Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some of its components. Fault tolerance is achieved through redundancy. A common approach to fault tolerance is hardware redundancy by replicating one or more physical components of the system. Fault detection and fault location are two important techniques in the testing of these circuits, which are realized with redundancy. These techniques involve detecting the presence of faults and finding the location of these faults [4].

Although, many works on the efficient detection of faults exist. Hence, to achieve a near-optimal solution, a review of fault models, test approaches, and cost metrics have been collected from the literature. This is done by providing low-cost and straightforward designs to derive in terms of the quantum costs and fault coverage rate compared to existing designs. This paper presents approaches for identifying all fault models in reversible circuits to neutralize the effect of the faults in the circuit. It generates the correct output, as well as identifies the location of faults. Moreover, the test of sequential reversible circuits is also considered in this paper.

This paper addresses three key issues:

- A fault detection and correction approach based on the complement of the circuit is presented.
- A fault detection approach is presented for reversible sequential circuits.
- A fault detection and correction approach based on generating a specification table is presented.

The paper is structured as follows. In the next section, the basic background is presented followed by Sect. 3, describing the related works and explaining existing fault detection and correction approaches. The two proposed techniques of detection and location of all faults in reversible circuits and a fault detection technique are proposed for reversible sequential circuits to identify all fault models are discussed in Sect. 4. The results are shown in Sect. 5, and finally, a brief conclusion is presented in Sect. 6 to provide a new perspective on fault detection and correction techniques in a reversible circuit.

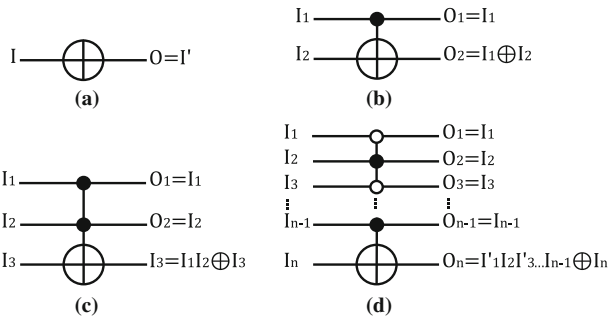


Fig. 1 Reversible gates in NCT gates family. **a** NOT gate, **b** CNOT or Feynman gate, **c** 3 × 3 Toffoli gate, and **d** n × n-Toffoli gate with multiple and negative control

2 Background

This section introduces the preliminaries on the quantum and reversible circuits and cost metrics used to evaluate the efficiency of reversible circuits. A brief review of fault tolerance and fault models in the reversible circuits is also summarized at the end of this section. In this section, an attempt is made to provide the required basic concepts to keep this paper self-contained.

2.1 Reversible circuits

In reversible circuits, inputs can be inferred from the outputs. These circuits contain equal numbers of inputs and outputs. In contrast, a reversible circuit can be generated with a cascade of reversible gates without fan-out branches and feedbacks [5, 6]. In reversible logic, loops and fanouts are not possible. For this reason, reversible logic performs computations and communications simultaneously. The reversible logic functions are implemented by the reversible gates. In other words, n-input and n-output of a reversible function $f(x_1, x_2, \ldots, x_n) \rightarrow y_1, y_2, \ldots, y_n$ is the reversible function that the equal number of inputs and number of outputs and one-to-one mapping between input vectors and output vectors [7, 8]. Reversible logic operations are lossless (N-to-N) operations, where it can uniquely derive any signal at the input end through backward operations on the signals at the output end only [9].

The two most widely used categories of reversible logic gates are the NCT and the SF gate family. The NCT gate family consists of NOT, CNOT, and Toffoli gates. Reversible gates in the NCT gate family are shown in Fig. 1 [10–12].

2.2 Quantum circuits

A quantum circuit is a sequence of quantum operations. Each operation is represented by a quantum gate. In 2017, IBM launched the IBM's QX project with the goal to provide access to quantum computers to conduct quantum experiments on 5-qubit and 16-qubit quantum computers. Available quantum computers in IBM's QX project work

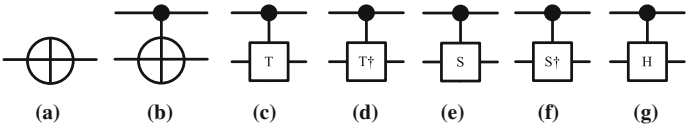


Fig. 2 Clifford+T quantum library. **a** NOT, **b** CNOT, **c** T, **d** T†, **e** S, **f** S†, and **g** H

Table 1 The quantum cost of NCT gate family

Size	Gate	QC
1	NOT	1
2	CNOT/2 × 2 Toffoli	1
3	3 × 3 Toffoli	5
4	4 × 4 Toffoli	13
5	5 × 5 Toffoli	29
n	n × n Toffoli	2^n-3

with the quantum gates from the Clifford+T library. Therefore, in order to implement well-known circuits in such architectures, they need to be mapped to Clifford+T gates. The Clifford+T library consists of the gates NOT, CNOT, H (Hadamard), S, S†, T, and T†. Figure 2 shows the gates of Clifford+T libraries [13, 14].

2.3 Cost metrics in reversible circuits

There are three major metrics to evaluate the efficiency of the reversible circuits. These metrics are quantum cost, ancilla inputs, and garbage outputs [15]. Definitions and a brief review of these metrics in the literature are as follows.

2.3.1 Quantum cost

The quantum cost (QC) is the most popular metric used to compare different reversible logic circuits. The quantum cost of a reversible circuit is the total number of quantum primitive gates, which are used to form an equivalent quantum circuit [16–19].

The quantum cost of 1 × 1 and 2 × 2 reversible logic gates is considered to be a unit cost. A 3 × 3 Toffoli gate and a 3 × 3 positive-controlled Fredkin gate can be implemented using 5 quantum primitive gates. So, the quantum cost for both is 5. The generalized Toffoli gate is implemented by $2^n - 3$ of 2 × 2 quantum gates. The quantum cost of these implementations is equal to $2^n - 3$ of 2 × 2 quantum gates [20, 21]. The quantum cost of the NCT gates family is shown in Table 1.

2.3.2 Ancilla input

The number of ancilla input bits is primarily considered as an optimization criterion as it is extremely difficult to realize a quantum computer with many qubits [22]. An ancilla input (AI) or constant input is required to retain the feature of a one-to-one mapping between input vectors and output vectors in the reversible circuit. Adding constant inputs is a basic technique to convert an irreversible function into a reversible circuit. Additional constant inputs to the reversible circuit may reduce the quantum cost [23].

2.3.3 Garbage output

In the synthesis of reversible functions, garbage output (GO) is neither the primary output nor required for future computation. So, all logic gates (except inverters) require garbage outputs and ancilla inputs to satisfy one-to-one mapping between inputs and outputs. The garbage outputs increase the information loss of a reversible circuit. Therefore, it is desired to decrease the number of garbage outputs [21, 24]. As the optimization of the garbage outputs may degrade the design in terms of the quantum cost, thus the quantum cost parameters are also considered for optimization with the optimization of the garbage outputs [22].

2.4 Cost metrics in quantum circuits

Apart from the above-mentioned cost metrics, three new cost metrics of Qubit Cost, T-count, and T-depth have been introduced, which are sometimes used to judge the design efficacy in quantum circuits.

2.4.1 Qubit cost

The total number of qubits required by a quantum circuit is an important performance measure. Quantum circuit performance is evaluated in terms of T-count and T-depth because the implementation costs of the T gate are significantly greater than the implementation costs of the other Clifford+T gates. Qubit cost is the total number of qubits required to design the quantum circuit [25].

2.4.2 T-count

The T-count of a Clifford+T circuit is the total number of T and T† gates in the circuit. The CNOT gate and the SWAP gate both have a T-count of 0, while the Toffoli gate has a T-count of 7 [25].

2.4.3 T-depth

Any number of primitive gates of Clifford+T quantum library that can be applied in parallel are considered as one logic level in Clifford+T circuit. The number of logical

levels is called T-depth. In other words, the depth of a quantum circuit is the number of slices, where each slice contains at least one quantum gate along the same vertical line [26]. The T-depth of a Clifford+T circuit is the number of T gate layers in the circuit that contains one or more T or T† gates, where quantum operations in any layer can be performed simultaneously.

The T-depth is less than or equal to the number of T or T† gates. The logical depth can be envisaging the execution time of a reversible circuit. The depth of a quantum circuit must be minimized in order to improve the circuit performance [26]. The CNOT gate and the SWAP gate both have a T-depth of 0. The Toffoli gate has a T-depth of 3 because the most T-gate layers encountered by any qubit in the Toffoli gate is 3 [25].

2.5 Test approaches

2.5.1 Offline test

In the offline test approach, the circuit is out of normal operation and can be tested by using test vectors. Therefore, a key element in offline testing for a given fault model is the calculation of the test vector set [4].

2.5.2 Online test

In online testing, the circuit is operating normally and detects faults. This may require adding a circuit. Therefore, the online test approach requires additional overhead to detect faults [27, 28].

2.6 Fault tolerance and fault models

Faults are a type of circuit defect which can occur due to a variety of reasons, such as a defect in the system, a defect in the system components, and a defect in the external environment. Functional abilities of a system long-lastingly or for a limited period of time, and termed as permanent and nonpermanent faults, respectively. Fault detection is essential to ensure the accuracy and reliability of reversible circuits. The concept of fault tolerance is to recover a system from a possible failure state. A fault-tolerant system should be able to produce the expected result even if there are faults by correcting or bypassing the faults [4].

Sometimes, there are physical defects in the manufacturing process of circuits. Therefore, it is necessary to check for such defects in the circuit and ensure the correct operation of the circuit. The existence of this type of defect has also been proven in reversible circuits. As a result, this technology needs to provide a solution to identify faults in the circuit. A fault model describes the types of faults that occur in a system and considers all the probabilities of faults in a circuit. The package of fault models consists of five different categories of faults: Stuck-at Fault (SAF), bridging fault (BF), missing gate fault (MGF), cell fault (CF), and partial missing gate fault (PMGF). Gate operations in reversible circuits are likely to be by means of pulses. SMGFs and MMGFs may occur in a reversible circuit for short, missing or mistuned gate pulses.

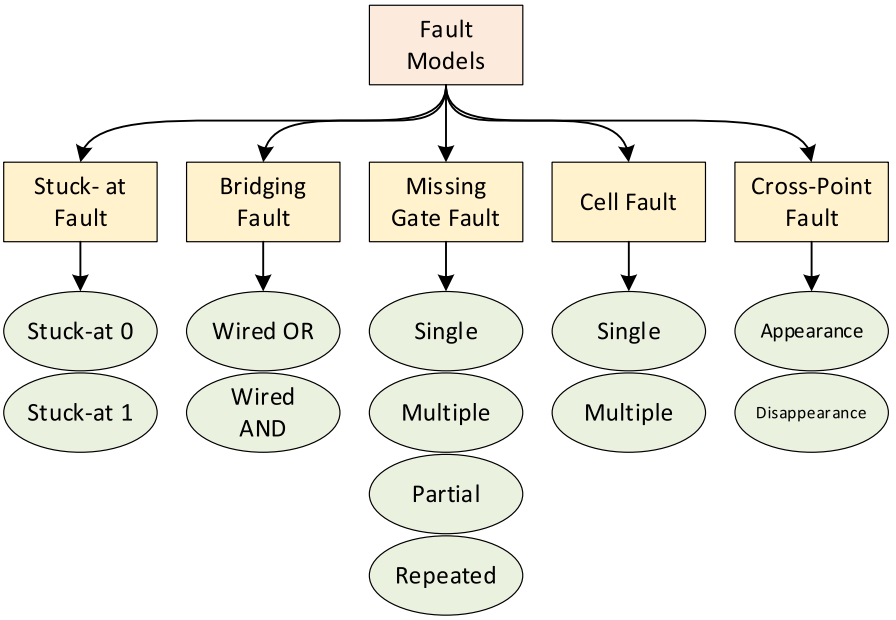


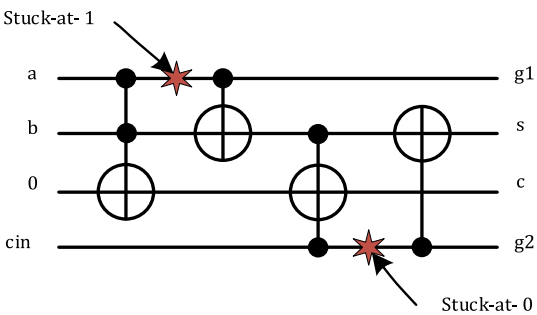
Fig. 3 The fault models in reversible circuits

RGFs may occur due to long or duplicated gate pulses, and PMGFs may occur due to partially mistuned gate pulses [29, 30]. Different fault models have been reported for reversible circuits. A summary of the models of the various faults in the reversible logic circuits is presented in [31] and that is shown in Fig. 3.

2.6.1 Stack-at fault model

This fault model causes one of the inputs or outputs to become a constant value of zero (stuck-at 0) or 1 (stuck-at 1) regardless of the value of the input or output line. For example, Fig. 4 shows a reversible circuit where a stuck-at 0 fault on the fourth line causes zero to be output on the g2 output, followed by a stuck-at 1 fault on the first line that causes 1 to be output on the g1 output [32, 33].

Fig. 4 The stuck-at fault model



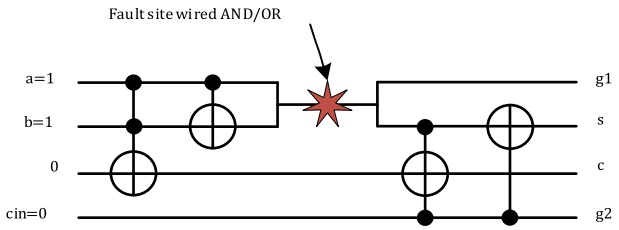


Fig. 5 The bridging fault model

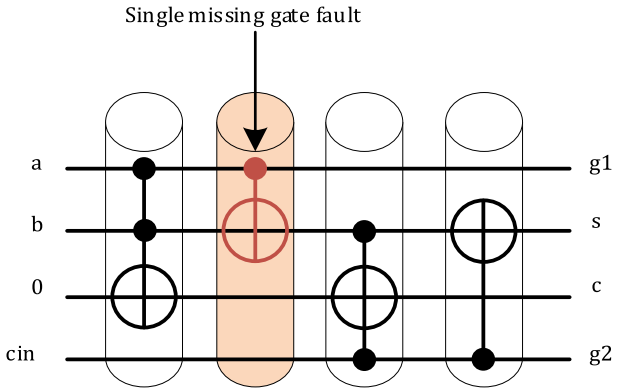


Fig. 6 The single missing gate fault model

2.6.2 Bridging fault model

The fault models occur when two or more adjacent wires are physically connected, similar to AND/OR connections, leading to malfunction. This fault model is shown in Fig. 5 [34].

2.6.3 Single missing gate fault model

The missing gate fault model occurs only when a K-CNOT gate is deactivated from the circuit. In other words, this deleted gate cannot perform the intended operation. This gate may produce an incorrect output. This fault model is shown in Fig. 6. If a = 1, b = 1, and cin = 0 to the inputs of the circuit, the correct output will be s = 0 and c = 1. If SMGF is considered as shown in the figure where there is no second CNOT gate due to the presence of SMGF in the circuit. The output can be s = 1 and c = 1. The behavior of this model shows the incorrect output of the circuit [31, 35].

2.6.4 Multiple missing gate fault model

The multiple missing gate fault model is very similar to the single missing gate fault model and eliminates two or more K-CNOT gates. An example of the two missing

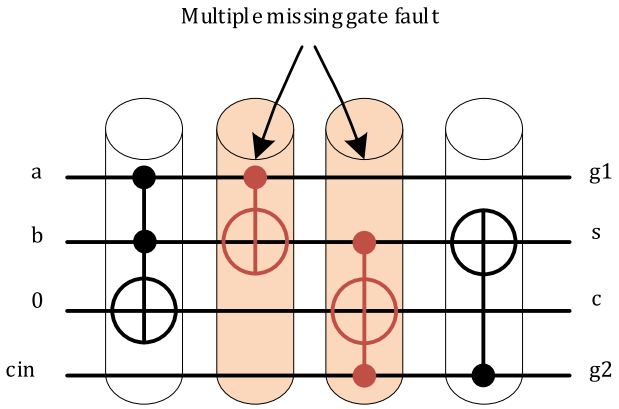


Fig. 7 The multiple missing gate fault model

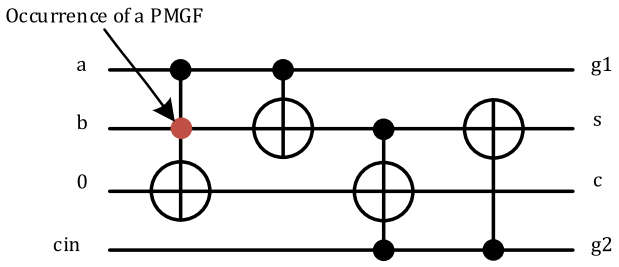


Fig. 8 The partial missing gate fault model

gates is shown in Fig. 7. The second and third CNOT gates are lost. If a = 1, b = 1, and cin = 0 to the inputs of the circuit, the outputs s = 1 and c = 1 can be obtained, instead of correct outputs s = 0 and c = 1, which are incorrect [35].

2.6.5 Partial missing gate fault model

The partial missing gate model occurs when some parts of the gate are deactivated. In other words, one or more control points of a gate are disabled. The concept of PMGF is similar to the concept of the cross-point fault model. For example, if a control point is lost, a K-CNOT gate becomes a (K-1) -CNOT gate. An example of this is shown in Fig. 8 [31, 32].

2.6.6 Repeated gate fault model

The repeated gate fault model shows faults that are repeated several times from one gate in the circuit. One or more unwanted items from a gate in a circuit can cause an incorrect output. An unwanted number of gates for the repeated gate fault model is based on whether the number of this gate is an even number or an odd number of the same gate. It has two different effects [31].

- *Case 1* If the number of unwanted items of the gate is even, then the effect of the RGF model will be the same as the effect of the SMGF on the same gate.
- *Case 2* If the number of unwanted items of the gate is odd, the fault does not affect the output of the circuit.

Figure 9 shows an example of the occurrence of the RGF model with an even number of unwanted items in a reversible circuit. The two 1-CNOT gates replace one CNOT gate. It can be seen that the effect of the SMGF model is the same as the effect of the RGF model. In other words, concerning a gate, the effects of the SMGF and the RGF are the same when a gate is replaced by an even number of instances of the same gate.

Figure 10 shows an example of the occurrence of the RGF model with an odd number of unwanted items. A 1-CNOT gate is replaced by three identical gates. It can be seen that the effect of the RGF model is the same as when there is no fault in the circuit. In other words, this unwanted iteration does not affect the final output of the circuit.

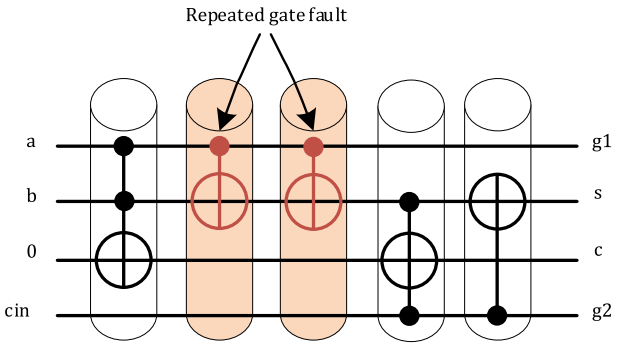


Fig. 9 The repeated gate fault model with an even iteration

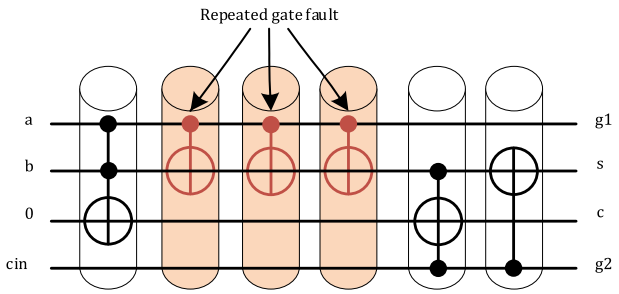


Fig. 10 The repeated gate fault model with an odd iteration

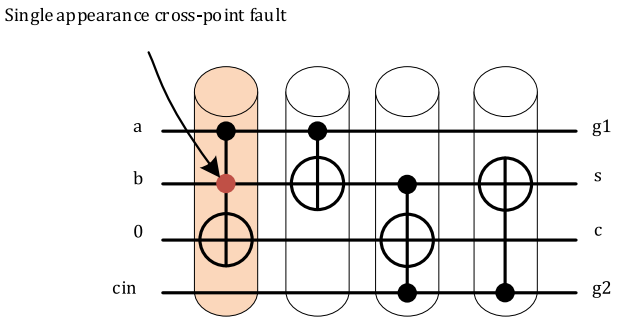
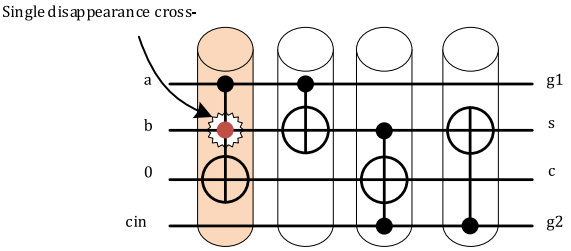


Fig. 11 The single appearance cross-point fault model

Fig. 12 The single disappearance cross-point fault model



2.6.7 Cross-point fault model

The faults that occur at control points are known as cross-point faults. A fault at a control point can lead to incorrect output. The cross-point fault model, which is divided into two types of disappearance and appearance fault models. A cross-point fault occurs when a control point is added or removed. Figures 11 and 12 are shown an example of the disappearance and appearance fault model in a reversible circuit. When a fault occurs, the circuit generates incorrect outputs. A complete test vector set based on the cross-point fault model can also detect all cross-point faults. Selecting an input test vector is sufficient by setting 1 to an input line that has control points and setting the other input lines to 0 [30].

2.6.8 Bit fault model

In the bit fault model, one or more lines change to the fault state, which changes the behavior of the gate output. The difference between the bit fault model and stack-at fault is that in the bit fault model, the output changes from 0 to 1 or from 1 to 0 and depends on the input value. The bit fault occurs due to the incorrect operation of each gate in a reversible circuit [29, 36].

Whenever any fault occurs in the circuit, it is the result of changing single or multi-bit values on each wire. When the value of a line changes, the fault is called the single-bit fault, and if the values of two or more lines change, the fault is called a

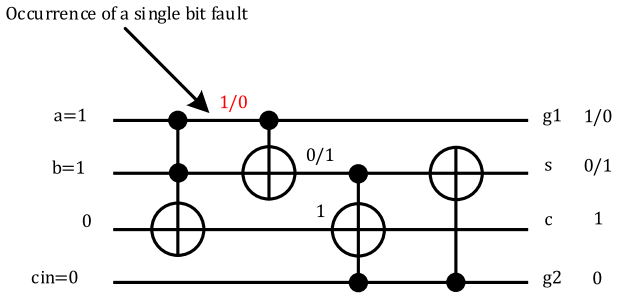


Fig. 13 The single-bit fault model

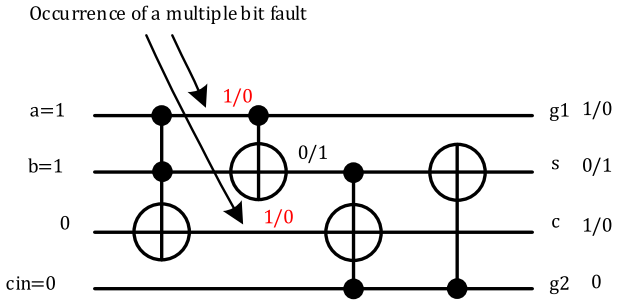


Fig. 14 The multiple bit fault model

multiple-bit fault. Figures 13 and 14 show the single-bit fault model and the multiple bit fault model in circuit, respectively.

2.6.9 Cell fault model

Any change of the gate in the circuit that results in an incorrect output is called a cell fault model. The gates are like cells. A fault in a circuit causes the bit values to be inverted. When the value of a bit changes, it can be a single-bit fault, and if several values change, it can be called a multiple bit fault. Figures 15 and 16 are shown the

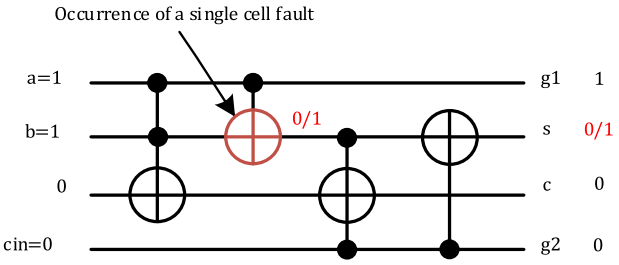


Fig. 15 The single-cell fault model

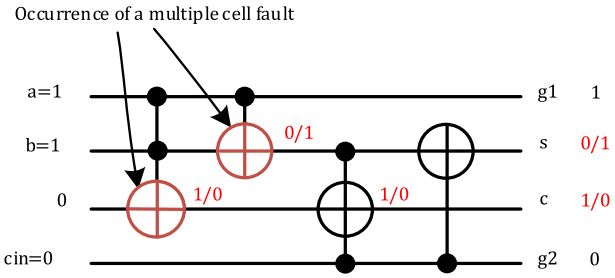


Fig. 16 The multiple cell fault model

patterns of change in bit values due to the corresponding faults in the circuit [29, 36].

2.7 Limitation

Fault detection and fault localization are two important phases in the testing of the reversible circuits. With the increasing importance of the use of reversible logic circuits, testing of the reversible circuits is necessary to ensure their reliability. A test set must be identified to detect all possible faults in a reversible circuit. It must also establish that the generated test set is complete and minimal. The proposed approach to detect all possible faults is performed by an input test vector set. The test vector set for the input of assumed reversible circuits is random. However, providing a method that can provide the test vector set in two phases of combinational and sequential reversible circuits is one of the main limitations of this paper. In particular, the main challenge in sequential circuits is that they are used from memory and feedback. For the input test vector set for this type of sequential circuits, more research and work is required and it is also approved for future work.

3 Related works

Some of the existing research works that are related to the fault-tolerant design of reversible circuits are briefly reviewed in this section.

In 2005, Hayes et al. [29], proposed a design for test (DFT) offline testing approach. Their proposed approach works for NCT family gates and can detect only missing gate faults using only a test vector. According to the DFT-based approach, a reversible circuit can be tested by adding a DFT line to one MGF that contains control points for one or more CNOT gates.

In 2010, Mahammad et al. [37], automatic conversion of any given reversible circuit into an online testable circuit that can detect online any single-bit faults, including soft errors in the logic blocks, using theoretically proved minimum garbage, which is significantly lesser than the best reported in the literature. P_i and P_x input lines are parity faults from two DRGs. The output values of P_i and P_x indicate whether the circuit is faulty or fault-free. If $P_{ix} = P_i$, it indicates that the output is correct.

In 2010, Kole et al. [38], a method for detecting missing gate faults was proposed that can detect SMGFs in NCT-based circuits. According to this approach, each k-CNOT gate of the main circuit becomes an Augmented Reversible Gate (ARG) accordingly. Their approach also requires an additional parity line. An ARG consists of four gates, three additional gates, and one main gate. Additional gates are connected to the parity line. It shows the incorrect output when the output bit is complemented to the input bit.

In 2011, Nayeem et al. [28] proposed an online test approach for the detection of single-bit faults. In the proposed design, we used two sets of CNOT gates and a single-parity line. In this approach, all k-Toffoli gates of an original circuit are transformed into (k + 1)-Extended Toffoli Gates (ETG). In this proposed design, all Toffoli gates are replaced with ETGs and an additional parity line is added to the main circuit to achieve an online test. According to this approach, four changes are required to the online test of a reversible circuit. In the first change, for each input line, a reversible circuit is necessary to add a 1-CNOT gate before and after the main circuit. The second, a line L is added to the circuit. The added CNOT gate lines are connected to the parity line. The third change is that all n-Toffoli gates in the main circuit are replaced by (n + 1)-ETG gates. These three changes are essential for designing an online reversible circuit based on this approach. Fourth change if the NOT gate is in the main circuit. In this case, an additional NOT gate is added at the end of the parity line. If the number of NOT gates is even, a fourth change is not required. Therefore, if a fault occurs and affects the output of a gate, the fault changes the value of L from 0 to 1, which results that the output of the system is incorrect.

The approach proposed by Nayeem et al. [28] examined only the single-bit fault model. Also, the authors consider the cases that occur only as a fault in the main circuit. They do not consider the occurrence of faults in the additional circuit. To solve this problem, in 2015, Nashiry et al. [27] presented an online fault testing approach in reversible circuits based on the NCT gate library for detecting three types of faults in reversible circuits: single-bit fault, missing gate fault, and cross-point fault. In the proposed design in [27], an additional line is added to the circuit to transform a reversible circuit to its online testable equivalent. Next, each k-CNOT gate converts the circuit into a Duplicate Gate Block (DGB). A total of L 1-CNOT gates are added at the beginning and the end of DGBs. This set of 1-CNOT gates are known as the preamble block and postamble block, respectively. With this proposed approach, an entire testable circuit consists of three blocks: preamble block, DGBs, and postamble block. One major advantage of [27] is that circuit overhead reduces significantly for circuits. In addition, this approach is easy to design and reduces design complexity. The proposed approach requires 2(L + N) additional gates in order to make a reversible circuit consisting of L lines and N gates online testable. This approach can also detect a fault even if the fault occurs in the additional circuitry, unlike other approaches in the literature. According to our approach, for a reversible circuit with L lines and N gates, it is necessary to include a parity line, 2L CNOT gates, and N additional duplicate gates to make the circuit online testable.

4 Proposal works

4.1 The proposed design of fault detection and location in reversible combinational circuits

There is a possibility of an incorrect condition during the calculation in any computation device. This incorrect condition is a fault, and the occurrence of faults can affect the performance of a system. Fault models represent the physical description of these faults. The fault detection and correction are very important to ensure the accuracy of reversible circuits. Test vectors play an important role in detecting as well as correcting faults in circuits. The offline test approach is used for fault detection and location. There is a fault detection algorithm to identify all possible faults and then a fault correction method to find the fault location for the detected faults. The main circuit and its complement are connected by a cascade. A reversible circuit can be divided into several levels. An ancilla input is added to the circuit for each level of the circuit. Then 1-CNOT gate is added to ancilla input and gates inputs in the main circuit and complement circuit. Any state of any level of a reversible circuit can be generated with the appropriate input. Any fault in the main circuit and its complement changes the values of level and it will change the output of the circuit. The structure of the implementation of fault detection and location is shown in Fig. 17. The fault detection and location algorithm description are as shown in Algorithm 1. The number of ancilla inputs is calculated as Eq. (1).

$$\mathrm{NL} = \mathrm{NG}, \mathrm{NG} = \text{Number of gates} \tag{1}$$

Algorithm 1: Algorithm for Detection and Location of Fault

```
1   Complement of main circuit is obtained.
2   All gates of circuit and its complement are cascaded
      to test.
3   NG ◄—— Number of gates
4   k ◄—— 1
5   while k < NG do
6       A 1-CNOT gate is added to k gate inputs of main
        circuit and k ancilla input.
7       A 1-CNOT gate is added to complement circuit inputs
        of k gate and k ancilla inputs.
8       If Output of k ancilla inputs == 0 then
9       |     circuit is fault-free
10      else
11      |     circuit is faulty
12      end
13      k ◄—— k+1
14  end
```

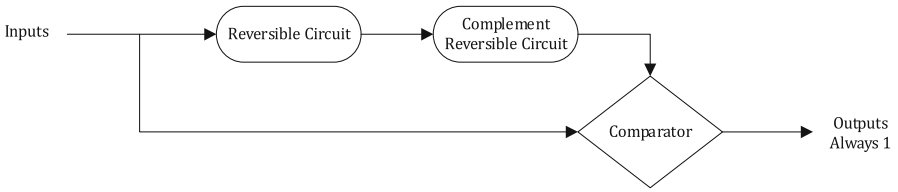


Fig. 17 Structure of the implementation of fault detection and location

The most important mathematical operation is addition. Other operations are usually implemented by adders. An efficient adder can be of great assistance in designing arithmetic circuits [39]. Thus, a reversible full adder circuit shown in Fig. 18a consisting of only four gates and four levels is used as the main circuit. The complement of the reversible full adder circuit is shown in Fig. 18b. The details of the proposed technique based on the complement of the reversible full adder circuit are shown in

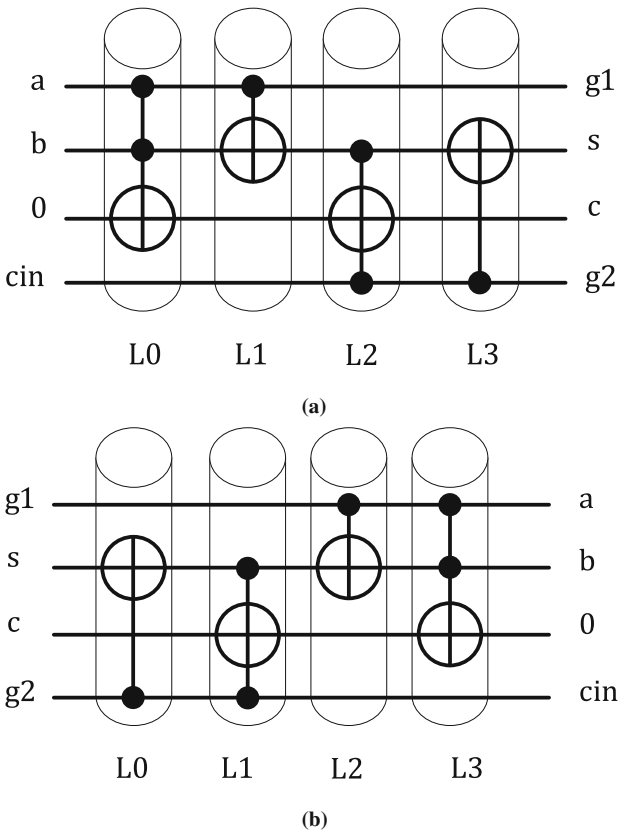


Fig. 18 An example of a reversible circuit for the proposed technique based on its complement. **a** The reversible full adder circuit. **b** The complementation of reversible full adder circuit

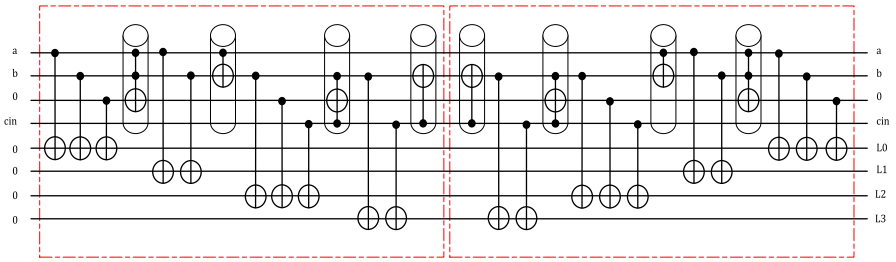


Fig. 19 The proposed technique based on the complement of the reversible full adder circuit without fault

Table 2 Correction and detection table-based on the proposed method

Input a b c d	Output a b c d	Fault location
0 0 0 0	0 0 0 0	Fault-free
0 0 0 1	0 0 0 1	Fault-free
0 1 0 0	0 1 0 0	Fault-free
0 1 0 1	0 1 0 1	Fault-free
1 0 0 0	1 0 0 0	Fault-free
1 0 0 1	1 0 0 1	Fault-free
1 1 0 0	1 1 0 0	Fault-free
1 1 0 1	1 1 0 1	Fault-free

Fig. 19. The correct and incorrect values are presented by correct/incorrect notation in the figure. A comparator for fault detection is used to compare the inputs and outputs of the reversible circuits. A value of '0' in the output of the comparator indicates that the circuit is fault-free. Output '1' indicates that the circuit is faulty. The trust table of the proposed method is shown in Table 2.

4.1.1 Fault location in single missing gate fault

The proposed approach based on the complement of the reversible full adder circuit for the fault location in SMGF is shown in Fig. 20. An input vector (a, b, 0, cin) = (1, 1, 0, 0) can detect a difference between the correct output and the incorrect output. The output of this circuit for fault-free operation is (1, 1, 0, 0). However, in the presence of this fault, the output is (1, 0, 1, 0). The value '1' at the outputs L1 indicates that there is a fault in the second gate of the circuit.

4.1.2 Fault location in multiple missing gate fault

The proposed approach based on the complement of the reversible full adder circuit for the fault location in MMGF is shown in Fig. 21. For the test vector (a, b, 0, cin) = (1, 1, 0, 0), the circuit generates the output vector (1, 1, 0, 0). Any value other than

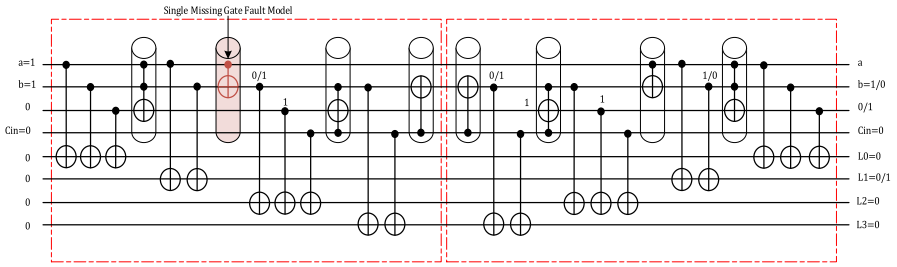


Fig. 20 The proposed technique based on the complement of the reversible full adder circuit with SMGF

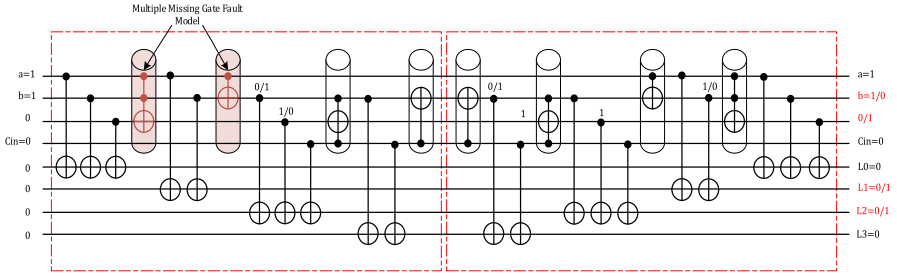


Fig. 21 The proposed technique based on the complement of the reversible full adder circuit with MMGF

this output vector indicates that MMGF is present in the circuit. The value '1' at the outputs L1, L2 and incorrect outputs in b and constant input lines indicates that there is MMGF in the first and second gates of the circuit.

4.1.3 Fault location in partial missing gate fault

The process of using the proposed method based on the complement of reversible full adder circuit for fault location with disappearance cross-point fault model and appearance cross-point fault model are shown in Figs. 22 and 23, respectively. The

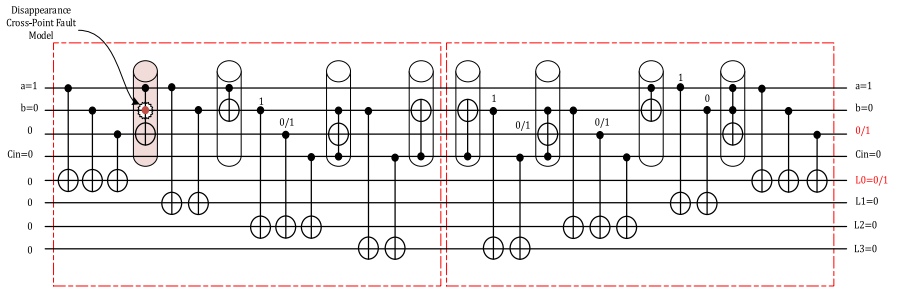


Fig. 22 The proposed technique based on the complement of the reversible full adder circuit with disappearance cross-point fault model

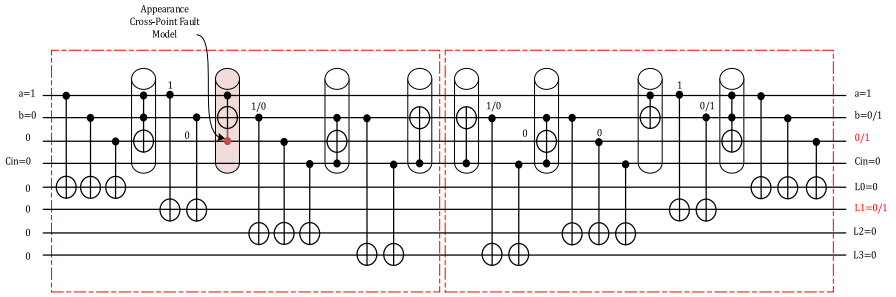


Fig. 23 The proposed technique based on the complement of the reversible full adder circuit with appearance cross-point fault model

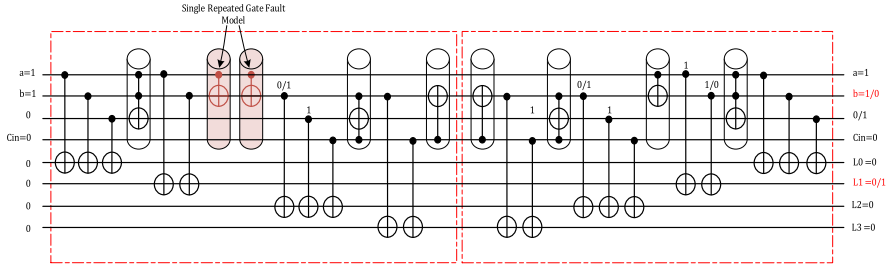


Fig. 24 The proposed technique based on the complement of the reversible full adder circuit with a single repeated-gate fault model

input vector (a, b, 0, cin) = (1, 1, 0, 0), the output vector will be (1, 1, 0, 0). This output is incorrect for both figures. However, in Fig. 22, the value '1' at the output L0 identifies the occurrence of a fault in the first gate and the value '1' at the output L1 identifies the occurrence of a fault in the second gate.

4.1.4 Fault location in repeated gate fault

The process of using the proposed method based on the complement of the reversible full adder circuit for the fault location in RGF is shown in Fig. 24. For this input vector, (1, 1, 0, 0), the circuit output will be (1, 1, 1, 0) instead of the correct output (1, 1, 0, 0). It is seen that output L1 = 1, which indicates that the circuit is faulty. There is a fault in the second gate of the circuit.

4.1.5 Fault location in single-bit fault

The process of using the proposed method based on the complement of the reversible full adder circuit for the fault location in SBF is shown in Fig. 25. When test vector (a, b, 0, cin) = (1, 1, 0, 0), the circuit output becomes (1, 0, 1, 0), and the output L1 = 1, which indicates that the output is incorrect and the second gate of the circuit is faulty.

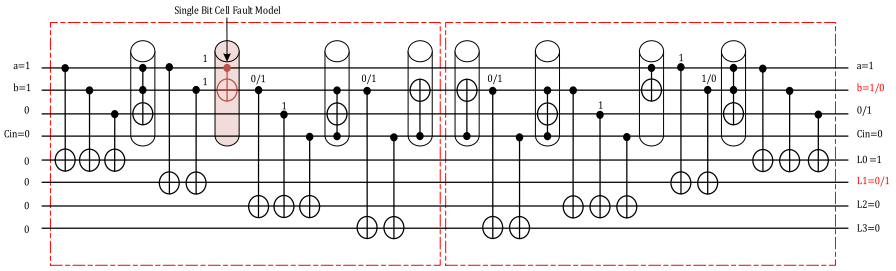


Fig. 25 The proposed technique based on the complement of the reversible full adder circuit with single-bit cell fault model

4.2 The proposed design of detection and location in reversible sequential circuits

In this section, an approach to fault detection in reversible sequential circuits using the complement of the main circuit is presented. Reversible sequential circuits use positive and negative edge triggering. The positive edge triggering of the clock is used to activate the main circuit and complement of the circuit, and the negative edge triggering of the clock is used for the comparator. The output of the complement of the circuit is compared to the input of the main circuit. The result of the comparison must always be equal to 0. This approach to fault detection in reversible sequential circuits has not been proposed in the literature so far. The structure of the implementation of a fault detection method for reversible sequential circuits is shown in Fig. 26. For example, the design of the reversible realization of the 4-bit falling-edge triggered up/down counter is shown in Fig. 27. The details of the proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter is shown in Fig. 28. A comparison of the input of the main circuit and the output of the complement circuit indicates all fault models in the circuit.

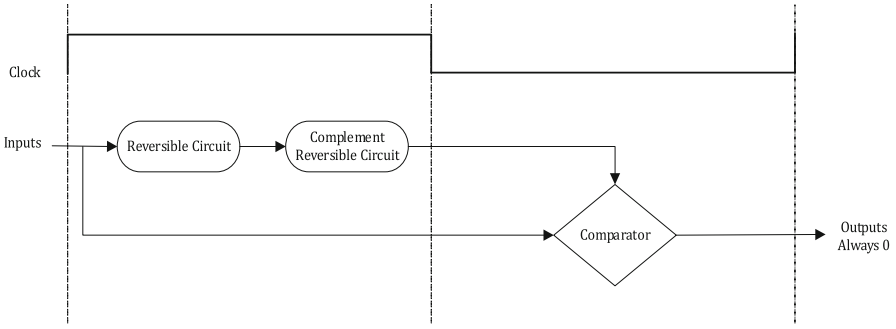


Fig. 26 Structure of the implementation of a fault detection method for reversible sequential circuits

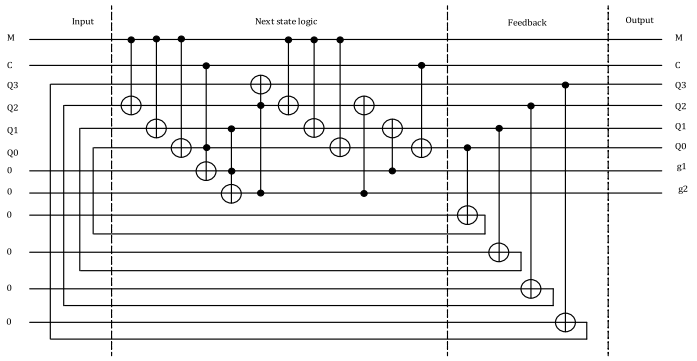


Fig. 27 Design of the reversible realization of the 4-bit falling-edge triggered up/down counter

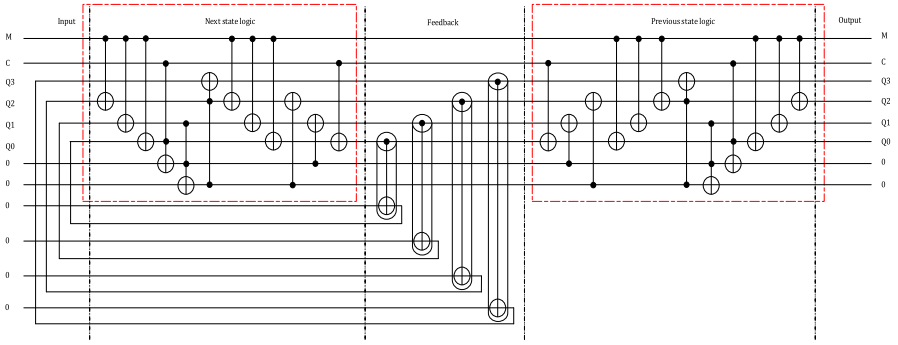


Fig. 28 The proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter without fault

4.2.1 Fault location in single missing gate fault

Fault detection in SMGF by using the proposed method based on the complement of circuit realization of the 4-bit falling-edge triggered up/down counter is shown in Fig. 29.

An input vector (Q_0, Q_1, Q_2, Q_3) = (0, 0, 1, 0) and M = 0 can detect a difference between the correct output and incorrect output. The value '0' at the output Q_2 instead of '0' indicates that there is a fault in the circuit.

4.2.2 Fault location in multiple missing gate fault

The process of detection fault in MMGF by using the proposed method based on the complement of the circuit realization of the 4-bit falling-edge triggered up/down counter is shown in Fig. 30. For the test vector (Q_0, Q_1, Q_2, Q_3) = (0, 1, 1, 0) and M = 0, the circuit generates the $Q_1 = 0$, $Q_1 = 0$. This output indicates that fault is present in the circuit.

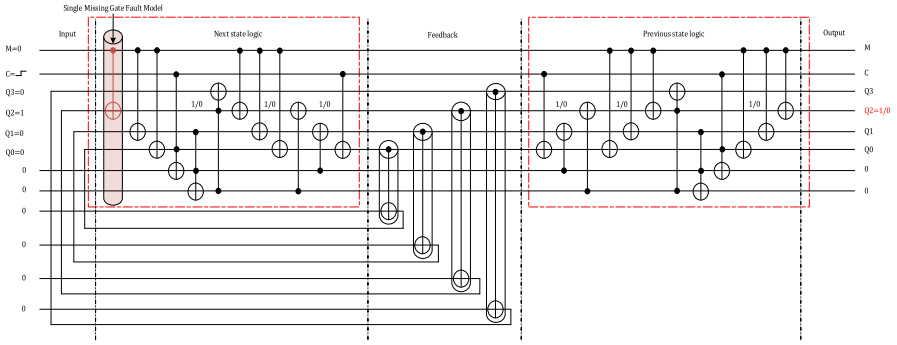


Fig. 29 The proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter with SMGF

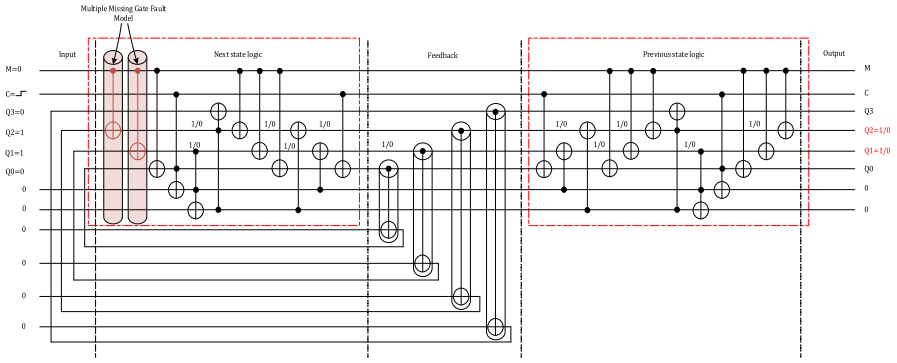


Fig. 30 The proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter with MMGF

4.2.3 Fault location in partial missing gate fault

The fault detection in PMGF consists of two models of disappearance and appearance cross-point fault models. The fault detection in disappearance cross-point fault model by using the proposed method based on the complement of circuit realization of the 4-bit falling-edge triggered up/down counter is shown in Fig. 31 and the fault detection in appearance cross-point fault model in Fig. 32. The input vector (Q_0, Q_1, Q_2, Q_3) = (0, 0, 1, 0) and M = 0 for disappearance and (Q_0, Q_1, Q_2, Q_3) = (0, 0, 0, 0) and M = 1 for appearance cross-point fault model, the output vector will be $Q_2 = 0$. This output is incorrect for both fault models, which identify the occurrence of a fault in the circuit.

4.2.4 Fault location in repeated gate fault

The fault detection in RGF by using the proposed method based on the complement circuit realization of the 4-bit falling-edge triggered up/down counter is shown in

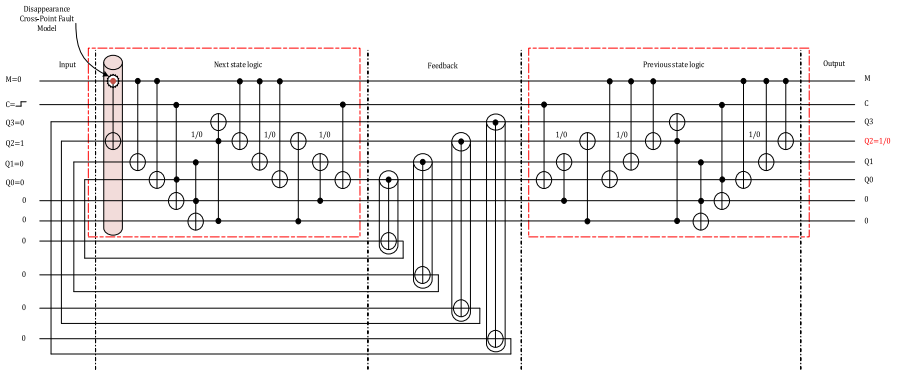


Fig. 31 The proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter with disappearance cross-point fault model

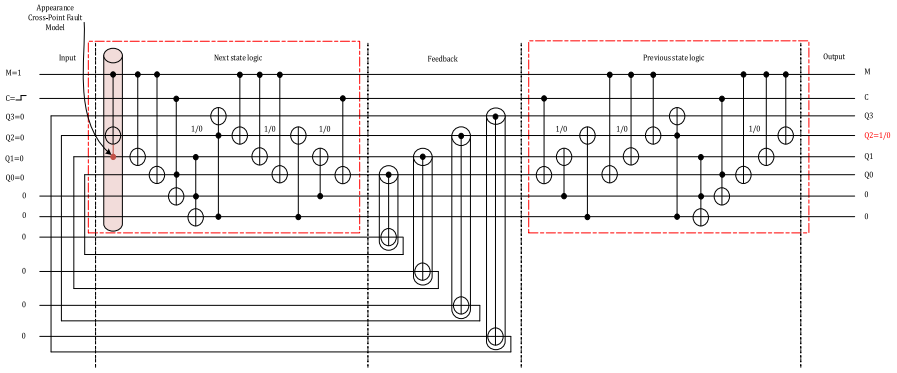


Fig. 32 The proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter with appearance cross-point fault model

Fig. 33. For input vector $(Q_0, Q_1, Q_2, Q_3) = (0, 0, 0, 0)$ and $M = 1$, the circuit output will be $Q_2 = 1$ instead of the correct output $Q_2 = 0$. It is seen that output $Q_2 = 1$, which indicates that the circuit is faulty.

4.2.5 Fault location in single-bit fault

The fault detection in SBF by using the proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter is shown in Fig. 34. When test vector $(Q_0, Q_1, Q_2, Q_3) = (0, 0, 1, 0)$ and $M = 0$, the circuit output becomes $Q_2 = 0$, and the output $Q_2 = 0$ indicates that the output is incorrect and the circuit is faulty.

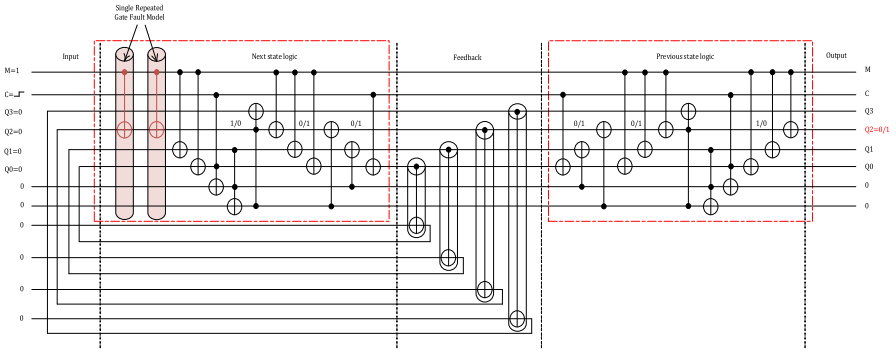


Fig. 33 The proposed method based on the complement of the reversible realization of the 4-bit falling-edge triggered up/down counter with single repeated gate fault model

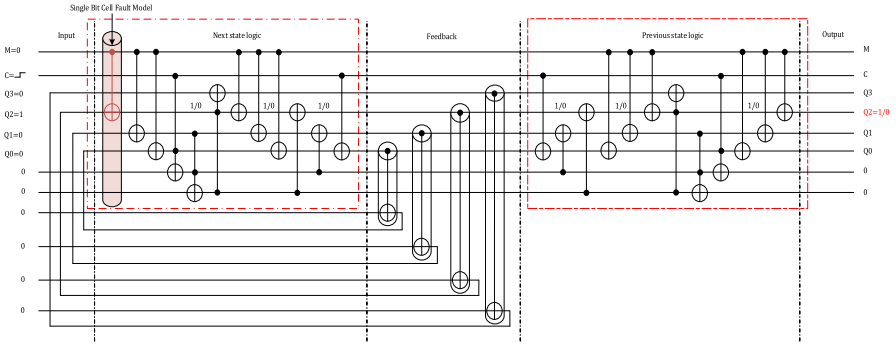


Fig. 34 The proposed method of the reversible realization of the 4-bit falling-edge triggered up/down counter with single-bit cell fault model

4.3 The proposed LUT-based automatic of fault correction in reversible circuits

Assume that the specification table of the reversible circuit is given or that it is manually generated by a technique. If the simulation and other techniques show that the reversible circuit is not exactly equivalent to the specification table. As a result, the fault must be corrected. If a fault occurs in the circuit. Instead of restoring the new circuit, it is often best to equate the existing circuit with the specification table. In other words, it is best to convert the circuit to the equivalent of the given specification table. Because the circuit topology is more preserved.

A technique for the automatic correction of fault parts in reversible circuits is proposed. In this method, the missing parts of the circuit are automatically filled so that the whole circuit is equal to the given specification table. The details of the proposed approach are shown in Fig. 35. The inverse of a specification table is created, and a comparator is used so that the output of the value should always be equal to 0.

Fault correction consists of two steps.

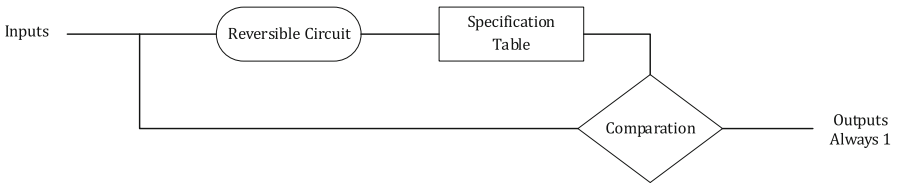


Fig. 35 Structure of the implementation of LUT-based automatic fault correction in reversible circuits

- *Step 1* When a circuit is incorrect according to the validation method. It indicates a fault in the circuit.
- *Step 2* The faulty parts are replaced with new sub-circuits so that the whole circuit is equivalent to the specification table.

For example, it is assumed that the circuit shown in Fig. 36a is not faulty, while Fig. 36b has a fault that can be replaced with the correct part as shown in Fig. 36c.

If the Toffoli network is faulty, the faulty Toffoli gate is identified. The LUT equivalent circuit with three inputs is replaced for the faulty part. Since the circuit must be reversible, the cascades of the Toffoli gate obtained for LUT must be a reversible function. In other words, in a reversible function, the input value and the output value must be a one-to-one mapping. The circuit is faulty if the input values are different from the output values. The structure of the implementation for automatic fault detection and correction design by complement specification table is shown in Fig. 37.

4.4 Realizations with Clifford+T

In order to implement reversible circuits on a real quantum computing platform like IBM's QX architecture, they should be mapped to Clifford+T gates and then implemented on IBM's QX architecture. An implementation based on the complement of full adder is demonstrated with Clifford+T gates in Fig. 38.

5 Comparisons

A number of fault detection approaches have been proposed for reversible logic. In the paper, all of the fault models for reversible logic have been studied. This section offers a comparison between the proposed approach and five methods on [27–29, 37, 38]. For comparison, an example of a testable reversible full adder circuit based on proposed approaches in [27–29, 37, 38], and the proposed approach are presented.

The approaches presented in [28, 29, 38] fail to detect a PMGF. Similarly, the approaches presented in [28, 37, 38] cannot detect correct output for other reversible fault models, such as MMGFs, RGFs, and SAFs. In [28, 37], the authors proposed an online testable reversible full adder circuit and examined their proposed approach against only the SBF model. In addition, the authors only consider the case when a fault occurs in an original circuit. They did not consider the occurrence of faults in the extra circuitry. In [29], the proposed approach works for NCT family gates and can

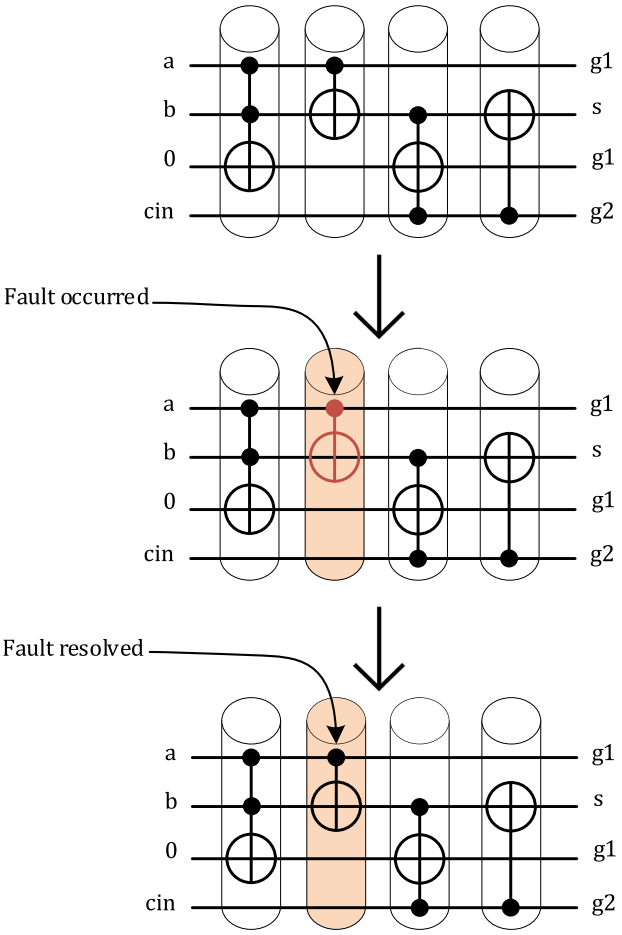


Fig. 36 Example of implementation for LUT-based automatic fault correction in reversible circuits

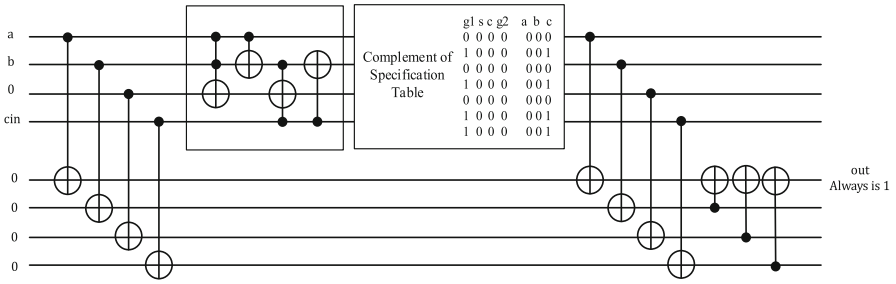


Fig. 37 Structure of the implementation for automatic fault detection and correction design by complement specification table

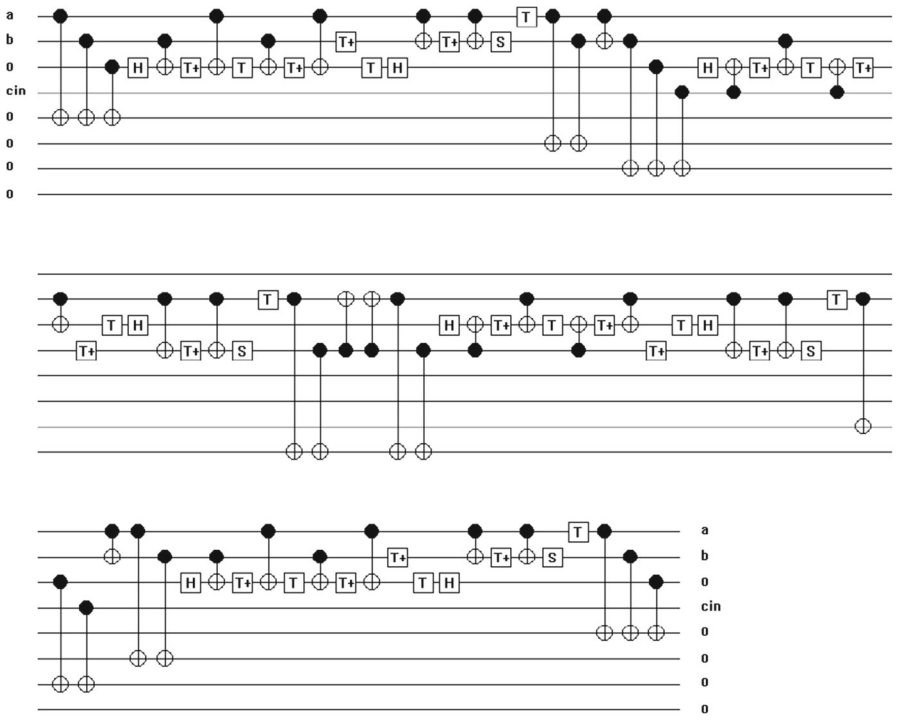


Fig. 38 The proposed method is based on the complement of the reversible full adder circuit that is realized with Clifford+T library

detect only missing gate fault using only a test vector. In [38], the authors proposed an online testable approach that can detect SMGFs in NCT-based circuits. According to this approach, in order to implement a full adder circuit requires a testable circuit with QC = 32. The other resulting testable circuit has QC = 15 for [29] and QC = 44 for [37]. While the QC of the proposed approach is 44. The QC of the proposed approach is slightly higher as compared to the approaches described in [27–29, 38]. Whereas the proposed approach can affect all fault models and, in most cases, in the first proposed approach, it can also detect the location of the faults. But, the proposed approach in [28] only considers single-bit faults, and the proposed approach in [27] can detect three types of faults, which are the single bit fault (SBF), missing ate fault (MGF), and Cross-point Fault, and proposed approach in [38] considers only single missing gate fault (SMGF).

The proposed online testing approach is well-suited for fault detection and location in a reversible sequential circuit, which is presented for the first time in the literature. Some of the optimal metrics like Quantum Cost (QC), Ancilla Input (AI), Garbage Output (GO), Quantum Cost (QC), and Total Logic Calculation (TLC) are used in the evaluation. It is assumed that: α = the count of CNOT gate, β = count of Toffoli gate, γ = count of Fredkin gate, and T = Total logical calculation. Table 3 presents the QC, AI, and GO of a testable reversible full adder circuit based on proposed approaches in

Table 3 Comparison of the test approaches with the proposed design in cost, identification of fault models, and location fault

Approaches	Cost				Cost realized with Clifford+T library			Two-qubit cost model		Identification of fault models						Location fault
	QC	AI	GO	TLC	Qubit Cost	T-count	T-depth	No. of 1-qubit gates	No. of 2-qubit gates	SMGF	MMGF	PMGF	RGF	SBF	SAF	
Design [27]	32	1	3	12α + 4β	36	28	12	40	36	✓	✓	✓	NR	✓	NR	×
Design [28]	28	1	3	8α + 4β	36	28	12	40	36	NR	×	×	×	✓	×	×
Design [29]	15	1	3	5α + 2β	17	14	8	20	17	✓	✓	×	NR	NR	NR	×
Design [37]	44	2	4	14α + 6β	50	42	18	60	50	NR	×	NR	×	✓	×	×
Design [38]	32	1	3	12α + 4β	36	28	16	40	36	✓	×	×	×	NR	×	×
Proposed design	44	4	4	24α + 4β	48	28	16	40	48	✓	✓	✓	✓	✓	✓	✓

[27–29, 37, 38] and the proposed approach. This table also shows the ability to detect and locate faults for a variety of fault models. As shown, only the proposed approach is capable of fault detection for all known fault models so far. In this proposed approach, an adaptation for reversible sequential circuits is also considered, which perform the fault detection capability for a variety of fault models. For a more detailed comparison of the designs in literature and the one presented in this paper, they should be mapped to Clifford+T gate. To evaluate the quantum circuit, metrics of T-count and T-depth have been considered because the implementation cost of the T gate is significantly greater than the costs of the other Clifford+T gates. In this table, the results of the proposed approach, in terms of Qubit cost, T-count, and T-depth in comparison to related work in [27–29, 37, 38] are reported, too.

6 Conclusion and future work

In this paper, all available fault models for reversible circuits are investigated. Then, two approaches for fault detection and correction to ensure accuracy and reliability in reversible circuits are presented.

The cost metrics of the proposed approach are slightly higher as compared to the existing approaches in the literature. However, the proposed approach considers all fault models, and in most cases, it can also detect the location of the faults. In addition, the proposed approach is well-suited for fault detection and location in reversible sequential circuits, which is presented for the first time in the literature.

For future work, the fault models should be considered carefully depending on the implementation technology of the gate, they can have a specific meaning. Consequently, again, faults that are relevant to quantum computing technologies can be discussed. Some fault models, such as MGFs and RGFs, do not conform to state-of-the-art quantum computing like IBM QX architecture. This section can be reviewed for future research in this direction to make it more technologically relevant. Moreover, new algorithms for fault detection can be presented specifically for these technologies.

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