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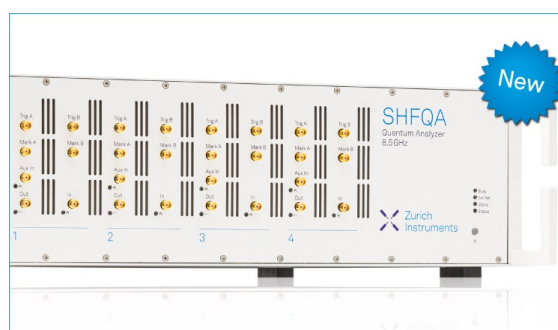
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ABSTRACT

Superconducting junctions are widely used in a multitude of applications ranging from quantum information science and sensing to solid-state cooling. Traditionally, such devices must be fabricated on flat substrates using standard lithographic techniques. In this study, we demonstrate a highly versatile method that allows for superconducting junctions to be fabricated on a more complex topography. It is based on maskless direct laser writing and two-photon lithography, which allows writing in 3D space. We show that high-quality normal metal–insulator–superconductor tunnel junctions can be fabricated on top of a 20- μm -tall three-dimensional topography. Combined with conformal resist coating methods, this technique could allow sub-micron device fabrication on almost any type of topography in the future.

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Superconducting tunnel junctions have many applications, for example, in sensing,¹ quantum information,^{2,3} and nanoscale thermal sciences.⁴ Their fabrication is done using the well-established techniques of ultraviolet photolithography or electron-beam lithography, which produce good results except for one major flaw: those methods are designed for patterning on flat 2D substrates. This is a limitation for more complex device designs, which may, in some cases, require or benefit from the junctions sitting on uneven or sloped surfaces, at the bottom of a trench, or on elevated platforms, for example, on top of a three-dimensional (3D) phononic crystal for strong thermal isolation. It is the purpose of this study to demonstrate a simple technique that facilitates such more difficult, yet high quality superconducting junction fabrication on substrates of varying topography.

As the first proof-of-principle demonstration, in this study we fabricate and characterize normal metal–insulator–superconductor (NIS) tunnel junctions⁵ on complex topography. This choice is based on two reasons: (i) the electrical response of a NIS junction is a sensitive probe of the quality of the superconducting material and the insulating barrier, as it allows a direct measurement of the density of states of the superconductor, and (ii) our own immediate application is in sensitive local thermometry of complex nanoscale 3D structures. The fabrication technique is, however, perfectly suited for the fabrication of superconductor–insulator–superconductor (SIS) or superconductor–normal metal–superconductor (SNS) Josephson junctions, as well.

NIS junctions are particularly suited for low-temperature thermometry, because the current through an NIS junction has a strong temperature dependence at energies close to the superconducting gap,^{4,6,7} and they can even be considered, in some cases, as primary electron thermometers.⁸ Due to their sensitivity and the possibility to fabricate them in sub-micron scales, they are excellent local sensors for heat transfer measurements,^{9–12} can be operated fast in microsecond time scales with a microwave readout,^{13,14} and could work as the sensor element in bolometric radiation detection^{15–18} or in direct measurement of temperature fluctuations.¹⁹ Typically, the superconducting material used is Al, limiting the use of NIS devices to below 1 K. However, by using higher transition temperature superconductors, the temperature range of NIS thermometers has been extended with Nb,^{20,21} NbN,²² TaN,²³ and TiN.²⁴

Other possible applications of NIS junctions are in metrology,^{25,26} thermal rectification,²⁷ and electronic cooling,^{28,29} with demonstrations of cooling of macroscopic and mesoscopic platforms,^{30–32} nanoscale beams,^{33,34} radiation detectors,³⁵ remote devices via photons,^{36,37} and quantum information circuit components.³⁸

In this Letter, we demonstrate high quality microscale Cu–AlO_x–Al NIS junction fabrication both on flat surfaces and on three-dimensional (3D) topography, using direct laser writing (DLW), which is a recently developed fabrication technique based on two-photon absorption (TPA), originally developed for writing arbitrary

3D polymer structures from negative photoresists.^{39–41} In contrast, here we use DLW to develop a positive photoresist without a photo-mask in combination with metal deposition and liftoff, as introduced in Refs. 42 and 43. Here, we show that well-behaving junction devices can be made using a two-layer nonstandard photoresist with an undercut structure, without degradation due to the used resists and processes. The junctions were fabricated both on flat substrates and, in particular, on top of a 20- μm -tall 3D platform. Such devices have not been made before, as they are difficult to make with standard lithographic techniques. Electrical characterization of the junctions demonstrates that the junction quality is high, as the standard junction theory fits the data extremely well, with a low level of excess sub-gap current. The temperature sensitivity extends to the lowest refrigerator temperatures used, demonstrating the application potential for thermometry and cooling of complex 3D device platforms.

The complex topography used is a 3D cuboid structure with an area of $100\ \mu\text{m} \times 100\ \mu\text{m}$ and a height of $20\ \mu\text{m}$ with sloped ramps (Fig. 1), fabricated from a negative photoresist (IP-Dip, Nanoscribe GmbH) on a nitridized Si substrate using DLW (Nanoscribe Photonic Professional), similar to the cuboid structure in Ref. 43. An additional $200\ \text{nm}$ AlO_x capping layer was evaporated on the whole cuboid structure to strengthen it and to obtain more homogeneous and flat surfaces to increase the yield. AlO_x was chosen out of convenience, but other materials could also have been used.

The actual junction fabrication proceeds as follows: the sample is spin coated first with a bottom resist (AR-BR 5460, Allresist GmbH),

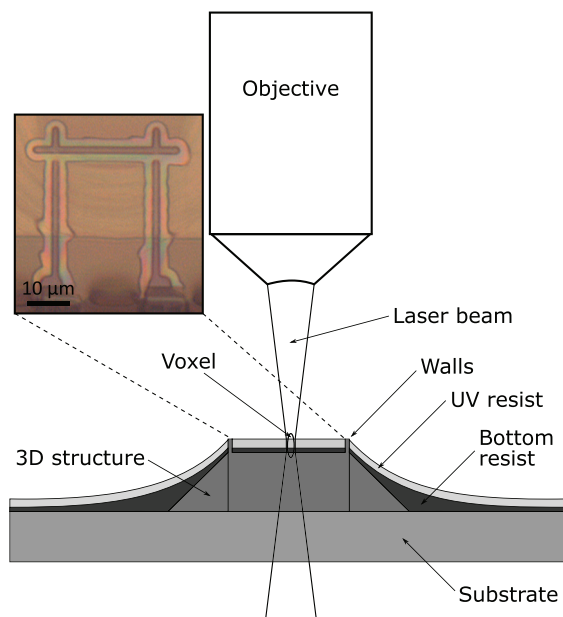


FIG. 1. Schematic of the two-photon laser exposure method used for patterning the junctions. An air-gap objective is used in order to expose from the top side of the 3D structure without being in contact with the substrate. The focus spot of the laser beam travels in 3D space, following the existing topography on the front surface, where the TPA process forms the voxel. Inset: optical micrograph of the exposed pattern on the 3D structure after development. The linewidth here is around $2.5\ \mu\text{m}$ giving a junction area of $6.25\ \mu\text{m}^2$. A large ($\sim 2\ \mu\text{m}$) undercut and a bridge structure are visible.

which was diluted with propylene glycol methyl ether acetate (PGMEA) to a solid content of 9% to get a $450\ \text{nm}$ thick film on a flat surface. This layer will allow for an undercut in the resist structure. We do not bake the bottom resist but, instead, keep it in vacuum overnight to remove the solvent. This allows for deeper undercuts and makes it possible to fabricate bridge structures for the subsequent shadow evaporation step. Then, the sample is spin coated with the UV sensitive positive-tone resist (AR-P 3540, Allresist GmbH) to a nominal thickness of $2.8\ \mu\text{m}$ and baked at $100\ ^\circ\text{C}$ for $140\ \text{s}$. To allow for the resists to remain on top of the cuboid structure during spinning, small vertical walls of height $3.5\ \mu\text{m}$ were incorporated at the edges of the 3D platform, as shown in Figs. 1 and 2. Such walls could be left out if direct spray coating were used.⁴⁴

The lithographic exposure of the junction geometry is done with the same Nanoscribe Photonic Professional tool (pulse rate: $80\ \text{MHz}$ and wavelength: $780\ \text{nm}$) that was used for the fabrication of the topography. Because now solid resists are used (as opposed to liquid), the objective ($63\times$, $\text{NA} = 0.75$) cannot be in contact with the resist, and an air gap to the sample remains, as shown in Fig. 1. A writing speed of $v = 25\ \mu\text{m}/\text{s}$ and a laser power of $P = 4\ \text{mW}$ were used for the exposure on top of the platform, producing a single-pass linewidth $\approx 1\ \mu\text{m}$ through the whole top resist layer. The size of the voxel (line resolution) can easily be controlled with the power and speed, scaling as P^2/v , with possible speeds up to a few mm/s . As the aspect ratio of the voxel is naturally high (height:width 5:1), it is straightforward to expose micrometers thick resist layers on one pass. Moreover, a large voxel height allows for significant, even micrometer scale variations of the actual resist thickness, which invariably exist when spin coating such tall topographical features. Even thicker resists can be exposed by layering the writing pattern, and this technique was used in areas near the base of the platform structure where the resist was the thickest.

In our setup, the focus of the laser cannot automatically follow the topography and thus the height changes need to be included in the

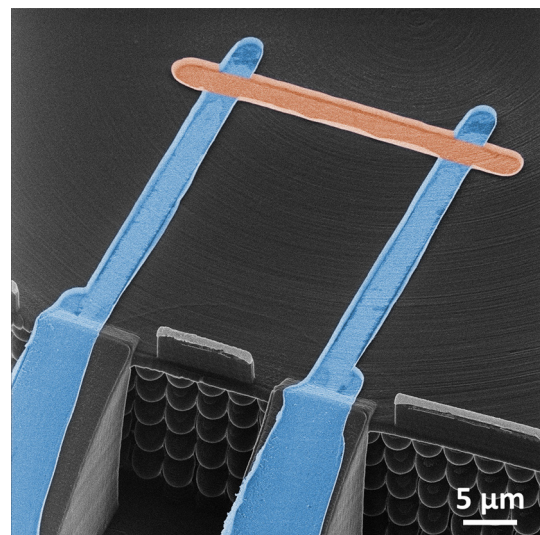


FIG. 2. False color helium ion micrograph of a finished SINIS junction on the 3D structure (blue = Al, red = Cu). For this sample, the linewidth is around $3\ \mu\text{m}$, giving a junction area of $9\ \mu\text{m}^2$.

pattern of the laser writing path. This means that the dimensions of the topography need to be known in advance for this method. Fortunately, this information does not need to be very precise due to the size of the voxel. The alignment of the sample was done with the integrated optical microscope of the Photonic Professional tool.

After the exposure, the sample is developed in a 1:1 mixture of an AR 300–47 developer (Allresist GmbH) and de-ionized water and rinsed with de-ionized water. With the two layers of resists used, the depth of the undercut can be controlled simply with the development time. This is because the bottom resist is not exposed at all and just slowly dissolves into the developer. The development times used for our samples were around 15 s, producing a micrometer-scale undercut profile (inset, Fig. 1).

After the patterning and development, the metals are evaporated using an ultra-high vacuum electron-beam evaporator. First, a 30 nm layer of aluminum is evaporated along the patterned leads that climb the ramps. This was done from two opposing directions, in four different steps from an angle decreasing from 70° to 60° with respect to the surface normal, with the rotation axis being along the patterned line for the copper (Fig. 2). This sequence ensured better coverage over the roughness of the underlying structure. The aluminum is then thermally oxidized in 200 mbar of pure oxygen for 9 min, producing an AlO_x tunnel barrier. Finally, the sample is rotated 90° around the surface normal, and a 60 nm copper layer is evaporated similar to the aluminum, with the rotation axis for the angle evaporation now being along the Al leads (Fig. 2). Angle evaporation is also used for the copper so that no copper will land on the aluminum leads on top of the platform. After the evaporation, liftoff is done with hot acetone. A helium ion micrograph of a finished double junction SINIS device is shown in Fig. 2.

The current through a high-quality NIS junction is given by the expression

$$I = \frac{1}{2eR_T} \int_{-\infty}^{\infty} d\varepsilon N_S(\varepsilon) [f_N(\varepsilon - eV) - f_N(\varepsilon + eV)], \quad (1)$$

where R_T is the tunneling resistance of the junction, $N_S(\varepsilon)$ is the density of states of the superconductor, and f_N is the Fermi-Dirac distribution in the normal metal.^{4,6} For the density of states, we use the expression taking into account non-idealities,

$$N_S(\varepsilon, T_S) = \left| \operatorname{Re} \left(\frac{\varepsilon + i\Gamma}{\sqrt{(\varepsilon + i\Gamma)^2 - \Delta^2(T_S)}} \right) \right|, \quad (2)$$

where Γ is the so-called Dynes parameter and $\Delta(T_S)$ the temperature dependent superconducting energy gap. Γ describes, in general, the non-ideal broadening of the density of states⁴⁵ due to barrier and material non-idealities. For the case of high-quality Al junctions, it was shown to result from environmentally photon-assisted tunneling events.⁴⁶

To study the properties of NIS junctions fabricated with the DLW method, we first fabricated junctions on flat nitridized Si substrates and measured them using a ³He/⁴He dilution refrigerator with a base temperature of 60 mK. Examples of sets of I - V and dI/dV - V measurements on such a single NIS junction device with $R_T = 2$ k Ω , as a function of the bath temperature, are shown in Figs. 3(a) and 3(b). They are plotted together with theory fits based on Eqs. (1) and (2), with the electron temperature fitted but constant for each curve and Δ and R_T fitted but kept constant for the whole set. We can see that the

fits are extremely good for both the I - V and the dI/dV data, demonstrating that the DLW method can produce junctions of equal quality to standard lithography.

The fitted temperatures match almost exactly the measured bath temperatures, except at the lowest temperatures, where the fitted electron temperatures are slightly higher. This is a well-known effect, caused by absorbed spurious thermal radiation from the higher temperature stages of the cryostat, in combination with the strong thermal decoupling of the electron system from the lattice at the lowest temperatures.^{10,33,47} From the fits, we determined the zero temperature superconducting gap of the aluminum to be $\Delta(0) = 0.208$ meV, agreeing with previous results on a thin film Al of similar thickness deposited in the same evaporator.³³ The Dynes parameter for this device was $\Gamma/\Delta(0) = 6.5 \times 10^{-4}$, fitted using the level of the subgap current at the lowest temperature. It is roughly consistent with what has been measured in the same setup before,³⁵ and low enough to allow for efficient NIS cooling.^{23,48} However, for this particular device, electronic cooling was not observed due to the large size of the normal metal electrode in the single junction geometry and due to the lack of normal metal quasiparticle traps contacting the Al electrode.⁴⁹

After demonstrating that NIS junctions can be fabricated, we wanted to produce samples for our intended application, where SINIS junction pairs are needed on top of the 3D topography. Therefore, in Figs. 3(c) and 3(d), similar measurements are shown for a double junction SINIS device on top of the 3D topography (Fig. 2). This time, the fits with the simplest constant temperature model do not produce good results anymore. However, by incorporating the thermal resistance of the small normal metal island due to the electron-phonon interaction and the effect of Joule self-heating,^{4,7} the fits become nearly perfect. The impact of the self-heating is particularly noticeable as the rounding of the differential conductance peaks of the lowest bath temperature data [Fig. 3(d)].

In the thermal model, described in more detail in Ref. 7, we used the usual relation⁴⁷ $P = \Sigma V(T_e^5 - T_p^5)$ for the power flow between electrons and phonons for thick metal films on bulky substrates, where V is the normal metal volume, and a typical value $\Sigma = 2 \times 10^9$ W/(K⁵ m³) for the electron-phonon coupling strength in Cu was used.⁴ In addition, the modeling included the parameter $\beta = 0.25$, giving the fraction of dissipated power that back-flows from the superconducting electrodes into the normal metal.⁵⁰ This value is higher than what is typically observed ($\beta < 0.1$) for NIS junctions that are optimized for cooling,^{29,33} which is expected, as we have a thin superconducting film without quasiparticle trapping.

For this SINIS junction, the Dynes parameter has a quite low value $\Gamma/\Delta(0) = 9 \times 10^{-5}$, which is much lower than for the single NIS junction sample. This improvement is most likely due to the higher value of R_T , leading to less efficient absorption of environmental radiation power and thus smaller current due to photon-assisted tunneling, as second order Andreev tunneling was estimated to be much too small to be able to explain the sub-gap current for our junction and material parameters.^{51,52} Surprisingly, even with an identical oxidation recipe, R_T was always much higher for junctions on top of the structure. Possible causes are the different substrate material or the higher surface roughness, but detailed understanding is currently lacking. The superconducting gap is now $\Delta(0) = 0.181$ meV, smaller than for the simpler NIS junction but still in agreement with the literature.⁵³

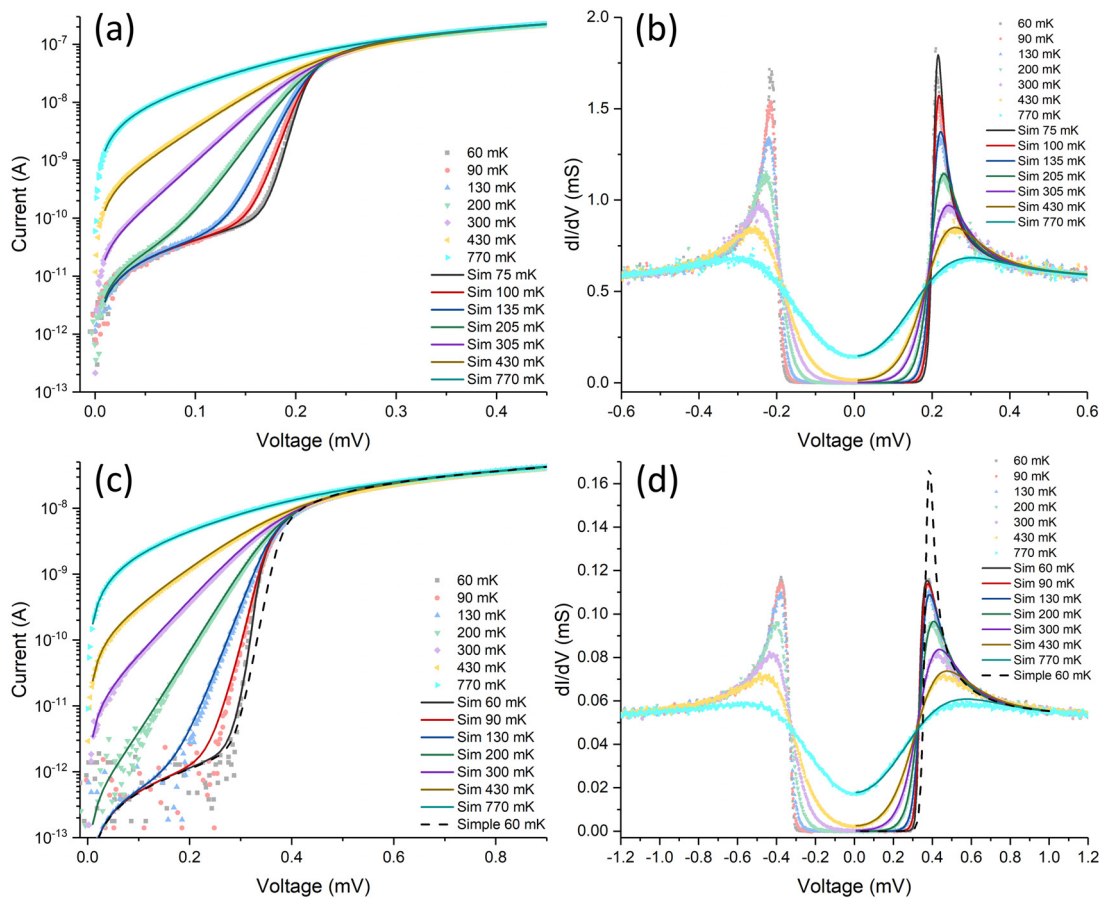


FIG. 3. The measured low-temperature (a) I - V and (b) dI/dV - V characteristics for the DLW fabricated NIS junctions on a flat substrate (symbols) (junction area $5 \mu\text{m}^2$, $R_T \sim 2 \text{ k}\Omega$). Theory fits to Eq. (1) and its voltage derivative are shown as lines, with the electron temperature as a fitting parameter. The experimental dI/dV data were produced by numerical differentiation of the I - V curve. [(c) and (d)] The same for a SINIS junction pair on top of the fabricated topography (junction area $4 \mu\text{m}^2$, $R_{T,\text{tot}} \sim 20 \text{ k}\Omega$). The solid lines are the theoretical results based on Eq. (1) with the thermal modeling described in the text. The dashed line shows the simple theory result of Eq. (1) with fixed T (no thermal model) for the data at a bath temperature of 60 mK.

In this study, the most challenging step of the process was, in fact, the resist coating. With the simple spin coating used here, we had to fabricate ramps for the wiring and additional walls to contain the resist on top of the platform topography. However, we anticipate that by using more conformal resist coating methods, such as spray coating, the fabrication could be done over almost any type of topography, with much steeper vertical gradients.

In conclusion, we have shown that direct laser writing based on two-photon lithography can be used for the fabrication of high-quality superconducting tunnel junction devices, with our case study concentrating on normal metal-insulator-superconductor (NIS) tunnel junctions. This method can be used for fast maskless fabrication over large areas down to sub-micron scales, and it is very versatile since it uses established positive photoresists and the well-known angle evaporation and liftoff techniques. Even more importantly, we have demonstrated that the method can be used for superconducting tunnel junction fabrication on highly varying 20- μm -tall 3D topography, something that has not been demonstrated with standard lithography techniques. Such fabrication opens up a multitude of possibilities to integrate

superconducting devices with 3D geometries for applications in SQUID sensors, ultrasensitive radiation detectors, and quantum information processing, for example. We aim to use this method first to fabricate samples, which allow direct measurements of the thermal conductance of 3D nanostructures, which could provide better thermal isolation or thermalization for such applications.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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