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## Carbon nanotube field-effect devices with asymmetric electrode configuration by contact geometry

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## Carbon nanotube field-effect devices with asymmetric electrode configuration by contact geometry

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We have studied experimentally the conductive properties of single walled carbon nanotube (SWNT) based field-effect type devices, with different contact geometries at the connecting electrode. The device designs are asymmetric with one end of the SWNT having the metal electrode deposited on top and immersing it, while at the other end, the SWNT is on top of the electrode. The devices were made with either gold or palladium as electrode materials, of which the latter resulted in different behavior of the different contact types. This is argued to be caused by the existence of a thin insulating layer of surface adsorbents on the palladium, possibly  $\text{Pd}_5\text{O}_4$ , the effect of which is enhanced by the 1D nature of the contact area in the configuration with SWNT on top of electrode. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4880955>]

### INTRODUCTION

The extensive experimental research on field-effect transistors and other devices, based on individual single walled carbon nanotubes (SWNT-FET), contain as an essential element the issue of satisfactory and suitable connecting micro-electrodes. As the fabrication techniques have progressed and settled into proven procedures, the prevailing technique has been deposition of a noble metal on top of the nanotubes. Palladium (Pd) has for some time now<sup>1</sup> been the metal of choice for contacting carbon nanotubes, since it wets the nanotube well and has a work function that, if problems related to contamination of the SWNT surface are addressed well, yields a low resistive ohmic contact.

However, the superb mechanical and chemical properties of carbon nanotubes enable other solutions, as were employed already in the early years of nanotube research. Contacts to individual tubes were fabricated either by deposition of nanotubes randomly on top of pre-fabricated gold electrodes (Au)<sup>2</sup> or by depositing nanotubes first and then fabricating gold contacts directly on top of them. Note that the geometries of the nanotube-electrode contacts in these two different methods, which we henceforth call “line” and “embedded” contacts, are in principle radically different, which is illustrated in Fig. 1(a); in the line contact, the nanotube on top of the metal electrode makes a contact only along a line (black dashed line), if we ignore factors such as flattening and elasticity of the metal surface, while in the embedded contact, the nanotube surface is nearly completely interfaced by the metal of the electrode. Therefore, the difference of these two types of contact corresponds to that between 1D and 2D contact interfaces, although the distinction in this case is blurred due to the 1D character of the SWNT itself. Moreover, the line contact is much more exposed than the embedded type to the ambient environment of the device.

The experimentally verifiable differences between contacts of the type describe above, line contact vs. embedded contact, has not been explored previously. Combining them in the same nanotube would yield devices asymmetric via their contact geometry. In an earlier contribution, we studied the conductive properties of an asymmetrically contacted nanotube device where one end of the tube had a line contact with tunneling via the native oxide of a non-noble metal electrode.<sup>3</sup> However, due to the dominance of the tunneling barrier, this work did not really address the aforementioned difference between contact types.

There has been substantial work on a number of related topics: One is that on asymmetrically contacted SWNT-FET's having two different metal electrodes as embedded contacts.<sup>4-6</sup> The driving motivation has been the possibility

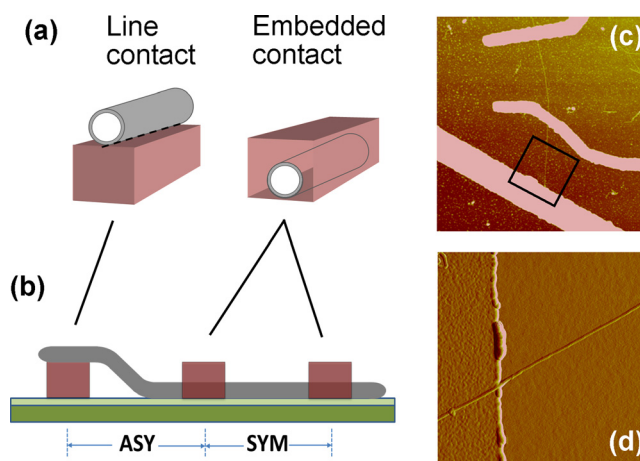


FIG. 1. (a) Illustration of different types of nanotube-metal contacts. Line contact: nanotube on top of electrode. Embedded contact: metal deposited on top of and covering the nanotube. (b) The SWNT-FET design with asymmetrically (ASY) and symmetrically (SYM) contacted sections. (c) AFM image of an actual device used in the experiments. Upper electrode pair forms the SYM section and the lower the ASY section. SWNT diameter is 2.9 nm. The square indicates the area that forms the close up image (d) (size  $1 \mu\text{m}$ ), of the line contact part of the ASY section, with SWNT on top of electrode.

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to choose the different metals so that their work functions match the valence and conduction bands at either end of the SWNT-FET. This configuration then results in Schottky barrier controlled diode behavior in semiconducting SWNT devices, and, subsequently, numerous device and circuit applications.<sup>7,8</sup> A recent development of particular interest for fundamental research has been the emergence of techniques for CVD-growth in situ of SWNT's on top of specially prepared electrodes (e.g., Pt/W),<sup>9</sup> which results in exceptionally clean nanotubes. Another closely related topic in very recent years is that on devices with carbon nanotube-graphene junctions,<sup>10,11</sup> which corresponds to the concept of a line junction. A low resistive contact between a metallic SWNT and graphene was presented in Ref. 10.

By and large, neither contact type, line or embedded, has been utilized for their intrinsic qualities. Rather, the choice has been governed for reasons of convenience or utility not directly related to the contact type. The embedded contact type has been mostly used due to ease and repeatability of fabrication and the matching of work functions. However, the line contact is potentially very interesting for some characteristic properties, where perhaps the prime one is the full exposure of the contact to the ambient, which naturally is appealing for sensor applications.

In this work, we forward the concept of device asymmetry via contact geometry, with a device design shown in Fig. 1(b), consisting of one line contact and two embedded contacts, which make up for one asymmetric and one symmetric section. We have investigated basic conduction properties in such SWNT devices. As electrode metals we have used Pd and Au (separately, that is), which are both counted as noble metals. The asymmetric device design gives us the opportunity to investigate the differences and particular properties of the contact types.

## EXPERIMENTAL

Figure 1(b) shows schematically the typical SWNT-FET device design used in this experiment, with two embedded and one line contact. The pairwise distribution of these divide the SWNT into two sections, acronymically called "ASY" and "SYM" sections, referring to asymmetric and symmetric, respectively. The ASY section has, as illustrated with Figures 1(a) and 1(b) together, one line contact and one embedded contact, while the SYM section consists of two embedded contacts. The devices were fabricated on a highly doped silicon (Si) wafer with 500 nm of thermally grown SiO<sub>2</sub>, acting as an insulator between the SWNT and the Si backgate electrode. Devices were made with either Pd or Au as the metal of the electrodes. Two steps of e-beam lithography were required for the fabrication. In the first step, the electrodes for the line contact in Fig. 1(b) were fabricated with a thickness of 20 nm. Next, SWNT (NanoCyl S.A.) suspension in dichloroethane was spin-coated onto the chip. Atomic force microscopy (AFM) was used to locate such SWNT's which had one end on top of these metal electrodes. Figure 1(d) shows a close-up AFM image of a typical such SWNT end. Then, e-beam lithography was again employed to pattern the electrodes which make up the embedded

contacts in Fig. 1(b). The last metallization was carried out to create these on-top electrical contacts with a thickness of 20 nm. Figure 1(c) shows an AFM image of a completed SWNT-FET device. The electronic measurements of all SWNT-FET's were performed in ambient condition and in a rough vacuum ( $\sim 0.01$  mbar) at room temperature, as well as at 4.2 K. The source-drain potential of  $V_{DS} = 10$  mV was kept fixed while the backgate potential ( $V_G$ ) was swept, typically in the voltage range  $-15$  V... $+15$  V. For measurements of temperature dependence, the devices were slowly cooled down to 4.2 K with a dip-stick cryogenic setup.

## RESULTS

Figure 2 shows for two Pd-based devices the current  $I$  vs. gate voltage  $V_G$  characteristics ( $I(V_G)$ ) of both ASY and SYM sections, measured at 300 K and 4.2 K. Figure 2(b) also shows more closely the temperature dependence of the  $I(V_G)$  of the SYM section. The device of Fig. 2(a) is semiconducting, with a strong transport gap with ON/OFF ratio by more than 2-3 orders of magnitude at 300 K, while in the other device (Fig. 2(b)), the transport gap opens up in earnest only upon cooling to low temperatures. In both cases, it can be observed that the ON-state current of the ASY section is significantly smaller than the ON-state current of the SYM section, by approximately 1 order of magnitude. The corresponding room temperature resistances are in the ranges 200–300 k $\Omega$  and 1–3 M $\Omega$ , for the SYM and ASY sections, respectively. At the lowest temperatures, Coulomb blockade-type oscillations of  $I(V_G)$  appears.

In Figure 3, is shown for a typical Pd-contacted device the drain-source current-voltage  $I(V_{DS})$  characteristics, measured at 300 K and 4.2 K, while the backgate potential was kept neutral ( $V_G = 0$  V). The  $I(V_{DS})$  relations of both ASY and SYM configurations are linear at 300 K, whereas being non-linear at 4.2 K. Interestingly, while the SYM configuration displays a roughly symmetrical  $I(V_{DS})$  characteristics, it is strongly asymmetrical in the case of the ASY section.

Figure 4 displays the results for two Au-contacted SWNT-FET's, on which  $I(V_G)$  characteristics were measured at 300 K and 4.2 K. The room temperature ON-state resistances vary in the range 15–500 k $\Omega$ , and for both devices, and both SYM and ASY sections, the conductance exhibits almost no gate modulation. Here, and in other Au-based devices, as

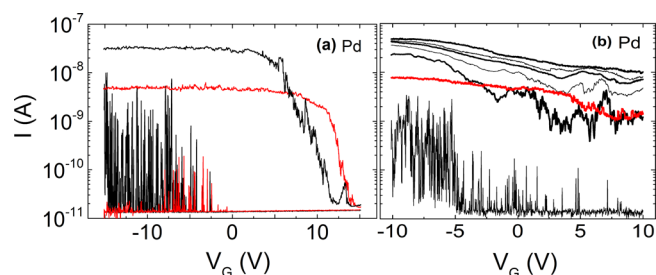


FIG. 2. The drain-source current  $I$  vs. gate voltage  $V_G$  ( $I(V_G)$ ) of two Pd-contacted SWNT-FET devices measured at different temperatures. Both devices have SYM (black) and ASY (red) sections as defined in Fig. 1(b). (a)  $I(V_G)$  measured at 300 K (upper curves) and at 4.2 K (lower) (b)  $I(V_G)$  of ASY section measured at 255 K, and of SYM section at 245, 190, 155, 97, 36, 4.2 K (in order from upper to lower).



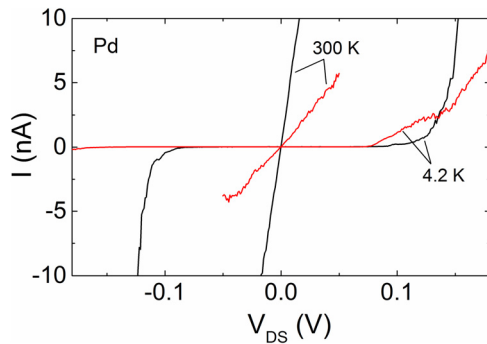


FIG. 3.  $I(V_{DS})$  characteristics (at  $V_G=0$  V) of the SYM (black) and ASY (red) sections of the Pd-based SWNT device shown in Fig. 1(d), measured at 300 K and at 4.2 K.

opposed to the case with Pd-devices, no systematical dependence on the type of contact is observed. For example, in the device of Figure 4(a), the ASY section is more conductive than the SYM section, while in Figure 4(b), the reverse is the case. Again, the Coulomb-type oscillations of current are prominent at low temperatures in both samples.

Finally, the sensitivity of the ASY and SYM contacted Pd-based devices to air has been monitored in ambient and vacuum ( $\sim 0.01$  mbar) conditions. Figure 5 shows the results for 6 devices. It is clearly seen that in all SWNT-FET's the ASY sections are more resistive, and in nearly all devices the ASY sections are more sensitive than the SYM sections to the presence of air. The resistance always decreases as air is brought to the devices.

## DISCUSSION

Before discussing those effects that stem from the asymmetric contact configuration, we briefly give a general analysis of the transport properties. The room temperature ON-state resistance values for the Pd- and Au-based devices are in the range  $10\text{ k}\Omega$ - $1\text{ M}\Omega$ . We obtain in the best case, for an ASY section in an Au-device, a resistance which is close to the limit of ballistic resistance to SWNT's,  $h/4e^2 = 6.5\text{ k}\Omega$ , while in general, the resistance can be up to two orders of magnitude higher. From the gate voltage controlled conductivity and its temperature dependence, we can deduce for certain samples a strong semiconducting behavior stemming from a sizable energy gap, as for the device of Fig. 2(a). But in the majority of samples, both Au- and Pd-based devices, there was weak gate modulation at room temperature together with a strong temperature dependence and domination of

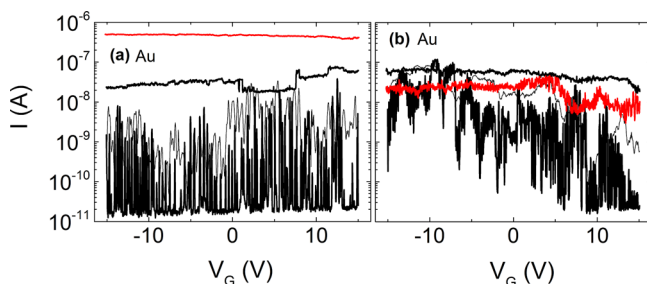


FIG. 4. The drain-source current  $I$  vs. gate voltage  $V_G$  of two Au-contacted SWNT-FET devices. The ASY (red) sections were measured at 300 K, and the SYM (black) at 300, 65, and 6 K (in order from upper to lower).

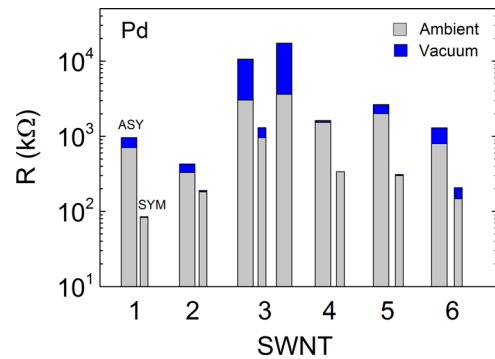


FIG. 5. Resistance at ON-state of asymmetric (ASY, wide bars) and symmetric (SYM, narrow bars) sections of Pd-based SWNT devices, measured at 300 K in ambient and vacuum conditions. Device Nr. 3 has exceptionally two ASY sections.

irregular Coulomb blockade-type conductance oscillations in the gate conduction at low temperatures, as in the samples of Figs. 2(b) and 4(a), 4(b). This latter type of behavior, and the large range of resistances, can be assigned to metallic or small-gap SWNT's which form multiple quantum dots between the connecting electrodes of the SWNT device. In both cases, we observe p-type gate controlled conductivity, which is typical to Pd-contacted single SWNT devices. These features are well known from previous work on single SWNT devices.<sup>12</sup> We next proceed to the main topic of this work.

The results clearly indicate that the ASY section, and by implication the line contacts, of Pd-based devices have a reduced electrical conductance compared to the ordinary SYM configuration, while for Au-based devices no such systematic difference was observed. The large range of resistances may imply that uncontrolled contamination give some of our contacts a rather small transmissivity, but the consistently higher resistance for the ASY sections of the Pd-devices in Fig. 5 strongly point towards an inherent cause for this.

The difference between Pd and Au as line contacts can be sought from the surface oxidation or adsorption properties of these metals. Both are considered noble metals in the most commonly used definition. However, for example, it is known that Pd adsorbs in UHV condition molecular surface layers from the ambient much more readily than does Au.<sup>13</sup> Several studies have found the emergence of 2D layers of  $\text{Pd}_5\text{O}_4$  at modest temperatures and under the presence of oxygen environment.<sup>14-16</sup> We therefore believe that an atomically thin insulating layer of palladium oxide or some other substance is formed at the surface of Pd electrodes during the fabrication of the SWNT-devices. Note that the lithographic fabrication process of the Pd electrodes include baking steps at  $\sim 100^\circ\text{C}$ . However, the thickness is very small, the layer is decisively thinner than the native oxide layer of non-noble metals like Al, Ti, etc., and in many more ordinary circumstances not even detectable, unlike the latter which are readily apparent as insulating surface coatings.

Conceivably, we see two factors at play in the resistance of the Pd line contacts. First, the line contact is close to 1D in nature, as discussed in the introduction, and thus has a lesser effective contact "area," than the embedded contact. Second, the molecularly thin insulating layer at the surface of Pd can easily exist between the Pd and the SWNT in the

line contact, but it's presence at all in the nanotube-Pd interface of the embedded contact is questionable. But even if it does exist, the much larger interface area in the embedded contact geometry compared to the line contact geometry, makes it very likely to have much lesser influence in the former. We thus postulate that the ASY section of Fig. 1(b), for Pd devices, which structurally is asymmetric, is electronically asymmetric for charge transport due to the thin insulating layer of the Pd electrode surface on the left side. Moreover, we propose that the geometry of the line contact is crucial for the exceedingly thin insulating layer to have an effect on the charge transport.

We can then discuss our measurements with this model in mind. The very residual thickness means that the insulating layer on Pd is a true tunneling barrier, without an inherent temperature dependence. The results seemingly support this conclusion as the temperature dependence of the ASY and SYM sections are rather similar. A low resistance of the palladium oxide tunneling resistance is also supported by the fact that it's energy gap is only around 1 eV.<sup>17</sup> The tunneling barrier is manifested in the  $I(V_{DS})$  curves of Fig. 3, where the asymmetry becomes apparent at low temperatures, in that the ASY section  $I(V_{DS})$  curves are strongly asymmetric, while the corresponding SYM sections are symmetric. The voltage and current range where this asymmetry is significant is quite limited compared to the case with what has been reported for the conventional asymmetric SWNT devices made from different contact metals.<sup>4-6</sup>

The results presented in Fig. 5 showed that the ASY sections of all Pd-based SWNT-FET devices are less resistive in the presence of air, while the SYM sections typically show little difference in resistance to whether the ambient is air or vacuum. Air sensitivity has also been observed, for example, in Ref. 18 for SWNT films. Based on previous experience in air, the reactive component is oxygen and the effect of nitrogen is negligible.<sup>3,18</sup> Upon O<sub>2</sub> exposure and adsorption, its electron-withdrawing power causes the doping of SWNTs with hole carriers,<sup>19</sup> which then should affect equally the resistances of ASY and SYM sections. As this is not so, one assumes the sensitivity of the line contact in particular to the air exposure, given the previously noted radically different susceptibility to the ambient of the line contact, compared to the embedded one.

The work functions of Pd and SWNT, are 5.22–5.6 eV (Ref. 20) and 4.9 eV (Ref. 6), respectively. Oxygen doping of carbon nanotubes results in an increase of its work function.<sup>3,19</sup> Assuming that the work function of Pd is not affected significantly by the oxygen, then the work function difference between Pd and the SWNT would decrease, which would roughly explain the increased conductance in air compared to vacuum. It is very well conceivable that an optimization of this kind of line contacts, e.g., with functionalization of either the metal or nanotube surfaces, could yield a very good sensitivity of it as a gas sensor.

## SUMMARY

In summary, we have explored the basic conduction properties of asymmetrically contacted SWNT devices, with

line and embedded contact types, that are well known, but the differences of that have not been properly explored before. With Pd as the electrode material, the asymmetric section has a substantially higher resistance, exhibits asymmetric  $I-V_{DS}$  characteristics, and enhanced sensitivity to oxygen in its environment. This is seen as a consequence of a molecularly thin insulating surface layer on the line contact, possibly Pd<sub>5</sub>O<sub>4</sub> formed at the interface between Pd and the SWNT. It is also argued that the effect of this molecular layer on the contact resistance is accentuated by the one dimensional nature of the line-type contact. Line contacts, as described here, utilize the unique mechanical strength and chemical inertness of SWNT's and are promising for further studies in niche applications such as nanoscale gas sensors. These results should be of interest both for fundamental studies on the character of the electronic contact between metal electrodes and nanotubes and for various applications.

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