Measurements on Electric Breakdown in Dielectric Barriers between Carbon Nanotubes and Electrodes

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Preface

This Master's thesis was commenced in fall 2008 in Molecular Technology research group at the Department of Physics at the University of Jyväskylä. Most of the experiments were done during spring 2009 with the collaboration of other members of the group: Professor Markus Ahlskog, PhD Andreas Johansson and MSc Peerapong Yotprayoonsak.

I would also like to thank MSc Davie Mtsuko who has helped me with the measurement equipment and given user comments on the LabVIEW program which was used for device control and data acquisition. I thank my parents Päivi and Erkki, my sister Laura and my brothers Martti and Anton for encouragement and prayers.

Finally, I would like to express my deepest gratitude towards my husband Matti for all the help and support I have received.

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Tiivistelmä

Eristeen (eristevakio κ) läpi kulkevaan virtaan tarvitaan niin sanottu läpilyöntikenttä. Tässä työssä tarkastellaan nanoputken ja johtimen välissä olevan eristeen läpi kulkevaa läpilyöntivirtaa ja sitä aiheuttavaa jännitettä. Virta tunneloituu ohuiden ($\sim$nm) eristeiden läpi jo pienillä jännitteillä.

Uutta, nopeampaa ja pienikokoisempaa teknologiaa odotetaan niin kutsutuilta hiilinanoputkikanavatransistoreilta (*engl.* CNTFET), joiden erilaisia hilarakenteita esitellään ja vertaillaan keskenään. CNTFETit rakennetaan tavallisten kanavatransistorien lailla korvaamalla kanava hiilinanoputkella. Transistoreja käytetään digitaalielektroniikassa kytkiminä.

Virran ON/OFF suhde $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ kuvaa transistorin hyvyyttä. Sen arvoksi mitattiin $I_{\mathrm{ON}}/I_{\mathrm{OFF}} \approx 100$, mikä on kohtuullinen arvo verrattuna parhaisiin tuloksiin, jotka yltävät jopa miljoonaan yksikköön. Mitattu transistori käytti nk. pohjahilaa (*engl.* bottom gate), joka ei ole yhtä tehokas kuin viime aikoina suosittu päällishila (*engl.* top gate).

Luotettavan toimivuuden takaamiseksi kanavatransistoreiden kytkimenä toimivan hilan eristeen läpi ei saisi kulkea virtaa, ja työssä testattiin hilaoksidin kestävyyttä eli läpilyöntiä. Oksidin hajoamista tutkittiin kahdessa eri eristeessä: titaanioksidissa TiO_2 ja alumiinioksidissa Al_2O_3. Tunneloitumisilmiötä ei tapahtunut kummassakaan materiaalissa.

Materiaaleissa ei ollut huomattavaa eroa läpilyönnin jälkeisen differentiaalisen vastuksen ja läpilyöntijännitteiden arvoissa. Differentiaalinen vastus oli luokkaa $10 \ldots 1000\ \mathrm{M\Omega}$. Läpilyöntijännitteiden itseisarvoiksi saatiin $0.2\ \mathrm{V} \ldots 6\ \mathrm{V}$ alumiinille ja $3.3\ \mathrm{V} \ldots 16\ \mathrm{V}$ titaanille. Titaanin läpilyöntikestävyydeksi saatiin siis noin $20\ \mathrm{MV/cm}$ ja alumiinille noin $10\ \mathrm{MV/cm}$.

Tuloksista voidaan päätellä, että Al_2O_3:lla ja TiO_2:lla läpilyönti ei ole symmetrinen jännitteen suhteen, eli positiiviset ja negatiiviset läpilyöntijännitteet eivät ole itseisarvoiltaan samansuuruisia.

Jokaisen läpilyöntimittauksen aikana oksidissa tapahtuu pysyväisluotoisia muutoksia, jotka vaikuttavat seuraaviin mittauksiin. Kuitenkaan mittausten järjestysluvulla ei näyttänyt olevan selvää riippuvuutta läpilyöntijännitteeseen. Läpilyöntijännite on myös aikariippuvainen: oksidi hajoaa tietyn ajan jälkeen, vaikka jännite ei ylittäisi kriittistä arvoa.

Näytteiden alustana toimivan 300 nm paksuisen piioksidin läpilyöntijännitteksi saatiin $50 \ldots 77\ \mathrm{V}$, joten oksidin kestävyys on $1\ \mathrm{MV/cm}$.

Abstract

The main focus of this Master's thesis is in carbon nanotubes (CNTs) and dielectric breakdown (BD), with a discussion of carbon nanotube field-effect transistors (CNTFETs).

Carbon nanotubes have given a new approach to micro- and nanoscale physics. In particular, carbon nanotube field-effect transistors have created expectations and demand for smaller and faster electrical elements. CNTFETs are field-effect transistors (FETs) with the channel between the source (S) and drain (D) electrode replaced with a carbon nanotube.

Current ON/OFF ratio I_{ON}/I_{OFF}, a central property of a CNTFET, was measured to be $I_{ON}/I_{OFF} \approx 100$. This coincieds more or less with previous studies in CNTFETs, I_{ON}/I_{OFF} being up to 10^6. The measured CNTFET used back-gating which is not as efficient as top-gating which has recently become more popular.

Oxide breakdown and tunneling in two insulators, aluminium oxide Al_2O_3 and titanium dioxide TiO_2, was researched. Only breakdown phenomenon was noticed even though the thickness of the oxides is of the order of 2 nm.

There seemed to be no remarkable difference in these two materials with respect to post-BD differential resistances and threshold voltages. Differential resistance was of the order of $10 \ldots 1000$ MΩ and threshold voltages (in absolute value) were between 0.2 V and 6 V for aluminium and 3.3 V and 16 V for titanium. This corresponds to a breakdown electric field of circa 2 $^{MV}/_{cm}$ for Ti and 10 $^{MV}/_{cm}$ for Al.

Furthremore, it was discovered that the BD behaviour is asymmetric in both materials, i.e. sequential positive and negative threshold voltages differ in absolute value. The reason for this behavour is supposedly in time-dependent breakdown (TDDB): the positive breakdown was measured before the negative BD, damaging the sample between the experiments. However, there was no clear correlation between the ordinal number of the experiment and its threshold voltage.

The breakdown of a 300 nm thick silicon (back gate) oxide occured at $50 \ldots 77$ V. This suggests that SiO_2 has a breakdown strength of 1 $^{MV}/_{cm}$, correlating well with earlier research in low-κ dielectric breakdowns.

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Chapter 1

Introduction

The research on carbon nanotubes face not only great expectations but – during the past ten years – also progress. Although nanotubes were identified already in the 1970s [67; 88], it took decades until they were studied profoundly. This was also due to lack of technology: microscopy methods, such as scanning tunnelling microscopy and atomic force microscopy, were only developed in the 1980s. These methods have become a necessity for modern sample fabrication.

Carbon nanotubes, previously known as carbon nanotubules, were first of the size of tens of nanometers. Because carbon nanotubes were only at times small [24, p. 14-15], CNTs were long thought to be only multi-walled nanotubes (MWNTs) [23, p. 676-9].

As MWNTs were rediscovered – actually third time in a century [67] – in 1991 by Sumio Iijima [36], a new era of nanophysics began. Single-walled carbon nanotubes (SWNTs) were discovered two years later in 1993 by NEC and IBM groups [9; 37]. Carbon nanotubes are of great interest, possibly replacing traditional materials in electronics in the future.

Both MWNTs and SWNTs are part of devices fabricated for this project. SWNTs are utilized for basic $i - v$ curves and CNTFET experiments, whereas MWNTs used for oxide breakdown measurements.

One part of a carbon nanotube field-effect transistor is the gate where the switch's ON/OFF voltage is applied. The gate is insulated from the rest of the transistor with a gate dielectric. The insulator is crucial point regarding the CNTFET's operation; no current through the dielectric is allowed in order for the CNTFET to function normally. In other words, breakdown is not tolerated.

Electronic breakdown (BD) is a complex, irreversible process which takes place when applying an unbearably amount of voltage over a sample. The voltage causing this sudden current rise is called the threshold voltage V_T. In this work, breakdown is studied in electrode oxides, representing the CNTFET's gate oxide.

Breakdown is a very important topic in electrical applications: the temperature rises with leakage current which makes the BD process harmful for integrated circuits (ICs). In addition, moisture in low-κ dielectrics (such as the popular SiO_2) reduces its breakdown strength and time-to-failure (TF) in TDDB [90].

Chapter 2

Theory

Current, breakdown, tunneling and dielectrics are central concepts in electronics, being of interest in this Master's thesis. In addition, single-walled carbon nanotubes (SWNTs) and their electrical properties are presented.

The last sections address carbon nanotube field-effect transistors (CNT-FETs) and scanning probe microscopy (SPM).

2.1 Short introduction to single-walled carbon nanotubes

Single-walled carbon nanotubes are formed by rolling a layer of graphene into a tube, see figure 2.1. Graphene is a single layer of graphite which is an allotrope of carbon. The name of graphite comes from the Greek $\gamma\rho\alpha\phi\epsilon\iota\nu$ (graphein) [93].

Figure 2.1 demonstrates the molecular structure of graphene. Van der Waals (vdW) force keeps the graphene layers together; the same force that holds a bundle of SWNTs together [15].

The synthesis of carbon nanotubes is not discussed here but described in detail e.g. in [47].

2.1.1 Chirality

Single-walled carbon nanotubes can be either metallic or semiconducting. The $i - v$ curve of the semiconducting SWNTs is nonlinear even at room temperature [64, p. 272-273] whereas the metallic tubes have a linear response, with resistivity increasing linearly with temperature [50].

The type of conductivity (metallic/semiconducting) is determined by the chiral vector $\mathbf{C_h}$ of the tube i.e. in which angle the tube has been rolled up together, see figure 2.1. The diameter of the carbon nanotube is $d = |\mathbf{C_h}|/\pi$ [5, p. 606].The chiral vector is defined as

$$\mathbf{C_h} = n\hat{\mathbf{a}}_\mathbf{1} + m\hat{\mathbf{a}}_\mathbf{2}, \tag{2.1}$$

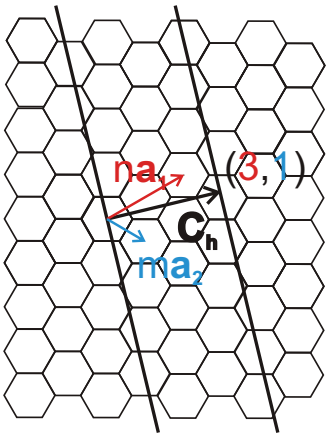


Figure 2.1. A carbon nanotube is formed from a graphene honeycomb lattice by rolling it along the chiral vector C_h. The diameter of the carbon nanotube is $d = |\mathbf{C_h}|/\pi$. The CNT in the figure is (3,1) and is semiconducting; see equation (2.2). Adapted from [5].

where $\hat{\mathbf{a}}_\mathbf{1}$ and $\hat{\mathbf{a}}_\mathbf{1}$ are the unit vectors of the graphene lattice [7; 58]. The chiral indices (n, m) determine whether the nanotube is semiconducting or metallic, see equation (2.2).

$$\text{CNT is } \begin{cases} \text{metallic}, & \text{if } n - m = 3j, \text{ where } j = 0, 1, 2, \ldots \\ \text{a semiconductor}, & \text{if } n - m \neq 3j \end{cases} \tag{2.2}$$

[5, fig. 1]. About $2/3$ of the CNTs are semiconducting, which can be seen from (2.2): in two out of three cases $n - m \neq 3j$ ($\Rightarrow$ CNT is a semiconductor), if n and m are arbitrary.

The chiral indices (n, m) were first determined by electron diffraction, which is still much in use. Both Bessel-function analysis and intrinsic layerline distance analysis belong to the recently used techniques of electron diffraction [46, p. 70]. One can also use Raman spectroscopy to find the chiral indices [31].

Special cases of the chiral vectors have a specified name:

$$\text{CNT is } \begin{cases} \text{armchair type}, & \text{if } n = m \\ \text{zigzag type}, & \text{if } n > 0 \text{ and } m = 0 \\ \text{chiral}, & \text{if } n \neq m \end{cases} \tag{2.3}$$

[3; 15; 86]. The usage of zigzag and armchair words was suggested by Dresselhaus et al. already in 1992 [22, p. 44-45]. The names come from the shape of the C-C bonds' edge cut orthogonally to the tube.

2.1.2 Band structure

Graphite is a semimetal or zero-gap semiconductor [5, p. 606]. There are two kinds of C-C bonds in graphene: π and σ bonds. The π and π^* state overlap in the vicinity of the Fermilevel E_F, but the σ and $\sigma*$ have a 12 eV gap between each other and thus these band do not play a big role in the band structure and the graphite becomes a zero-gap semiconductor. [15, p. 672-7]

The band structure of a CNT is formed from that of a graphene sheet: all the bands are split into subbands as the 2D graphene is processed into a 1D nanotube [7, p. 2][10, p. 455-493] . The band gap E_g of the tube is inversely proportional to its diameter, $E_g \propto 1/d$ [7, p. 3, 11], or more specifically,

$$E_g = \frac{4\hbar v_F}{3d_{\text{CNT}}} = \gamma \frac{2R_{\text{C-C}}}{d_{\text{CNT}}}, \tag{2.4}$$

where γ is the hopping matrix element ($\sim$3 eV), R_{CC} is the CC bond length and d_{CNT} is the CNT diameter [80].

The subbands can be found by plotting the CNT capacitance against top gate voltage [38, p. 690].

2.1.3 Schottky-barrier in carbon nanotubes

Schottky-barriers (SB) affect the electronic properties of CNT devices. The SB height determines whether the tube is n or p type i.e. the polarity of the material [6, p. 435]; this leads to the fact that high work-function metals (Pd, Rh) make p-type contacts to tubes and low work function make good n-type contacts [10, p. 461].

While the SB height determines polarity of the CNT, the SB width is a function of the gate oxide thickness and the dielectric constant. The SB width does not strongly depend on the CNT diameter [6; 29; 76].

2.1.4 Defects in carbon nanotubes

Disorder in CNTs can cause for example bending [2, p. 141] and changes in the CNT's electrical, thermal, optical and mechanical properties [10; 89]. The determination of the level of defects is important in manufacturing since defects have a strong influence especially on devices [89, p. 5].

Some defects are, though, interesting and not necessarely a disadvantage: e.g. a heptagon-pentagon pair in the CNT lattice can turn the CNT into a diode if the other part of the tube is metal and the other semiconducting [46, p. 77].

There are three main sources of defects: lattice defects, electrostatic potential fluctuations and mechanical deformations. The first type, lattice defects, are localized and are many times due to harmfull sample processing. The defects influence the electronic properties of CNTs: molecules

adsorbed on the CNT changes the electrostatic potential and mechanical defects have effect on the local bandgap [10; 66].

Strong defects influence the CNT's properties already at room temperature whereas weaker defects can only be detected in low temperatures [10, p. 463]. This means that cleaner samples should only be measured at room temperature. However, the Johnson noise during the measurement is $V^2_{\text{noise}} \sim k_B T$ which states that the thermal noise is smaller in low temperatures [33, p. 431] and so low temperatures should be favored in all measurements.

Sample processing is one of the reasons for CNT lattice defects: the deposition of CNTs may harm the sample and form defects if the sonication method is used, see section 4.4.8.

2.2 Short introduction to multiwalled carbon nanotubes

Monthioux and Kuznetsov [67] show that multiwalled carbon nanotubes were in some sense discovered already in 1889. Since then many articles have been published on MWNTs [67, p. 1623].

Multiwalled carbon nanotubes differ from single-walled in various ways. Having many shells, MWNTs are more complex and their electronic characterization is more difficult. At room temperature, MWNTs have a linear voltage response [1, p. 1] (see section 5.2.1 for measurement data) as semiconducting SWNTs are nonlinear [64, p. 272].

The $i - v$-curve of the MWNT changes with temperature. In 1998 it was suspected that multi-walled carbon nanotubes do not usually show gate field-effect unlike single-walled [61, p. 2447]; this would make them quite unsuitable for CNTFETs. In the same article it was found that collapsed (i.e. transformed) MWNTs do fit for CNTFETs as the defect changes the tube's electrical properties. However, in 2008 there was a successful study about MWNTs as FETs which stated that also MWNTs can be used for CNTFETs [57].

2.3 Carbon nanotube field-effect transistors

Carbon nanotube field-effect transistors are field-effect transistors where the semiconductor channel has been replaced with a semiconducting carbon nanotube. The silicon gate in the CNTFET is usually highly doped so that it is conducting still at low temperatures [31].

CNTFETs and MOSFETs are quite similar with a few differences. CNTFETs act as Schottky-barrier (SB) transistors when MOSFETs act as bulk-switching transistors [6; 40]. Different gate structures of CNTFETs are discussed in section 2.4.

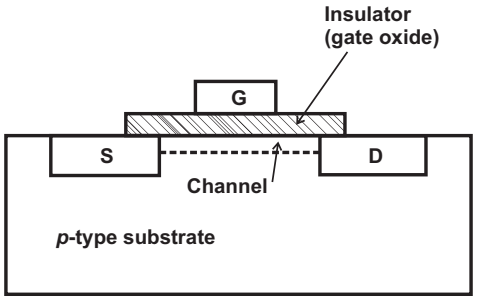


Figure 2.2. A side view of an $n-$type MOSFET or an NMOS FET. When the gate voltage V_g is high enough an n-type channel is created between source and drain allowing source-drain current to flow, setting the transistor to ON state. Adapted from [25].

2.3.1 Field-effect transistors

A significant breakthrough in electronics took place in 1962 when Steven Hofstein and Frederic Heiman invented the metal-oxide field-effect transistor (MOSFET) [87], see figure 2.2. MOSFETs are frequently used as ON/OFF switches, see the comparison of MOSFETs to CNTFETs in [6, p. 435].

2.4 Different gate structures of CNTFETs

There are various ways of constructing CNTFETs. The bottom gate structure is in figure 2.3a and the top gate structure is in figure 2.3b. Both top and bottom gate can be used in the local gate structures, see figures 2.4a and 2.4b.

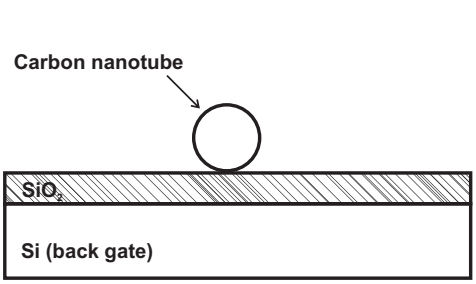
In this section silicon (Si) is used as the back gate and silicon oxide (SiO_2) as the back gate oxide. If no local gate (see section 2.4.3) is used, Si works as the gate. Substrate material is discussed in detail in section 4.4.1.

2.4.1 Bottom-gate structure

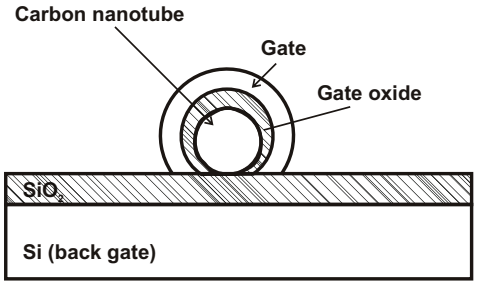
The bottom gate structure uses the Si back gate as the gate and the silicon oxide as the gate oxide. The CNT lies on top of the gate, see figure 2.3a. The drain and source electrodes have been omitted for clarity. Bottom-gating was the dominant gating method until 2002 when also top-gating was successfully studied [96].

2.4.2 Top-gate structure

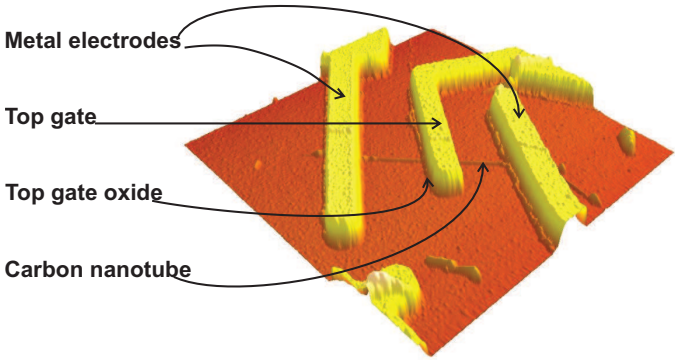
The top gate structure is in figure 2.3b. In this structure, the CNT is on top of the silicon chip and is surrounded be the gate oxide and finally, the gate. The silicon can be used as the back gate and if the CNT is not covered in



(a) The bottom-gate structure from side: the CNT is on top of the gate oxide. The CNT is affected totally by the gate, in contrast to local gates, see figure 2.4. The CNTFET uses the Si back gate as the (bottom) gate.



(b) The top-gate structure: the (local) gate is on top of the carbon nanotube. The area of the CNT affected by the gate is considerably larger in the top gate structure compared to the bottom gate structure, see figure 2.3a.



(c) A top local gated CNTFET structure from top. Carbon nanotube, the FET's channel, is connected to metal source and drain electrodes from its ends. Top gate is deposited on top of the CNT, with an oxide layer in between. Jaakko Leppäniemi, Master's thesis, 2008

Figure 2.3. Side views of bottom and top gate structures for a CNTFET. The contact area is considerably smaller in the bottom gate than in the top gate structure. Source and drain electrodes have been omitted for clarity.

whole by the gate (oxide), the gate works as a local gate, see section 2.4.3. The drain and source electrodes have been omitted for clarity.

Comparing top and bottom gate figures 2.3b and 2.3a one can observe that the contact area of the CNT and the gate oxide is considerably larger in the top gate structure. This might lead to the fact that top gates are more stable and thus have been researched more during the past years.

Wind et al. [96] found out that top-gate devices with a thin gate dielectric are more effective bottom-gated structures: the subthreshold slope is steeper and the transconductance is higher.

2.4.3 Local gating

A carbon-nanotube FET can be modified and made into a FET with more than one gate: the silicon acts as a back gate (common to all parts of the CNT) and the gates touching only parts of the CNT act as local gates. The local gate affects only one part of the CNT. There are both top local gates and bottom local gates, see figures 2.4b and 2.4a.

Local gating acts mostly the same way as the back gate. However, while the back gate affects the whole structure (source, drain and the CNT), the local gate only has effect on the CNT and this way high value of V_G does not break the S and D electrodes [77].

Another way of constructing a local gate is to use split-gates. This method is discussed in [10] and [55].

Bottom local gate

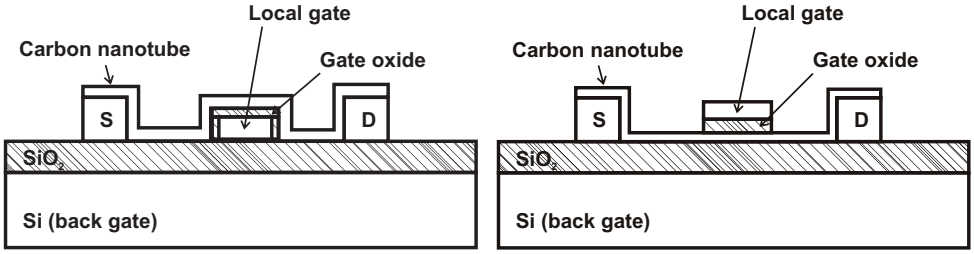
The bottom local gate structure is shown in figure 2.4a. Like in the "normal" bottom gate structure (see section 2.4.1), the bottom local gate has little physical contact with the nanotube.

Because the CNTs are often spinned randomly on the sample it is very unlikely that a single CNT would cross the three electrodes (source, drain and the local gate). That is why the S and D electrodes are usually deposited after the CNT deposition and they are on top of the CNT (unlike in the figure). This does not affect the device's electrical properties, though.

Top local gate

Figure 2.4b shows the top local gate structure. Top local gating has become quite popular because they enable having many devices on a single CNT [43].

Top local gating also has the good sides of top gating such as good transistor performance when using high-κ gate dielectric. Transistor performance is evaluated by the subthreshold swing $S = \log_{10}(\mathrm{d}V_{\mathrm{G}}/\mathrm{d}V_{\mathrm{DS}})$, de-



(a) The bottom local gate structure: the CNT is on top of the local gate.

(b) The top-local-gate structure: the local gate is on top of the CNT.

Figure 2.4. Bottom and top local gate structures. Compare to figure 2.3.

scribing the effectiveness of the gate voltage in turning off the device. [10, p. 467]

2.5 Dielectric breakdown

Oxide breakdown (BD) means an irreversible process where the gate leakage current grows abruptly [60] through the oxide, see figure 2.5. The value of the threshold voltage (above which the BD occurs) depends on the material and its dielectric constant κ, including time dependence.

The breakdown current starts flowing after the bulk defect density has grown to a critical point, the size of the defect being of the order of 1 nm [60].

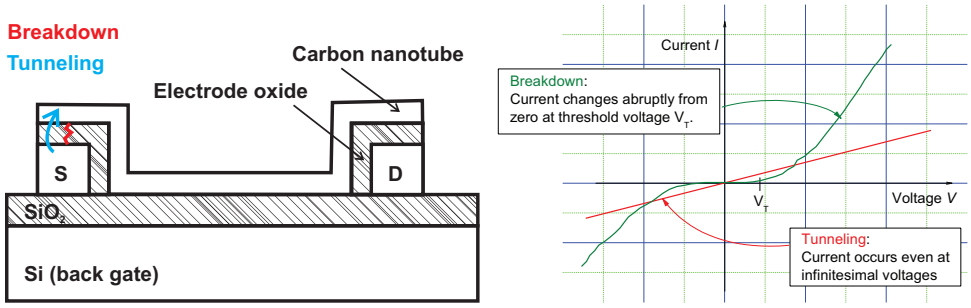
By now (2009) many new high-κ dielectrics have been found after the article of Lombardo et al. in 2005. These high-κ insulators have made it possible to apply greater voltages to thinner gate oxides with much less or no damage by the BD. See section 3.3.1 for more information on high-κ and ultra-thin gate dielectrics.

There are two types of breakdowns: dielectric [60] and intrinsic [83] BDs. The dielectric BD is due to malfabrication which might show as ununiform gate oxide (see section 5.1.1), metal impurities and other defects. This type of BD can be observed at low electric fields and can, by definition, be minimized by developing the sample processing technology [60].

Unlike the dielectric BD, the intrinsic BD is observed at high fields. There is still discussion whether the intrinsic BD is totally intrinsic or not: There is evidence that hydrogen (H) produces partly the intrinsic BD by impurifying Si and SiO_2. This is called hydrogen cracking [20].

It is also possible that the intrinsic BD is purely intrinsic as proposed by the anode hole injection (AHI) model [20]. AHI suggests that BD is created at high electric fields as energy is released from current carriers travelling through the dielectric and is then reformed to defects in the oxide [60].

Insulators of over 3 nm of width have a small probability of tunneling



(a) The current through the electrode oxide and the nanotube is due to either tunneling or breakdown. Tunneling occurs at small voltages, forming a linear $i - v-$ curve. If the electrode oxide is this and the electrons cannot tunnel through it, breakdown occurs at the threshold voltage V_T breaking the oxide.

(b) The difference of tunneling and BD $i - v$ curves. Tunneling current flows at infinitesimal voltages. BD occurs at the threshold voltage V_T, allowing sudden current change.

Figure 2.5. The differences in breakdown and tunneling in dielectrics. The tunneling electrones appear on the other side of the oxide quantum mechanically whereas breakdown current flows through the oxide damaging the sample.

but rather confront breakdown at the threshold voltage V_T. Too high a current rise during a BD measurement might cause changes in the V_T value, see section 5.2 for measurement results.

In addition, BD may affect possible defects in the oxide, destroying the insulator and letting the current flow at infinitesimal voltages.

Electrical applications and devices can all suffer from BD, it is only a matter of time and applied electric field E. For low-κ dielectrics, the time-to-failure increases exponentially as the electrical field decreases [90] – evidently, it is vital to know the operating field of an electrical device for it to function properly. The operating field is the maximum field at which a device works for a minimum of 10 years [73; 90].

2.5.1 Carbon nanotube breakdown

Carbon nanotubes only endure a certain amount of current density J (up to 10^9 $\mathrm{A/cm^2}$ [98]); above this level the overload of current crashes the CNT sample. If the radius of a CNT is 1 nm to 10 nm, ideally, the maximum current it can carry is

$$\begin{aligned} I_{\max} &= 10^9 \cdot \pi r^2 \\ &\approx 3 \cdot (10^{-5} \ldots 100^{-5})\ \mathrm{A} \\ &\approx 30\ \mu\mathrm{A} \ldots 3\ \mathrm{mA}. \end{aligned} \tag{2.5}$$

The current due to dielectric breakdown supposedly causes a punch-through in the CNT, too, see figure 2.5a.

Unlike the oxide, the CNT undergone a BD does not allow the current to flow due to physical breaking of the C-C bonds in the nanotube. This changes the post-breakdown behaviour: In the ensuing measurement the BD takes place at the BD level of SiO_2.

2.6 Tunneling

Tunneling is a quantum phenomenon which exceeds the laws of classical mechanics. Electrons may tunnel through a potential barrier (a classically forbidden area) of finite height and finite width.

More specifically, this means that current can flow through a thin oxide. The probability of tunneling is the greatest with very thin oxides (circa 10-20 Å [53, p. 364][23, p. 482] or 3 nm according to [60]), decreasing exponentially with oxide thickness.

The tunneled electron appears on the other side of the oxide without harming the insulator in any form, see figure 2.5a. At small voltages, the $i - v$ curve of tunneling is a constant-slope curve [23; 53]. Tunneling can be distinguished from the BD graph by having a linear output already at infinitesimally small voltages, see figure 2.5b.

2.7 Measuring breakdown and tunneling in carbon nanotube devices

Breakdown and tunneling effects are measured on similar devices. Consider we have a metal-oxide-CNT-oxide-metal sample and that the CNT is a semiconductor, see figure 2.6. By placing a voltage source and an ammeter between the source and drain electrodes, following properties of the sample can be found:

$$\begin{cases} i - v \text{ curve of the CNT,} & \text{if } d \text{ is leaky or non-existing} \\ \text{direct tunnelling measurements,} & \text{if } d \text{ is small} \\ \text{oxide BD measurements,} & \text{if } d \text{ is large} \end{cases} \tag{2.6}$$

where d is the thickness of the oxide layer. However, if there is no sample between the electrodes, we can find the BD of the silicon oxide (back gate), see section 5.2.

2.8 About electrode materials in the work

The choice of electrode material has a widespread effect on the functionality of an electronic device. The usage of three different electrode materials

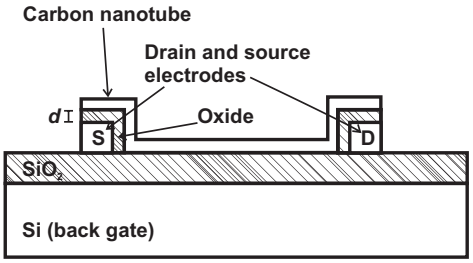


Figure 2.6. The width of the oxide layer d determines what can be measured, see equation (2.6).

is discussed: aluminium (Al), palladium (Pd) and titanium (Ti).

Palladium seems to work exquisitely as the electrode material: the high work-function ($\phi_{\mathrm{Pd}} = 5.1$ eV [16]) metal has a low contact resistance and it makes ohmic contacs to tubes [10; 16; 41]; high work-function does not assure ohmic contacts, however [10, 462].

Of the three metals, Pd makes the best contacts to carbon nanotubes (to tubes preferably of over 1.4 nm in diameter) and thus should be favoured as the drain/source material. [16; 42]. On the other hand, palladium as a noble metal [51] does not suit well for tunneling or BD measurements because it does not form a native oxide.

Aluminium forms a native oxide Al_2O_3 on top of it, making it a good choice for BD measurements. Aluminium is a low work-function ($\phi_{\mathrm{Al}} = 4.1$ eV [16]) material [10] and of the three metals, its ON current I_{ON} in a CNTFET is the smallest [16] i.e. the SB at the nanotube-metal junction limits the conductance the most [42].

The electrical properties of titanium are closer to that of the aluminium than to palladium. Titanium forms an oxide layer (TiO_2), too, and it is a low work-function ($\phi_{\mathrm{Ti}} = 4.3$ eV [16]) material.

Even though there are significant contact differences in various metals, it is important to note that the ratio between the CNT length and the CNT-metal contact area should always be maximized [4].

Future challenges include research on improving contacs to metals other than gold (Au) or palladium which evidently make good contacts. One solution could be achieved by altering the SB height by coadsorption at the metal-CNT junction, as was done in [19]. Furthermore, CNTs with diameter less than 1.5 nm do not yet make ohmic contacts to electrodes [10].

2.9 Scanning probe microscopy

Scanning probe microscopy (SPM) is an umbrella term for microscopies using a sharp tip to discover properties of a small sample [46, p. 71-6]. The two most used methods of SPM are scanning tunneling microscopy (STM)

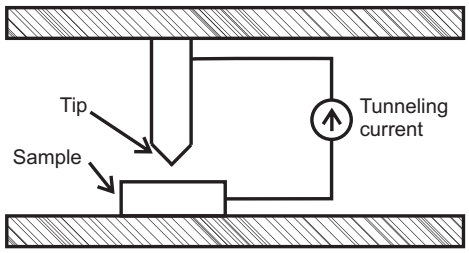


Figure 2.7. A scanning tunneling microscope (STM). Both the sample and the tip have to be conducting so that the tunneling current flows. The magnitude of the current gives information about the electrical properties of the sample.

and atomic force microscopy (AFM).

2.9.1 Scanning tunneling microscopy

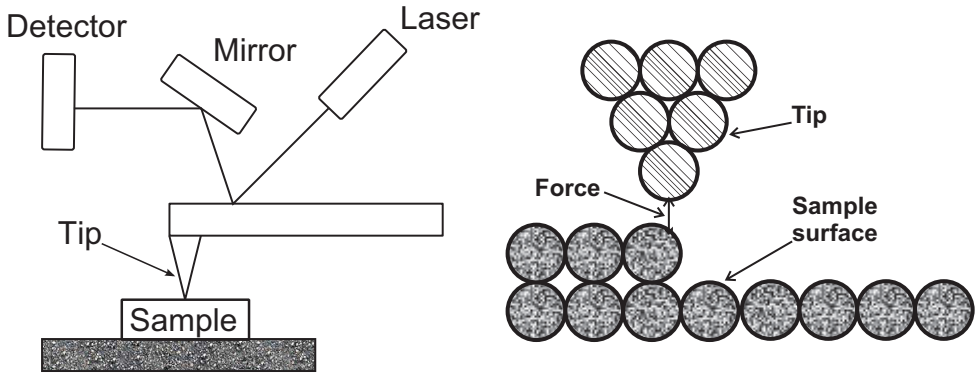
Scanning tunneling microscopy (STM) is used to find electronical properties of a sample. It was invented in 1982 by Gerd Binnig and Heinrich Rohrer, being the first SPM in the world. In STM, both the sample and the tip have to be conducting so that the tunneling current flows [30], see figure 2.7. STM method is used despite imaged samples are limited to conducting ones, because the STM method is more precise than the AFM method.

The idea behind the STM theory is simple: The tunneling current between the probe and the sample is kept constant by changing the altitude of the probe. This way also the distance between the sample and the probe is unchanged (the probe follows the surface of the sample from a distance) and the controller saves the path of the probe forming an image of the surface. [71]

2.9.2 Atomic force microscopy

Atomic force microscope (AFM), in turn, finds the molecular structure of a sample by touching the surface with a tiny tip. AFM was invented the same year Binnig and Rohrer received the Nobel prize for STM, 1986 [30]. The operation of an atomic force microscope is in figure 2.8a.

AFM uses a laser beam to detect the surface of a material: the beam is directed onto a cantilever and reflected via a mirror to a detector. The force between the sample and the tip is kept constant by moving the cantilever up and down, see figure 2.8b. The force in question is a sum of many different conservative and dissipative [26, p. 51] forces and interactions [32, p. 6]: steric repulsion, van der Waals, electrostatic, elastic [75], magnetic and specific chemical binding interactions [35, p. 992].



(a) An atomic force microscope. The laser is reflected from the laser source to the detector via a mirror. The cantilever changes its altitude according to the sample surface and the path of the laser is drawn to the detector.

(b) The force between the sample surface and the tip. This force is kept constant by altering the altitude of the tip. The force is a sum of many long and short range forces making exact calculation difficult. Adapted from [71].

Figure 2.8. Figures show the AFM and the force between the tip and the sample.

Because the force of the tip is propotional to the distance between the cantilever tip and the surface, changes in the sample surface cause changes in the laser beam position at the detector and the image of the surface is acquired. See more of AFM usage in this thesis in section 4.5. [71]

Atomic force microscopy can be used also e.g. for studying the mechanical properties of carbon nanotubes: if, for example, the AFM tip bends the nanotubes, the lateral force of the tip can be measured. [97, p. 169] [59]

Chapter 3

Previous Studies

Technology needs discoveries. A recent invention of the 45-nm technology by Intel Corporation [13; 63] was an opening to nanotechnology: high-κ transistors with metal gate solved many problems including the size of one transistor.

Already in 2006 Chen et al. brought off an integrated circuit on a single carbon nanotube [17]. This was a promising step towards more complex circuits. In the beginning of 2009 Rinkiö et al. published an article about high-speed CNTFET memory elements [78]. The article shows that CNTFETs can operate with 100 ns write/erase speed; this is faster than the fastest flash memory elements [77].

3.1 Research on carbon nanotubes

Novoselov et al. [72] studied the electric field effect in thin carbon films. This material, few-layer graphene (FLG), gives information on e.g. carbon nanotubes and other carbon-based material [72]. The differences between the properties of the studied graphene films and carbon nanotubes are considerable, however: CNTs are one-dimensional and metallic or semiconducting as the studied films are two-dimensional and always metallic.

Charlier et al. [14] had a theoretical aspect in their paper about electronic transport properties of CNTs in 2007. Quantum dots were researched by Mason et al. in 2004 [62] and by Grove-Rasmussen et al. in 2008 [28].

The "nanotube rush" has also reached the traditional literature. Springer published a book about carbon nanotubes in 2008 by Ado Jorio et al. (eds.) [45] for reviewing past years' articles as nanoscience is becoming nanotechnology [88, Preface].

The CNT band structure was researched in 2004 by Stojetz et al. [84] and by Avouris et al. [7], among others.

3.2 Carbon nanotube field effect transistors in literature

Carbon nanotube field-effect transistors are studied in a number of articles. In 2004, Seidel et al. [81] researched nanotube FETs with sub-20 nm channels that gained over 10^6 on/off current ratios. The same year also Avouris et al. [7] wrote an article about carbon nanotube electronics and optoelectronics. They studied CNTFETs comparing them to MOSFETs. Avouris continued the same subject in 2008 [6].

Carbon nanotube field-effect transistors have also been researched by Bachtold et al. in 2001 (bottom gate structure) [8], by Biercuk et al. in 2004 (local gating and bottom local gating) [11; 12], by Kaminishi et al. in 2005 (CNTFETs with Si_3N_4 passivation films, bottom gating) [49], by Weitz et al. in 2007 (SAM) [92], by Hu et al. in 2007 (top gate complementary inverter; comparison of top gate and back gate) [34], by Lefebvre et al. in 2008 (electric-field dependence of PL) [56] and by Stokes et al. in 2008 (single electron transistors with local gate) [85].

3.2.1 Top-gate structure

The interest towards top gating of CNTFETs has risen steadily. Wind et al. studied top gated FETs in 2002 [96], Nihey et al. in 2003 [69] and in 2004 [70], Li et al. in 2004 [82], Zhang et al. in 2006 [99] and Avouris et al. in 2004 [40] and in 2007 [5]. In 2007, Kim et al. studied passivation layers made of polymethylmetacrylate (PMMA) and chemical vapor deposited (CVD) Si_3N_4 [52]. The top-gate structure is explained in chapter 2, section 2.4.2.

Top local gating (see sections 2.4.3 and 3.2.1) was researched Javey et al. in 2002 [43] and in 2004 [41], by Wei et al. in 2003 [91] and by Chen et al. in 2008 [18].

Top gating method has become more popular than bottom gating during the past years. This is because top-gated CNTFETs can be placed on complicated circuits, work at lower voltages when used as a local gate and they are fast switches [82].

Many of the high performance CNTFETs are $p-$type (e.g. Pd), and only few stable $n-$type (e.g. Al) CNTFETs [34].

3.2.2 Bottom-gate structure

The literature of bottom gating in CNTFETs is mostly limited to the silicon wafer and its oxide. It used to be the main type of gating but has recently been replaced by top gating.

Wind et al. compared bottom and top-gate structures in 2002 with the conclusion of TG being more efficient [96].

3.3 Studies in oxide breakdown

Breakdown of the gate oxide was studied in 2005 by Lombardo et al. [60]. Low-κ dielectrics (such as silicon oxide) was studied by Tsu et al. in 2000 [90] and by Ogawa et al. in 2003 [73].

Jiang et al. [44] quite recently (2008) studied the CNT nano-to-micro contact via electrical breakdown, and Kolodzey et al. [54] researched Al oxide and McPherson et al. [65] did research in 1998 on time-dependent dielectric breakdown. Osburn et al. studied the same subject in 1972 [74] (self-healing) and DiMaria et al. in 1993 [21] (SiO_2).

3.3.1 Ultra-thin gate insulators

The thickness of the often-used SiO_2 has a strong inverse correlation on the gate leakage [13, p. 7] which makes the atomically small ($\leq$5 atoms [13, p. 2]) transistors unuseful. The tunneling current flowing through the atomically thin gate dielectric also produces unwanted heat [63, p. 25].

Ultra-thin gate insulators are gained by replacing the silicon oxide with a high-κ insulator. High-κ insulators demand a bit thicker gate oxide for higher density of FETs but at the same time the gate voltage decreases considerably [13, p. 7] making these oxides very useful for applications. In addition to the contribution of Bohr et al. , the high-performance high-κ transistors were studied by Biercuk et al. in 2008 [10].

Intel Corporation used a hafnium-based (Hf) material as the ultra-thin gate in MOSFETs [63, p. 25]. Its dielectric constant κ is $\kappa_{HfO_2} = 25$, significantly higher in value than that of silicon, $\kappa_{SiO_2} = 3.9$ [79]. After finding good choices for high-κ gate dielectric Intel had new problems: the chemical vapour deposition (CVD) technique had to be changed to ALD and semiconductor gate had to be changed to a metal one. The ALD method was used in [40] and [78].

The demand for the above-mentioned changes to field-effect transistors rose from the electrical properties of semiconductors. The deposition method was changed because electrons were trapped between the uneven surfaces of the gate dielectric and the gate and ALD allowed the deposition of smooth surfaces.

Furthermore, the material of the gate was changed from polysilicon to metal due to electron scattering phonons in the channel: the negative effect of the phonons in the channel decreased significantly because of the rise in the number of electrons. [13]

Chapter 4

Experiments

The samples used in the experiments were fabricated by Peerapong Yotprayoonsak, Andreas Johansson and me. Peerapong Yotprayoonsak did the lithograpy and the electrode deposition procesesses. I did the CNT deposition, the bonding of the wires and took the AFM images. The electrode deposition and the carbon nanotube deposition were made in the cleanroom of the Jyväskylä University Nano Science Center.

4.1 Introduction to experiments

The first idea was to build and measure local-gated CNTFETs (see section 5.1.4) but after having so much trouble making good and reliable contacts to aluminium (which would act as a local gate amid the aluminium oxide), the objective changed to oxide breakdown measurements. The change of focus was as well due to lack of time.

The understanding of dielectric breakdown is vital for well-designed CNTFETs especially with local gate, see figure 4.1. The gate dielectric is supposed to insulate perfectly, letting no tunneling current flow through. Breakdown threshold voltages and the corresponding post-BD differential resistances were measured.

In order to model BD in a CNTFET, a "finger structure" electrode pattern consisting of a metal-oxide-CNT junction was invented. Two types of metals were used as the electrode material in the breakdown measurements:

- Aluminium electrodes covered with aluminium oxide Al_2O_3 and MWNTs
- Titanium electrodes covered with titanium oxide TiO_2 and MWNTs.

In addition, CNT $i - v$ curves were measured for comparison:

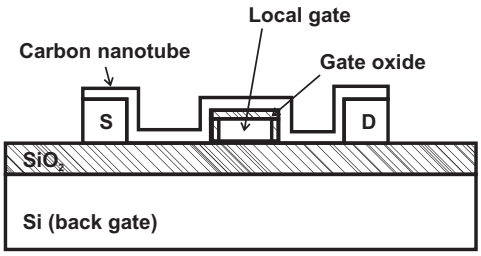


Figure 4.1. Gate oxide measurements are important especially for local-gated CNTFETs. The gate dielectric is supposed to insulate perfectly, letting no tunneling current flow through.

- Palladium samples with no oxide were measured to gain $i - v$ and gate field-effect curves for SWNTs and temperature-dependent $i - v$ curves for MWNTs.

4.2 Measurement setup

The data acquisition was realized similarly in all the measurements, see figure 4.2. If not otherwise noted, sample is at room temperature (RT). Using cool-down instruments (see appendix C.2) does not change the measuring setup: instead of connecting the BNC cables to the sample box (see figure C.2b), the sample is connected to the circuit from the BNC connections of the dipstick, see figure C.2a.

In figure 4.2 there are two voltage sources. The upper one is for the drain-source voltage and is always used. The other DC source is for gate measurements and is omitted if not needed. Three different types of DC voltage sources were used: BNC-2090 DAQ board, Keithley 6517 Electrometer and Yokogawa 7651 DC source. BNC-2090 data acquisition (DAQ) board has both input and output channels. As an input, the DAQ board collects the data (in volts) to its 16 input channels and sends it to the computer to be analysed (e.g. to be multiplied by the current gain) and saved. Both the input and the output have a limit of ± 10 V.

The BNC-2090 DAQ board was convenient as an output, having up to two output channels. The weakness of the output was its 5 mV big step size. The BNC board is controlled through PXI.

Yokogawa 7651 DC source was the most accurate of all, with the step size as small as $\pm 0.01\%$ of setting ± 200 μV. The device was controlled via General Purpose Interface Bus (GPIB) from the computer. The output voltage is limited to ± 30 V.

The Keithley electrometer was used for high output voltages (up to 200 V). For our purposes, there was really no limitation in the output voltage: Keithley 6517 can apply as much as 1000 V. The step size of the Keith-

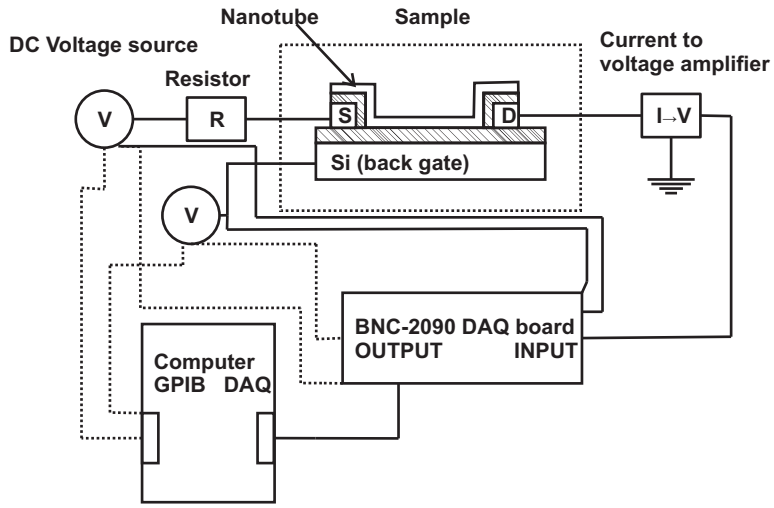


Figure 4.2. The measurement setup. Three different types of voltage sources were used as the source-drain voltage V_{DS} and the gate voltage V_G : BNC-2090 DAQ board (through PXI), Keithley 6517 Electrometer (GPIB) and Yokogawa 7651 DC source (GPIB), see the dashed lines. V_G was optional and mostly unused. The current had to be converted (and amplified) because the DAQ board only reads volts, not amperes. The output voltages were read by the DAQ board unless the voltage exceeded 10 V. Both the input and the output were computer-controlled.

ley device was equivalent to the BNC board's: 5 mV. Like the Yokogawa source, Keithley 6517 was controlled via GPIB.

Because the PXI input could only measure up to 10 V, the input voltage was taken from a voltage divider when the applied DC voltage exceeded ± 10 V. After a while the voltage divider became unreliable (due to excess heating, presumably), forcing to take the theoretical (not measured) value of the applied voltage as the input. However, this did not cause noteworthy error.

All these voltage sources and data inputs were controlled by a LabVIEW program that I programmed and modified to fit to different voltage sources, see appendix D.

In some cases the data capture was operated manually. The voltage source was either a Keithley 6517 or a Yokogawa 7651 and a multimeter was used as the data acquisition input. This method was much slower and less accurate because of the lack of multitude of data points.

4.3 The tiers of the sample processing

There are different names for each tier of sample processing: The **silicon wafer** is the largest bundle of chips. The round, 15 cm in diameter wafer

is cut halfway into small pieces with a silicon saw, see figure 4.3a. A part separated from the wafer is called a **batch**.

The batch a set of chips that are processed with the same parameters (e.g. material and electrode pattern), see figure 4.3b. There are around ten or less **chips** in a batch.

The chip is a 5 mm $\times$ 5 mm square piece separated from a batch. The chip consists of the substrate, electrodes and samples, see figure 4.3c. The small, square dots on the chip are bonding pads which the bonder connects to the chip carrier with a bonding wire, see section 4.4.9.

The **electrode pattern** is in the center of the chip and is the same for all chips in a certain batch. Nanotubes are deposited separately on each chip and this way each chip is different, see figure 4.3d. The distance of two marker structure crosses (small dots under the structure) is around 7 μm.

Sample or **device** is part of the chip that consists (here) of a CNT crossing a gate electrode, see figure 4.3e. There might be several samples on one chip – the only physical limitation is the number of pins (28).

4.4 Sample fabrication

In this section the main phases of sample fabrication are presented and measurements of the fabricated devices are addressed later in chapter 5.

4.4.1 Substrate

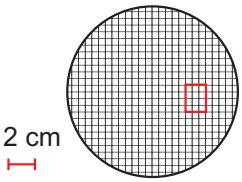
Silicon (Si) is used as the substrate material of the samples. Silicon is an indirect band gap semiconductor i.e. it does not emit light but releases energy to the lattice. This broadens the radiation bandwidth. [25, p. 169]

The silicon wafer comes in round piece which need to be cut with a silicon saw in order to fit the batch into the oxidation oven, see the following section. There is a picture of the silicon saw in appendix B.1.

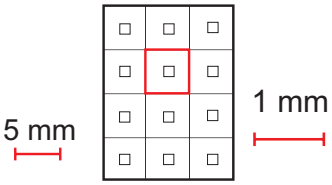
Silicon oxidation

Si also works as the back gate (BG) so an oxide is needed on top of it. There are two ways to construct the oxide on top of the (back) gate: natural oxidation in an oven and atomic layer deposition (ALD) [82]. In some cases, when the size of the device matters, the back gate oxide is good to be very thin and e.g. zirconium silicate ($ZrSi_xO_y$) can be used as the back gate oxide which is deposited directly on top of the silicon [95].

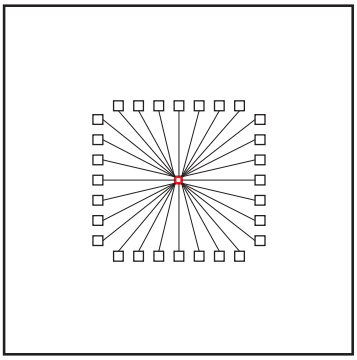
In this thesis the silicon substrate is covered with SiO_2 which is built by natural oxidation in an oven, see figure B.2 in appendix B.2. The thickness of the naturally built SiO_2 cannot be specifically determined beforehand and so the natural oxidation is only applicable to those samples that don't



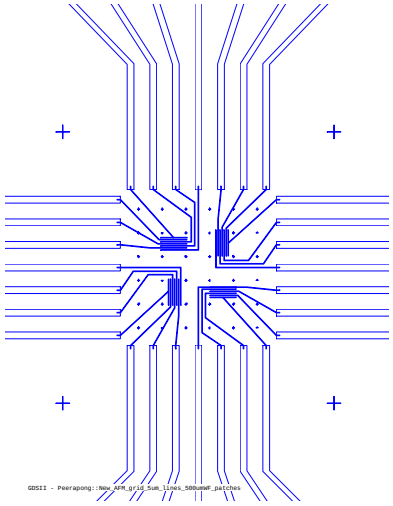
(a) The silicon wafer is cut into pieces with a silicon saw. The silicon wafer is around 15 cm ⌀.



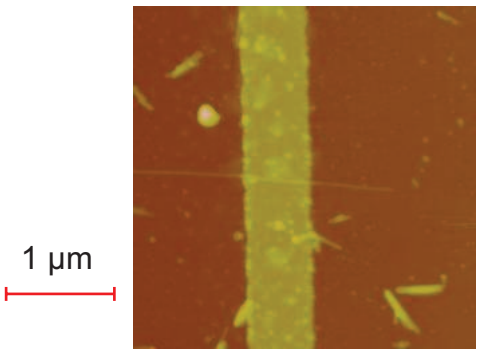
(b) Batch is a set of chips that are processed with the same parameters (e.g. material, pattern). There are around ten or less chips in a batch.



(c) Chip is a 5 mm × 5 mm square piece consisting of the substrate (see figure 4.3a), electrodes (see figure 4.3d) and samples (see figure 4.3e). The small, square dots on the chip are bonding pads which the bonder connects to the chip carrier with a bonding wire, see section 4.4.9.

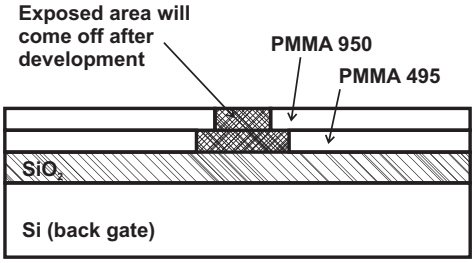


(d) Electrode pattern is the same for all chips in a certain batch. Nanotubes are, though, deposited separately on each chip and this way each chip is different. The distance of two marker structure crosses (small dots under the structure) is around 7 μm.

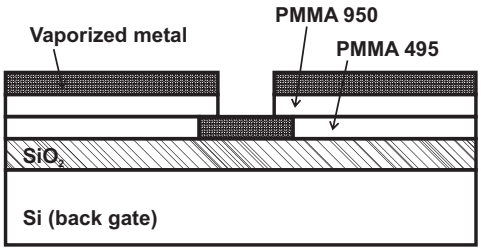


(e) Sample or device consists (here) of a CNT crossing a gate electrode. There might be several samples on one chip – the only physical limitation is the number of pins (28).

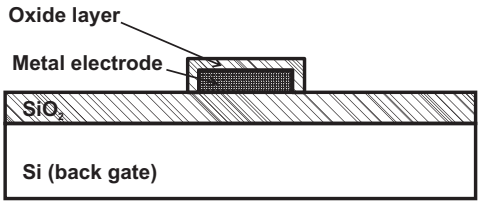
Figure 4.3. From wafer to sample. The round silicon wafer cut into several batches which are processed and cut into chips, see sections 4.4.2 through 4.4.7. After the CNT deposition the samples are imaged with the AFM and measured. The red square in each figure represents the area that the following figure covers. The scale is shown in each of the figures separately.



(a) Sample after resists, exposure and development: the first developer takes off PMMA 950 and the second PMMA 495 in the exposed area.



(b) Sample after metallization: chosen electrode metal is heated and vaporized on the sample.



(c) Sample after oxidation and lift-off: the oxide is grown on the electrode metal and during the lift-off resists and everything on top of it is dissolved in acetone.

Figure 4.4. The stages of sample processing: resists, exposure, development, metallization and lift-off.

need a particular silicon oxide thickness; e.g. if the silicon substrate is not used as the BG. Silicon oxide is a low-κ insulator, its dielectric constant being $\kappa = 3.9$ [73].

4.4.2 Resists

Two layers of resist is spinned on the batch: PMMA 495 and PMMA 950. The numbers after PMMA refer to the length of the polymer (in nanometers), see figure 4.4a. Before, after and between the spinnings the sample is baked for 3 minutes in order to insure a clean surface. The pictures of the resists and baking equipment are in figure B.3.

4.4.3 Pattern exposure

The e-beam lithography was done with a Raith eLiNE electron beam writer. The electron beam is directed onto the desired pattern to make the exposed area chemically reactive, see figures 4.4a and B.4. The PMMA covering this area is then removed by developing, see section 4.4.4.

4.4.4 Developing

The development is done immeadiately after the exposure. The intention of development is to remove the exposed area of resists. Figure 4.4a shows the sample after development. The first developer takes off PMMA 950 and the second removes PMMA 495, see figures 4.4a and B.5.

4.4.5 Metallization

The metal is vapourized on the sample in ultra high vacuum (UHV) chamber where the sample is held upside down. See figure 4.4b to see the sample after metallization and figure B.6 for the UHV chamber.

4.4.6 Electrode oxidation

The oxide on the metallic electrodes can be grown either naturally or in a UHV chamber by applying oxygen into the UHV chamber. The latter way gives a cleaner result and is thus preferable. If the sample electrodes are oxidized the sample receive an additional oxide layer on top of the metal, see figure 4.4c.

4.4.7 Lift-off

After the chip has been metallized it is dipped in acetone overnight. This is called the lift-off: acetone disengages the PMMA materials and the metal on top of it from the chip forming the electrode structure, see figure 4.4c.

If the acetone vaporizes during the lift-off not all the PMMA comes off and it looks like there are additional electrodes or that the electrodes are connected to each other, see figures 5.5b and 5.8.

4.4.8 Carbon nanotube deposition

Individual SWNTs can be deposited in two ways on the SiO_2 substrate. A stamping technique has been developed in Columbia University and is somewhat slower than the CNT sonication method. The process is also more difficult yet the outcome of the stamping technique is better as far as the sample is concerned [46, p. 73].

In this Master's thesis, the CNT deposition was executed by the sonication method: first, the carbon nanotubes in dichloroethane [48] were sonicated for 20 minutes in a Finnsonic ultrasonic processor, see figure B.7. Sonication may easily cut the CNTs into many pieces or change their chemical properties when using chlorinated solvents [68]. Sonication is, however, inevitable if the CNTs are deposited with a spinner to prevent CNT bundles that are kept together by the vdW force [39].

4.4.9 Bonding

A bonder connects the sample to the chip carrier with a metal wire, see figure B.8b.

Challenges with bonding

The needle of the bonder broke the SiO_2 layer of the chip quite often. This caused leakage current from the bonded wires to the back gate, see section 5.1.1. Also, it seemed that when the needle of the bonder touched the pad, it scratched both the gold pad and the SiO_2 away bonding the wire directly to the silicon surface.

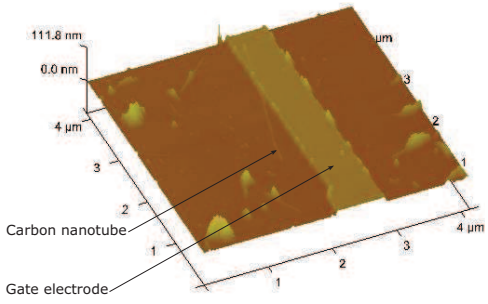
In some cases the area without the oxide was larger the the area of the bonded wire and thus the wire had no contact with the gold pad. This assumption was proved by adding a small piece of indium of top to connect the bonded wire to the pad. After adding the indium dot the current was flowing between the wire and the pad.

Part of this problem was solved by decreasing the force of the needle. The gate leakage problem was, however, much reduced by replacing the SiO_2 with a considerably thicker one, see section 5.1.

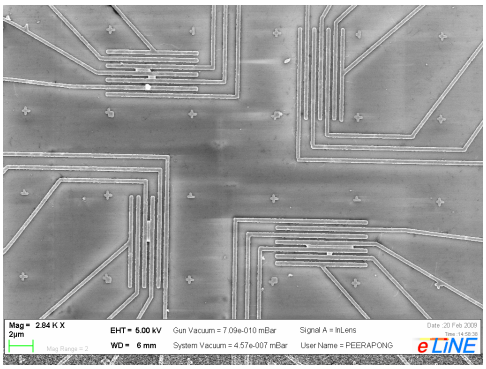
Another problem had to do with the bonding wire not sticking on the oxide surface. This challenge derived from a dirty oxide surface and was solved by cleaning the sample with acetone and IPA before bonding. All of the challenges mentioned above were to some extent due to lack of knowl-

edge and experience. Some of the problems vanished (e.g. the problem with the non-sticking bonds) naturally after a while.

4.5 Sample imaging



(a) An atomic force microscope image of a CNT on top of a gate electrode.



(b) A sample of an e-LiNE image.

Figure 4.5. Sample imaging. An AFM and an eLiNE image.

Samples that were manufactured and measured for this Master's thesis have been imaged with Raith e-LiNE and an atomic force microscope. Atomic force microscopy (AFM) is one type of scanning probe microscopy (SPM), see section 2.9. The e-line technique is faster, but it harms the sample during imaging.

4.5.1 Atomic force microscope imaging

Atomic force microscopes Nanoscope IV and Nanoscope V were used to locate the CNTs. With the AFM, one can get images with the size of $(1\ \mu\text{m})^2$ up to $(15\ \mu\text{m})^2$. A sample AFM image is in figure 4.5a.

The usage of an atomic force microsope

AFM usage is quite simple if you just follow the steps. First, the laser and the mirrors are aligned. Then the cantilever tip is located, the sample is loaded on the sample stage, the probe is taken down close to the sample and the laser is focused on the cantilever. The last procedure is to autotune the tip and engaged it on the sample surface.

The tapping mode was used which means that the tip only taps the sample without harming it. In this mode you can change e.g. the amplitude and the offset of the sine-wave motion of the tip.

The advantage of AFM imaging is that one can change the structure of the sample during the imaging e.g. remove debris or bend nanotubes. AFM also lets the user manipulated the images: you can e.g. take a side view of and image and this way find out the CNT diameter.

4.5.2 eLiNE imaging

As mentioned earlier, eLiNE imaging is faster and the image is more clear (compare figures 5.5b and 5.8) but also more damaging. Figure 4.5b shows an eLiNE image of a Pd sample with single-walled Nanocyl tubes on top. eLiNE images are taken with the same instrument which does the pattern exposure, see section 4.4.3. There is a picture of the Raith e-LiNE in appendix B.4, see figure B.4.

Chapter 5

Results and Analysis

5.1 Snake structure measurements

The intention of fabricating CNTFETs with local gate (see figure 5.1) lead to the invention of the "snake structure", see figure 5.2. There are two patterns, "snakes", of which the wider one is 2 μm wide and the narrower one is 500 nm wide.

The idea was to use the snake structures as the local gate if a CNT was found on crossing the structure. The long pattern of the structure was to maximize the probability of finding such a nanotube.

Both of the snakes were designed for local gate measurements, with slightly different aspects. The narrower stucture is more advantageous than the wider one, as the nanotube length to local gate width ratio is greater, providing better results. However, having a larger area, the wider structure is more likely to attract a CNT on top (at least half way).

One of the snake structure chips we got very close in forming a CNTFET, see figure 5.4 in section 5.1.4. However, the second electrode deposition in this chip was unsuccesful with the metal electrode crossing on the local gate, compelling to discard the sample, as was mentioned. Due to insufficient time frame, the idea of local CNTFET measurements transformed

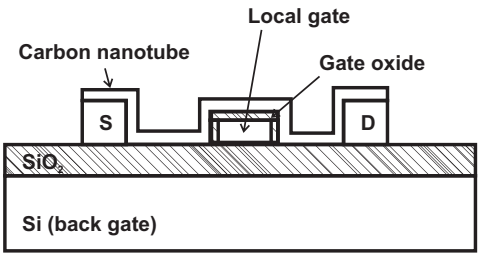


Figure 5.1. The intended bottom local-gated CNTFET structure. One of the fabricated samples almost reached the goal, see figure 5.4.

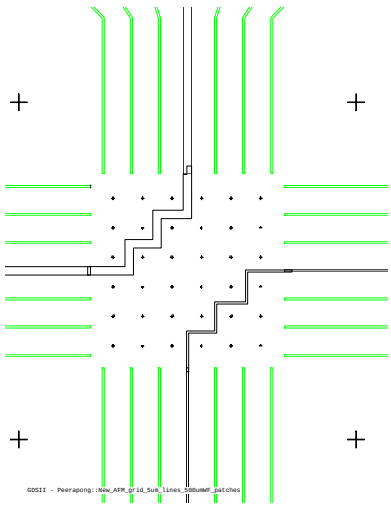


Figure 5.2. Snake structure. The structure between pins 11-18 is 2 μm wide and the thinner structure between pins 4-25 is 500 nm wide.

to gate oxide breakdown measurements, see section 5.2.

There were altogether 8 batches with the snake electrode structure made of aluminium and titanium.Leakage current through the snake gate oxide was tested in five of the baches, see sections 5.1.1 (silver paint method), 5.1.2 (structure method) and 5.1.3 (island method).

Two batches were were abandoned before measuring them on the grounds of previous measurements with poor results of the batches' silicon oxides. In addition, one batch showed no response and was thus abandoned.

Bonding was quite challenging as described in section 4.4.9 in all batches. However, changing the back gate (silicon) oxide to a thicker one worked: there was no leakage through the thickest oxide which states that thin silicon oxides could not stand the bonder's needle force.

The main focus of the snake structure measurements turned out to be the finding of the best silicon wafer with a non-leaking oxide which would not break when bonding. This particular oxide was used for the finger structure measurents, see section 5.2.

5.1.1 Testing the current leakage to the back gate

One of the gate leakage methods was to test the leakage with the help of silver paint.

The back gate leakage was measured by testing the conductance between the wires, see figure 5.3. To be certain that there is no current leakage to the back gate (or $R_1 = \infty$) we had to be sure that the silver is really connected to the back gate: the current has to flow between the two silver dots (i.e. $R_2 < \infty$) and through the structure, see figure 5.3.

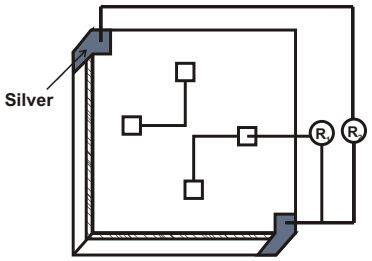


Figure 5.3. Testing current leakage to the back gate. There is no current leakage if $R_1 \approx \infty$ and $R_2 < \infty$. This proves that the gate oxide is good dielectric and thick enough.

Most of the samples tested this way did not turn out to conduct, proposing that the structures would be broken. The suggestion was tested by covering the whole structure of one chip with conducting silver paint. As the samples didn't start conducting the conclusion was that at least the bonding was poor, not necessarily the structure.

To find out whether the leakage in a Ti sample was due to temperature-dependent defects in the silicon oxide we cooled one of the chips down to 4 K with a helium (He) dewar, see figure C.2a. However, there was not noticeable difference in conductance and the leakage remained.

5.1.2 Leakage measurements between the two snake structures

Due to trouble in leakage currents in previous experiments, two Al batches were dedicated to leakage testing. There were no back gate contacts; only current from one structure to the other was measured.

However, this was sufficient to prove that the current was leakage current through the back gate. As the two structures were separate (see figure 5.2) current could only flow through the silicon oxide.

To get confirmation of the leakage, a satisfactory condition was to find one of the four pairs (pins 11-25, 4-11, 18-25 and 4-18) conducting, see figure 5.2.

The result of the leakage measurements was undeniable: clear leakage was found in half of the chips, two chips had no contact to one of the structures and one was totally dead. One of the chips was cooled with liquid nitrogen abruptly to 50 K to test if the leakage dissappears. As was suspected, the chip could not bear the sudden temperature difference and would not conduct at all after the experiment.

One interesting remark was that both leaking, highly contact-problematic batches were made of aluminium. The leakage in these two batches was supposedly due to thin and ununiform silicon oxide and so the oxide was changed for the titanium measurements, see section 5.1.4.

5.1.3 Oxide testing

The last two snake batches do not actually have a specific structure but only a couple of separate metal "islands" on top of the silicon oxide. These samples were fabricated in order to check oxide leakage and to measure the resistance of the bonding wires.

This island test demonstrated that the thickest silicon oxide was the most reliable.

5.1.4 Local gate measurements

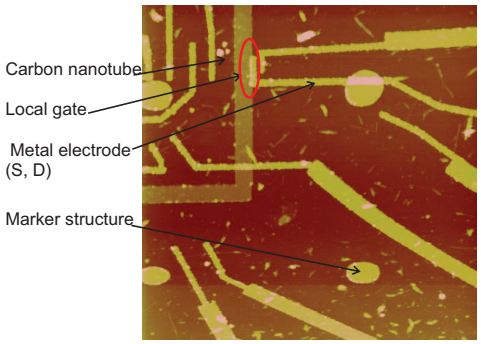


Figure 5.4. Titanium snake structure sample with an attempt at a local-gated CNTFET: a carbon nanotube is crossing a Ti electrode with an oxide on top acting as a local gate, with source and drain electrodes deposited on top. The red area shows the unsuccessfully deposited D and S electrodes one which was accidentally deposited partly on top of the Ti local gate electrode. The marker structure is not well-aligned, presumably causing the failure of the S and D electrode deposition.

As mentioned in section 5.1.1, the back gate oxide in titanium samples was reasonably reliable and could be used for further measurements.

Both single-walled (*Nanocyl*) and multiwalled (*Iijima*) nanotubes were deposited on seven Ti chips. Of these, two Iijima and one Nanocyl chips were imaged with the AFM.

Seven promising CNT samples were found in one of the Iijima chips. The other two chips showed no more than one CNT crossing the snake electrodes. Depositing a new set of electrodes is very time-consuming and so it was decided to concentrate on the first chip where the probability of achieving successful CNTFET is much higher compared to the other two chips.

The variety of the seven carbon nanotubes created a great opportunity for different CNTFET structures to be fabricated, see section 2.4. To our disappointment, only one of the seven possible CNTFETs seemed to conduct, being back-gated. The SiO_2 in the conducting CNTFET was seemingly poor

because current breakdown appeared at 6 V and not even "normal", back-gated CNTFET gate curves were achieved.

The not conducting samples included CNTFET structures with local gate, being the initial measurement target, see figure 5.4. This sample was otherwise perfect with a Ti local gate and S and D electrodes, but the other electrode was partly on top of the Ti gate, making the sample unuseful. Besides, the sample did not conduct.

The project of local-gated CNTFETs ended to this samples due to limited time. The following measuments on gate oxide breakdown (see section 5.2 support well the investingations on CNTFETs. One of the crucial factors of functioning CNTFET structures is the gate oxide leakage as noticed in this section.

5.2 Finger structure measurements

The finger electrode structure was invented for tunneling and breakdown measurements, see equation (2.6). Figure 5.5a shows the electrode pattern of the finger structure. The purpose was to deposit and find only one or at most a few CNTs crossing two adjacent electrodes, measuring oxide BD and/or tunneling currents.

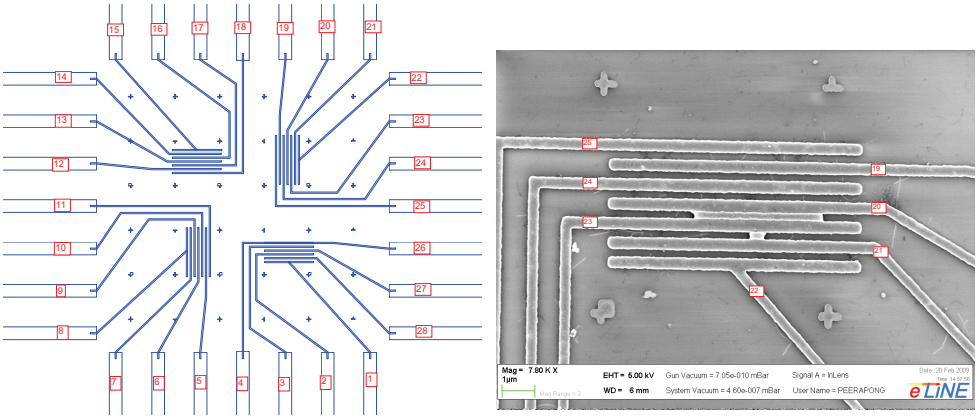
Depending on the electrode material there would or would not be an oxide on top of the drain and source electrodes. Three different materials were used: aluminium (Al), palladium (Pd) and titanium (Ti).

The samples were fabricated as explained in chapter 4. The method of CNT deposition makes the CNTs spread randomly all over a chip, often resulting in having multiple or no CNTs on top of a structure. In breakdown measurements the number of CNT is given but otherwise the sample is assumed to include more than one or two CNTs even if the sample is refered to as *a* CNT.

Since Pd has no native oxide layer (see section 2.8), the material is ideal for $i - v$ curve measurements of deposited CNTs.

Having a thermally-grown native oxide on top, the Al samples are optimal for tunneling or breakdown measurement, having an oxide thickness of around 2 nm. Similarly, Ti samples have an oxide layer, too, but it has been grown in clean oxygen gas in a UHV evaporator. This suggests the oxide having less defects, allowing higher breakdown voltages.

Seventeen of the 28 fabricated finger structure chips were imaged and/or measured. Each of the chips have 28 electrodes, that is, $4 \times 6 = 24$ pairs (consisting of two adjacent pins) possibly having a CNT crossing over. Of these seventeen checked chips, six were palladium, eight were aluminium and three were titanium, see sections 5.2.1, 5.2.2 and 5.2.3.



(a) Finger structure pattern image from E-Line. The numbers in red refer to the corresponding pads in the chip carrier.

(b) An e-Line image of the sample F_009 (SWNT on Pd), see section 5.2.1. Electrode numbers are in red.

Figure 5.5. Finger structure images from the eLiNE.

5.2.1 Palladium samples

Palladium chips were finger structure samples with no oxide layer, see section 2.8. Both SWNT and MWNT samples were measured, giving distinct responses at room temperature as expected. All the measurements except for the cool-down measurements had a 1 MΩ resistance in series.

Naturally, Pd chips could not be used for oxide BD measurements but is meant for gate field-effect and $i - v$ curve measurements. Of the six palladium chips, one chip was utilized for testing the Pd-CNT contacts (chip covered in SWNTs), three chips were dedicated to SWNT measurements and 2 chips for MWNTs, see table I.

Table I. Palladium finger structure chips

Chip	Nanotubes	Experiments	Conclusion
F_007	SWNTs	Contact test	13/21 samples conduct
F_008	SWNTs	$i - v$ curves	4/10: nonlinear $i - v$
F_009	SWNTs	$i - v$ curves	3/24: linear $i - v$ 4/24: nonlinear $i - v$
		Gate field-effect	$I_{ON}/I_{OFF} = 10 \ldots 100$
F_010	SWNTs	$i - v$ curves	3/10: linear $i - v$ 2/24: nonlinear $i - v$
F_014	MWNTs	Cool-down $i - v$	Linear at RT, nonl. at 4K

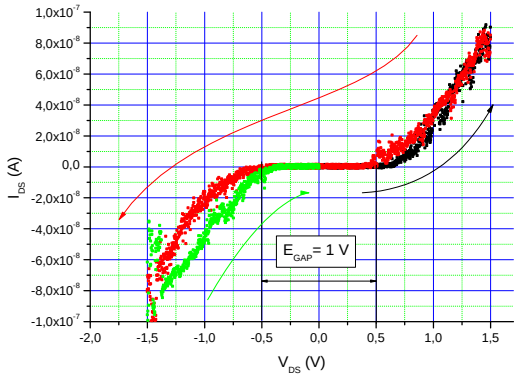


Figure 5.6. An $i - v$ curve of a SWNT with palladium electrodes (sample F_008_03-27). The energy gap $E_G \approx 1$ V.

Conductance experiments

One of the Pd chips, F_007, was covered with single-walled carbon nanotubes to test the conductance of the CNT-Pd junction. An inestimable amount of CNTs in dichloroethane was sonicated for a short time, resulting in a pitch-dark solution, and deposited by pouring the liquid on the chip.

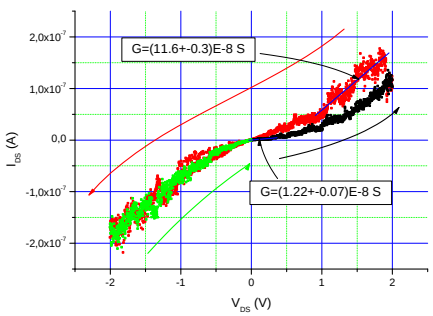
As was expected, Pd conducted well to SWNTs: 13 of the 21 samples were conducting with the range of 5 kΩ...30 GΩ. It is not, however, certain that the non-conducting samples had CNTs on top (the sample was not imaged) and so the conclusion is that in at least $13/21 \approx 62\%$ of the cases the SWNT-Pd junction conducts well.

Single-walled carbon nanotube measurements

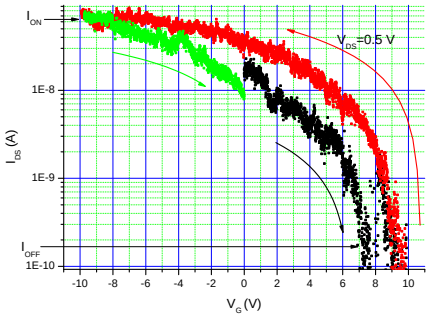
Both $i - v$ and gate field-effect curves of SWNT samples were measured. Chip F_008 had four samples with nonlinear response. The purpose of this chip was to find the $i - v$ curve of a SWNT, to be able to compare it to MWNTs, see section *Multiwalled carbon nanotube measurements*.

One of the four nonlinear, semiconducting SWNT samples is presented in figure 5.6. The measured energy gap E_G seemed to be reasonable [94], $E_G \approx 1$ V, see figure 5.6.

A graph of another semiconducting device (on chip F_009) is presented in figure 5.7a. The gate dependence of the same sample is in figure 5.7b with a constant DS voltage of $V_{\mathrm{DS}} = 0.5$ V. The current ON/OFF ratio of this sample is $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 100$.



(a) $i - v$ -curve measurements of the sample F_009, pins 19-24. The energy gap E_g can be seen as a plateau in the vicinity of $V_{\mathrm{DS}} = 0$ V.



(b) Gate measurements of the Pd sample F_009, pins 19-24. Single-walled carbon nanotube at room temp. Logarithmic scale. A small hysteresis can be seen in the vicinity of zero gate voltage. The current ON/OFF ratio is $I_{\mathrm{ON}}/I_{\mathrm{OFF}} = 100$.

Figure 5.7. The $i - v$ characteristics and the gate field-effect.

Multiwalled carbon nanotube measurements

In addition to three SWNT Pd chips, there were as many MWNT Pd chips. One of the measured chips, F_014, had five conducting MWNT samples. One of the these samples (F_014_01-28) was measured at room temperature and in liquid helium (around 4.2 K), see figure 5.9. See figure 5.8 for an AFM image of the sample.

Figure 5.9 presents the temperature dependence of a MWNT: the energy gap E_G in the $i - v$ curve increases with decreasing temperature. At the boiling point of helium, semiconducting behaviour is seen, whereas at room temperature the response is linear.

5.2.2 Aluminium samples

The Al finger structures were deposited on the (almost) non-leaking silicon wafer which was tested on snake structure chips. The contact to the structure and the gate leakage were first explored (without depositing nanotubes), moving to breakdown measurements.

The measurement setup is in figure 4.2, omitting the gate voltage source. The gate leakage to each sample was tested separately; occuring severe gate leakage is always mentioned.

There seemed to be leakage in some of the Al samples, but the experiments on this material were continued.

One of the chips having MWNTs showed breakdown response, see section 5.2.2. All other chips had no contact or their local gate oxide (that is,

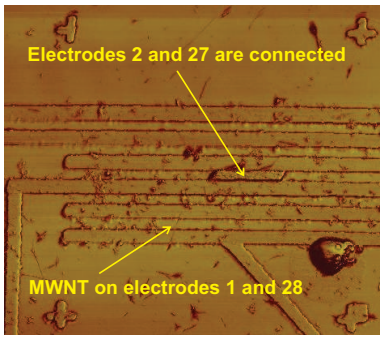
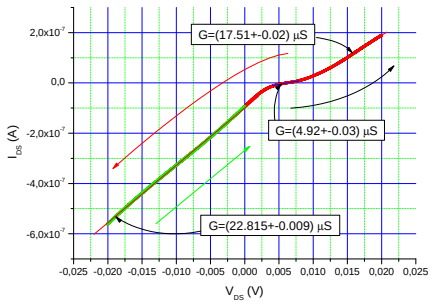
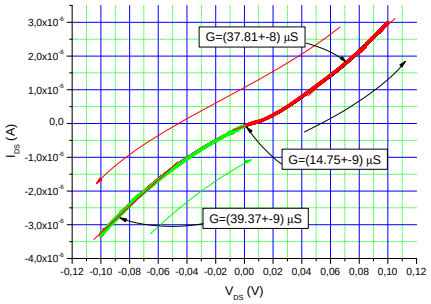


Figure 5.8. An atomic force microscope image of a multiwalled carbon nanotube on top of palladium finger stucture (sample F_014). Note that electrodes 2 and 27 are connected with palladium. This is due to an error in the lift-off process, being quite common considering all the chips, but fortunately, not to a great extent.



(a) $i - v$ curve measurements in liquid He (4 K). The energy gap E_g can be seen as a plateau in the vicinity of $V_{\mathrm{DS}} = 0$ V: the tube seems to be semiconducting.



(b) $i - v$ curve measurements warming up from liquid He (between RT and 4 K). The energy gap E_g has slightly diminised. The slope of the curve is between linear (RT) and that of the curve 5.9a.

Figure 5.9. The $i - v$ characteristics and the gate field-effect of a MWNT Pd sample (F_014_01-28) at room temperature and in 4 K.

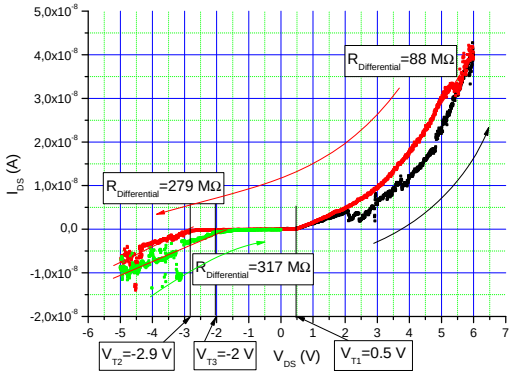


Figure 5.10. The fifth Al_2O_3 breakdown measurement between pins 21-22 (chip F_005) shows hysteresis: after each BD the aluminium oxide damages, making the measurements non-repeatable. The post-threshold differential resistance is taken from the farthermost part of the slope when the curve has straightened.

the AlO_2 finger structure) not break down, not even at as high voltages as 100 V.

Breakdown measurements

Two non-leaking, working, MWNT Al finger structure samples (F_005_21-22 and F_005_21-23) showed BD response, see the following sections. Both of these samples had only one CNT crossing the D and S electrodes.

Sample F_005_21-22

One of the BD measurement $i - v$ curves of sample F_005_21-22 is in figure 5.10. The graph exhibits unexceptional characteristics: at a certain positive and negative source-drain voltage V_{DS}, called the threshold voltage V_T, the current increases suddenly to a non-zero value. This nonlinearity is not due to the energy gap of the MWNT, being very small at RT, but due to the breakdown in the aluminium oxide.

The first sample 21-22 was measured seven times in a row, acquiring sequential BD curves. The post-BD differential voltage was calculated for each of the curves, see figures 5.11a and 5.10. The first and the second measurements did not reach the threshold voltage and thus are not in the figure.

Excluding the first BD measurement (third in total), the graph addresses that the negative BD voltages are higher in absolute value. The order of the BD measurements most likely affect: each time, the V_{DS} was sweeped from zero to positive to negative to zero. After the positive voltage BD

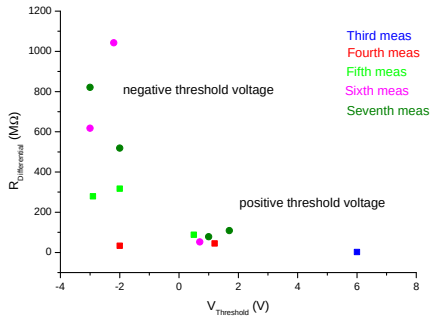
something irreversible happened to the sample and the negative threshold value was no longer comparable to the positive one.

Between the consequent threshold values (both positive and negative) there was no clear correlation. The differential resistance at the positive side appeared to stay quite constant as the resistance at the negative side seemed to alter.

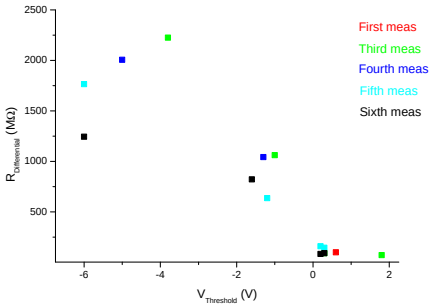
Sample F_005_21-23

Sample 21-23 was measured six times of which the second measurements did not reach the threshold voltage and thus is excluded from the figure, see figure 5.11b. As in figure 5.11a, the negative threshold voltages seems to be higher in absolute value compared to the positive threshold voltages. In addition, the differential resistance at the negative side was substantially higher.

The range of the threshold voltages and the differential resistance was similar in both Al MWNT BD samples.



(a) Post-threshold differential resistance as a function of threshold voltage between the pins 21-22 (chip F_005, MWNT Al). See one of the $i - v$ curves (fifth measurement) in figure 5.10. The positive threshold voltage seems to be lower than the negative one. The first and the second measurements did not reach the threshold voltage and thus are not in the figure.



(b) The post-threshold differential resistance as a function of the threshold voltage between the pins 21-23 (chip F_005, MWNT Al). The second measurements did not reach the threshold voltage and thus are not in the figure.

Figure 5.11. The post-BD differential resistance by the function of threshold voltage in a MWNT, Al chip. There is no significant correlation in the graphs: both the differential resistance and the threshold voltage changes from sample to sample, from positive to negative and from measurement to measurement. Both of the samples have only one CNT on top of the D and S electrodes.

From the oxide thickeness measurements we can calculate the BD electric field. For one sample, there are two oxide-CNT junctions (see fig-

ure 2.5), so the critical field is

$$E_{\mathrm{BD}} = \frac{1}{2} \cdot \frac{V_{\mathrm{threshold}}}{d_{\mathrm{oxide}}}, \tag{5.1}$$

where $V_{\mathrm{threshold}}$ is the threshold voltage and d_{oxide} is the oxide thickness. As the thickness of Al_2O_3 is $d_{Al_2O_3} \approx 2$ nm, a rough approximation for its BD strenght is $E_{Al_2O_3} = \frac{1}{2} \cdot \frac{4\ \mathrm{V}}{2\ \mathrm{nm}} = 10\ \mathrm{MV/cm}$.

5.2.3 Titanium samples

Titanium chips were deposited on a different wafer than the rest of the finger structure chips. This was to assure the silicon wafer to be conducting: the same wafer was successfully used in earlier measurements. The silicon oxide for Ti samples was as reliable as the *VTT2* oxide previously used. The ceSiO2 was measured to be 300 nm thick.

Two of the Ti chips had multiwalled carbon nanotubes deposited to find the BD threshold voltages, see table II. Unluckily, only the other chip (F_018) had CNTs crossing the electrodes. Chip F_028 was used for contact testing, see section *Contact testing*.

Table II. Titanium finger structure chips

Chip	Nanotubes	Experiments	Conclusion
F_018	MWNTs	SiO_2 and TiO_2 BD	TiO_2 and SiO_2BD
F_028	MWNTs	Contact test	Ti electrodes conduct

Contact testing

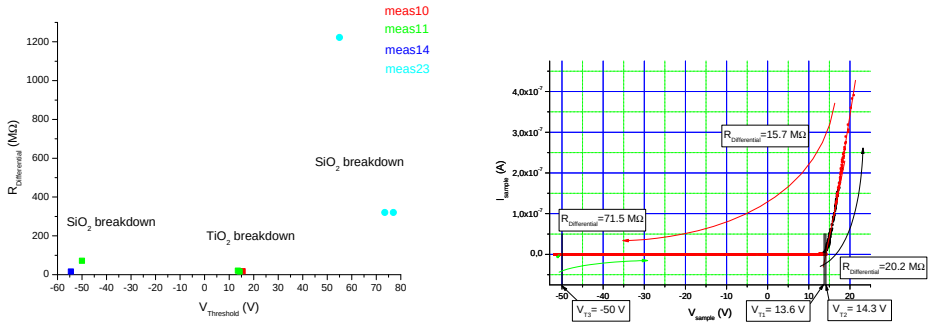
Part of the titanium finger structure pattern of a Pd chip was covered with Indium (In). Carefully, a tiny dot of In was positioned on over half of the finger structure, enabling conductance tests through the Ti structure.

Indium forms a native oxide on top of it but it is very thin, allowing current flow through. It was reasoned from the measurements that the titanium structure conducts and that it is reasonable to begin the BD measurements on the Ti structures.

TiO_2 breakdown measurements

In chip F_018, there were six CNT samples. Four of them were noisy but two of the samples had oxide BD output: F_018_12-18 and F_018_13-17.

The two TiO_2 BD samples showed no correlation of differential resistance with respect to threshold voltage, the data point were totally random; see figures 5.12a.



(a) Post-BD differential resistance against voltage in a MWNT Ti sample. There can be found no correlation between the threshold voltage and post-BD differential resistance. SiO_2 took place after the titanium oxide broke down totally. There are five single CNTs on top of the BD structure.

(b) $i - v$ curve of the eleventh measurement of the MWNT Ti sample in figure 5.12a. No differential resistance existed when increasing the voltage from -50 V, presumably due to time-dependent breakdown.

Figure 5.12. Post-BD differential resistance against voltage in a Ti sample with MWNTs. In addition, one of the $i - v$ curves is shown.

The thickness of the TiO_2 is assumed to be the same as for aluminium, around 2 nm. The threshold voltages of the TiO_2 was 3.3 V $\rightarrow$ 16 V, corresponding to a breakdown electric field of circa

$$E \approx \frac{10\ \text{V}}{2 \cdot 2\ \text{nm}} \approx 20\ \frac{\text{MV}}{\text{cm}}.$$

SiO_2 breakdown measurements

In addition to TiO_2 BD, silicon oxide BD measurements were executed. This was to check the reason for such high threshold voltages in some of the Ti samples (see figure 5.12a). The range of the SiO_2 BD threshold voltage was verified by mesuring the BD voltage of two Ti electrodes that were not connected to each other by anything but the silicon wafer.

Two of the SiO_2 threshold voltages exceeded 200 V. This means that the breakdown strenght exceeds

$$\begin{aligned} E &> \frac{200\ \text{V}}{2 \cdot 300\ \text{nm}} \\ &\approx 3\ \frac{\text{MV}}{\text{cm}}. \end{aligned}$$

This value is adequate compared to earlier reseach [90]. Otherwise, the SiO_2 breakdown occured at 50 ... 77 V, which corresponds to around 1 MV/cm.

Chapter 6

Conclusions

Aluminium and titanium were used as electrode metals, studying oxide breakdown and tunneling in a dielectric-CNT junction. Neither of the materials showed tunneling effect which is quite suprising, both materials having a 2 nm thin oxide. Thus results for only BD could be achieved.

In addition, palladium electrodes connected to carbon nanotubes were researched. Since palladium does not create an oxide layer on top of it, the samples were used for CNT $i - v$ curves and gate field-effect measurements. Furthremore, a MWNT sample was cooled down to 4 K in order to study the temperature dependence of its $i - v$ curve.

Post-breakdown differential resistance was measured to be $10 \ldots 1000\,\mathrm{M}\Omega$ and the absolute values of the BD threshold voltages were between $0.2\,\mathrm{V} \ldots 6\,\mathrm{V}$ for aluminium and $3.3\,\mathrm{V} \ldots 16\,\mathrm{V}$ for titanium. These correspond to a breakdown strengths of $20\ ^{\mathrm{MV}}/_{\mathrm{cm}}$ for TiO_2 and $10\ ^{\mathrm{MV}}/_{\mathrm{cm}}$ for Al_2O_3.

As a conclusion, there was no remarkable difference in the breakdown voltages between the Al and Ti. After repeating the same measurement multiple times, I noticed that the threshold voltage altered each time i.e. the measurements were not repeatable. The $V - R$ plot in figure 5.12 addresses that the post-threshold differential resistance is not symmetric nor is the value of threshold voltage.

The lack of symmetricity in the threshold voltages in the sequent measurements might be caused by the BD damage: once the CNT and/or the SiO_2 has gone through a BD the structure of the material has changed irreversibly. Time-dependent BD (see e.g. [65]) might be part of the reason: once the BD current rose too high during a measurement, I had to stop the experiment, just to start it again by taking the voltage down. Naturally, some time would pass before I could start decreasing the voltage.

As was predictable, palladium had good contacts to CNTs and $i - v$ curves could be acquired. The current ON/OFF ratio $I_{\mathrm{ON}}/I_{\mathrm{OFF}} \approx 100$ which is a relatively good value although ratios of even 10^6 have been achieved in literature.

The titanium chips were deposited on different wafer than the rest of the finger structure chips. This is probably the reason why SiO_2 broke down in the Ti samples but not in the Al samples; in Ti samples, the silicon oxide started breaking at $50 \ldots 77$ V when no TiO_2 BD could be observed anymore. When the SiO_2 broke after the TiO_2, it is uncertain whether the CNT or the TiO_2 or both broke. A CNT should be able to carry up to 3 mA of current (see section 2.5.1), so it is likely that only TiO_2 broke.

A further study of the oxide breakdown would be greatly appriciated. As the oxide thickness in electronic devices decreases the risk of over-heating and leakage currents increases. Also tunneling currents have to take into account when researching very thin oxide films.

The biggest challenge in the BD measurements is the non-repeatability: to gain accurate and reliable results, the experiments should consist of tens of samples of each material.

In addition, the temperature of the sample affects the results with amount of $k_B T$ (thermal noise). To minimize the noise, one option would be to use AC voltage sources with lock-in amplifiers, as seen in [27], and measure at low temperatures. It was, however, discovered in a few cases that decreasing the temperature would not make non-conducting samples into conducting ones.

CNTs have been studied and researched for over 15 years efficiently. Still, some fundamental questions remain. How to control whether the CNT produced is semiconducting or metallic? Scientists still don't know how to define the chiral indices (n, m) when producing CNTs [45, Foreword].

Another challenge is to make good contacts between metals and carbon nanotubes. Still, only CNTs with diameter $d > 1.5$ nm have been able to have ohmic contacts to metals [10, fig. 4, p. 462]. What could be seen in the experiments, Pd structures connected well to tubes but especially aluminium samples were too often not conducting.

What was intresting is that breakdown never took place in a couple of Ti samples even at 200 V. It would be interesting to do more research on why this happens, is the phenomena repeatable or not and whether replacing the CNT with a metal electrode would change the result.

To be able to observe tunneling, how thin should the oxide be? It would be absorbing to measure dielectics of different thicknesses and compare the results. Moreover, would one find significant differences between TiO_2 and Al_2O_3 if the oxides were thinner?

As mentioned earlier, I had to stop the measurement a few times to limit the BD current. Would the results be different if there was no time difference between the measurement? What is the effect of TDDB in a scale of minutes?

In the experiments in this project, aluminium had a native oxide and titanium a clean one. How does the cleanliness affect the results, i.e. is there

a difference in results between a clean oxide and a less clean one? Presumably, the answer would best be discovered if the two different oxides were on the same metal.

All in all, there are many unanswered questions on breakdown. As electrical devices become smaller and smaller, the this effect becomes more important. Both dielectric breakdown and carbon nanotubes have been researched diligently, but more could be focused on their interaction– after all, it is possible that one day computers use carbon nanotube field-effect transistors.

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Appendix A

List of Used Abbreviations and Constants

2D 2-dimentional

AC Alternating current

AFM Atomic force microscope

AHI Anode hole injection

Al Aluminium

ALD Atomic layer deposition

Al_2O_3 Aluminium oxide

Au Gold

Å Ångström$= 1 \times 10^{-10}$ m

BD Breakdown

BG Back gate; bottom gate

BIPM Bureau International des Poids et Mesures

BNC Bayonet Neill Concelman -connector

C Carbon

CNT Carbon nanotube

CNTFET Carbon nanotube field-effect transistor

CVD Chemical vapor deposition

d Diameter; width

D Drain

DAQ Data acquisition

DC Direct current

E Energy

$\boldsymbol{E}$ Electric field

E_F Fermilevel

E_g Energy gap

eV 1 electron volt = $1.60217646 \times 10^{-19}$ joules (unit of energy E)

FET Field-effect trasistor

FLG Few-layer graphene

G Gate

G Conductance (unit: Siemens, S)

GPIB General Purpose Interface Bus (a.k.a. IEEE-488 bus)

H Hydrogen

He Helium

$\mathbf{HfO_2}$ Hafnium dioxide

$\boldsymbol{i}$, $\boldsymbol{I}$ Current (unit: Ampere, A)

IC Integrated circuit

In Indium

IPA Isopropanol

$\boldsymbol{J}$ Current density

K Kelvin, unit of temperature ($T_{\text{in Kelvins}} = T_{\text{in }^\circ\text{C}} + 273.15$)

κ Dielectric constant

k_B Bolzmann constant= $1.3806503 \times 10^{-23} \text{m}^2\text{kg/s}^2\text{K}$

m^* Effective mass (of a CNT)

MOSFET Metal-oxide semiconducter field-effect transistor

MWNT Multi-walled carbon nanotube

N Nitrogen

O Oxygen

PCI Peripheral Component Interconnect

Pd Palladium

PL Photoluminescence

PMMA Polymethylmetacrylate

PXI PCI eXtensions for Instrumentation

R Resistance (unit: Ohm, Ω)

RT Room temperature

S Source; Siemens (unit of conductance G)

S Subthreshold swing (of a transistor)

SAM Self-assembled monolayer

SB Shottky barrier

SI International System of Units

Si Silicon

SiO_2 Silicon dioxide

Si_3N_4 Silicon nitride

SPM Scanning probe microscopy

STM Scanning tunneling microscopy

SWNT Single-walled carbon nanotube

TDDB Time-dependent breakdown

TF Time-to-failure

TG Top-gate

Ti Titanium

TiO_2 Titanium dioxide

UHV Ultra high vacuum

v, V Voltage (unit: Volt, V)

v_d Drift velocity (of charge carriers)

vdW van der Waals (force)

VI Virtual instrument (in LabVIEW programming)

ZrSi$_x$O$_y$ Zirconium silicate

Appendix B

Pictures of the Sample Fabrication Instruments

Most of the sample fabrication instruments are located in the cleanroom in the Nano Science Center at the University of Jyväskylä.

B.1 The silicon saw

Figure B.1. The silicon saw which cuts the silicon wafer into chips.

The silicon saw cuts the round, approximately 15 cm in diameter silicon wafer into 5 mm$\times$5 mm chips, see section 4.4.1. The instrument is in the cleanroom corridor and is fairly simple to use. A picture of the saw is in figure B.1.

B.2 The oven for natural oxidation

Some of the materials (e.g. titanium and silicon in this project) are thermally oxidated in an oven, see figure B.2. The device is located in the cleanroom.

Read more of natural oxidation in section 4.4.1. The oxide which is created is not as clean as in the UHV evaporator, see figure B.6.

Figure B.2. The oxidation oven for oxidizing silicon and other naturally oxidized materials.

B.3 The spinner for the resists and CNT deposition

The resists are spinned and baked on the Si wafer before electron lithography. See figure B.3b for the spinner and figure B.3a for the baking. Both of the instrument are in the cleanroom.

The spinner is used for multiple purposes, for example in this project it was used for carbon nanotube deposition, see section B.7. Read about the function of the resists in section 4.4.2.

(a) The sample is baked before, between and after spinning the resists.

(b) Spinning the resists. The spinner is the same device that is used for the CNT deposition.

Figure B.3. Baking and spinning the resists.

B.4 The Raith e-LiNE for pattern exposure

We used a Raith eLine electron beam writer to make the electrode patterns, see figure B.4 and section 4.4.3. In addition, the device can be used for sample imaging, see section 4.5.2.

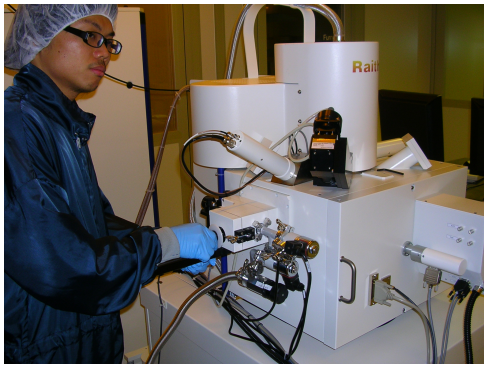


Figure B.4. Peerapong Yotranprayoonsak is using the Raith eLiNE for making the eletrode pattern. eLiNE can also be used for imaging the samples.

B.5 Development

The development instruments can be seen in figure B.5. Two different developer are used because of the two resists; one developer takes only one layer of resists away, see section 4.4.4.

Figure B.5. The development instruments. Two solutions are needed: the first developer takes off PMMA 950 and the second removes PMMA 495.

B.6 The UHV chamber for metallization and electrode oxidation

The metallization and the clean oxidation of electrodes are done in a UHV chamber, see figure B.6. Read more in sections 4.4.5 and 4.4.6.

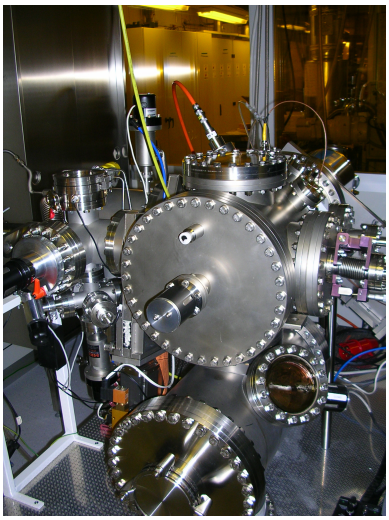


Figure B.6. The ultra high vacuum (UHV) evaporator is used for both the metallization and oxidation of electrodes.

B.7 Depositing CNTs: the sonicator

The CNTs were deposited with the sonication method (see section 4.4.8): first, the CNTs are sonicated in a Finnsonic sonicator (see figure B.7) and then spinned on the sample with a spinner, see figure B.3b. There are several sonicators in the NSC Jyväskylä, both inside and outside the cleanroom. The one in the picture is from outside the cleanroom.

B.8 The bonder

The bonder is used for connecting the sample to the chip carrier, see figure B.8a. The bonded chip in a chip carrier is ready to be measured, see figure B.8.

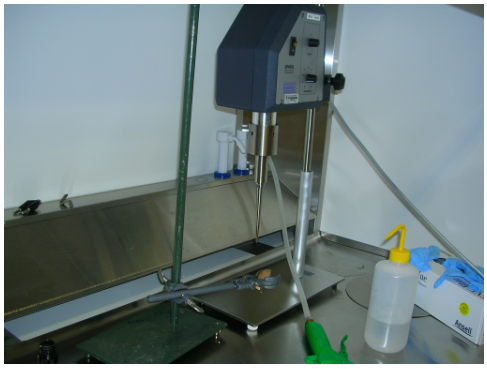
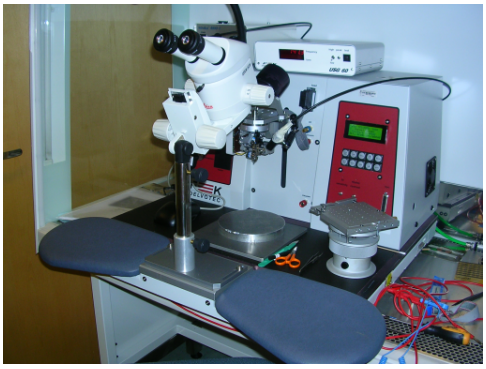
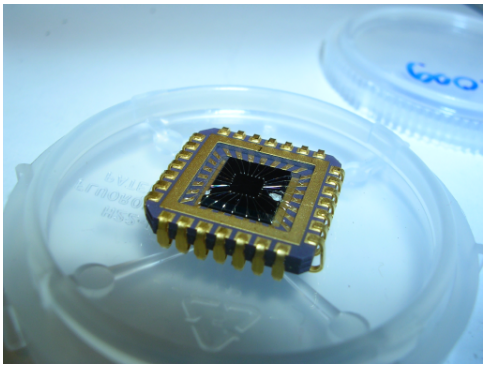


Figure B.7. The ultrasonic sonicator is used to sonicate the CNT-dichloroethane



(a) The bonder connects the sample to the chip carrier with thin metal wires.



(b) The ready sample glued on a chip carrier and bonded. The bonding wire connects the sample to the chip carrier so that it can easily be measured.

Figure B.8. The bonder and a bonded chip.

Appendix C

Pictures of the Measurement Instruments

C.1 The Nanoscope IV atomic force microscope

An atomic force microscope is in figure C.1. There are two AFMs in the Nano Science Center, this being Nanoscope IV. The AFM is sensitive to vibrations, being built on a separate base. Read about AFM theory in section 2.9.2 and AFM imaging in section 4.5.

AFM is used in these measurements only for imaging, but it can be used for e.g. surface manipulation as well.

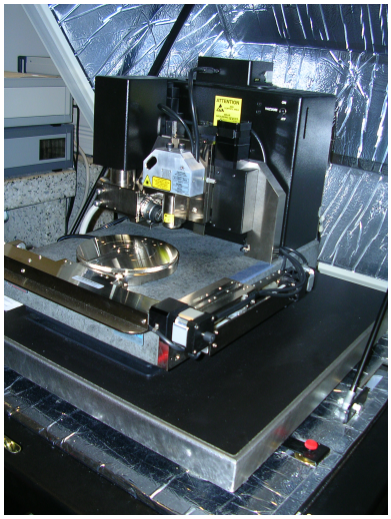
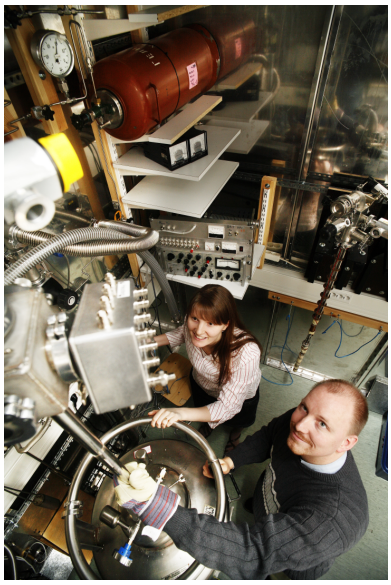


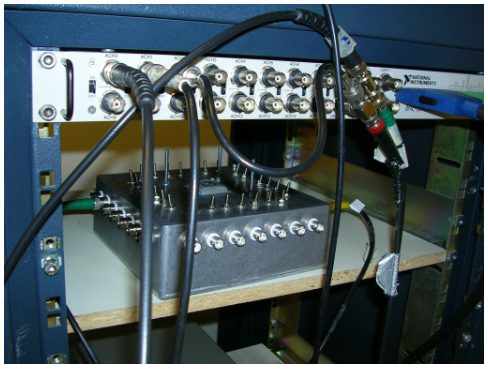
Figure C.1. An atomic force microscope (Nanoscope IV).

C.2 Cool-down instruments

The vast majority of the measurements were done at room temperature, but some samples were measured in 4 K, see figure 5.9. The cool-down helium dewar is in figure C.2a. Some of RT measurement devices are in figure C.2b, such as the sample box and the DAQ board.



(a) Andreas Johansson and me using the helium dewar to cool a sample down to 4 K. © 2009 Petteri Kivimäki.



(b) The DAQ board and the sample box.

Figure C.2. Measurement instruments: a helium dewar, a sample box and a DAQ board.

Appendix D

The LabVIEW Program for Device Control and Data Acquisition

Most of the measurements (excluding some of the gate leakage tests) were computer-controlled. The use of tailored programs for device control and data acquisition saves time and enables complex and repeatable measurements.

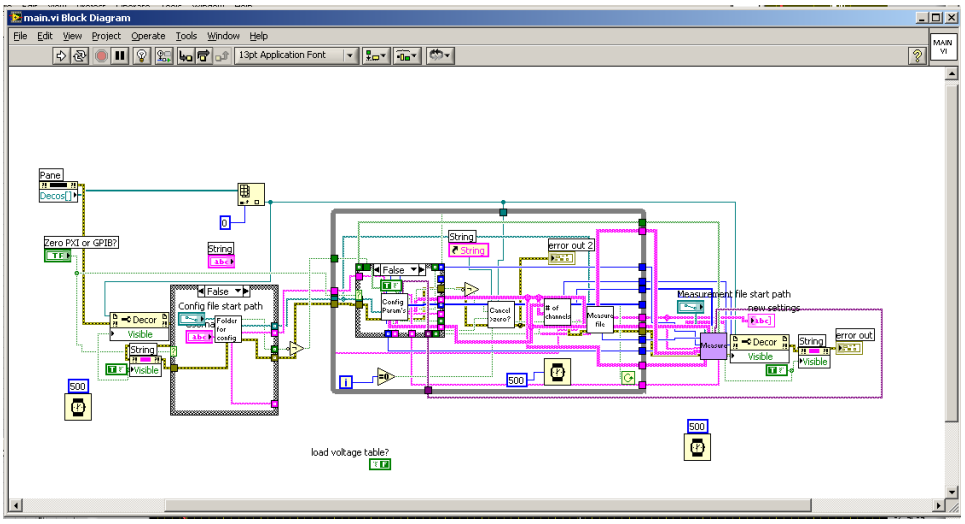
A figure of the measurement setup is in section 4.2. The key role of the LabVIEW computer program is to control the voltage output and acquire the data (input). The LabVIEW I programmed (see figure D.1) uses both PXI and GPIB to communicate with devices. For all the three voltage sources there was a unique LabVIEW program, based on the same framework.

A program in LabVIEW is called a virtual instrument or a VI, referring to the program's ability of functioning as a real instrument, for example as a DC voltage source.

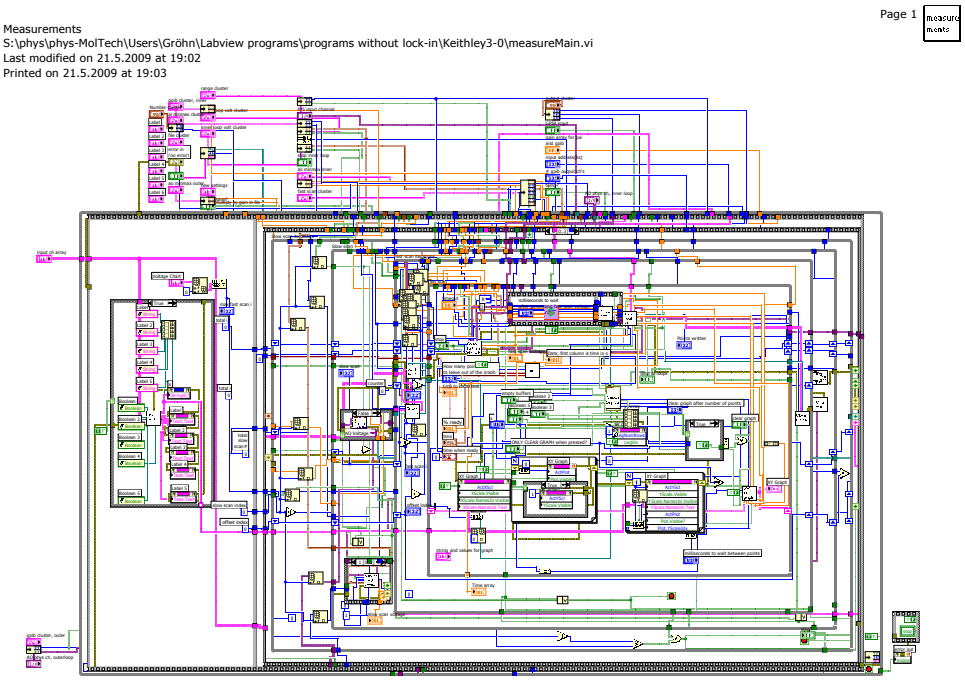
Figure D.1a shows the block diagram of the main voltage control program. All the around 200 subVIs are included in this program and run either in parallel or sequentally with respect to each other.

One of the most important subVIs is in figure D.1b. It sends the command to instruments, controlling the output, and receives data (here) through PXI, enabling easy acquisition and saving of thousands of data points.

Graphically programmed VIs might look slightly tangled and confusing at first glance. However, the learning of graphical programming is faster than coding.



(a) The main program or a *virtual instrument* (VI): sets the input and output parameters and initializes the measurement devices.



(b) One of the most important subprograms (or a subVIs) among the 200 programs. It is designed for voltage control and data capture, plotting a graph as the data is collected and saves it to the computer.

Figure D.1. LabVIEW program for device control and data acquisition.

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