Master RADMEP

Master *Radiation and its Effects on MicroElectronics and Photonics Technologies* (RADMEP)

EXPLORING AND MODELING OF NON-LINEARITY IN BJT TO OPTIMIZE IT FOR WIFI-7 POWER AMPLIFIER

Master Thesis Report

Presented by

Arnab Saha

and defended at

University Jean Monnet

09 September 2024

Academic Supervisor(s):	Prof. Sylvain Girard, University Jean Monnet
	Prof. Paul Leroux, Katholieke Universiteit Leuven
Host Supervisor:	Philippe Cathelin, STMicroelectronics, France
Jury Committee:	Prof. Sylvain Girard, University Jean Monnet
	Dr. Arto Javanainen, University of Jyväskylä
	Prof. Paul Leroux, Katholieke Universiteit Leuven
	Prof. Frédéric Saigné, University of Montpellie

Erasmus+ UNIVERSITÉ JEAN MONNET SAINT-ÉTIENNE JYVÄSKYLÄN YLIOPISTO UNIVERSITY OF JYVÄSKYLÄ KU LEUVEN UNIVERSITÉ DE MONTPELLIER

Exploring and Modeling of Non-linearity in BJT to Optimize it for WIFI-7 Power Amplifier

Abstract

Power Amplifiers are an integral part of modern-day wireless communication systems. Nonlinearity in power amplifiers is an undesirable problem but is a common phenomenon in its applications. For advanced wireless applications of modern days, reducing nonlinearities has become a challenging task. Studies have been done to understand the origin mechanisms of these nonlinearities and their mitigation techniques. HBTs provide higher gain and speed compared to CMOS, but the advanced HBTs have complicated architecture, and the Equivalent Circuits are often not comprehensible for designers to gain insight into the origin of nonlinearity. Thus, an efficient method to investigate these nonlinearities and find an easier way to understand them has always been of interest to designers. A systematic way of investigating the nonlinearity in HBT of PA was reported in this study. A custom model was built to help circuit designers understand the physical effects involved in the nonlinearity, without having to dive deep into transistor architecture or the equivalent model. The key effects and regions playing a role in this nonlinearity were identified, such as exponential IV characteristics between I_C and V_{BE}, especially at high power, the BC saturation effect, the early effect especially the reverse early effect, the high-injection effect, and the transit time effect. To get more insight into the origin of these nonlinearities, the components of the HICUM/Lo model were also investigated. From over a hundred components/parameters that make up the equivalent model HICUM/Lo, the key parameters that impact the linearity of the power amplifier's performance were identified. With the help of Monte Carlo simulation, a comprehensive relation between these parameters and the transistor's physical architecture is also presented in the report. The correlation between these parameters/regions with the transistor and the performance metrics was also identified. The proposed framework provides a systematic way of analyzing nonlinearity in the PA with key insights into the nonlinear effects and their origins.

Keywords: Power Amplifier, HBT, Nonlinearity, HICUM, Monte Carlo Analysis

Preface

In front of you is my master's thesis titled, "Exploring and Modelling of Non-linearity in BJT to Optimize it for WiFi-7 Power Amplifier.", which was produced in order to receive my graduate diploma from the Erasmus Mundus Joint Master's Degree program called RADMEP. During my six-month internship, I had the opportunity to work at STMicroelectronics in Crolles, France, a prominent multinational technology firm. There I worked as a Radio Frequency Circuit (RFC) design engineering intern under the RFC-Management & PMO team in Microcontrollers, Digital ICs, and RF products (MDRF) division.

First and foremost, I want to sincerely appreciate my host supervisor Philippe Cathelin for his dedication and insightful feedback throughout the entire period. Without the constant assistance and support from him, this task would have never been accomplished. I would also like to thank Christophe Arricastres, Didier Celi, and all the other members of my outstanding team, who helped me steer in the right direction with their expertise throughout the internship. I would also like to extend my sincere gratitude towards Prof. Sebastien Fregonese, Prof. Thomas Zimmer, and Prof. Nathalie Deltimple from IMS Lab, University of Bordeaux for their constant encouragement and unwavering support as supervisors during this past few months and warm welcome to the IMS Lab. Being a part of this team for the last six months was an invaluable learning experience and has helped me push myself beyond the boundaries.

I would also like to thank my academic supervisors Prof. Paul Leroux from KU Leuven and Prof. Sylvain Girard from University Jean Monnet for their insightful remarks and important discussions throughout the entire time and for always providing help whenever needed. As this is the end of my two-year long master's degree, I would also like to thank all of my professors from JYU, KU Leuven, and UJM for the knowledge, help, and guidance that they have given us for these last two years. And special thanks go to Leena and Amelie for their constant help with everything, without which this two-year long journey would never have been this smooth.

I would also like to thank my dearest friends Ralph, Nadia, Mauricio, Alan, and Lan with whom I have shared this journey and created some wonderful memories to cherish. Last but not least, I would like to thank my parents and my brother for their unconditional encouragement and support, without which none of this would have been possible.

Table of Contents

Abstract i
Preface ii
List of Figures v
List of Tables vii
List of Acronyms viii
Chapter 1: Introduction 1
1.1 Background 1
1.1.1 Wi-Fi 7 standards 1
1.1.2 Implementing Wi-Fi Standards 2
1.1.3 Non-Linearity in PAs and Its Impact on WiFi-7 2
1.1.4 Designing Linear Power Amplifier for WiFi-7 3
1.2 Objective of the Thesis 4
1.3 Thesis Overview 4
Chapter 2: Theoretical Background 5
2.1 Heterojunction Bipolar Transistors (HBT) 5
2.1.1 Structure and Operating Principle 6
2.1.2 Operating region 7
2.1.2 Transistor Configurations 7
2.1.3 HBT vs CMOS in Analog RF Communication 8
2.1.4 Performance Metrics for HBT Selection 9
2.2 HBT Compact Models 10
2.2.1 HICUM/L2 Model 11
2.2.2 HICUM/Lo Model 12
2.2.3 Compact Model Comparison 13
2.3 Nonlinearities in HBT 14
2.4 Figure of Merits of PA 14
2.5 Linear RF Theory 15
2.6 VerilogA 18
2.7 Monte Carlo Simulation 18
2.7.1 Variance Contribution 19
2.7.2 Correlation 19
Chapter 3: Methodology 20
3.1 Overview 20
3.2 Experimental Setup and Simulation Parameters 21

3.2.1 Bias Conditions 21
3.2.2 Frequency Range 21
3.2.3 Harmonic Balance Simulation 22
3.3 Top-Down Approach: Custom Equivalent BJT Model 22
3.4 Bottom-Up Approach: Investigating HICUM/L0 Parameters 23
3.5 Monte Carlo Simulation Analysis 24
Chapter 4: Results & Discussion 25
4.1 Overview of the Simulation Setup 25
4.2 Top-down Approach: Custom Equivalent BJT Model 26
4.2.1 Building the Custom Equivalent Model 26
4.2.2 Analysis of Non-linearity in the Custom Model 27
4.3 Bottom-Up Approach: Analysis of HICUM/L0 Parameters 30
4.3.1 Identifying Key Parameters 30
4.3.2 Impact of Key Parameters 30
4.3.3 Reduced Parameter Analysis 33
4.4 Linking Parameters to the Custom Model 38
4.4.1 Parameter Mapping 38
4.4.2 Enhancing the Custom Model 38
4.5 Monte Carlo Simulation Analysis 42
4.5.1 Overview of Monte Carlo Simulation 42
4.5.2 Results of Monte Carlo Simulation 42
4.5.3 Cross-Correlation of Model Parameters 44
4.6 Correlation between Model parameters and FoMs 44
4.7 Summary of Findings 45
Chapter 5: Conclusion 47
5.1 Future Work and Implications 47
Bibliography 48
Appendix 1 49
Appendix 2 52

List of Figures

Figure 1: The increase in Wi-Fi data transmission rates [1] 1

Figure 2: Standard Wi-Fi 7 access point schematic diagram. 2

Figure 3: A typical block diagram of a radio frequency (RF) circuit. 2

Figure 4: (a) A decision boundary and constellation diagram; (b) an error vector [2] .. 3

Figure 5: Cross-sectional diagram of a SiGe HBT's CBEBC structure [3] 5

Figure 6: (a) Lateral transistor and (b) Vertical transistor. 6

Figure 7: BJT operating regions. 7

Figure 8: BJT Configurations 8

Figure 9: Comparison of BJT and CMOS technology. 9

Figure 10: Schematic Cross-section of a BJT 10

Figure 11: The HICUM/L2 model with all the associated elements of a BJT [7] 12

Figure 12: The HICUM/L0 model with the associated elements of a BJT [7] 12

Figure 13: Conduction angles, power, and efficiency of different PAs at maximum drive level [11] 16

Figure 14: Different components of the Output Current [11] 17

Figure 15: VerilogA: A Verilog-AMS Language subset. 18

Figure 16: Overview of the Methodological Approach 20

Figure 17: Transconductance of the PA for different frequencies 21

Figure 18: Overview of the Top-Down Approach 22

Figure 19: Overview of the Bottom-Up Approach 23

Figure 20: Overview of the Monte Carlo Simulation 24

Figure 21: Single Stage Common-Emitter Power Amplifier. 25

Figure 22: ST-BJT small signal equivalent circuit. 26

Figure 23: Extracting model parameters from the DC operating points. 27

Figure 24: Response of the linear model compared to B9MW. 27

Figure 25: Custom nonlinear Equivalent BJT model response. 28

Figure 26: Transient response of the collector voltage and current. 29

Figure 27: Reducing Parameters in Priority 1. 31

Figure 28: Reducing Parameters in Priority 2. 31

Figure 29: Reducing Parameters in Priority 3. 32

Figure 30: Model parameter effects on input power at 1dB compression point. 34

Figure 31: Model parameter effects on output power at 1dB compression point. 34

Figure 32: Model parameter effects on power gain at 1dB compression point. 35

Figure 33: Model parameter effects on PAE at 1dB compression point. 35

Figure 34: Model parameter effects on THD at 1dB compression point. 36

Figure 35: Mapping reduced parameter list to the custom model. 38

Figure 36: Finding Parameters from the Reduced list in the Custom model. 39

Figure 37: High injection effects and Transit time effects in the custom model. 40

Figure 38: IC and IB in log scale as an exponential function of VBE. 40

Figure 39: Phase shift in IC and IB due to the transit time effect. 41

Figure 40: Circuit used for the Monte Carlo Analysis 42

Figure 41: Contribution of design parameters to model parameters. 42

Figure 42: Correlation Matrix of Design Parameters and Model Parameters. 43

Figure 43: Correlation Matrix of Model Parameters and FoMs of PA. 45

List of Tables

Table 1: Biasing conditions of different operating regions in HBT 7

Table 2: Comparison between BJT and CMOS..... 9

Table 3: Comparison of the compact models.....13

Table 4: Modes of operation for conducting class PA. 17

Table 5: Reduced HICUM/L0 parameters for B9MW. 33

Table 6: Relation of parameters with PA performance 37

Table 7: Cross-correlation between model parameters..... 44

Table 8: Parameters of HICUM/L0 with their associated parts of the EC model 52

List of Acronyms

RF	Radio Frequency
Wi-Fi	Wireless Fidelity
QAM	Quadrature Amplitude Modulation
SGPM	Spice Gummel-Poon Model
SCR	Space Charge Region
BJT	Bipolar Junction Transistor
HBT	Hetero-junction Bipolar Transistor
CMOS	Complementary Metal Oxide Semiconductor
PA	Power Amplifier
LNA	Low Noise Amplifier
EVM	Error Vector Magnitude
HICUM	High Current Model
VBIC	Vertical Bipolar Inter-Company
MEXTRAM	Most Extended TRAnsistor Model
FoM	Figure of Merit
NPNVHS	NPN Very High Speed
BiCMOS	Bipolar CMOS

Chapter 1: Introduction

1.1 Background

In the modern communication world, the need for wireless communication is seeing an unprecedented rise. Reliable and efficient wireless communication is becoming increasingly essential in today's world due to the rise of smart devices, the IoT, and the demand for fast internet. As Wi-Fi technology supports wireless connections in private residences, businesses, and public areas, it has particular importance to this development. Since the introduction of Wi-Fi technology, it has experienced tremendous growth. Wi-Fi protocols have continuously improved since the technology was initially made available to customers in 1997, as seen in Figure 1, giving users access to higher speeds and more network/spectrum efficiency.

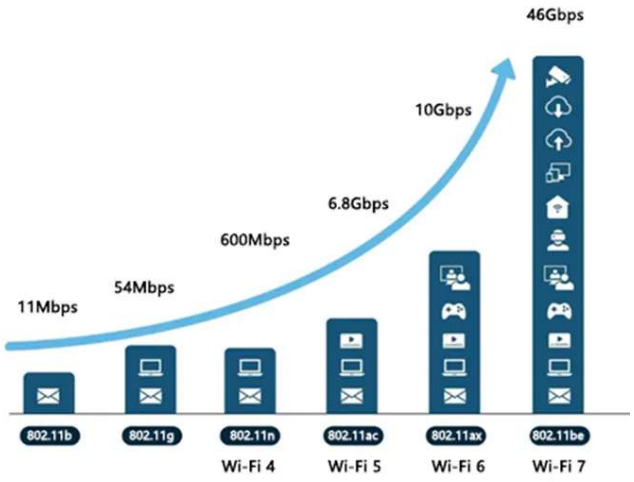

Figure 1: The increase in Wi-Fi data transmission rates [1]

1.1.1 Wi-Fi 7 standards

Wi-Fi 7 (IEEE 802.11be) is the most recent advancement in the ongoing growth of wireless technology. This technology guarantees unparalleled improvements in data speeds, latency, and network efficiency, making it an essential facilitator for next-generation wireless applications. Wi-Fi 7 is designed to attain 4x times faster data rates (46Gbps), twice the bandwidth (320 MHz channels), and tri-band (2.4GHz, 5GHz, and 6GHz) operations with very little delay, and enhanced utilization of the wireless spectrum. Furthermore, 4K QAM modulation allows peak rates to spike for incredibly rapid data transmission. These technological developments are crucial to meet the growing requirements of high-definition video streaming, virtual reality, augmented reality, and other applications that need a large amount of bandwidth [1].

1.1.2 Implementing Wi-Fi Standards

Enabling these Wi-Fi standards requires advanced technology, including routers and Wi-Fi chips. These devices have diverse components that regulate signal processing, modulation, and demodulation. Figure 2 illustrates a conventional implementation of a Wi-Fi chip for the wifi-7 standard.

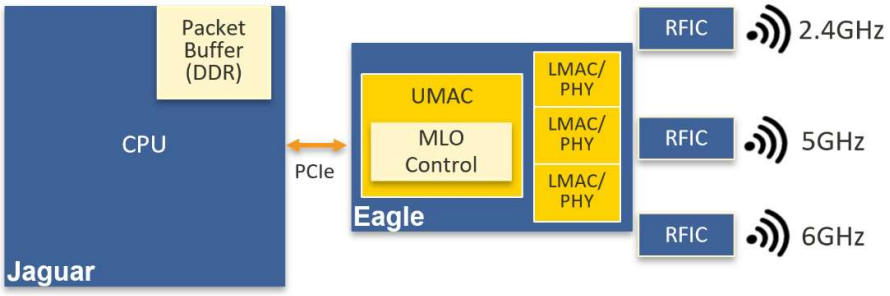

Figure 2: Standard Wi-Fi 7 access point schematic diagram.

The RFIC houses the RF front-end modules used in wireless communication. The RF front-end modules, including amplifiers, mixers, and filters, play a vital part in these processes. These components guarantee that the signals being broadcast and received remain intact and comply with the prescribed standards. Figure 3 shows a typical block diagram of a radio frequency (RF) circuit.

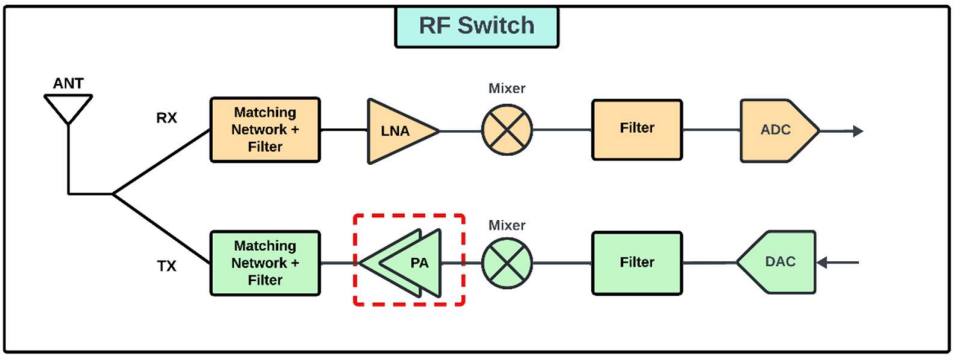

Figure 3: A typical block diagram of a radio frequency (RF) circuit.

1.1.3 Non-Linearity in PAs and Its Impact on WiFi-7

Every wireless system uses one or more power amplifiers, and the linearity and efficiency of these devices often determine how well a wireless system performs. Power amplifiers (PAs) play a major role in guaranteeing the transmission of signals with enough power to reach their intended destinations, while also maintaining the necessary level of quality. Nevertheless, modern linear power amplifiers have significant inefficiency and nonlinearity issues. Often most commercial PAs are designed with a tradeoff between these two. RF power amplifiers are impacted by different kinds of nonlinearities, such as gain compression, harmonic distortion, intermodulation

distortion, phase distortion, etc., which can significantly alter the desired performance of the circuit.

The output signal's divergence from being a linear function of the input signal is a major effect of nonlinearity. The influence of HBT nonlinearity becomes increasingly crucial as WiFi-7 promises to offer unprecedented data speeds, ultra-low latency, and increased spectral efficiency. Nonlinearity-induced distortions have the potential to drastically lower the signal-to-noise ratio (SNR) and raise the error vector magnitude (EVM), which would negatively impact WiFi-7 performance. Error Vector Magnitude (EVM) is a significant indicator for assessing the performance of RF systems, especially in high-speed communication protocols such as WiFi-7. EVM measures the inaccuracy in the signal constellation by quantifying the discrepancy between the ideal transmitted signals and the actual received signals. The transmitted signal's amplitude and phase are distorted by nonlinearities in the PA, as a result, the constellation points spread out and shift away from optimal places, increasing the EVM.

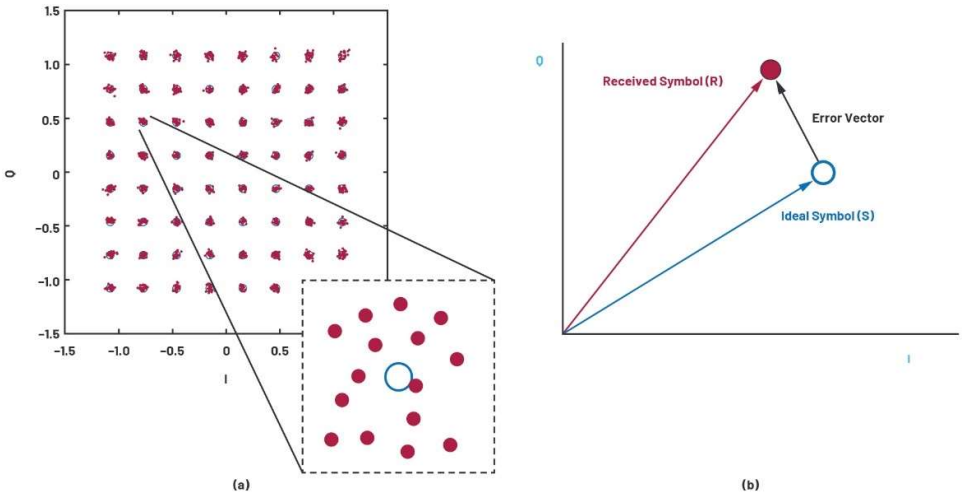

Figure 4: (a) A decision boundary and constellation diagram; (b) an error vector *[2]*

Figure 4 shows the visual representation of the constellation diagram and EVM. The 4K QAM modulation specified for WiFi-7 standard, is extremely susceptible to nonlinearities. Owing to the dense constellation of 4096 points, the signal quality can be greatly affected by any distortion or deviance from the original signal. The IEEE standard increases the performance requirement by 3 dB in WiFi-7 compared to previous WiFi-6, by setting a transmitter target Error Vector Magnitude (EVM) level of -38 dB for 4096 QAM [1]. Due to the extreme sensitivity of 4K QAM to nonlinearities, it is crucial to decrease EVM through careful power amplifier design and optimization.

1.1.4 Designing Linear Power Amplifier for WiFi-7

It is crucial to design a linear power amplifier which can achieve the high-performance requirements for Wi-Fi 7. This design strategy can be divided into two parts: circuit level design solutions and transistor level design solutions. A lot of circuit level design solutions are available to enhance the linearity of the PA, such as feedback and feedforward techniques, predistortion, matching networks, biasing techniques etc.

Transistor level design on the other hand deals with transistor technology, device modelling and simulation etc. In both cases, understanding the source and physical mechanism of nonlinearity in the PA is of essence to mitigate this. The scope of this study is to understand the origin of nonlinearity in the transistor and the associated physical effects of it. The goal is to improve the B9MW HBT technology, which is a 130nm HBT technology used for high-speed application, which in this case is to make it more compatible for WiFi-7 PAs.

1.2 Objective of the Thesis

The primary objective of this thesis is to:

- Examine the fundamental mechanisms of nonlinearity in BJT/HBT for applications requiring high frequency and high power.
- Identify an effective approach for examining the nonlinearity of the transistor characteristics.
- Provide recommendations for optimizing the BJT/HBT to improve the technology and linearity in PA.

1.3 Thesis Overview

The thesis report is organized as follows:

- **Chapter 1** gives a brief introduction to the RF and Wi-Fi systems, highlighting the technological advancements in WiFi-7. It also discusses the need for improved PAs needed in modern Wi-Fi chips to meet the standards of Wi-Fi 7. Additionally, it highlights the impact of nonlinearity on Wi-Fi 7 performance. Finally, a summary of the thesis's basic requirements is provided.
- **Chapter 2** covers the theoretical foundations of heterojunction bipolar transistors (HBTs), different configurations, and operating principles of the transistors. It also discusses the compact models used in this study for analysis. Additionally, it provides insight into different performance metrics that are important for PA and the nonlinearities. It also gives a brief background on the Monte Carlo analysis.
- **Chapter 3** outlines the systematic approach that was followed in this study. The motivations for using various techniques are also discussed.
- **Chapter 4** shows the results and discussions of this study, the key findings, and proposals to meet the objective of this study. It provides a comparative analysis between different techniques used and linking them together to find an efficient solution.
- **Chapter 5** concludes this work and provides the outline for future research in this study.

Chapter 2: Theoretical Background

2.1 Heterojunction Bipolar Transistors (HBT)

A bipolar junction transistor, or BJT, is a semiconductor device having three terminals and two p-n junctions formed by three layers of doped material. These regions are referred to as the base, collector, and emitter. By transporting and collecting charge carriers—holes and electrons—through these junctions, BJTs enhance electric current. The utilization of both electrons and holes as charge carriers is referred to as "bipolar" behavior. When two distinct semiconductor materials with differing bandgaps merge in the base and emitter regions, it creates a heterojunction. This improves speed and efficiency by enabling better control over charge carriers.

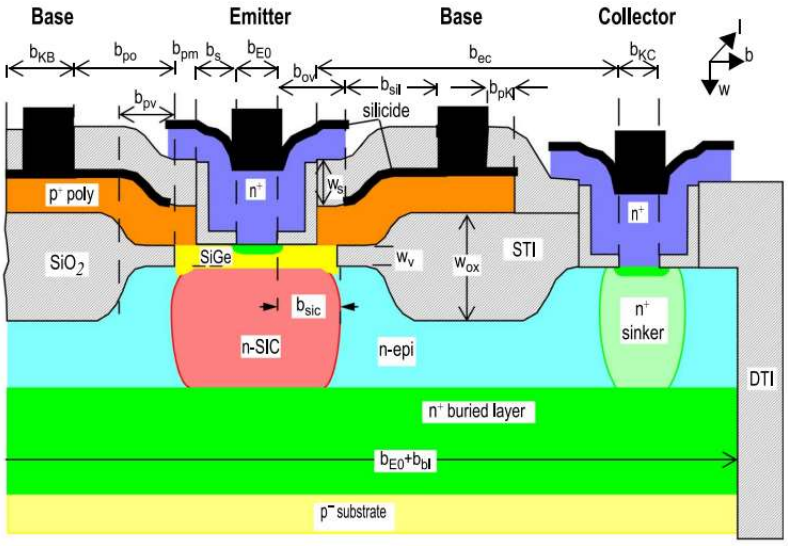

Figure 5: Cross-sectional diagram of a SiGe HBT's CBEBC structure [3]

In this research, a BiCMOS-based transistor called B9MW was studied. B9MW is a SiGeC HBT. Figure 5 shows the cross-section of a typical modern SiGe HBT structure in TCAD. SiGeC is an advanced type of HBT that has been used to develop the B9MW transistors. SiGeC HBTs improve performance by using the distinctive qualities of silicon, germanium, and carbon. Because of its thermal characteristics and availability, silicon makes a good foundation. Germanium performs better at high frequencies because of its lower bandgap, which lowers carrier transit times. Carbon (<1%) is used to improve thermal stability, sharpen doping profiles, and offset germanium's lattice strain [3] [4]. The collector-to-emitter breakdown voltage (BV_{CEO}) is improved, and the base current is increased by having a higher carbon dosage in the base region. The incorporation of SiGeC HBTs with CMOS technology improves their functionality and performance while lowering their cost.

2.1.1 Structure and Operating Principle

The primary advantage of BJTs over CMOS technology lies in their superior speed. Consequently, although BJTs may be categorized as either NPN or PNP, the majority of BJTs used in modern applications are of the NPN type. The preference for NPN transistors over PNP transistors is attributed to the greater mobility of electrons, which are the primary charge carriers in NPN transistors, in contrast to holes, which are the primary charge carriers in PNP transistors. An HBT consists of a base that is lightly doped, a collector that is moderately doped, and an emitter that is heavily doped. The base must possess sufficient physical strength and thinness to ensure proper operation, while also being thick enough to avoid "punch through," which is the undesired merging of the depletion zones at the emitter-base and base-collector junctions. Depending on the current flow and construction, HBTs can be classified into two categories:

- **Lateral HBT:** A lateral HBT is a transistor in which the current runs horizontally across the device. These types of transistors are more convenient to manufacture and incorporate into other components on a microchip. However, the speed and power handling capabilities of these components are restricted because of the longer paths that the electric current must travel.

- **Vertical HBT:** The current in a vertical transistor moves from the emitter to the collector vertically. This results in shorter current channels, which enables the achievement of faster speed and improved power handling capabilities. The vertical HBT is often used in high-speed, high-power communication applications because of its exceptional performance in terms of speed and power capacity.

Figure 6 illustrates the two distinct categories of HBTs. In this study npnvhs, which stands for “NPN Very High Speed”, from the B9MW technology was used. This is a vertical type transistor.

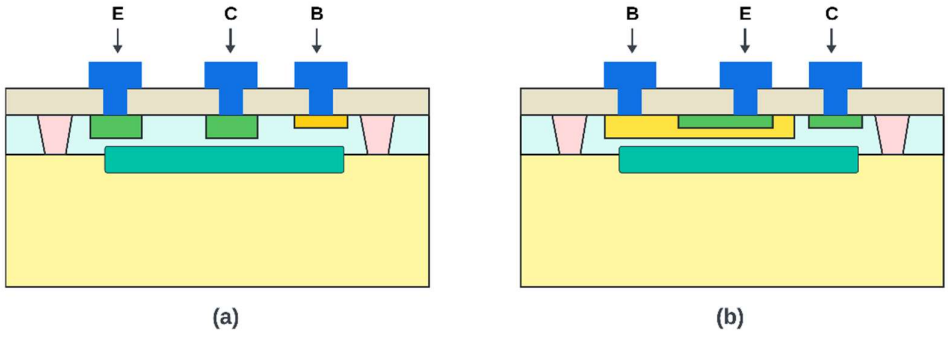

Figure 6: (a) Lateral transistor and (b) Vertical transistor.

2.1.2 Operating region

BJT can operate in four different regions: linear, saturation, cutoff, and reverse, depending on the applied voltage in the B-E and B-C junctions as shown in Figure 7. The intended operating region for RF applications is the BJT's linear region. However, because a PA's input power can fluctuate greatly (Large Signal Variations), the device may reach saturation which can cause nonlinearity in the circuit's behavior.

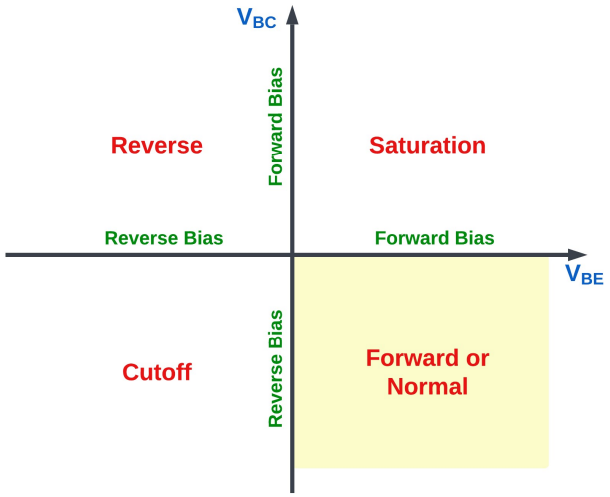

Figure 7: BJT operating regions.

Table 1 contains the conditions for different operating regions of HBT. Understanding these different operating regions is a fundamental requirement for understanding the transistor operating principle.

Region of Operation	BE Junction	BC Junction
Forward	$V_{BE} > 0$	$V_{BC} < 0$
Saturation	$V_{BE} > 0$	$V_{BC} > 0$
Reverse	$V_{BE} < 0$	$V_{BC} > 0$
Cutoff	$V_{BE} < 0$	$V_{BC} < 0$

Table 1: Biasing conditions of different operating regions in HBT

2.1.2 Transistor Configurations

BJT/HBT has three configurations for applications and based on the application, one configuration can be preferred over the other ones. Each configuration has its unique characteristics as given below [5]:

- **Common-Emitter Configuration (CE):** CE configuration offers a high voltage and current gain and is the most used configuration for amplification

applications. The Emitter is common to both the Base and Collector terminal. This provides a high input and output impedance and is easy to bias compared to other configurations. The high-power gain obtained from this configuration makes it suitable for RF Power Amplification applications.

- **Common-Base Configuration (CB):** CB configuration provides a small current gain (Less than unity) and a moderate voltage gain. The Base is common to both Emitter and Collector terminal and has a very low input and very high output impedance. Due to these characteristics, this configuration is often used in RF applications as a current buffer to match between a low-impedance source and a high-impedance load. The cascade RF power amplifier is another example of CB configuration.

- **Common-Collector Configuration (CC):** CC configuration provides a high current gain with a small voltage gain (Less than unity). The Collector is common to both the Emitter and Base terminal. This provides a very high input impedance and low output impedance, which makes it suitable for impedance matching between high impedance source and low impedance load. CC amplifier is often used as an emitter follower or voltage buffer circuit.

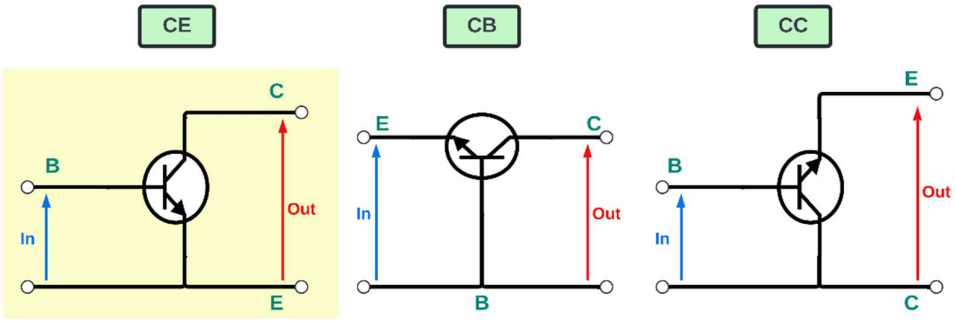

Figure 8: BJT Configurations

Figure 8 shows the different configurations of the transistors. For a linear PA, CE is the most suitable configuration. Modern PAs often consist of different transistor configurations in the different stages of the PA circuit to deal with different performance criteria.

2.1.3 HBT vs CMOS in Analog RF Communication

Heterojunction Bipolar Transistors (HBTs) are extensively used in analog RF transmission because of their superior electron mobility, enhanced linearity, and superior frequency capabilities. In contrast, CMOS technology has advantages such as reduced power consumption, increased integration density, and cost-effectiveness. Due to their lower performance in terms of speed and linearity, they are widely utilized in digital circuits but not well-suited for high-frequency analog RF applications. Figure 9 shows a comparison between the two kinds of transistors.

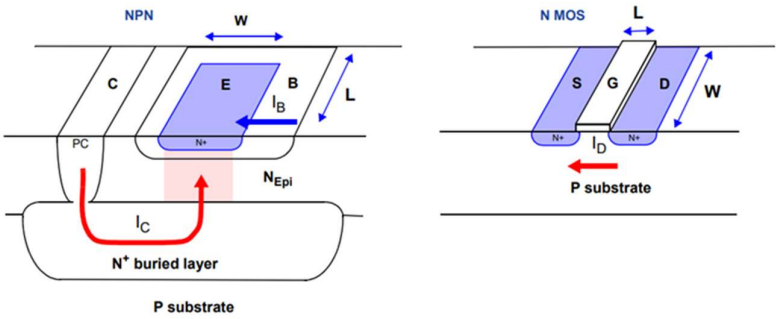

Figure 9: Comparison of BJT and CMOS technology.

From Figure 9 the NPN HBT is an active 3D device with two currents, I_C running perpendicular to the area and I_B flowing horizontally. This structure is asymmetrical. On the other hand, the NMOS is a 2D active device with just one current running perpendicular to the surface. In contrast to HBT, the MOS structure often exhibits a symmetrical configuration in which the drain current is directly proportional to the product of ID, W, and L. Table 2 shows the comparative description of these two technologies.

BJT/HBT	CMOS
3D Active Device	2D Active Device
2 Currents: I_C perpendicularly to the area, I_B horizontal	1 Current parallel to the surface
Nonsymmetrical structure	Symmetrical structure
$I_C \propto W.L \rightarrow$ I_C decreases when L increases	$I_D \propto \frac{W}{L} \rightarrow$ I_D increases when L decreases

Table 2: Comparison between BJT and CMOS

The B9MW technology is a BiCMOS based technology. BiCMOS technology combines Bipolar Junction Transistors (BJTs) and CMOS (Complementary Metal-Oxide-Semiconductor) transistors onto a single chip. It combines the low power consumption, high input impedance, and high integration density of CMOS with the fast speed, high gain, and low output impedance of BJTs.

2.1.4 Performance Metrics for HBT Selection

The key matrices to choose an HBT for RF PA are as follows:

- **Transition Frequency (f_T):** The cutoff frequency of an HBT indicates the frequency at which the transistor's AC current gain β (= i_c/i_b) drops to unity (0 dB). A transistor with a high f_T is preferred for high-frequency performance.

- **Maximum Oscillation Frequency (f_{max}):** Maximum Oscillation Frequency of an HBT indicates the frequency where the power gain of the transistor drops to unity (0 dB). This is crucial for applications like RF PA, where maintaining a higher gain at high-frequency operation is required.

- **Linearity:** The term "linearity" describes a transistor's ability to amplify signals in the desired range with little distortion.

- **Noise Figure:** The noise figure shows how much noise the transistor added to the signal after it was amplified. Lower noise figures are preferred for a greater Signal-to-noise ratio (SNR) in high-performance applications. Noise figures are more important for LNA than PA in RF applications.

- **Power efficiency**: The proportion of the transistor's total DC power used to its output RF power. Reducing power consumption and heat generation is vital for compact and battery-operated gadgets where high power efficiency becomes particularly necessary.

- **Breakdown Voltage:** The breakdown voltage of a transistor indicates the voltage between the CE or the BC junction that the transistor can withstand without damaging the device. RF PA is designed to withstand large signal variations for that a supply voltage is necessary. However, higher breakdown voltage can often lead to lower current gain due to the thick depletion region needed to sustain the high voltage. So, a trade-off is needed when choosing a transistor with high break-down voltage.

2.2 HBT Compact Models

To emulate the behavior of a transistor in spice simulators, equivalent circuit models are used. Discrete components, such as diodes, capacitances, resistances, and current or voltage sources, are the foundation of a compact model of these equivalent circuits. Therefore, understanding the related transistor components is a prerequisite to comprehending a compact model.

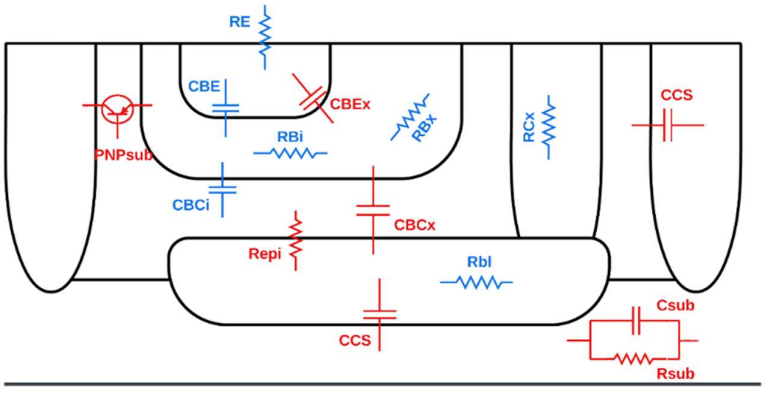

Figure 10: Schematic Cross-section of a BJT

Figure 10 shows the schematic cross-section of a bipolar transistor. The blue components in Figure 10, are implemented in the Standard Gummel-Poon Model (SGPM), which was used by majority of SPICE simulators in the early days. The SGPM does not take into consideration the red components. With increasing demands of high-frequency and high power for modern applications, these parameters started to become significant in the transistor and the circuit's overall performance, which resulted in the necessity of discovering more advanced compact models like VBIC, HICUM, and MEXTRAM. Here are some of the most advanced compact models used for BJT/HBT:

- **VBIC (Vertical Bipolar Inter-Company):** A sophisticated model that incorporates self-heating effects, avalanche breakdown, and other HBT-related phenomena into the Gummel-Poon model [6].

- **HICUM (High Current Model):** This model is very helpful for simulating HBTs in high-speed applications since it concentrates on high-current effects [7].

- **MEXTRAM (Most EXtended TRAnsistor Model):** A comprehensive model appropriate for RF applications that incorporates a variety of physical factors, including substrate coupling and noise [8].

In STM, HICUM-based models are incorporated for BJT/HBT simulations. The HICUM model has different levels. HICUM/L2 is the preferred model, which is very complicated compared to the SGPM model. This created the necessity to develop a simplified version of the HICUM/L2 model called HICUM/L0 which is more physics-based and improved compared to SGPM but will fall into the same class as SGPM in terms of simplicity. HICUM/L0 doesn't contain all the features like HICUM/L2 but contains the essential features of the transistor's behavior. There are often very few critical transistors, for which a very sophisticated and accurate model is required that considers all the effects. In this study the HICUM/L0 model was investigated and compared with the HICUM/L2 models. A brief discussion of both models is given in the next section.

2.2.1 HICUM/L2 Model

A compact model for homo- and heterojunction bipolar transistors that is based on geometry and physics. It is appropriate for cutting-edge process technologies because of its excellent precision at high frequencies and large current densities. The model contains over 100 parameters that are often difficult to grasp for designers who have little knowledge of the model. Figure 11 shows the complete EC of the HICUM/L2 model. HICUM/L2 represents all the known critical physical effects in a simpler way. But to circuit designers, it often appears as a fairly complicated model due to its resulting equivalent circuit and model equations. However, in most PA circuits, the transistor structure implemented tends to be somewhat big. They are often implemented as arrays of fixed-finger transistors (i.e., cells) or as multi-finger transistors. However, the resulting electrical and thermal effects distributed in the lump models can’t always be represented with sufficient accuracy, even with an advanced model like HICUM/L2.

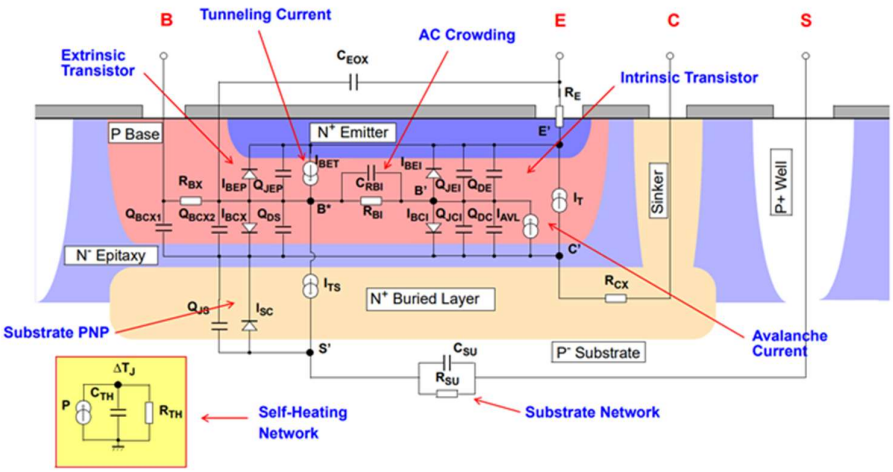

Figure 11: The HICUM/L2 model with all the associated elements of a BJT [7]

2.2.2 HICUM/Lo Model

A reduced-complexity variant of HICUM/L2 is intended to rectify the shortcomings of previous models such as the SPICE Gummel-Poon model. It is helpful in bigger circuit simulations when a complete HICUM/L2 model might not be required. Regarding the ease of use of the equivalent circuit and element equations, HICUM/Lo is comparable to SGPM; however, it addresses long-standing shortcomings of SGPM for more sophisticated process technologies. Compared to the SGP, it has better physics-based model equations. But unlike HICUM/L2, HICUM/Lo does not include all the transistor's effects. Among the effects absent from HICUM/Lo are the noise correlation between the transfer current and the dynamic base current, the strong avalanche effects, and the substrate network. Figure 12 shows the EC of the HICUM/Lo model. Parameters associated with different parts of its EC are given in **Appendix 2**.

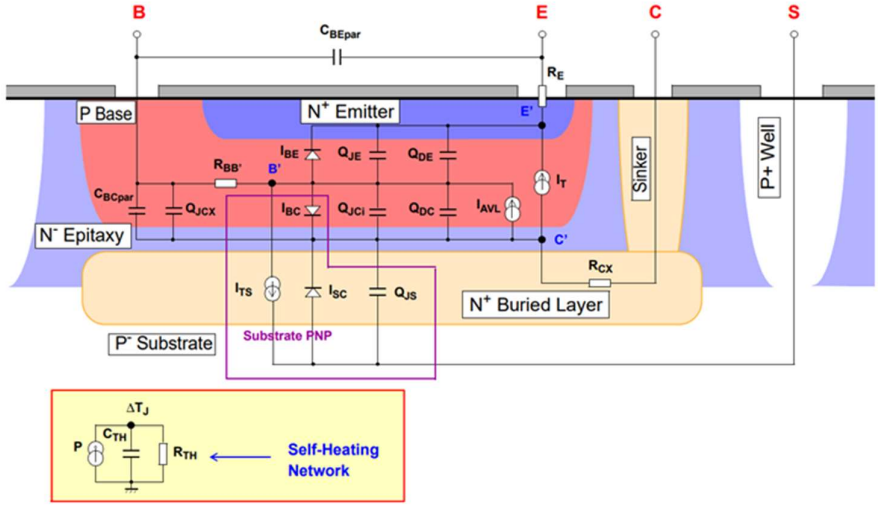

Figure 12: The HICUM/Lo model with the associated elements of a BJT [7]

2.2.3 Compact Model Comparison

Table 3 gives the list of physical effects that are not present in the HICUM/L0 and SGPM models compared to the HICUM/L2 model [7].

Physical Effects	HICUM/L2	HICUM/L0	SGPM
Partitioning of BE Capacitance	x		
Partitioning of BC Capacitance	x	x	x
BC Capacitance Punch-through	x	x	
Parasitic BE and BC oxide Capacitance	x	x	
Parasitic PNP Substrate Transistor	x	x	
Split of Base Resistance with BE and BC Capacitance	x		
Conductivity Modulation and Current Crowding of the Base Resistance	x	x	
BC Barrier Effect at High Currents	x		
Tunneling Current in the EB junction (at reverse mode)	x		
NQS Effect	x	x	x
Impact Ionization	x	x	
Physics-Based Transit Time Model	x	x	
Bias and Bandgap Dependent Reverse Early Effect (HBTs)	x	x	
Substrate Network	x		
Flicker Noise Associated with the Emitter Resistance	x		
I_C and I_B Noise Correlation	x		
Self-Heating	x	x	
Lateral Scaling	x		

Table 3: Comparison of the compact models.

From Table 3, the physical effects missing in the HICUM/L0 model compared to HICUM/L2 can be identified. As HICUM/L2 is the most accurate spice model, the data from HIUCM/L0 in this study are validated against the HICUM/L2 model.

2.3 Nonlinearities in HBT

The performance of Heterojunction Bipolar Transistors (HBTs), which are used in Power Amplifiers (PAs) for Wi-Fi 7 applications, can be greatly affected by nonlinearities in the device. The following are some significant nonlinearities that may be seen in HBTs:

- **Avalanche Multiplication:** When the movement of charge carriers in the device becomes sufficiently strong to generate additional charges, it creates a chain reaction which is referred to as Avalanche Multiplication. In single stage common emitter amplifier, this phenomenon plays a dominant role as the source of nonlinearities. At low bias, this effect limits the IIP3 (third-order intercept) producing nonlinearity in the device [9].

- **Collector-Base Capacitance:** The capacitance between the collector-base junction can introduce nonlinearities in the response of the HBT at high-frequency operations when operating at high bias. CBC is not bias dependent, and it changes with the input voltage as high input voltage can alter the bias point of the transistor. This phenomenon is also observed for CBE. This introduces the Miller effect, which means the equivalent capacitance varies with the voltage gain thus leading to gain compression. This can lead to poor performance in the gain and phase response of the circuit [9].

- **Thermal Effects:** At high-power and high-frequency applications like RF power amplifications, HBTs often become sensitive to thermal effects as the transistor's temperature varies with instantaneous power (Self-heating). Self-heating is a common issue when the transistor is operating at high power levels, which often leads to an increase in thermal resistances and variation in transistor parameters leading to instabilities in the circuit [10].

2.4 Figure of Merits of PA

Power amplifiers are frequently implemented to meet certain requirements, such as output power, efficiency, and linearity. Nonetheless, to get the necessary bit-error rate at the output, power amplifier designers frequently have to build their PA to operate with a certain combination of receiver characteristics and channel connection. In these situations, it is essential to become familiar with the Figure of Merits (FoM) of Power Amplifier.

- **Gain:** The Gain or Power Gain of a PA refers to its ability to amplify the input power to the output power. Usually, a higher gain is preferred for a good PA. The gain of a PA can be found from:

$$Gain, G = \frac{P_{out}}{P_{in}}$$

- **Output Power:** The output power of a PA indicates the power it can deliver to the load. The maximum output power indicates the power up to which the PA can operate linearly after which it starts to distort significantly.

- **1dB Compression Point:** The input compression point is the input power level at which the gain of the PA drops by 1dB and the Output Compression point is the output power at that point. The compression point is an important parameter to indicate the linearity of the PA.

- **Power Added Efficiency (PAE):** PAE indicates the efficiency of a PA to convert the DC supply power into the RF output power for amplification. Often designers need to make a trade-off between the efficiency and the linearity of the PA. PAE of a PA can be calculated as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\%$$

- **Third-order Intercept Point (IP3):** The third-order intercept point indicates the point at which the third-order intermodulation product will intersect the fundamental signal of the PA and cause intermodulation distortions in the output signal.

- **Total Harmonic Distortion (THD**): The total harmonic distortion in the PA indicates the distortions that are introduced by all the harmonics in the signal. Harmonics are usually generated as the integer multiple of the fundamental signal. Harmonic distortion can cause severe degradation in the output signal quality of a PA.

2.5 Linear RF Theory

The goal of linear RF PAs is to boost signals without significantly distorting them. They ensure that the output signal accurately reproduces the input signal by operating in the linear zone of the transistor's transfer characteristics. For various purposes, several PA topologies are used. The main consequences of different PA topologies or classes are reflected in three figures of merits: Linearity, Gain, and Efficiency. PA classes can be divided into two primary categories: The conducting class and the switching class. Based on the current waveforms, conducting class PA can be highly linear. In contrast, the switching class employs the transistor as a switch. The most often-used PA topologies are shown below [11].

- **Class A:** This type of transistor is biased in the middle of the transistor's linear region, which facilitates high linearity and low distortion but with a low efficiency (20-30%). Class A is suitable where great signal quality is required.

- **Class B:** Class B transistors are active for half of the input signal cycle and are biased in the cutoff region. When efficiency is the top concern and some distortion is acceptable for the application, Class B amplifiers should be considered over Class A amplifiers.

- **Class AB:** It combines the benefits of Class A and Class B amplifiers to strike a compromise between linearity and efficiency. To minimize crossover distortion, the transistor is biased with the Q-point being just above the cutoff region, which can yield an efficiency of around 50–60%.

- **Class C:** These amplifiers are suitable in situations where efficiency is critical, and linearity may be traded off. The transistor produces short impulses of current with an extremely high efficiency of 80–90% while it is biased much below the cutoff point and conducts for a small fraction of the input signal cycle.

- **Class D, E, and F:** Uses certain waveform shaping methods to operate in a switching mode as opposed to a linear mode. It provides high efficiency combined with different levels of linearity and is ideal for high-frequency applications.

Due to the switching operation of the switching class PAs, they exhibit high nonlinearity, making them unsuitable for the extremely precise QAM scheme employed in modern wireless systems. Figure 13 shows the comparison of conduction angle, power, and efficiency between different types of conducting class PAs. It can be observed that PAs can be made more efficient by reducing the conducting angle. However, reducing the conducting angle also lowers the gain and linearity of the PA. The clipping effect that occurs at the output current due to the reduced conduction mode introduces nonlinear effects in the output.

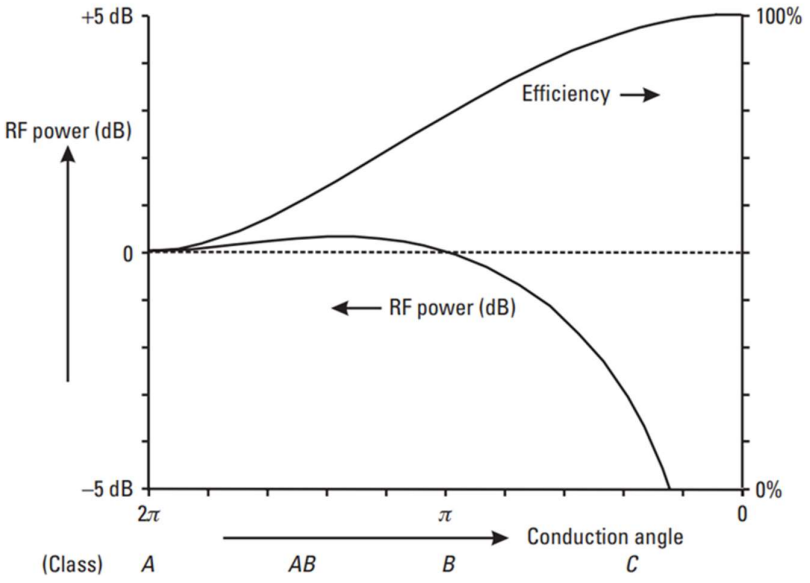

Figure 13: Conduction angles, power, and efficiency of different PAs at maximum drive level [11]

As the conduction angle starts to decrease, the harmonic currents start to increase. This can be observed from the current components of the output current shown in Figure 14. Between classes A and B, the fundamental output power is fairly stable. As the conduction angle lowers, the DC current falls, resulting in an enhancement in efficiency. However, the reduced conduction angle also induces an increase in harmonics, while the second harmonic is dominating over the entire conducting angle range, while other higher-order harmonics are small. Therefore, PAs are often biased in class AB to achieve the required performance for wireless transmission with some tradeoffs.

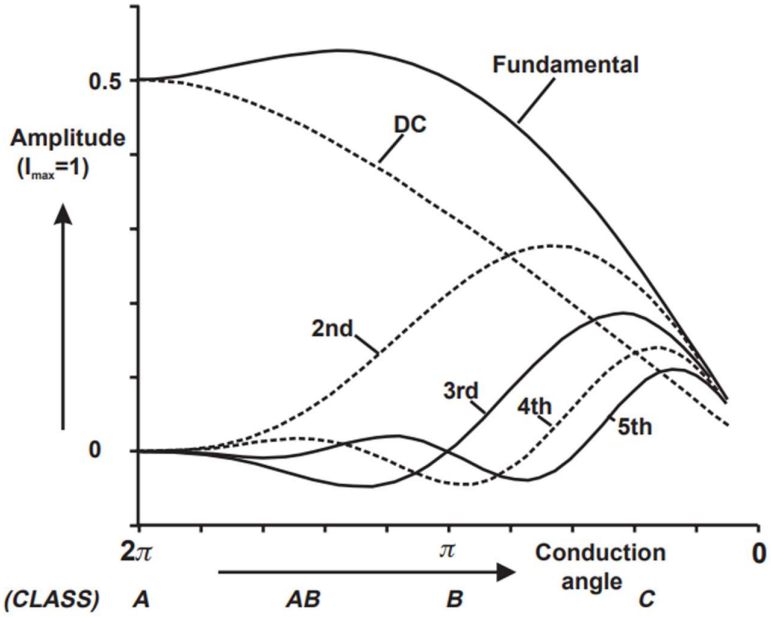

Figure 14: Different components of the Output Current [11]

Table 4 shows the biasing conditions of different conducting class PAs with their conducting angles.

	Quiescent Bias Point ($V_{bias} - V_{be\,(on)}$)	**Quiescent Collector Current (I_q)**	**Conducting Angle**
Class-A	$\frac{V_{in\_max}}{2}$	$\frac{I_{max}}{2}$	2π
Class-AB	$0 - \frac{V_{in\_max}}{2}$	$0 - \frac{I_{max}}{2}$	$\pi - 2\pi$
Class-B	0	0	π
Class-C	< 0	0	$< \pi$

Table 4: Modes of operation for conducting class PA.

2.6 VerilogA

Every semiconductor fabrication procedure that involves circuit design depends on an accurate depiction of the electrical behavior of components, such as transistors, diodes, and resistors, and those are referred to as "Spice models" or simply Compact Models. In recent years, major compact model developers have adopted the Verilog-AMS (Analog/Mixed Signal) hardware specification language and, especially, its analog-only version, known as VerilogA. VerilogA has similar constructs as C and is a subset of Verilog-AMS as shown in Figure 15.

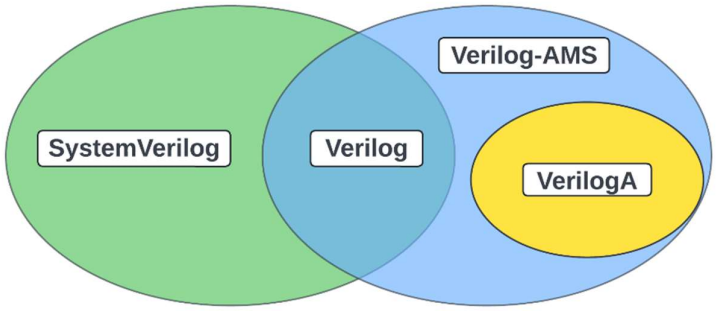

Figure 15: VerilogA: A Verilog-AMS Language subset.

VerilogA provides the basic structures to explain the model's behavior for the simulation tools. Circuit designers can define the characteristics of modules by defining the mathematical relationships among the current and voltage terminals of the modules (behavioral units in a circuit), which are generated by the programming language. Additionally, Verilog-A provides a powerful framework for specifying model parameters. It is possible to specify the range of effective values in addition to the default value in the declaration statement. The default value may be defined based on other factors as well, which makes it helpful for determining the relationship between input and output signals. All of this makes VerilogA a very effective programming language for developing compact models. [12]

2.7 Monte Carlo Simulation

When random variables interfere with a process and make it difficult to forecast, one method to estimate the likelihood of various outcomes is to use a Monte Carlo simulation. Numerous issues in a variety of disciplines, such as business, physics, engineering, and investment, can be solved by Monte Carlo simulations. It is sometimes called a simulation that includes multiple probabilities. In the case of a circuit design, Monte Carlo simulations are frequently used to analyze the impact of variations in different parameters on the performance metrics. The process variation of a semiconductor manufacturing process indicates the variance that can occur during the manufacturing process and how it can impact the performance of the circuit. This can be used to find the correlation between the process variation parameters and the model parameters. The process variation parameters then can be linked to the transistor architecture and properties to find valuable information about the optimization of the

device. In this study, two scopes of the Monte Carlo simulation were studied to explore the relation.

2.7.1 Variance Contribution

Variance contribution indicates which process parameters contribute how much to the variance of a performance matrix. It is usually expressed in percentages and is a good way to do a sensitivity analysis of the parameters. This is a very useful statistical analysis for circuit designers to identify key contributors to performance variability.

2.7.2 Correlation

Correlation coefficients are used to indicate the linear correlation between two parameters. It can be used to find the positive or negative correlation between two parameters and the strength of the correlation. Usually, the measure ranges from -1 to 1 to indicate the strength as well as the direction of the relationship between the parameters. Also, the Cadence Monte Carlo simulation tool allows us to find the cross-correlation of different performance matrices, which is significant for finding the trade-off between different parameters when optimizing.

Chapter 3: Methodology

3.1 Overview

This chapter provides an overview of the systematic approach used in this work to examine the non-linearity in Bipolar Junction Transistors (BJTs), with a focus on their use in Class AB Power Amplifiers (PAs) for WiFi-7. The two primary techniques of the methodological approach are the Bottom-Up Approach, which explores the HICUM/L0 model parameters in-depth, and the Top-Down Approach, which concentrates on creating and evaluating a unique equivalent BJT model as shown in Figure 16. Monte Carlo simulations are also used to confirm the results and pinpoint important design aspects that affect the transistor's overall performance.

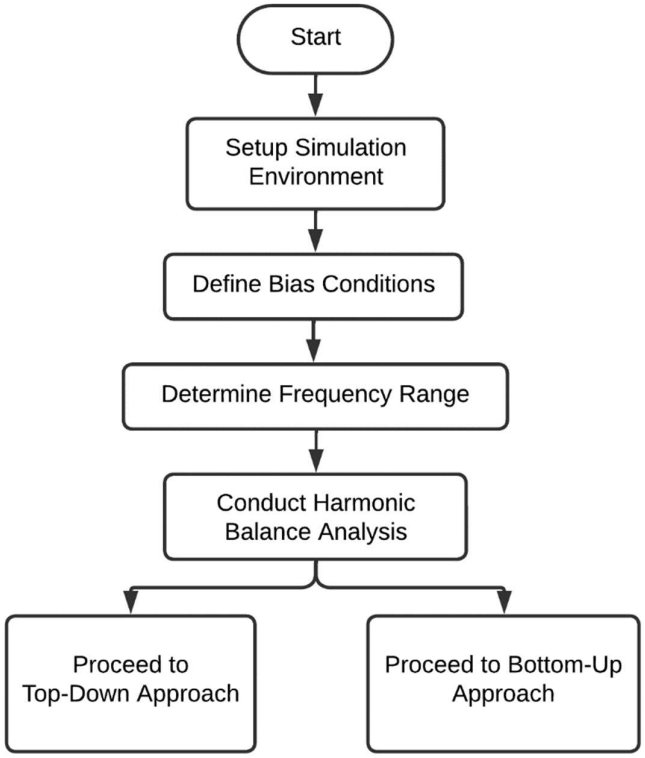

Figure 16: Overview of the Methodological Approach

For the reference data of B9MW, the HICUM/L2 model was used as it gives the most accurate response. Then the data from HICUM/L0 was compared with the reference B9MW.

3.2 Experimental Setup and Simulation Parameters

3.2.1 Bias Conditions

The B9MW BiCMOS technology utilized in this work has a variable emitter length of 0.6 µm to 15 µm and a fixed emitter width of 0.27 µm. The collector current (I_c) in that instance is proportional to the product of the emitter length (L) and width (W). To bias the PA, first the optimal load for the PA needs to be determined. The load line theory yields, optimum linearity, and output power can be obtained when the transistor is biased to have an equal swing between the collector saturation voltage and the maximum collector voltage. The load resistance is thus determined as 25 ohms from the voltage constraints and targeted output power of the amplifier. This gives the biasing current I_C = 10 mA. The transistor is determined to have V_{be}/L conditions to provide meaningful F_t/F_{max} for the application. It also determines the number of parallel transistors required to get 10 mA. Using this condition, the emitter length was set to 10 µm with eight transistors in parallel, to keep a balance between high current density and manageable thermal characteristics. Multiple parallel transistors also help in distributing the current load to reduce stress on individual transistors, while enhancing the total current capacity of the circuit. So, the quiescent bias of VCC=1 V and IC = 10 mA was chosen for the analysis to ensure high-frequency performance and efficient signal amplification while keeping power consumption in check.

3.2.2 Frequency Range

WiFi-7 has three frequency bands: 2.4 GHz, 5 GHz, and 6 GHz. Figure 17 shows the transconductance nonlinearity in the PA for these frequencies.

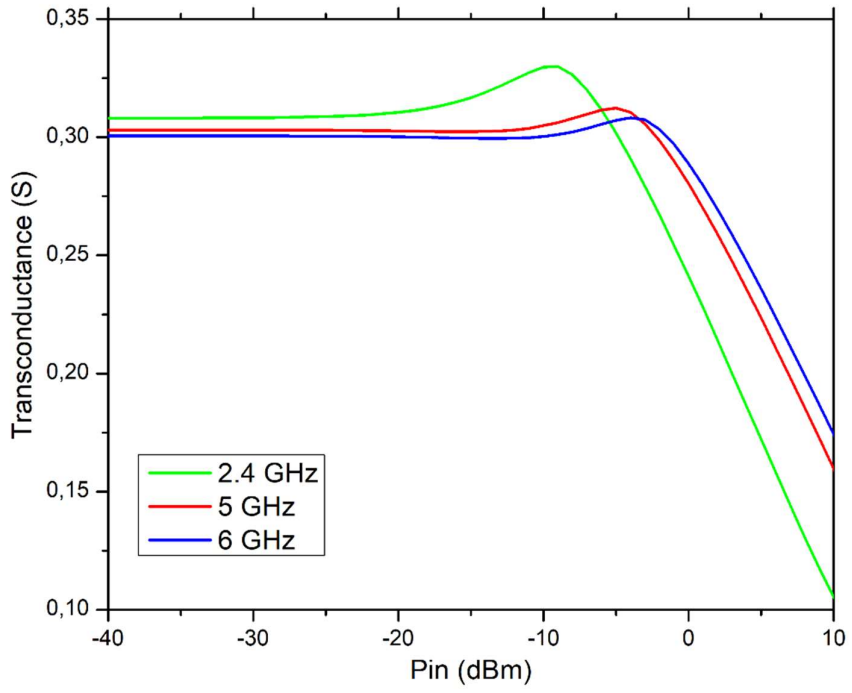

Figure 17: Transconductance of the PA for different frequencies.

From Figure 17, it can be observed that even though all the frequencies show similar nonlinear behaviors, different frequency bands will require different tradeoffs with different PA designs. In this study, the analysis is kept limited to 5 GHz.

3.2.3 Harmonic Balance Simulation

Nonlinear circuit analysis benefits greatly from the use of harmonic balance analysis, which can accurately project the behavior of the circuit. The range of the input power was adjusted at -40 dBm to 10 dBm. This range was chosen to see if the PA can amplify weak signals effectively while testing its ability to handle high-power signals without significant distortion. The number of harmonics to take into account was set to 13 so that the analysis could capture the nonlinear behavior of the circuit more precisely.

3.3 Top-Down Approach: Custom Equivalent BJT Model

In the top-down method, building a unique equivalent model of the BJT is the first step. The goal of this model is to represent the transistor's both linear and non-linear behavior. In order to construct the custom model, a small-signal model representing the behavior of the transistor with small input signals has to be developed first. The different non-linear effects seen in the BJT are then taken into consideration by adding non-linear components to this small-signal model. This was done by implementing the BJT with verilogA as shown in **Appendix 1**. Figure 18 shows the overview of this methodology.

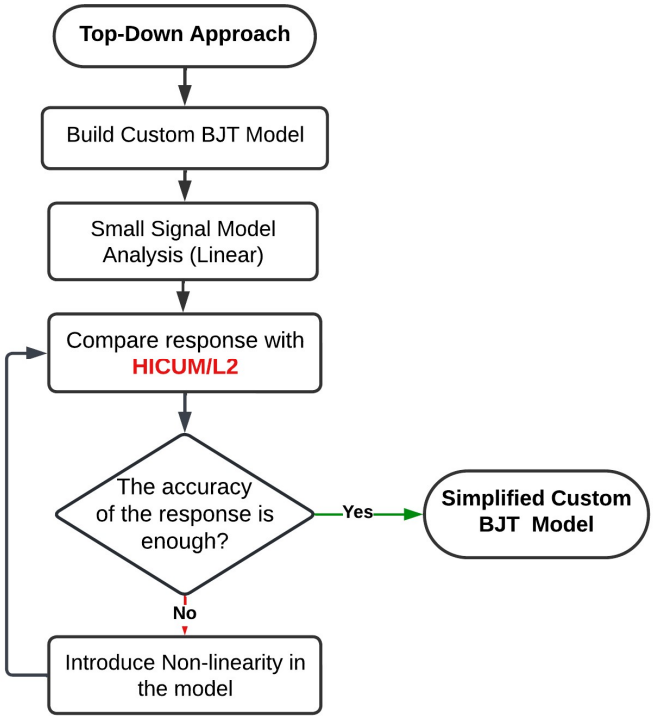

Figure 18: Overview of the Top-Down Approach

3.4 Bottom-Up Approach: Investigating HICUM/L0 Parameters

The first step in the bottom-up strategy is to extract the model card of HICUM/L0 for B9MW. Then identify the critical HICUM/L0 model parameters that affect the behavior of the BJT. Based on how these characteristics affect non-linearity, frequency responsiveness, and overall transistor performance, they are divided into three priority categories: Priority 1, Priority 2, and Priority 3. The priority was defined by the experts from the modelling team from their prior knowledge of transistors' linearity. Then the Default HICUM/L0 model file was taken, and the value of the parameters was changed one at a time with the value of B9MW. The default values of the HICUM/L0 model are set in a way that only reflects the Gummel-Poon Model of a general transistor unless the parameters are changed to the HICUM/L0 model card for that specific technology. The response was compared with the B9MW HICUM/L2 response, as the HICUM/L2 model considers all the physical effects of the transistor. After analysis of all the parameters, the reduced parameter list was identified that plays a significant role. Figure 19 shows the overview of the Bottom-Up approach.

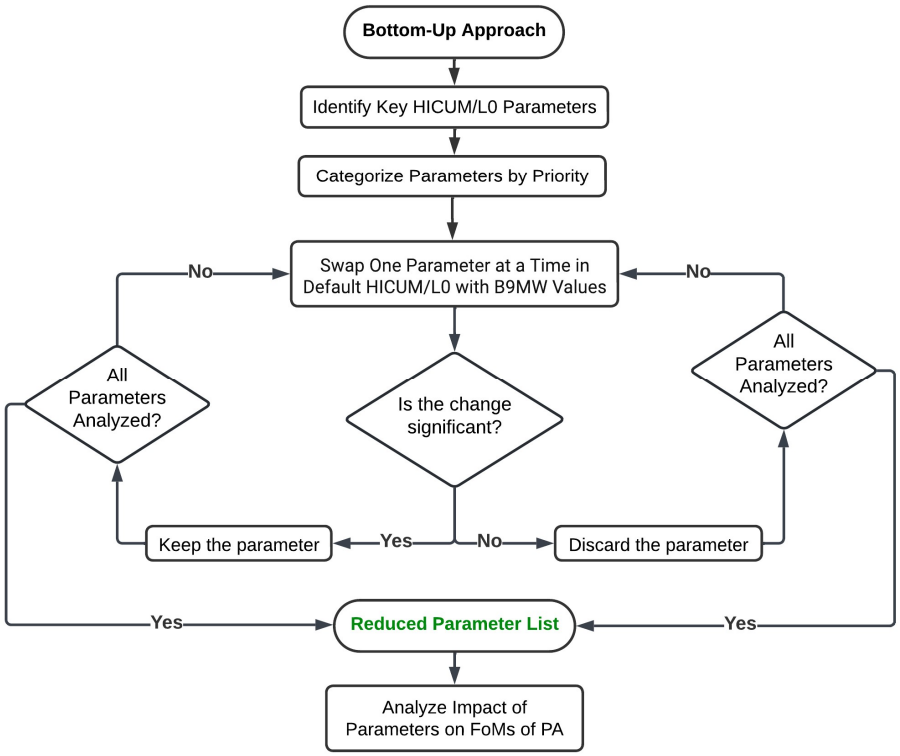

Figure 19: Overview of the Bottom-Up Approach

After identifying the key parameters, the impact of each parameter on the FoMs of the PA was analyzed.

3.5 Monte Carlo Simulation Analysis

Monte Carlo simulations are a statistical method that was used in this work to evaluate the effect of model parameter variability on FoMs of PA and design parameter variability on model parameters. The final objective was to create a link between the transistor's design parameter, model parameter, and FoMs of the PA. The statistical analysis of the design parameters was done to identify critical design parameters that are linked to the reduced parameter list of HICUM/L0. On the other hand, the statistical analysis of the model parameters was done to identify the link between them and the FoMs of the PA. The statistical variation of the design parameters that are associated with the process variation is defined in the STM's internal model file, which was used here to analyze the correlation. Figure 20 shows the overview of the Monte Carlo simulation analysis.

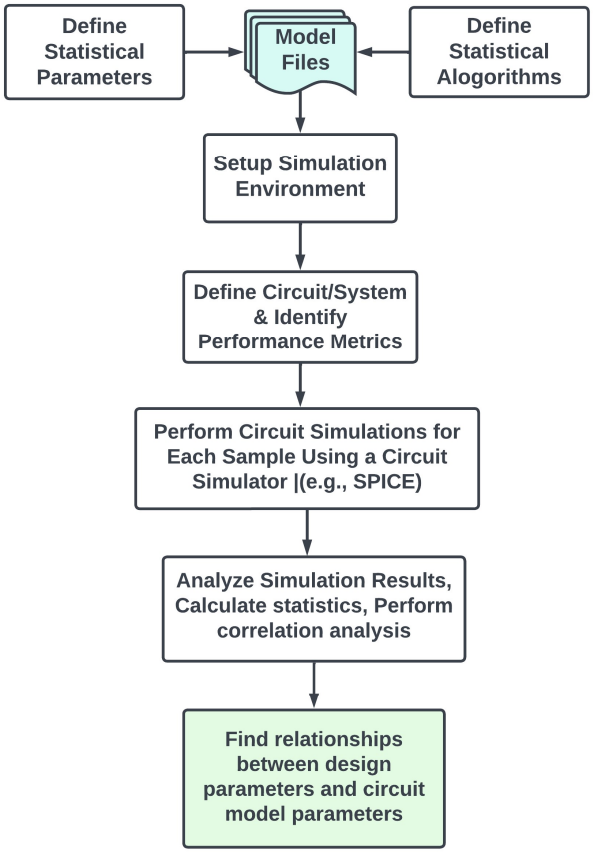

Figure 20: Overview of the Monte Carlo Simulation

To perform the Monte Carlo analysis, statistical parameters were set with the corresponding algorithms. The model file containing the statistical definition for transistor design parameters and HICUM/L0 model parameters are then loaded to do the Monte Carlo Analysis.

Chapter 4: Results & Discussion

4.1 Overview of the Simulation Setup

The study was conducted entirely through simulations using Cadence Virtuoso Spectre, a powerful tool for analog and RF circuit design and analysis. To investigate the nonlinear behaviors of PA, the simulation environment was built up using the comprehensive circuit layout shown in Figure 21.

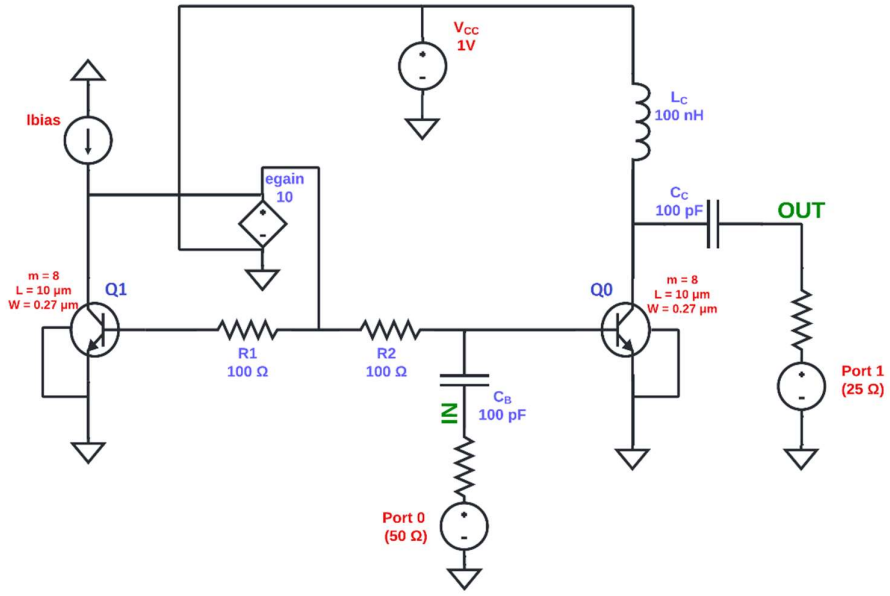

Figure 21: Single Stage Common-Emitter Power Amplifier.

Figure 21 shows the schematic of the PA used for this analysis. The inductor L_C is used as an "RF Choke" and its value is large enough to function as an AC open circuit at the operating frequency. The AC coupling capacitor C_B and C_C are used in the input and output to block the DC bias point of the amplifier. Port 0 serves as the input port which consists of a 50Ω input impedance and the source. Port 1 serves as the output port which consists of a 25Ω output impedance. The current source Ibias is used to set the desired biasing current to get the current Ibias at the collector of the amplifying transistor. The collector current in transistor Q0 is modulated by the negative feedback provided by base resistors R1 and R2. The biasing circuit in the schematic provides the quiescent bias V_C=1 V and I_C=10 mA.

After that, the simulation environment was set up, and the frequency and bias conditions were chosen for this study as described in the Methodology chapter.

4.2 Top-down Approach: Custom Equivalent BJT Model

4.2.1 Building the Custom Equivalent Model

The custom equivalent BJT model was constructed using the ST-BJT small signal model as shown in figure 22.

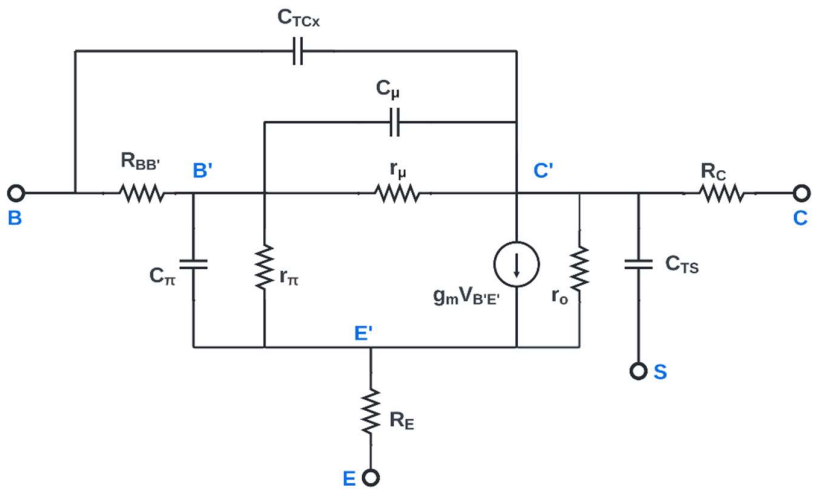

Figure 22: ST-BJT small signal equivalent circuit.

The ST-BJT small signal model is a simplified HICUM/Lo small signal equivalent circuit. The model is comprised of components such as resistors, capacitors, etc., each of which plays a specific role in the transistor's overall performance. A brief description of the parameters of the transistor is given below:

- C_{TCx} = Internal Collector to External Base Capacitance
- C_μ = Internal Base-Collector Junction Capacitance
- r_μ = Base-Collector Junction Capacitance
- C_{TS} = Internal Collector to Substrate Capacitance
- C_π = Diffusion Capacitance
- r_π = Internal Base to Internal Emitter Resistance
- R_E = Emitter Resistance
- R_C = Collector Resistance
- $R_{BB'}$ = Base spreading resistance
- g_m = Transconductance

At first, a DC analysis was done to extract the DC operating point of the transistor. To model the equivalent circuit of B9MW, the model parameters were extracted from the DC operating points as shown in Figure 23.

beta(A/A)=486.52127	crbi(F)=0	itf(A)=0.0099934362	rmui(Ohm)=-12869638	vbcx(V)=-0.16970761
betaac=418.13428	dtsh(C)=2.1786329	itr(A)=2.7543627e-19	rmus(Ohm)=inf	vbe(V)=0.82517765
betadc(A/A)=486.52127	ft(Hz)=8.7529509e+10	pwr(W)=0.0099274013	rmux(Ohm)=1.25e+11	vbei(V)=0.82363685
betar(A/A)=487.52127	gm(S)=0.32763693	qdci(Coul)=6.8859067e-29	ro(Ohm)=40443.809	vbep(V)=0.82364007
cbc(F)=1.4394126e-13	gmavl(S)=1.347424e-07	qdei(Coul)=4.8840306e-15	roi(Ohm)=40571.307	vce(V)=1
cbe(F)=4.2034921e-13	gmi(S)=0.32763693	qdsu(Coul)=0	ros(Ohm)=2.024571e+39	vcei(V)=0.99339186
ccs(F)=3.7427098e-14	gms(S)=8e-12	qf(Coul)=4.8840306e-15	rpii(Ohm)=1603.5001	vef(V)=403.17923
cdci(F)=2.6428987e-27	iavl(A)=4.1095428e-09	qjci(Coul)=-4.6108354e-15	rpix(Ohm)=6252.6205	ver(V)=-0.7931376
cdei(F)=1.6028501e-13	ib(A)=2.0540603e-05	qjcp(Coul)=-8.9528283e-15	rsu(Ohm)=3357.0941	vsc(V)=-1
cdsu(F)=0	ibci(A)=-1.1972118e-28	qjcx(Coul)=-1.1522057e-14	sfb=0.32763693	
cjci(F)=2.6438579e-14	ibei(A)=1.6361122e-05	qjei(Coul)=9.1208648e-14	sfc=2.4725663e-05	
cjcp(F)=5.0090977e-14	ibep(A)=4.1678471e-06	qjep(Coul)=2.7021216e-14	si(S)=2.4725663e-05	
cjcx(F)=6.7411706e-14	ibet(A)=0	qjs(Coul)=-1.0451682e-14	srb=9.0302255e-18	
cjei(F)=1.6504416e-13	ic(A)=0.0099934403	qp(Coul)=4.5347997e-13	src=-1.0571595e-17	
cjep(F)=4.1018142e-14	ie(A)=-0.010013981	rb(Ohm)=2.3478075	temp(C)=29.178633	
cjs(F)=3.7427098e-14	ieei(A)=0.010013981	rbi(Ohm)=0.19673843	tf(s)=4.8918589e-13	
cmui(F)=2.6438579e-14	ijbcx(A)=-3.5672992e-18	rbx(Ohm)=2.1510691	tk(K)=302.32863	
cmux(F)=1.1750268e-13	ijsc(A)=-1.0291915e-14	rcx(Ohm)=0.51180964	vbc(V)=-0.17482235	
cpii(F)=3.2532916e-13	is(A)=-1.0291915e-14	re(Ohm)=0.14913112	vbci(V)=-0.16975501	
cpix(F)=9.5020044e-14	it(A)=0.0099934362	region=1	vbcp(V)=-0.1697518	

Figure 23: Extracting model parameters from the DC operating points.

After extracting the model parameters, the values were used to create the ST-BJT small signal model of B9MW as shown in Figure 22.

4.2.2 Analysis of Non-linearity in the Custom Model

Linear Model:

After building the equivalent model, an initial investigation of the nonlinearities was performed. For comparative purposes, this linear model acts as the standard. It depicts the ideal linear dependence on collector current (I_c) with base-emitter voltage (V_{be}). The transconductance response of the linear model compared to the actual transistor is shown in Figure 24.

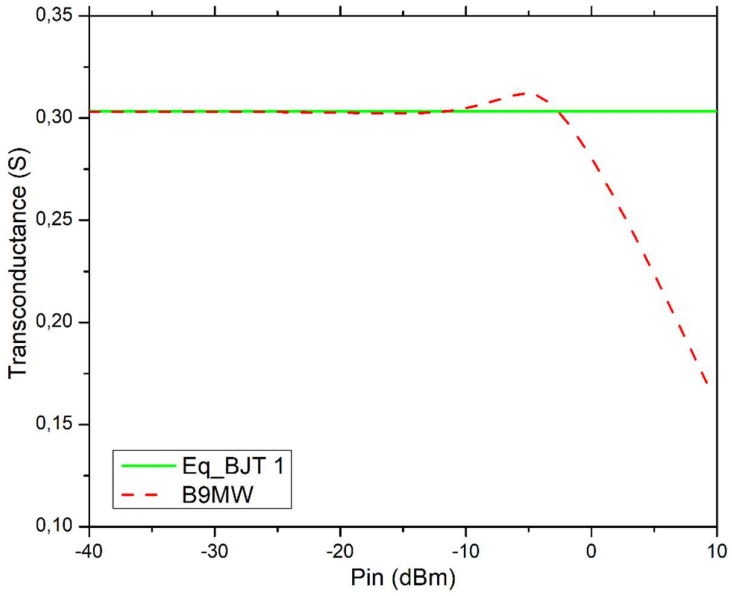

Figure 24: Response of the linear model compared to B9MW.

Figure 24 shows that the Eq BJT 1 (constant gm model) can effectively predict the transistor behavior when the input power is low. This is because, under low power conditions, the transistor operates in the linear region as the input signal variations are small. However, nonlinear models are needed to accurately predict the behavior of the transistors when there are large signal variations in the input.

Nonlinear Model:

Moving beyond the linear model and taking nonlinear factors into account was crucial in predicting the transistor's behavior under different input power conditions. The analysis was started by introducing nonlinearities in the model systemically to capture the different effects separately. This approach allowed us to comprehend the impact of nonlinearity in the transistor's overall performance in the power amplifier for applications like WIFI-7. Figure 25 shows the response of the different models compared to B9MW.

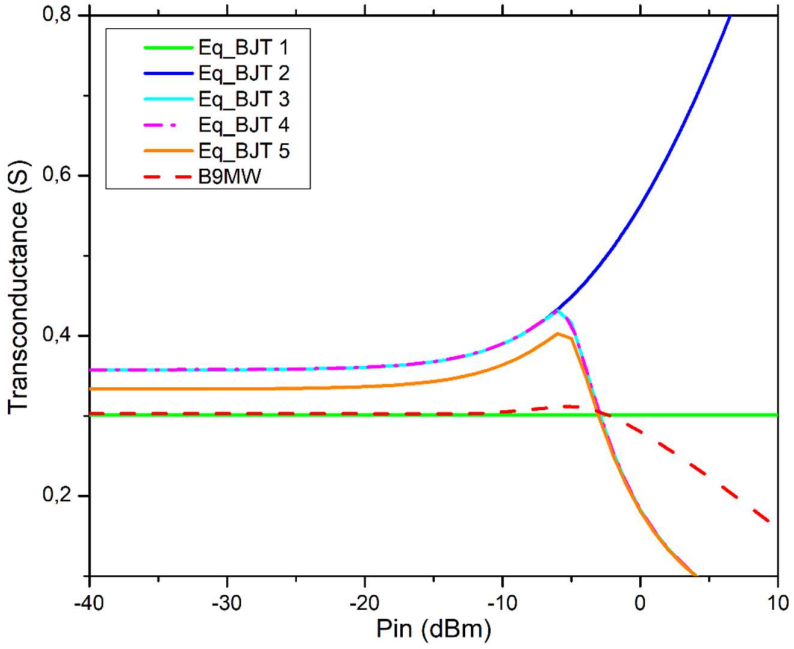

Figure 25: Custom nonlinear Equivalent BJT model response.

In Figure 25, the Eq BJT 2 was designed to capture the nonlinearity resulting from the exponential I-V characteristics of the diode. The base-emitter diode junction current's exponential relationship in figure 25 is modeled by the equation below.

$$I_C = I_S \left(e^{\frac{V_{be}}{V_T}} - 1\right)$$

But in the Eq BJT 2 model, the transconductance keeps increasing exponentially, whereas in B9MW, the transconductance starts to roll off and keeps dropping despite the increase of input power. The reason for the difference can be observed from the

transient collector voltage response of the Eq BJT 2 model and B9MW as shown in Figure 26.

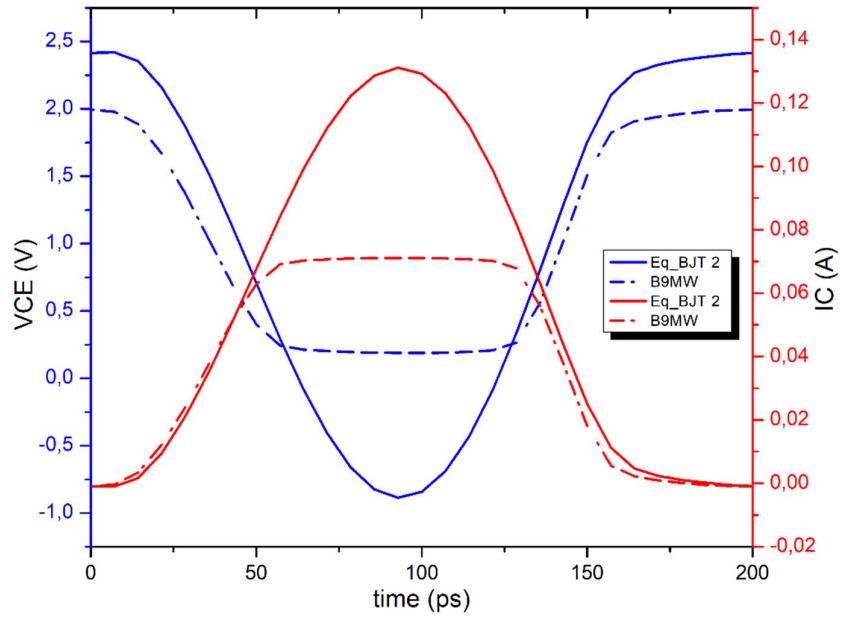

Figure 26: Transient response of the collector voltage and current.

From Figure 26, (at high power e.g. Pin = 0dBm) it can be observed that the collector voltage and current start to clip off at a certain value, whereas the Eq BJT 2 model has no such effect. This phenomenon appears because of the Base-Collector saturation at high input power. At low power, the BC junction is reversed-biased. But with the increasing power, the collector current increases, and upon reaching a certain level of collector current, the voltage drop across the CE junction (V_{ce}) drops. If V_{ce} falls beyond a certain level, the BC junction gets forward-biased. At this point, both the BE and BC junctions are forward-biased, and the transistor is operating in the saturation region. This saturation effect is captured in Figure 25 with the Eq BJT 3 model with the equation below.

$$I_C = I_S \left(e^{\frac{V_{be}}{V_T}} - e^{\frac{V_{bc}}{V_T}}\right)$$

The Eq BJT 4 model in Figure 25 captures the forward early effect in the equation below. The base width is modulated by the collector-base voltage, which causes the forward early effect, which affects the injections of the minority carriers in the BC junction.

$$I_C = I_S \left(e^{\frac{V_{be}}{V_T}} - e^{\frac{V_{bc}}{V_T}}\right)\left(1 + \frac{V_{bc}}{VAF}\right)$$

The forward early voltage (VAF) in this case, which was taken from the HICUM/L0 model, is around 403V. A relatively high VAF of 403V suggests that, while the transistor

is in the forward active zone, the BJT has very little fluctuation in current gain (β) with changes in the collector-emitter voltage (V_{ce}). This lessens the non-linear effects brought on by the forward early effect since the current gain is comparatively constant across a large range of $V_{ce\ as}$ can be seen in Figure 25.

The Reverse Early effect, which is the opposite of the Forward Early effect, is captured by Eq BJT 5 with the equation below.

$$I_C = I_S\,(e^{\frac{V_{be}}{V_T}} - e^{\frac{V_{bc}}{V_T}})(1 + \frac{V_{bc}}{VAF} + \frac{V_{be}}{VAR})$$

The reverse early effect appears when the base-emitter voltage is quite high, and the collector-base junction is heavily reverse-biased. As V_{ce} increases, this results in an effective increase in base width and an expansion of the depletion zone, which lowers collector current and in turn decreases transconductance. The reverse early voltage (VAR) in this case, which was extracted from the HICUM/L0, is around 1.1V. The relatively low VAR of 1.1V indicates a stronger reverse early impact since the BJT is more susceptible to changes in V_{ce} under reverse bias. In this instance, when V_{ce} grows, the base width increases noticeably, decreasing both the collector current and injection efficiency as we can see in Figure 25.

4.3 Bottom-Up Approach: Analysis of HICUM/L0 Parameters

4.3.1 Identifying Key Parameters

After extracting the HICUM/L0 model card for B9MW, the first task was to identify the key parameters out of the total 103 parameters with the help of the experts from the modeling team. The identified parameters were grouped into three different groups based on their significance in the transistor performance as given below:

- **Priority 1 (17):** IS, IBES, CJE0, T0, CJCI0, CJCX0, RBI0, RBX, RCX, RE, CBCPAR, CBEPAR, VEF, CJS0, VER, AVER, ZEDC
- **Priority 2 (23):** IQF, IQFH, VDE, ZE, AJE, THCS, AHC, TR, RCI0, VLIM, VCES, KAVL, EAVL, VDCX, ZCX, VDCI, ZCI, DT0H, TBVL, VPT, VPTCI, VDS, ZS
- **Priority 3 (9):** IQR, IBCS, TEF0, GTE, ITSS, ISCS FLSH, RTH, CTH

4.3.2 Impact of Key Parameters

First, each parameter of Priority 1 was analyzed and reduced to the only significant parameters that can still reflect the response for this application with an acceptable amount of deviation. Figure 27 shows the response of priority 1 parameters and the reduced list of priority 1.

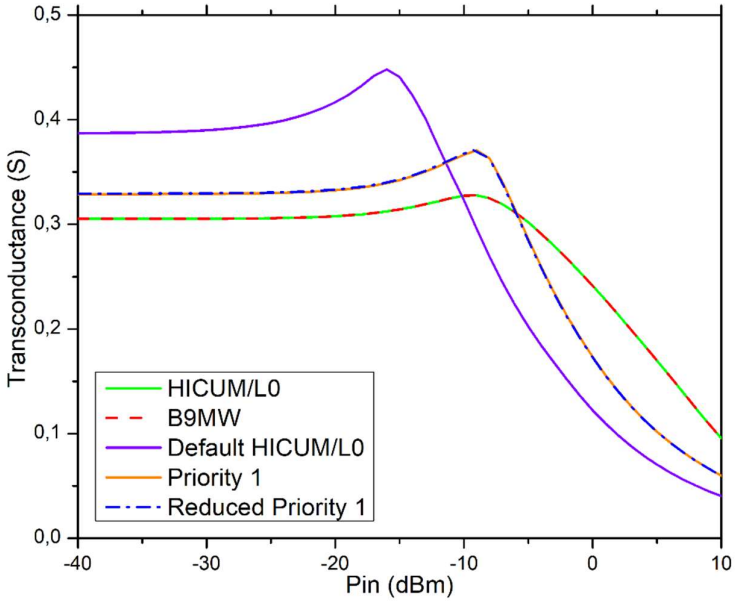

Figure 27: Reducing Parameters in Priority 1.

Reduced Priority 1: IS, IBES, VER, AVER, ZEDC, To, CJEo, CJCIo, CJCXo, RCX, RBX, RE, CBCPAR. These parameters are crucial because they have a direct impact on the transistor's high-frequency response, I-V characteristics, transconductance, and gain. Figure 28 displays the responses of the reduced priority list 1 + priority 2 (green) and reduced priority list 2 (blue).

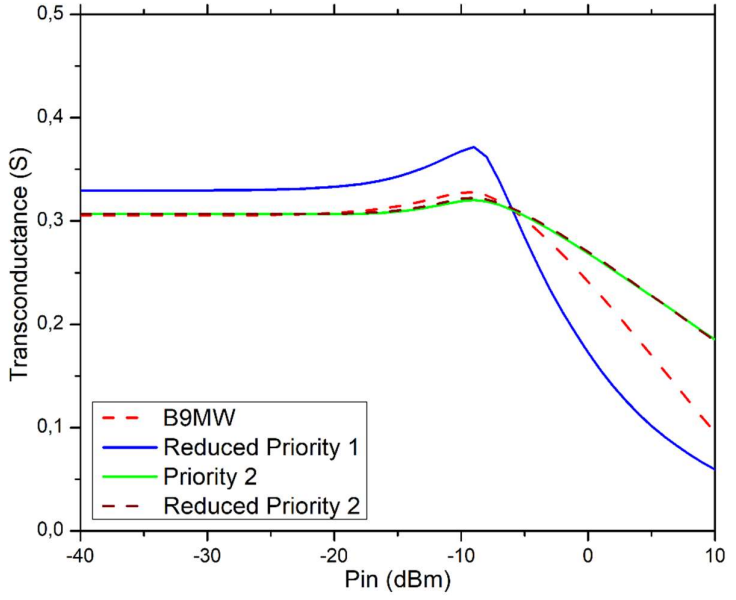

Figure 28: Reducing Parameters in Priority 2.

Reduced Priority 2: Reduced Priority 1 + IQF, IQFH, THCS, RCIo, TR. The characteristics in this list primarily impact the gain, high-current behavior, and frequency responsiveness of the transistor. Figure 29 shows the response of the reduced priority list 2 + priority 3 (blue) and the reduced list.

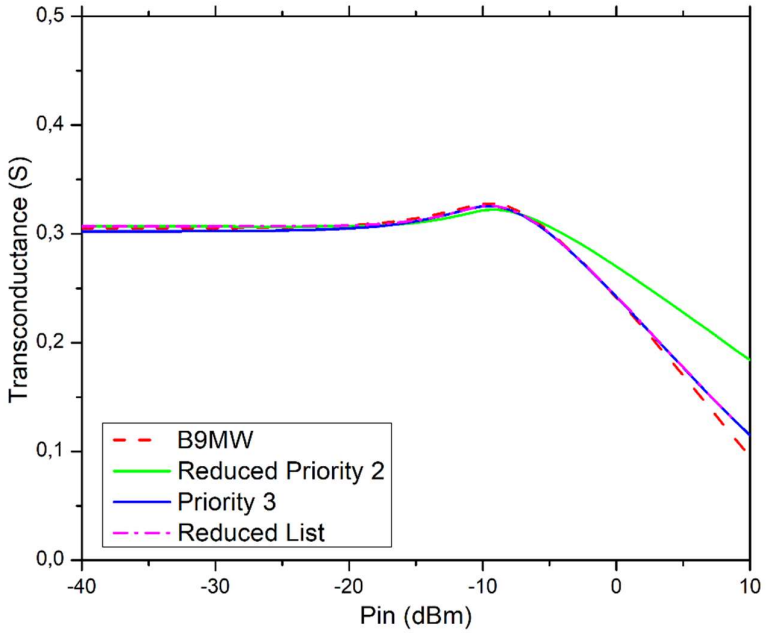

Figure 29: Reducing Parameters in Priority 3.

Reduced Priority 3: Reduced Priority 2 + IQR, MBE, IBCS. Although these characteristics are still significant, they have less of an effect on the overall performance in the primary operating mode of a Class A PA. They mainly affect the reverse mode behavior and base recombination processes. The final reduced HICUM/Lo parameter list is:

- **Reduced List (21):** IS, IBES, VER, AVER, ZEDC, To, CJEo, CJCIo, CJCXo, RCX, RBX, RE, CBCPAR, IQF, IQFH, THCS, RCIo, TR, IQR, MBE, IBCS.

These 21 parameters are the key parameters that are affecting the nonlinearity in the transconductance, and other performance matrices of the PA. Table 5 contains the description of each of these parameters, their default value, and the corresponding value of B9MW. The default values are set in the model such a way that it reflects a general transistor response with Gummel-Poon model irrespective of the technology. By changing the values of these parameters to the B9Mw value, the effects for them for the corresponding technology are turned on.

Parameter	Description	Default	B9MW
IS	Saturation Current	1.00E-16	7.42E-17
IBES	BE Saturation Current	1.00E-18	4.13E-20
VER	Reverse Early Voltage	1.00E+06	1.43
AVER	Bias Dependence of VER	0	4.23
T0	Low Current Transit Time	0	4.87E-13
CJE0	BE Depletion Capacitance	1.00E-20	1.41E-14
CJCI0	Internal BC Depletion Capacitance	1.00E-20	3.52E-15
CJCX0	External BC Depletion Capacitance	1.00E-20	8.28E-15
RCX	External Series Collector Resistance	0	4.08E+00
RBX	External Series Base Resistance	0	1.72E+01
RE	Series Emitter Resistance	0	1.21E+00
CBCPAR	BC Parasitic Capacitance	0	7.29E-15
IQF	Forward DC High-Injection Current	1.00E+06	4.23E-03
IQFH	High-Injection Correction Current	1.00E+06	1.41E-03
THCS	Saturation Time at High Current	0	9.78E-12
RCI0	Epi Collector Resistance	150	8.78E+00
TR	Reverse Transit Time	0	2.50E-10
IQR	Inverse DC High-Injection Current	1.00E+06	5.51E-05
MBE	BE Non-ideality Factor	1	1.01E+00
IBCS	BC Saturation Current	0	3.19E-19

Table 5: Reduced HICUM/L0 parameters for B9MW.

4.3.3 Reduced Parameter Analysis

After finding the reduced parameter list, five critical FoMs were chosen: P_{in}, P_{out}, P_{gain}, PAE, and THD. As the 1dB compression point is a direct indicator of the amplifier's linearity, all these FoMs are taken at 1dB compression point. Figure 30 shows how each parameter affects Pin|1dB. The arrow sign (↑ ↓) after the parameter names indicates whether the B9MW value of that parameter has increased or decreased compared to the default HICUM/L0 value. For example, IBES↓ indicates the base-emitter saturation current has decreased while it increases the Pin|1dB. A linear and efficient PA has higher P_{in}, P_{out}, P_{gain}, and PAE, while lower THD. Here, the analysis was done to identify the effect of increasing or decreasing each parameter on these FoMs.

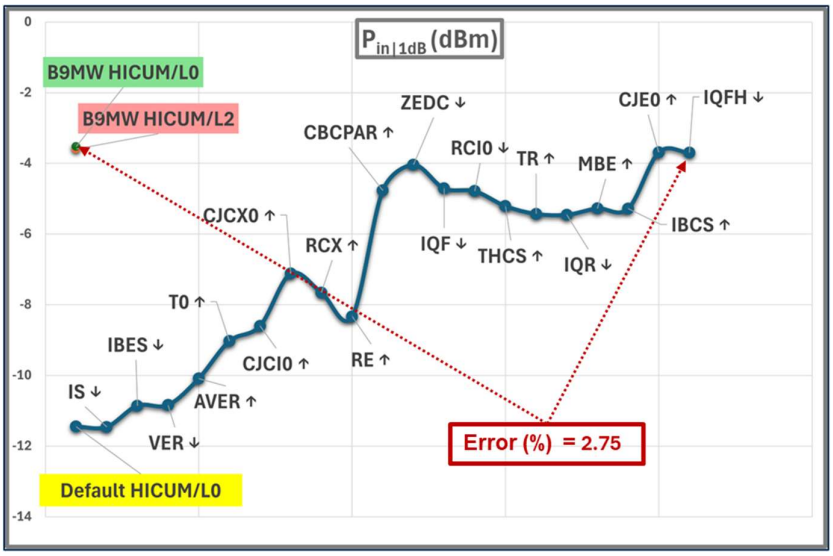

Figure 30: Model parameter effects on input power at 1dB compression point.

From Figure 30, it can be observed that Pin|1dB has:

- **Positive correlation:** IS, AVER, To, CJCIo, CJCXo, CBCPAR, IQF, RCIo, IQR, MBE, CJEo
- **Negative correlation:** IBES, VER, RCX, RE, ZEDC, THCS, TR, IBCS, IQFH

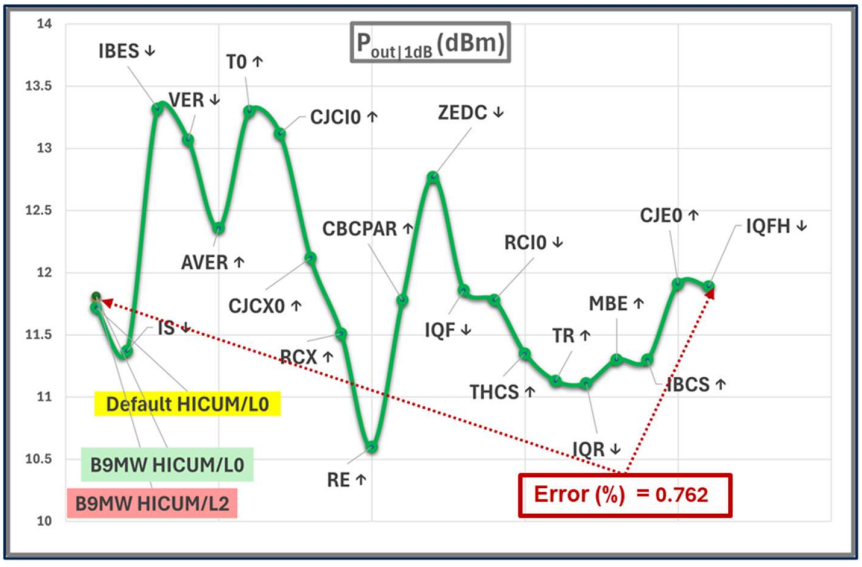

Figure 31: Model parameter effects on output power at 1dB compression point.

From Figure 31, it can be observed that Pout|1dB has a:

- **Positive correlation:** IS, VER, To, CBCPAR, IQF, RCIo, IQR, MBE, IBCS, CJEo, IQFH
- **Negative correlation:** IBES, AVER, CJCIo, CJCXo, RCX, RE, ZEDC, THCS, TR

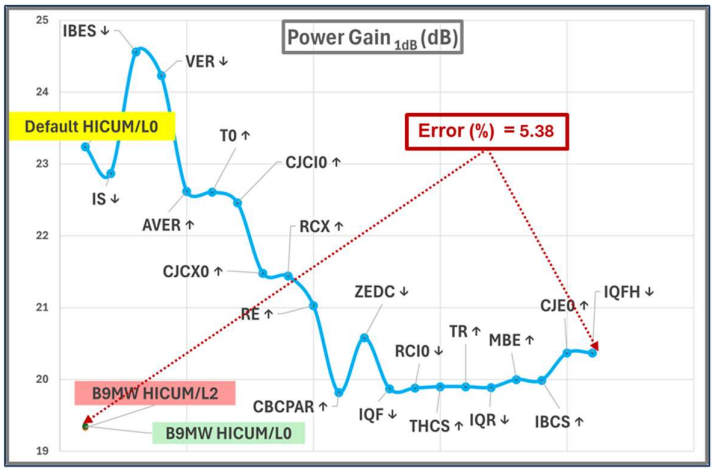

Figure 32: Model parameter effects on power gain at 1dB compression point.

From Figure 32, it can be observed that Pgain|1dB has:

- **Positive correlation**: IS, VER, IQF, THCS, TR, IQR, MBE, CJEo, IQFH
- **Negative correlation:** IBES, AVER, To, CJCIo, CJCXo, RCX, RE, CBCPAR, ZEDC, RCIo, IBCS

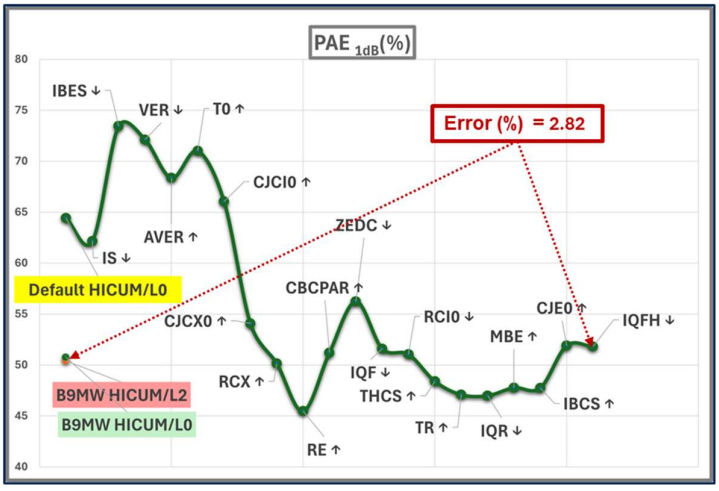

Figure 33: Model parameter effects on PAE at 1dB compression point.

From Figure 33, it can be observed that PAE|1dB has:

- **Positive correlation:** IS, VER, To, CBCPAR, IQF, IQR, MBE, CJEo, IQFH
- **Negative correlation:** IBES, AVER, CJCIo, CJCXo, RCX, RE, ZEDC, RCIo, THCS, TR, IBCS

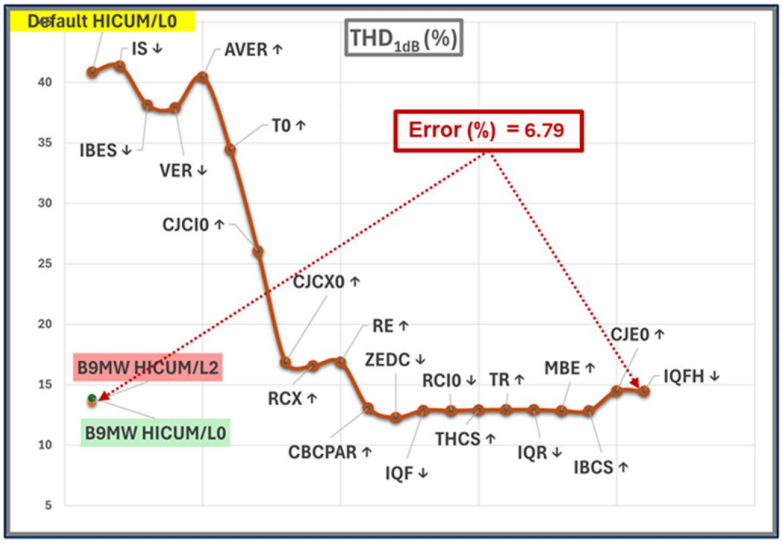

Figure 34: Model parameter effects on THD at 1dB compression point.

From Figure 34, it can be observed that THD|1dB has:

- **Positive correlation:** IBES, VER, RE, ZEDC, RCIo, THCS, TR, CJEo, IQFH
- **Negative correlation:** IS, AVER, To, CJCIo, CJCXo, RCX, CBCPAR, IQF, IQR, MBE, IBCS

From the above analysis, the relationship between the parameters and the performance matrices is obtained. From the positive and negative correlation, it can be determined which parameters are needed to increase or decrease to enhance the performance of PA. These parameters can be linked to the regions in the transistor to get more insight into the parameters.

The result is combined in Table 6 to indicate which parameters can increase (↑) or decrease (↓) the PA performance. To enhance the PA performance, P_{in}, P_{out}, $P_{gain,}$ and PAE need to be improved while THD needs to be lower with trade-offs among these parameters.

P_{in} ↑	**P_{out} ↑**	**P_{gain} ↑**	**PAE ↑**	**THD ↓**
IS ↑	IS ↑	IS ↑	IS ↑	IS ↑
IBES ↓	IBES ↓	IBES ↓	IBES ↓	IBES ↓
VER ↓	VER ↑	VER ↑	VER ↑	VER ↓
AVER ↑	AVER ↓	AVER ↓	AVER ↓	AVER ↑
To ↑	To ↑	To ↓	To ↑	To ↑
CJCIo ↑	CJCIo ↓	CJCIo ↓	CJCIo ↓	CJCIo ↑
CJCXo ↑	CJCXo ↓	CJCXo ↓	CJCXo ↓	CJCxo ↑
RCX ↓	RCX ↓	RCX ↓	RCX ↓	RCX ↑
RE ↓	RE ↓	RE ↓	RE ↓	RE ↓
CBCPAR ↑	CBCPAR ↑	CBCPAR ↓	CBCPAR ↑	CBCPAR ↑
THCS ↓	THCS ↓	THCS ↑	THCS ↓	THCS ↓
IQF ↑	IQF ↑	IQF ↑	IQF ↑	IQF ↑
RCIo ↑	RCIo ↑	RCIo ↓	RCIo ↓	RCIo ↓
TR ↓	TR ↓	TR ↑	TR ↓	TR ↓
IQR ↑	IQR ↑	IQR ↑	IQR ↑	IQR ↑
CJEo ↑	CJEo ↑	CJEo ↑	CJEo ↑	CJEo ↓
IQFH ↓	IQFH ↓	IQFH ↑	IQFH ↑	IQFH ↓
MBE ↑	MBE ↑	MBE ↑	MBE ↑	MBE ↑
IBCS ↓	IBCS ↑	IBCS ↓	IBCS ↓	IBCS ↑

Table 6: Relation of parameters with PA performance

4.4 Linking Parameters to the Custom Model

4.4.1 Parameter Mapping

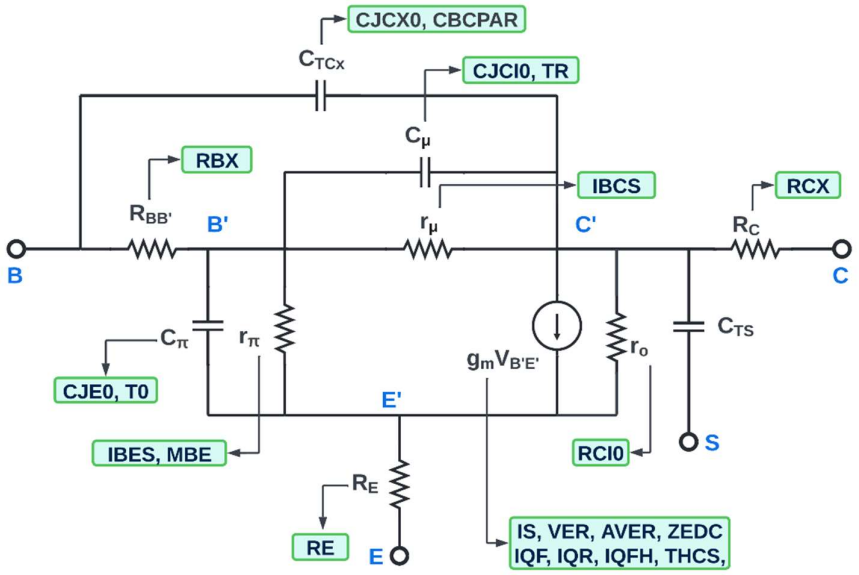

Figure 35: Mapping reduced parameter list to the custom model.

Figure 35 shows the mapping of the reduced parameter list on the custom model. Here even though these parameters are linked on the small signal model, in the large signal case, some of these parameters are involved in characterizing more than one circuit component from the figure. Here, the parameters are only assigned to the components that impact significantly.

4.4.2 Enhancing the Custom Model

To enhance the custom model, first, the parameters from the reduced list that the model can already reflect need to be identified. The parameter list Prime contains the parameters that are already implemented in the custom model as shown in Figure 36. The little discrepancy is because some of the parameters are bias-dependent on the HICUM/L0, whereas they are not in the Custom BJT model, e.g., saturation current IS. The parameters that are like the Eq BJT 5 model are listed in the parameter list Prime.

- **Prime (11):** IS, IBES, VER, AVER, ZEDC, CJE0, CJCI0, CJCX0, RCX, RE, CBCPAR

The remaining HICUM/L0 parameters and their associated effects are still missing in the custom model.

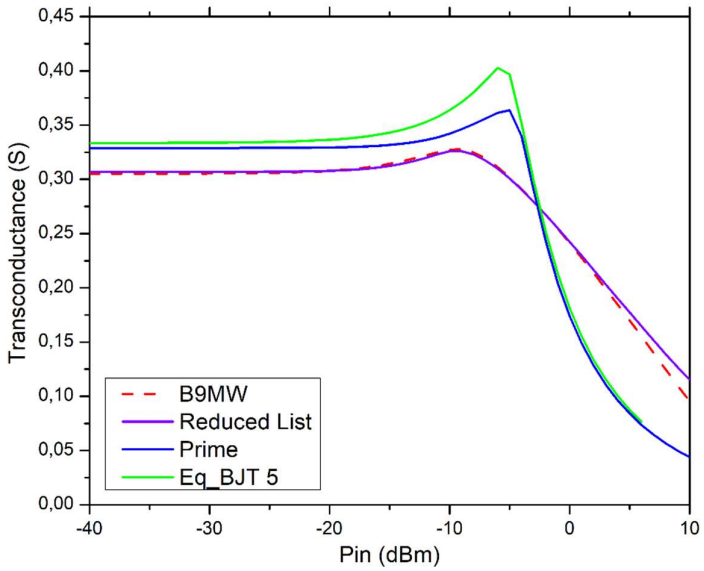

Figure 36: Finding Parameters from the Reduced list in the Custom model.

From the parameter list Prime compared with the reduced list of parameters, it can be concluded that the missing parameters reflect the high injection effect and transit time effect in the transistor. The high-injection effect alters the saturation current, which alters the response of the collector current IC as shown below:

$$I_S = \frac{I_{SS}}{q_b}$$

Where,

$$q_b = \frac{q_1}{2} + \sqrt{\left(\frac{q_1}{2}\right)^2 + q_2}$$

$$q_1 = 1 + \frac{V_{be}}{VAR} + \frac{V_{bc}}{VAF}$$

$$q_2 = \frac{\beta I_{SS}}{IKF}\left(e^{\frac{V_{be}}{V_T}} - 1\right) + \frac{I_{SS}}{IKR}\left(e^{\frac{V_{bc}}{V_T}} - 1\right)$$

Here, IKF and IKR indicate the forward and reverse high injection knee current, in other words, the value where the high injection effect starts to impact the transistor response. q_1 takes into account the effect of base width modulation and q2 takes into account the high injection currents. The combined effect of q_1 and q_2 is reflected in q_b, which then modulates the DC saturation current to reflect these effects. Figure 37 shows the transistor response after incorporating the high injection effect into the model.

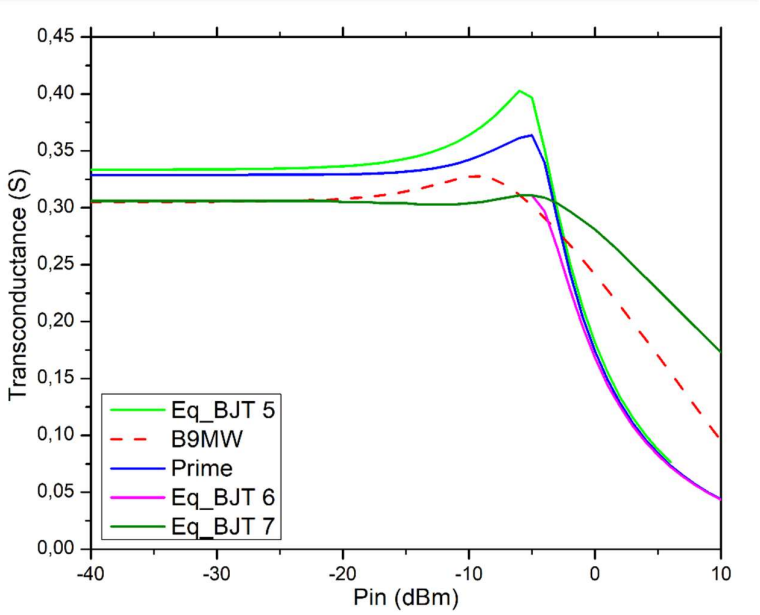

Figure 37: High injection effects and Transit time effects in the custom model.

The Eq BJT 6 model captures the high injection effect of the transistor. When the high injection effect occurs, the exponential relationship between IC and VBE shifts from 60 mV/dec to 120 mV/dec. This change reflects the excess charge carrier injection in the collector from the base which accounts for the increase in collector current as shown in Figure 37.

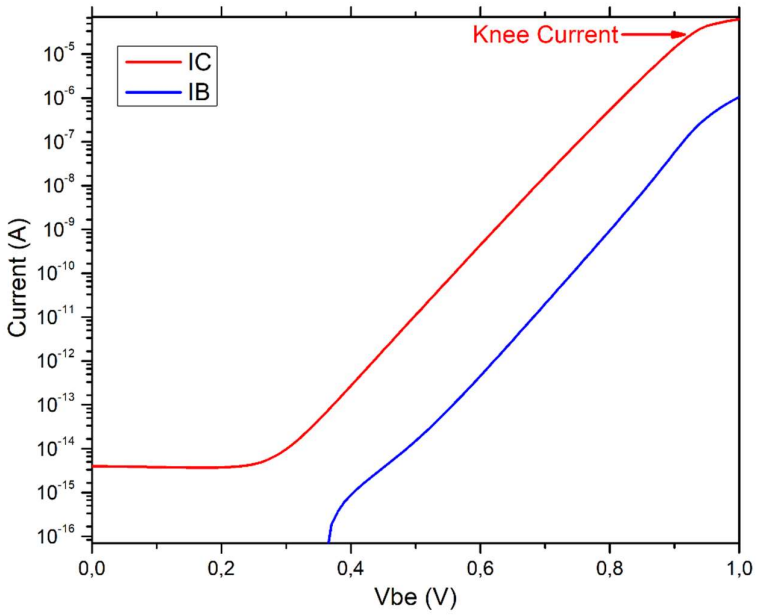

Figure 38: IC and IB in log scale as an exponential function of VBE.

The onset of this effect occurs at the knee current that is indicated in the figure. Due to this effect, the slope between I_C and V_{BE} is lowered which causes a reduction in the transconductance. The high injection effect also increases the recombination rate and lowers the current gain.

On the other hand, the transit time (TR) effect indicates the delay induced by the limiting speed at which charge carriers travel across the transistor's base region. Because the carriers from the emitter need time to cross the base area, changes in the base-emitter voltage do not immediately translate into changes in the collector current. The Eq BJT 7 model in Figure 37 can capture this effect.

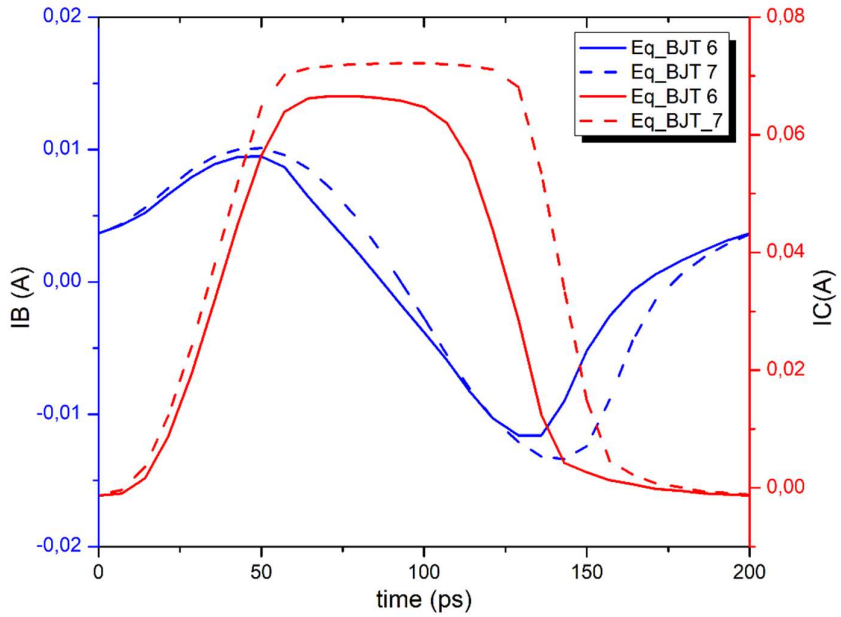

Figure 39: Phase shift in IC and IB due to the transit time effect.

As the frequency increases, the transit time starts to become significant. Because of the high injection effect and Kirk effect the effective base width increases with a larger number of carriers to transport to the collector. This reduces the carrier velocity and causes a phase shift in the current as can be seen in Figure 39 which was taken at Pin = 0 dBm. As the BC junction enters saturation, the base region can become quasi-neutral, causing a reduction in the effective transit time. This can temporarily give rise to the collector current causing the transconductance to decrease slowly after the roll-off in Eq BJT 7 compared to Eq BJT 6 as shown in Figure 37.

The custom model can now replicate the transistor behavior while still having some noticeable variations. To improve the model further by incorporating the rest of the parameters, careful nonlinear modeling of the other components of the model is necessary.

4.5 Monte Carlo Simulation Analysis

4.5.1 Overview of Monte Carlo Simulation

The simple circuit shown in Figure 40 was used to run the Monte Carlo analysis. Here the circuit is biased to turn on the transistor and run the simulation. With the Standard Monte Carlo method and Low-Discrepancy Sequence sampling method, 10000 points are simulated for the Monte Carlo analysis. Some of the parameters like AVER, CBCPAR, ZEDC, THCS, MBE, and IBCS were excluded as they are process-independent parameters and are defined in the model file as constant values.

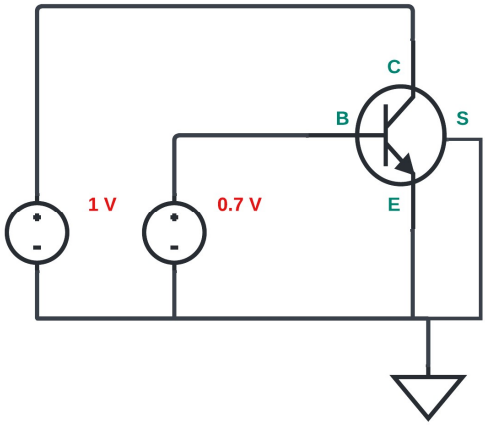

Figure 40: Circuit used for the Monte Carlo Analysis

4.5.2 Results of Monte Carlo Simulation

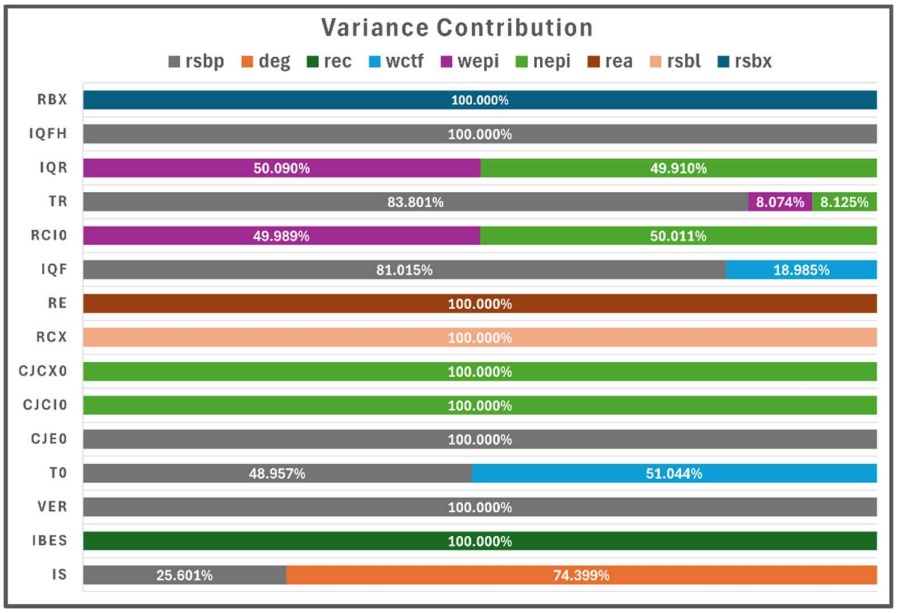

Figure 41: Contribution of design parameters to model parameters.

From Figure 41, the variance contribution of different parameters can be seen. This plot indicates the relative percentage of change in the model parameter from altering different design parameters. For example, the model parameter IS, which indicates the saturation current of the transistor can be changed by altering two parameters: DEG (74.4 %) and RSBP (25.6 %). From this figure, it can be determined which design parameters will contribute most to which model parameters.

The key takeaway from Figure 41 is that several important outputs, including VER, CJE0, IQF, and TR, are impacted by RSBP. Consequently, the main goal is to improve linearity in these outputs by optimizing RSBP. Since DEG has a significant impact on IS, bandgap fluctuation must be carefully managed. IBES is entirely within REC's control, which makes it essential for guaranteeing a steady saturation current behavior. Both NEPI and WEPI have a major effect on transit time and outputs linked to capacitance, which is essential for high-frequency performance.

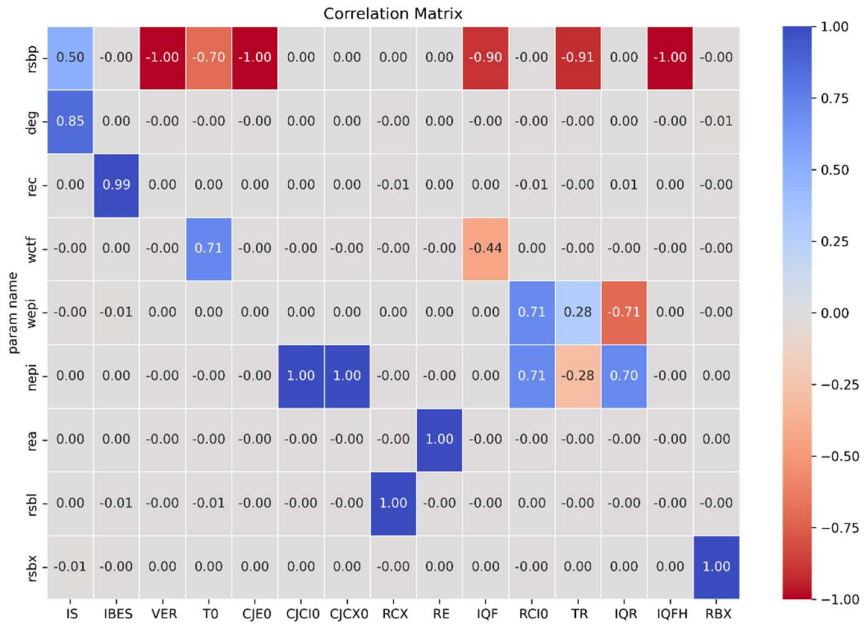

Figure 42: Correlation Matrix of Design Parameters and Model Parameters.

Figure 42 shows the correlation coefficient (r) between the technology/design parameters with the model parameters, where r=1 reflects the perfect positive coefficient, r=-1 reflects the perfect negative coefficient, r=0 reflects no coefficient, and the intermediate values reflect strong/weak relations(positive/negative).

The key takeaways from Figure 42 are: The three metrics that are essential for linearity—VER, T0, and CJE0—will probably improve significantly as a result of concentrating on reducing RSBP. Optimizing the DEG and REC parameters can have a substantial impact on the linearity because of their high positive relationships with IS and IBES. Precise control of epi layer doping can enhance performance at high frequencies since NEPI has a significant effect on capacitance characteristics (CJCI0 and CJCX0). Since WEPI and

WCTF have a significant link with both RCI0 and T0, making changes here may result in improvements to the collector resistance and transit time, which will enhance linearity.

4.5.3 Cross-Correlation of Model Parameters

The design approach should concentrate on these crucial inputs while seeking to improve transistor performance, making sure that adjustments to one parameter do not adversely affect other associated outputs. For this reason, the parameters' cross-correlation was generated and is shown in Table 7. For instance, T0 and TR have somewhat negative correlations with IS and substantial positive correlations with VER. According to this, VER will directly benefit from shorter transit times, which are essential for high-speed operation, whereas IS would suffer from them.

Parameter 1	Parameter 2	Correlation Coefficient
IS	VER	-0.501
T0	VER	0.699
T0	IS	-0.354
CJE0	VER	0.999
CJE0	IS	-0.504
IQF	VER	0.899
IQF	IS	-0.45
TR	VER	0.914
TR	IS	-0.458
IQFH	VER	0.999
IQFH	IS	-0.50

Table 7: Cross-correlation between model parameters.

4.6 Correlation between Model parameters and FoMs

After getting the standard deviation for the model parameters from the previous analysis, those values were used as Gaussian input distribution for the model parameters. As the values obtained are from the statistical process variation, the deviation is not significant, but it is enough to generate the correlation coefficient between the model parameters and the FoMs. Figure 43 shows the correlation between the model parameters and FoMs of PA. From the figure, it can be observed that IS has a strong positive correlation with the PA's Pin|1dB, Pout|1dB, PGain|1dB, THD|1dB, and the gm, while a negative correlation maximum PAE. It can also be observed that RCX and RE have negative correlation with most of the FoMs. So, the FoMS can be improved by reducing these resistances. Increasing the forward high injection current IQF can increase the linearity while losing efficiency.

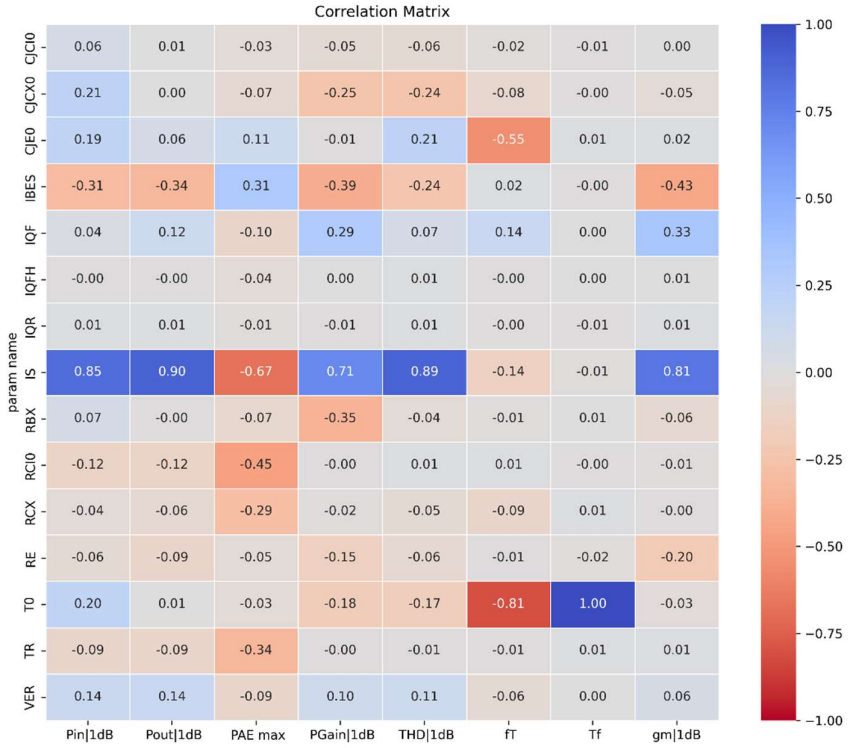

Figure 43: Correlation Matrix of Model Parameters and FoMs of PA.

4.7 Summary of Findings

To summarize the results, the nonlinearity occurring in the HBT for RF Power Amplifiers has been investigated in two different ways. The top-down approach, where a Custom Model was built to replicate the key effects while making it easier for designers to understand the mechanisms of nonlinearity. From the custom model, the key effects playing a role in different parts of the nonlinearity in transconductance were identified separately. The main effects impacting here are the exponential IV characteristics between I_C and $V_{BE,}$ specially at high power, the BC saturation effect, the early effect specially the reverse early effect, the high-injection effect, and the transit time effect. Using this model the impact of each of this effect can be analyzed separately making it suitable to comprehend the effects at the circuit level.

On the other hand, in the bottom-up approach, the HICUM/L0 model gives a more detailed understanding of the parameters in the transistors. It also gives an idea of the parameters that are bias and temperature-dependent and how they impact the circuit behavior. By finding out the reduced parameter list (IS, IBES, VER, AVER, ZEDC, T0, CJE0, CJCI0, CJCX0, RCX, RBX, RE, CBCPAR, IQF, IQFH, THCS, RCI0, TR, IQR, MBE, IBCS), which contains only 21 parameters from over 100 parameters in the HICUM/L0 model, it has been made easy to study these parameters further in-depth more easily. Most of the parameters in this list can be physically interpreted in the transistor, which is not usually easy to do with the HICUM/L2 model that is used in STM for commercial purposes. Most of these parameters can be directly related to the

transistor's physical architecture. Which makes it easier for the model team to focus on how they can improve these parts to deal with the nonlinearity.

The saturation current IS and BE saturation current IBES can be increased by increasing the doping in the emitter region which will also lower RE, while IS can also be increased by decreasing the base width and IBES can be increased by increasing the emitter area. The early voltages can be modified by adjusting the doping gradient in the base-collector region. Reducing the base width or increasing the base doping can result in reduced transit time. Increased base doping will also lower RBX. The increased doping concentration in the collector region can reduce RCX. Increasing the doping concentration in the emitter and collector region will also increase the high injection current parameters IQF and IQR. Parasitic capacitance CBCPAR can be tuned by optimizing the layout or with better isolation techniques. So, from this list, further fine-tuning of the transistor architecture can be suggested.

Finally, the Monte Carlo simulation gives a comprehensive idea of the contribution and correlation between different parameters, giving an idea of tuning which parameter can impact which performance matrix and how much the impact will be. It also helps to give the idea of cross-correlation between the parameters. As the data points taken were substantially large, the accuracy obtained from the simulation can be deemed reliable.

Chapter 5: Conclusion

This report provides a detailed idea in exploring the nonlinearity occurring in the HBT that impacts its performance in the application of it as a PA for RF communication. Through a comprehensive analysis and different approaches, the relationship between the nonlinearity appearing in the PA and the components responsible for those nonlinearities was identified. This study makes a bridge between the transistor design parameters, the equivalent circuit's model parameters, and the figure of merits of the PA. This analysis helps to comprehend the idea about fine-tuning key performance metrics, like, transconductance, output power, efficiency, and harmonic distortion. In summary, this study suggests that, by focusing on the key parameters and the regions in the transistors that play a key role in modulating the nonlinearity of the transistor, the linearity of the transistor can be improved more efficiently. This will help reach the performance requirements by WiFi-7 PA.

5.1 Future Work and Implications

There are several tasks involved in this work in the future. The first task will be to try to implement the remaining parameters from the reduced list of the HICUM/L0 into the custom model, as the custom model is still missing some key parameters and modeling to match the desired accuracy of the response.

After tuning that, the transistor model of B9MW will be implemented in the TCAD. The TCAD model will be fine-tuned based on the findings of this report to make it capable of more linear operation.

While improving the technology, another task will be to extend this work to other PA topologies. The work will also involve exploring topologies that can cancel the nonlinearity mechanisms from circuit level.

The final goal will be to design a PA that is linear and can be used for Wi-Fi7 with modified technology. By resolving these issues, future research can continue to push the limits of transistor performance in RF power amplifiers, opening the possibilities for more efficient and reliable high-frequency devices.

Bibliography

[1] "The evolution of wi-fi networks," [Online]. Available: https://www.wevolver.com/article/the-evolution-of-wi-fi-networks-from-ieee-80211-to-wi-fi-6e. [Accessed 30 07 2024].

[2] "Error vector magnitude (evm) measurement," [Online]. Available: https://www.analog.com/en/resources/technical-articles/how-evm-measurement-improves-system-level-performance.html. [Accessed 13 08 2024].

[3] D. J. Paul, "Si/sige heterostructures: From material and physics to devices and," *Semiconductor science and technology,* vol. 19, no. 10, R75, 2004.

[4] T. S. P. C. e. a. B. Barbalat, "The effect of carbon on neutral base recombination in high-speed SiGeC heterojunction bipolar transistors," *Semiconductor science and technology,* vol. 22, no. 1, S99, 2006.

[5] "BJT Configurations," [Online]. Available: https://www.geeksforgeeks.org/bjt-configurations/. [Accessed 13 08 2024].

[6] C. M. e. al, "VBIC95, the vertical bipolar intercompany model," *IEEE J. Solid-State Circuits,* vol. 31, pp. 1476-1483, 1996.

[7] M. Schroter, "Hicum/L0 a simple compact heterojunction bipolar transistor," 2001.

[8] J. P. a. W. Kloosterman, "The MEXTRAM Bipolar Transistor Model, Level 504," Nat. Lab. Unclassified Report NL-UR2000/811, Sept. 2001.

[9] Q. L. J. D. C. C. S. W. a. D. L. H. G. Niu, "Physics, Characterization and Modeling of RF Linearity in SiGe HBT and FinFET Technologies," *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS),* pp. 70-77, 2022.

[10] S. a. S. R. a. N. J.-M. a. J. J.-C. a. F. D. a. A. P. a. Q. R. Heckmann, "Characterization and modeling of bias dependent breakdown and self-heating in GaInP/GaAs power HBT to improve high power amplifier design," *IEEE Transactions on Microwave theory and Techniques,* vol. 50, no. 12, pp. 2811-2819, 2002.

[11] S. C. C. e. al, RF power amplifiers for wireless communications, Artech house Norwood, 2006.

[12] T. R. P. C. e. a. M. Schröter, "Sige hbt technology: Future trends and tcad-based roadmap," *Proceedings of the IEEE,* vol. 105, no. 06, p. 1068–1086, 2016.

[13] G. Gildenblat, "Compact modeling," *Netherlands: Springer,* 2010.

Appendix 1

Implementation of the Collector current using verilogA:

```
`include "discipline.h"
`include "constants.h"

//specify
   //specparam CDS_LIBNAME  = "Arnab";
   //specparam CDS_CELLNAME = "Equivalent_BJT";
   //specparam CDS_VIEWNAME = "schematic";
//endspecify

//Node definitions
//Bi = "internal base node"
//Ei = "internal emitter node"
//Ci = "internal collector node"

//Instance Parameter
//Is      = Saturation Current
//Isc     = BC leakage Current
//VAR   = Reverse Early Voltage
//VAF   = Forward Early Voltage
//gm     = Transconductance of small signal model
//IKF    = Forward Knee Current
//IKR    = Reverse Knee Current

module nonlinear_vccs(Ci, Ei, Bi, Eii);
inout Bi, Eii, Ei, Ci;
electrical Ei, Ci, Bi, Eii;
```

```
parameter real Is = 10f;
parameter real VAR = 1.1;
parameter real VAF = 403;
parameter real gm = 1;
parameter real IKF = 40.23m;
parameter real IQR = 55.12u;

real IsVbe, IsVbc, IscVbc, Q1, Q2, Qb, InvQ1;
real Vt;

parameter real select = 1;

analog begin
  @ (initial_step or initial_step("dc") ) begin
    Vt = $vt;
  end

  case (select)
    // Linear model
    1: I (Ci, Ei) <+ gm * V (Bi, Ei);
    // Base-Emitter diode junction current
    2: I (Ci, Ei) <+ Is * (exp (V (Bi, Ei) / Vt) - 1);
    // Base-Collector Saturation Effect
    3: I (Ci, Ei) <+ Is * (exp (V (Bi, Ei) / Vt) - exp (V (Bi, Ci) / Vt));
    // Forward Early Voltage
    4: I (Ci, Ei) <+ Is * (exp (V (Bi, Ei) / Vt) - exp (V (Bi, Ci) / Vt)) * (1 - (V (Ci, Ei) /
VAF));
     // Both Early Voltages
    5: I (Ci, Ei) <+ Is * (exp (V (Bi, Ei) / Vt) - exp (V(Bi, Ci) / Vt)) * (1 - (V(Bi, Ei) / VAR)
- (V(Ci, Ei) / VAF));
```

```
// High Injection Effect
      6: begin
            IsVbe = Is * exp (V (Bi, Ei)/Vt);
            IsVbc = Is * exp (V (Bi, Ci)/Vt);
            IscVbc = Isc * (exp (V (Bi, Ci)/Vt) - 1);

            //Early Effects
            InvQ1 = 1;
            if (VAF! = 1M) InvQ1 = InvQ1 - V(Bi, Ci)/VAF;
            if (VAR! = 1M) InvQ1 = InvQ1 - V(Bi, Ei)/VAR;
            Q1 = 1/InvQ1;

            //High Injection Effect
            Q2 = 0;
            if (IKF != 1M) Q2 = Q2 + (IsVbe - Is)/IKF;
            if (IKR != 1M) Q2 = Q2 + (IsVbc - Is)/IKR;
            Qb = (Q1/2)*(1 + sqrt(1 + 4*Q2));
            I(Ci, Ei) <+ (IsVbe - IsVbc)/Qb - IsVbc/br - IscVbc;
         end
      default: I (Ci, Ei) <+ 0;
   endcase
end
endmodule
```

Appendix 2

Table 8: Parameters of HICUM/L0 with their associated parts of the EC model

Step	Description	Parameters
1	Collector Current	IS, MCF, MCR, VEF, VER, AVER, RVER, IQF, FIQF, IQR, IQFH, TFH, AHQ, FLTEFT, FLITM
2	Base Current	IBES, MBE, IRES, MRE, IBCS, MBC
3	Depletion Capacitance in BE junction	CJE0, VDE, ZE, AJE
4	Transit Time	T0, DT0H, TBVL, TEF0, GTE, THCS, AHC, TR
5	Critical Current	RCI0, VLIM, VPT, VPT, VCES, VDCK, DELCK, AICK
6	Internal Depletion Capacitance in BC junction	CJCI0, VDCI, ZCI, VPTCI
7	External Depletion Capacitance in BC junction	CJCX0, VDCX, ZCX, VPTCX, FBC
8	Base Resistance	RBI0, VR0E, VR0C, FGE0
9	Series Resistances	RBX, RCX, RE
10	Substrate Diode's Transfer Current and Capacitance	ITSS, MSF, ISCS, MSC, CJS0, VDS, ZS, VPTS
11	Parasitic Capacitance	CBCPAR, CBEPAR
12	Avalanche Current in BC junction	FAVL, QAVL
13	Flicker Noise	KF, AF
14	Temperature Dependence	VGB, VGE, VGC, VGS, DVGBE, F1VG, ALT0, KT0, ZETAVGBE, ZETAVER, ZETAACT, ZETABET, ZETAIQF, ZETACI, ZETAIQFH, ALVS, ALCES, ALDCK, ZETARBI, ZETARBX, ZETARCX, ZETARE, ALRTH, ZETARTH, ALFAV, ALQAV
15	Vertical NQS Effect	FLNQS, ALIT, ALQF
16	Self-Heating	FLSH, RTH, CTH