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TIME INTERLEAVED SAR ADC

Master Thesis Report

Presented by

Muhammad Zeeshan

In collaboration with

NXP Semiconductors, France

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Academic Supervisor(s): Prof. Paul Leroux, KU Leuven
Prof. Frédéric Saigné, University of Montpellier
Host Supervisor: Eng. Stéphane Le Tual, NXP Semiconductors
Eng. Yann Carminati, NXP Semiconductors

Jury Committee: Prof. Paul Leroux, KU Leuven
Prof. Sylvain Girard, University Jean Monnet
Prof. Frédéric Saigné, University of Montpellier
Dr. Arto Javanainen, University of Jyväskylä

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Abstract

Several ADC architectures are found to exist such as Successive Approximation Register, pipeline, sigma-delta, flash etc. The choice of these architectures depends on the required sampling frequency and resolution of the application. ADCs are known to be an essential interface between the analog world and digital computer data. Due to this key function, ADC circuits have been thoroughly studied for over 4 decades, addressing numerous associated challenges. However, a new type of ADCs has recently emerged, capturing significant attention. These are high-speed time-interleaved ADCs (TI ADCs), typically ranging from 1 GS/s to over 50 GS/s, generally fabricated using CMOS process with low to medium resolution ranging from 6 to 12 bits. Even though, these ADCs can be utilized in high-speed electronic measurement devices and radar systems, their latest emphasis is driven by the next generation 100 Gbps/500 Gbps fiber optic transceivers. These transceivers use high speed ADCs and DSPs (Digital-Signal-Processors) to achieve ultra-fast data communication across long-haul networks (connecting cities, oceans and continents), metro networks (connecting enterprises within metropolitan regions) and data centers (interconnecting infrastructure within data centers). Owing to its outstanding power efficiency, the TI SAR ADC has been known as a preferred solution at such high sampling rates. However, this architecture encounters challenges associated with channel mismatches. The three major categories of mismatches include an offset mismatch, gain and a timing mismatch. The initial part of this thesis focuses on developing a MATLAB model to analyze the inherent mismatches found in time interleaved ADCs, which can adversely affect their overall performance. The MATLAB model plays a vital role for simulating these mismatches, offering valuable understanding about their effect on the overall functionality of time-interleaved ADCs. As technology evolves and the system requirements become more demanding, the high-speed ADCs are constantly pushed to their performance limits. A major challenge in ADC design encountered in wearable computing machines is that they need ultra-low power consumption combined with increasing the sampling rate demands of modern communication systems. After operational amplifiers, comparators are recognized to be the second most commonly used electronic component and play a significant part in ADCs by sampling and transforming input signals into digital equivalents. The speed of ADCs depends on a comparator's decision-making response time. Ultra-deep submicron (UDSM) CMOS technology introduces additional complications since devices are required to be operational at lower supply voltages. In contrast, threshold voltages have not scaled down proportionally. As a result, designing high-speed, low power and low noise comparators becomes exceptionally problematic, specifically under low voltage conditions. Additionally, a limited common-mode input range occurs from the low-voltage operation, which is vital for maintaining the effective performance of high-speed ADC architectures. As compared to typical comparators, dynamic comparators are remarkably more power-efficient. There are diverse architectures for dynamic comparators. The primary focus of this thesis will be the high-speed, low-power Strong-Arm Latch comparator for Time-Interleaved SAR ADCs. Initially, the Strong-Arm Latch Comparator was simulated (RC Extracted) using 28-nm bulk CMOS and was then ported to 22-nm FD-SOI technology. A layout was subsequently carried out in this 22-nm FD-SOI technology. An inclusive comparison (RC Extracted) was then

conducted between these two versions and numerous existing comparators. A Figure of Merit (FOM) was computed to facilitate this comparison, and the Strong-Arm Latch Comparator was evaluated based on its speed, noise and energy per cycle.

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Abbreviations and Symbols

ADC	Analog-to-Digital Converters
SAR	Successive Approximation Register
DSP	Digital-Signal-Processing
UDSM	Ultra-Deep Submicron
FOM	Figure of Merit
SNDR	Signal to Noise and distortion ratio
SFDR	Spurious free dynamic range
MOSFET	Metal–oxide–semiconductor field-effect transistor
FD-SOI	Fully depleted Silicon on Insulator
I_D	Drain current
g_m	Transconductance
ro	Output resistance
PMOS	P-type Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
g_{ds}	Output conductance
GSE	Generalized Sampling Expansion
V_{cm}	Common mode Voltage
Vin, diff	Differential Input Voltage
FOM	Figure of Merits

Chapter 1: Overview

1.1 Motivation

Currently, analog-to-digital converters (ADCs) play a vital role in governing the performance of communication systems. For achieving the advanced communication standards, rapid, high-resolution, and power efficient ADCs are required. Consequently, the measurement industry has observed a growing demand for sampling systems that can offer high-speed and resolution [1]. Current ADC technologies mainly operate on their limits and cannot be notably pushed further, because of a substantial increase in the design difficulties which occur due to advancements of IC technologies to deep sub-micron. Nevertheless, the higher component density within digital circuits enables the use of additional chip area with only minimal extra costs [2]. A viable approach to address such performance limits is the use of parallelism. In this process, data from the analog input signal is divided into various parallel channels, followed by their independent conversion and ultimately recombination into a single digital output signal. In theory, Papoulis' Generalized Sampling Expansion (GSE) [3] outlines several techniques about splitting the data of the input signal. But practically, among the limited parallel multi-channel sampling structures that have been extensively investigated, time-interleaved structure emerges as one of the most promising ones. In a Time-Interleaved ADC system having M parallel channels, each channel takes a single sample alternately, such that there is no need for its sampling frequency to comply with the Nyquist Criterion. But the combination of all the individual samples into one sequence in the digital domain results in a sampling frequency satisfying the Nyquist criterion. Thus, an ideal time-interleaved ADC (TI-ADC) with M channels for sampling is equivalent to an ideal ADC having an M times higher sampling rate. The channels in the TI-ADC can incorporate various converter technologies for obtaining low-power and fast ADCs or fast and high-resolution ADCs [4].

There are numerous fields where TI ADC architectures find extensive applications for example Medical Imaging, Wireless communication systems, Test and Measurement equipment (Oscilloscopes), Digital cameras and Imaging systems, Automotive Radars, optical transceivers, Smartphones and tablets [5]. Figure 1 indicates the ADCs Walden figure of merit presented at the ISSCC and VLSI Symposium [5]. A typical Walden figure of merit is given as [6]

$$FOM_W = \frac{P}{f_s . 2^{ENOB}} \tag{1.1}$$

Here f_s corresponds to the sampling frequency, P is the power while ENOB indicates the effective number of bits, which can be formulated as:

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{1.2}$$

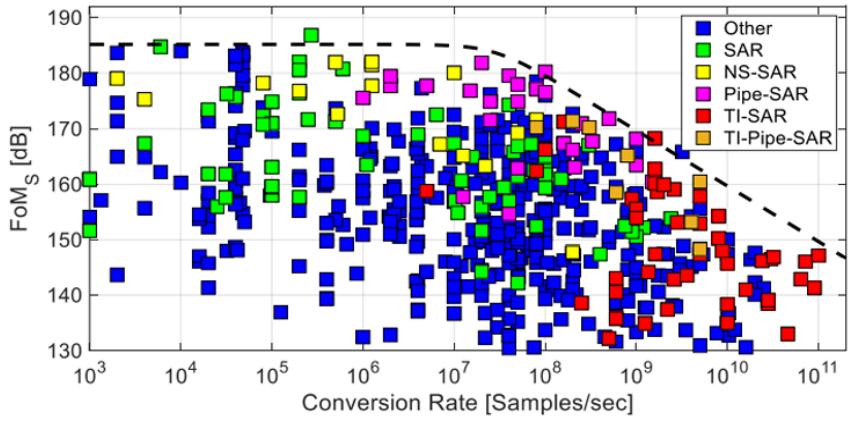


Figure 1 : Figure of merit data of all the ADCs reported at ISSCC and VLSI Symposium over the period 1997- 2023 [5]

It can be seen from the plot that depending on the required speed and performance characteristics, different architectures of ADC have been chosen for various applications. ADCs operating at multi-giga sample /second having moderate resolution are extensively used in high-performance radar/lidar sensing system as well as electronic/optical link.

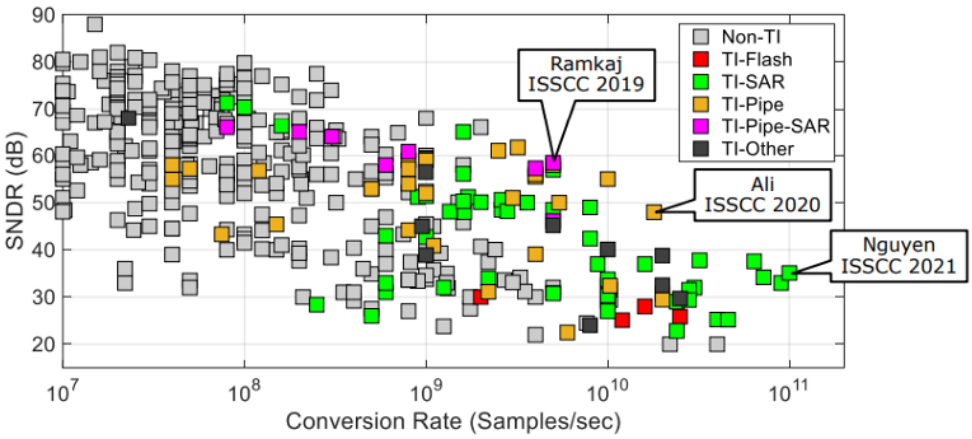


Figure 2 : SNDR of all the ADCs reported at ISSCC and VLSI Symposium over the period 1997 to 2021 [5]

1.2 Objectives of the study

This research targets three main objectives. Firstly, to develop a MATLAB model that can simulate channel mismatches (offset, skew, gain) and analyze how they impact the overall functionality of the Time-Interleaved ADCs. Secondly, carrying out the comparison of 28-nm CMOS BULK and 22-nm CMOS FD-SOI for a single transistor. The third objective is to simulate (RC Extracted) a strong-arm latch comparator across these two technologies, development of the layout design for the comparator in 22-nm CMOS FD-SOI technology and its evaluation against existing high-speed, low-power comparators.

1.3 Thesis Structure

The thesis is organized as below.

In the second chapter, complications associated with time-interleaved ADCs are described, a commonly adopted technique for increasing ADC systems' sampling rate. The chapter includes development of a MATLAB model for systematic analysis of impairments/mismatches present in time-interleaved ADC systems and their effect on TI ADCs. Chapter three is based on a comprehensive analysis of two well-developed semiconductor technologies: first one is 28-nm CMOS BULK, and the other is 22-nm FD-SOI CMOS technology. This comparison examines the performance of a single transistor, with special emphasis on critical parameters such as transconductance (g_m), output conductance (g_{ds}), gain, bandwidth, and gain-bandwidth product. By means of changing parameters as transistor width, length and current density, this study offers an in-depth evaluation of performance of each technology under different conditions. The fourth chapter focuses on simulating a low-power, high-speed comparator, an essential constituent of Time-Interleaved SAR ADCs. The comparator is simulated in 28-nm CMOS technology and then in chapter fifth it is ported to 22-nm FD-SOI technology. This chapter extensively analyses the comparator's performance, concentrating on offset, noise, speed, and power consumption. Chapter five also focuses on the comparison of the 28-nm BULK and 22-nm FD-SOI CMOS technology for strong arm latch comparator. Chapter six focuses on the overall conclusion and future work.

Chapter 2: Time-Interleaved ADCs

In this chapter, the fundamental concept of TI-ADCs and their non-idealities is explained. The first section discusses the concept of TI-ADCs while the second section outlines the problems that TI-ADCs can encounter.

2.1 History of the Time-Interleaved ADCs

Generally, high speed Analog to digital converters (ADCs) operate by means of different flash techniques where in order to obtain fast n bit conversion; 2^{n-1} comparators operate in parallel mode. Even though this method offers large Converter Bandwidth, it leads to large die area for (n >6) and has been observed to be unsuitable for (n >8). On the other hand, the idea of time-interleaved ADCs is not new and was originally introduced by Black and Hodges [7] for the very first time. The Time-Interleaved ADCs operate across M-parallel lanes of ADCs resulting in an overall output M-times than that of a single individual lane ADC. Consequently, it can accomplish enhanced sampling speeds which otherwise would be impossible by using a single ADC without extreme power penalty. Such useful idea was not very well known until like a decade ago. One of the earliest research works carried out by [8] indicated that the overall power consumption by an ADC can be considerably lowered when several slow single ADCs operate by means of a Time-Interleaved approach. From that time, extensive research has been carried out on Time-Interleaved SAR ADCs. Studies have shown that Time-Interleaved SAR ADCs technique can significantly decrease the die area and power over the flash-circuits (for n>6), yet without sacrificing signal-to-noise ratio, SNDR, SFDR or bandwidth. Therefore, for a particular resolution, the Time-Interleaved SAR ADCs are capable of overcoming the speed-power trade-off by improving the sampling speed and decreasing the net power consumption. Nonetheless, a mismatch between the lane-ADCs can introduce undesired spurious tones in the output, consequently degrading the overall performance of the total Time-Interleaved ADC.

2.2 Operation of Time-Interleaving ADCs

Generally, a Time-Interleaving ADC system contains M-number of ADCs working in a parallel mode, each operating at a conversion rate of fs/M, with f_s being the net sampling frequency while M indicating the total number of interleaving ADCs. These ADCs operate from different sampling phases, φi (where, i =0, 1, 2, 3, ... M-1) which are phase shifted from one another by a single sampling period T_s. Each ADC samples the input signal during these sampling phases. The overall data from the entire M interleaved ADCs is muxed together at the output for achieving a net sampling rate of f_s.

For getting a clearer understanding of the Time-Interleaved ADCs, let's imagine we have a four-channel interleaved ADC as indicated in the figure 3. Four ideal ADCs, sample the input analog signal x(t) and operate across different phases from φ_0 to φ_{M-1} producing output data indicated as $Y_{0(t)}$ to $Y_{M-1(t)}$ in digital form, respectively. However, due to device mismatch, practically every lane-ADC has a slightly different gain,

bandwidth, offset, and sampling time. The net output spectrum can have spurs depending on the source of such non-idealities.

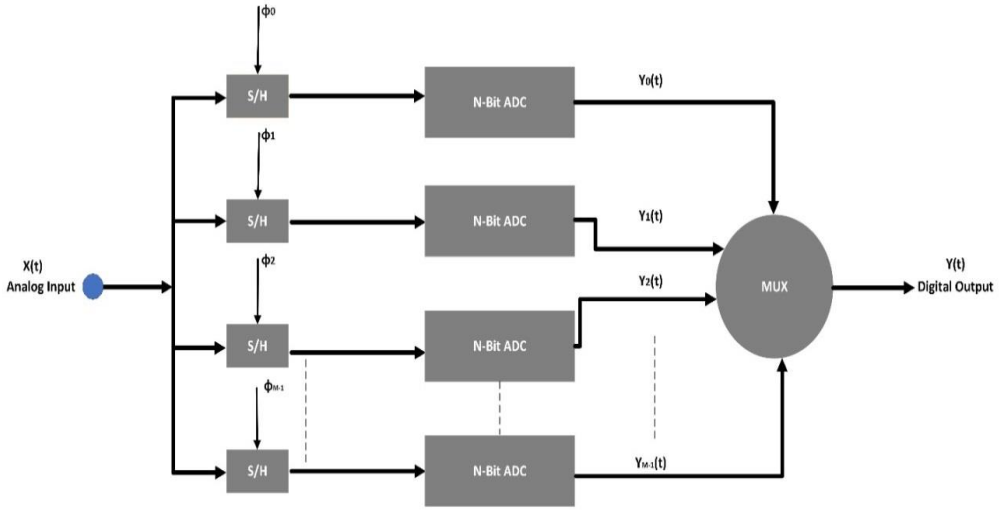


Figure 3 The Block diagram of a 4-channel TI ADC.

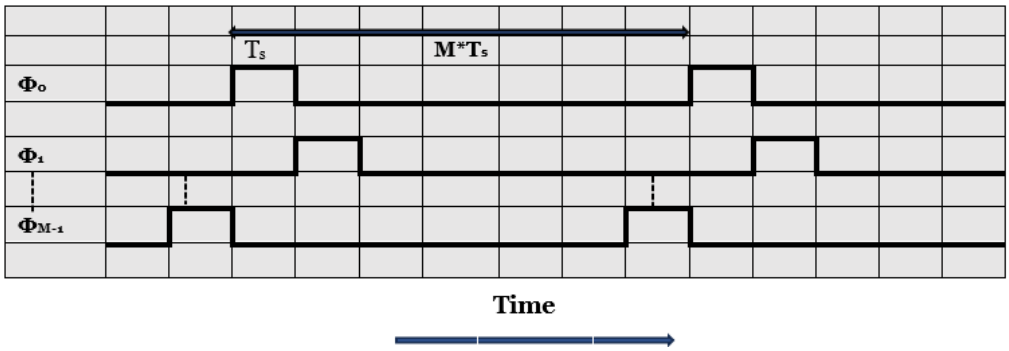


Figure 4 Different timing waveforms.

2.3 Ideal Time-Interleaved ADC

In the case of our MATLAB simulation of a 4-channel Time-Interleaved ADC system, no spurious tones were observed in the output signal because of the absence of channel mismatches in offset, gain or timing. A well-defined digital representation of the input signal without introducing any undesirable artifacts can be achieved by such absolute channel synchronization. In addition, the simulation indicated zero error in signal interleaving as well as processing, representing that it is possible to perfectly capture and reconstruct the input signal by our ideal TI-ADC model without any gain, offset and timing or phase errors. This shows the significance of addressing the channel mismatches in practical TI-ADC systems so that the overall signal performance and integrity can be maintained.

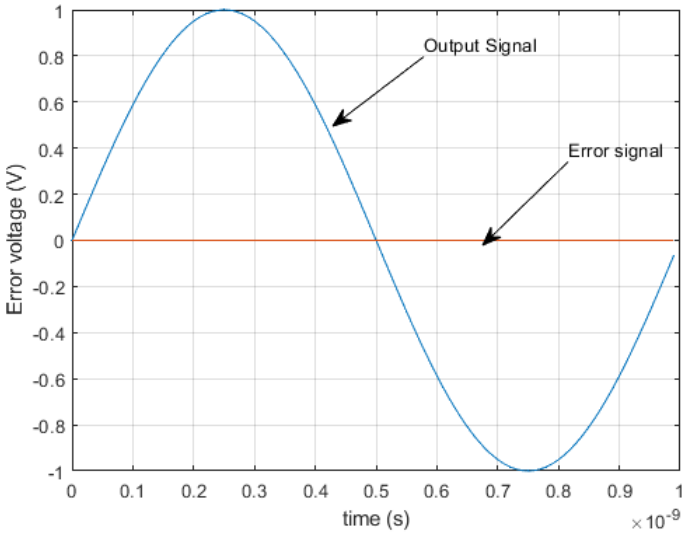


Figure 5 Ideal output of Time-Interleaved ADC signal.

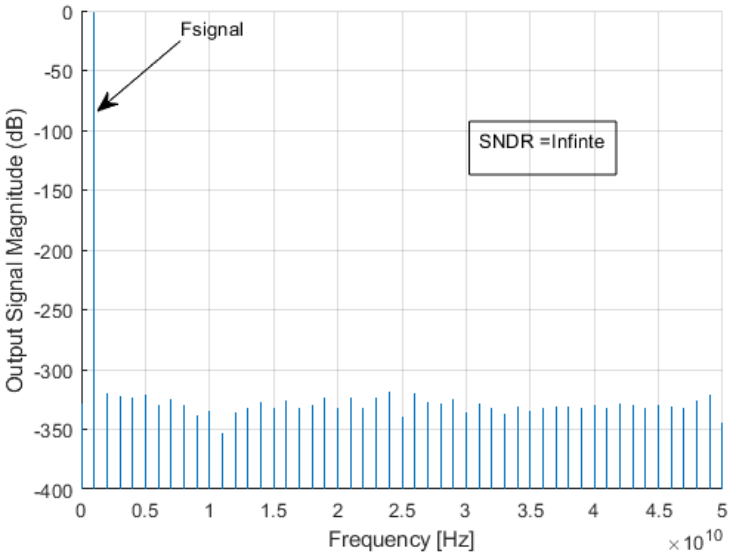


Figure 6 One sided output spectrum of the Time-Interleaved ADCs

2.4 Types of impairments in Time-Interleaving ADCs

The time-interleaving impairments mentioned here result from the mismatches between channels. They can have a mismatch in gain, offset, and timing or phase while the timing mismatch being the main issue in fast TI-ADCs. In the frequency domain, these limitations appear as spurious tones and thus degrade the overall TI-ADC's performance with respect to SNDR, SFDR, and signal-to-noise ratio.

2.4.1 Offset Mismatch:

To discuss the offset-mismatch, it is assumed that the offset errors vary for each channel while all other characteristics are considered to be the same. This is a random additive error which may originate from the mismatch of a comparator differential pair. Offset is basically a DC error within each sub-ADC and it becomes periodic over time with time-

interleaving. Thus, the offset mismatch is periodic having a periodicity of M*Ts and it does not depend on the input signal. This mismatch emerges as tones in the frequency-domain at frequencies that are independent of both, the input amplitude and the frequency. These equations can be derived as explained in [9].

$$y(t) = \sum_{n=0}^{M-1} \sum_{k=-\infty}^{\infty} (x(t) + O_n) \cdot \delta(t - kMT_s - nT_s) \tag{2.1}$$

The Fourier Transform of equation 2.1 is given below in equation 2.2

$$Y(j\Omega) = \frac{1}{MT_s} \sum_{n=0}^{M-1} \sum_{k=-\infty}^{\infty} \left[\frac{A\pi}{j} \left(\delta\left(\Omega - k\frac{\Omega_s}{M} - \Omega_0\right) - \delta\left(\Omega - k\frac{\Omega_s}{M} + \Omega_0\right) \right) + O_n 2\pi\delta\left(\Omega - k\frac{\Omega_s}{M}\right) \right] e^{-jkn\frac{2\pi}{M}} \tag{2.2}$$

Therefore, the tones are located at:

$$\Omega_{error} = k.\frac{\Omega_s}{M} \tag{2.3}$$

Here K is an integer= 0, 1, 2, 3.....M, T_s the sampling period, M represents the total number of interleaved ADCs, Ω indicates the angular frequency in the frequency domain, Ω_S is the sampling angular frequency and Ω_o is the input angular frequency. O_n is the offset error for channel n. Ω_{error} is the frequency location of the error tone.

While the amplitude and shape of a periodic error signal define the magnitude of the offset spurs, the location of such spurs remains unaffected by the input signal amplitude and frequency.

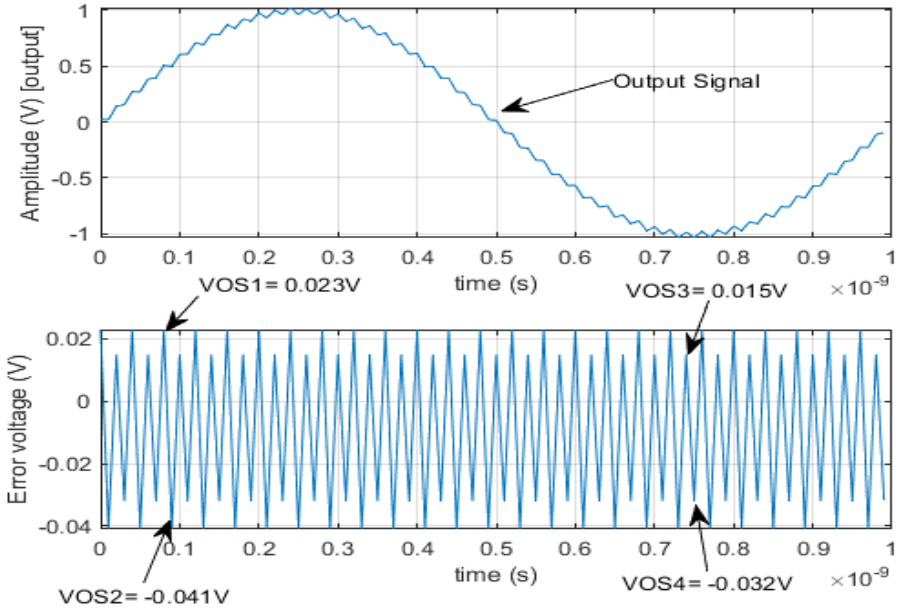


Figure 7 Output of Interleaved ADC, in the presence of offset error.

Figures 8 and 9 show the simulations of the Time-Interleaved ADCs having offset mismatch across various signal/input frequencies.

Offset mismatch values are V_{OS1} = 0.023 V; V_{OS2} = -0.041 V; V_{OS3} = 0.015 V; V_{OS4} = -0.032 V;

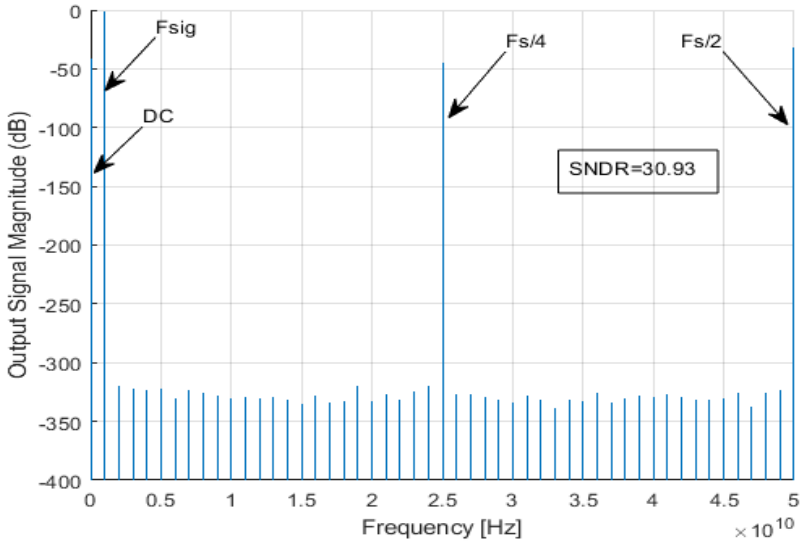


Figure 8 One sided spectrum of Interleaved output, in presence of offset error and F_{sig}=1 GHz.

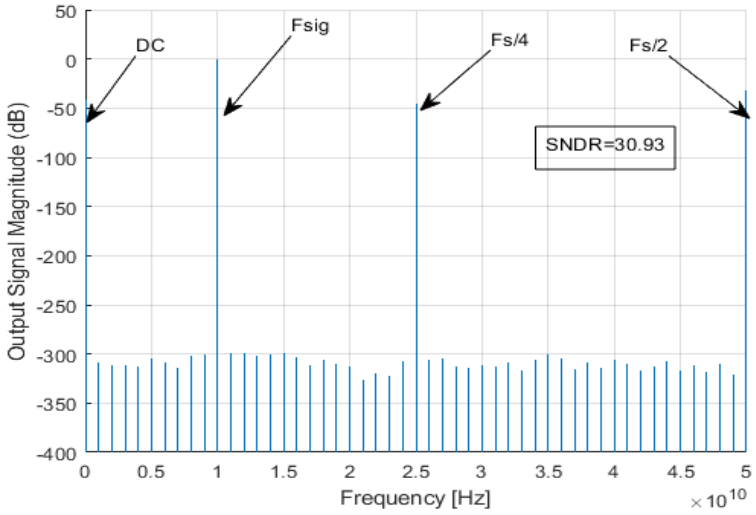


Figure 9 One sided spectrum of Interleaved output, in presence of offset error, and F_{sig}=10 GHz.

The SNDR in the presence of offset error can be calculated by using the formula given in [11].

$$\text{SNDR} = 20\log\left(\frac{A_{in}}{\sigma_{\text{On}}}\right) \tag{2.4}$$

Here σ_{On} represents the offset error's standard deviation while A_{in} is the input signal's amplitude. The simulation shows that the spurious tones appear at a fixed frequency and the SNDR is independent of input/signal frequency, consistent with the explanation given by [10].

2.4.2 Gain Mismatch:

In order to discuss gain-mismatch, let's say the gain errors are distinct for every single channel, but all the remaining characteristics are same. Discrepancy in reference voltages or the sampling circuit (such as clock feedthrough or charge injection) between several lane ADCs is considered a significant source of gain error. Just like offset mismatch, these errors also take place with a period of M*Ts; however, they are amplitude modulated with the input frequency Ω_0. The absolute errors are lowest when the input crosses zero and are greatest at the peaks of input signal. So, the magnitude of such errors is affected by the input signal's amplitude but remains unaffected by the input signal's frequency Ω_0. However, their position varies with the input/signal frequency.

This is represented by the following equations and derivation of these equations is given in [9]

$$y(t) = \sum_{n=0}^{M-1} \sum_{k=-\infty}^{\infty} g_n x(t) \,.\, \delta(t - kMT_s - nT_s) \tag{2.5}$$

Therefore, the tones are located at:

$$Y(j\Omega) = \frac{1}{MT_s} \sum_{n=0}^{M-1} \sum_{k=-\infty}^{\infty} \left[g_n \frac{A\pi}{j} \left(\delta\left(\Omega - k\frac{\Omega_s}{M} - \Omega_0\right) - \delta\left(\Omega - k\frac{\Omega_s}{M} + \Omega_0\right)\right)\right] e^{-jkn\frac{2\pi}{M}} \tag{2.6}$$

$$\Omega_{error} = k\frac{\Omega_s}{M} \pm \Omega_0 \tag{2.7}$$

Where K= 1, 2, 3 .....M and for the channel n: g_n is the gain error. Ω_{error} is the frequency location of the error tone.

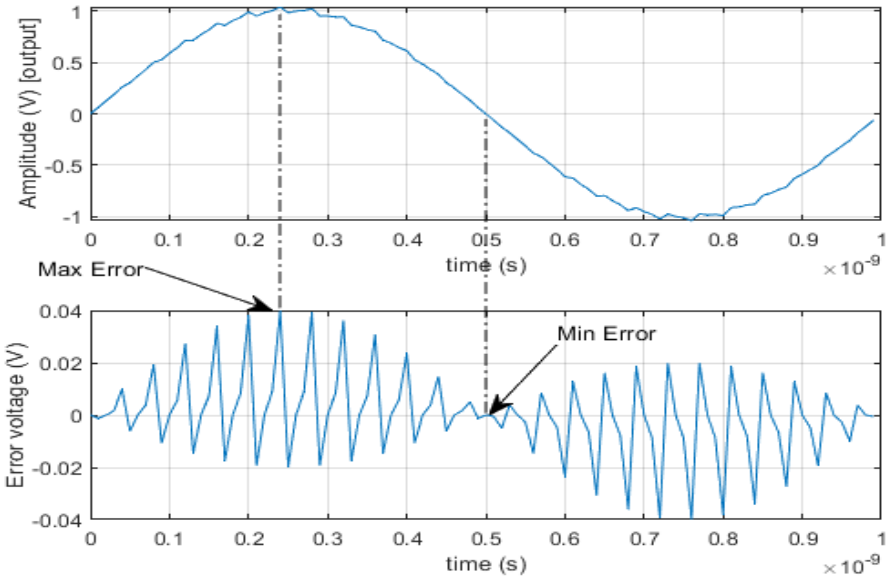


Figure 10 Output of Interleaved ADC when gain mismatch is present.

Figures 11 and 12 show the simulations of time Interleaved ADCs when gain mismatch is present with different signal/input frequencies.

The example gain mismatch values for the four channel TI-ADC are $A_1 = 1.04$; $A_2 = 0.98$; $A_3 = 1.0$; $A_4 = 1.009$.

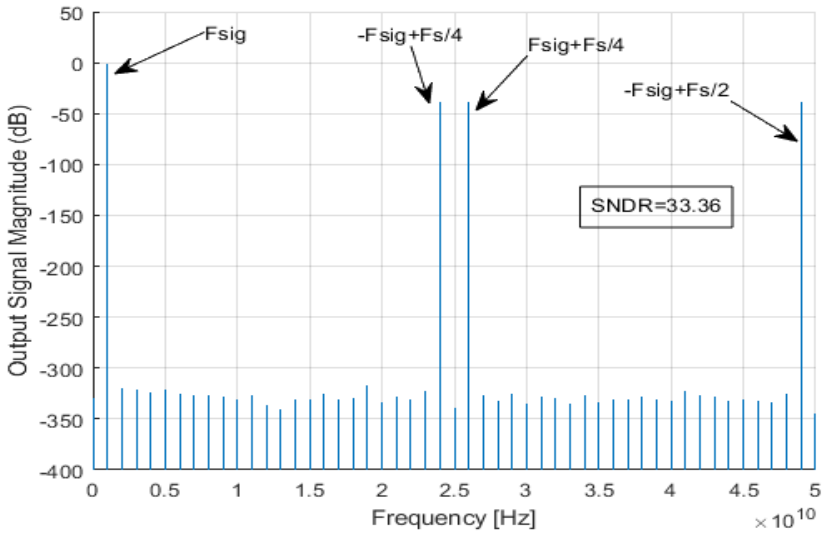


Figure 11 One sided spectrum of Interleaved ADC with gain mismatch and F_{sig}=1 GHz

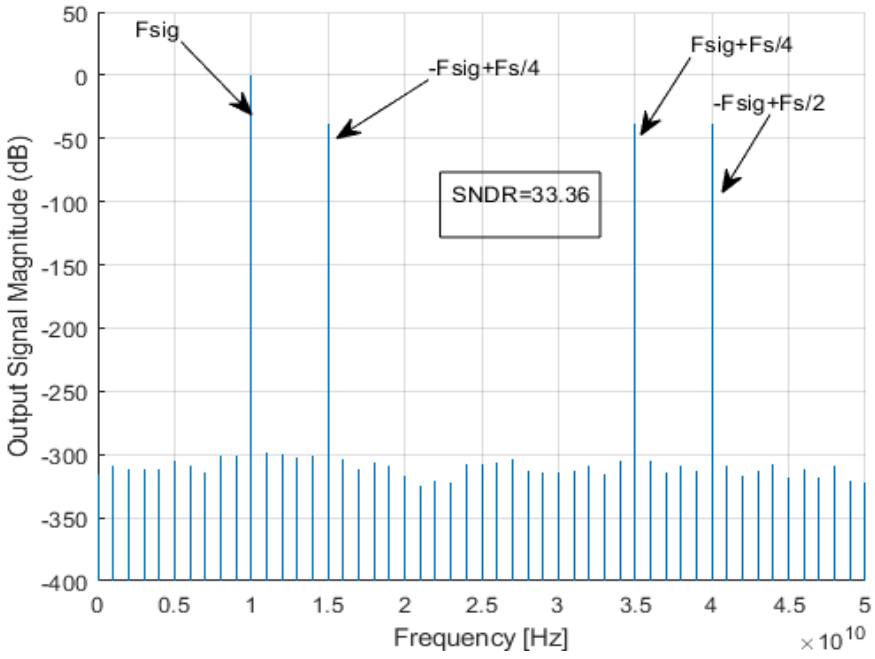


Figure 12 One sided spectrum of Interleaved ADC with gain mismatch and F_{sig}=10 GHz

The SNDR value in the existence of gain mismatch can be calculated using the formula given in [11].

$$\text{SNDR} = 20\log_{10}\left(\frac{\Delta g_n}{\sigma_{gn}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \tag{2.8}$$

Here Δ_{gn} is the mean of channel gain, M is the number of interleaved channels and σ_{gn} is the standard deviation of gain error. Results obtained from using this formula are exactly like our MATLAB simulation results. The simulation shows that the location of

the spurious tones is at a frequency dependent on the input frequency, however the SNDR is independent from it which is the same as explained in [10].

2.4.3 Timing-Mismatch

In this section the timing error, because of clock-skew, is considered to be different for all the channels but other characteristics are assumed to be same. The timing or phase errors are inevitable in practical terms, owing to the clock signal's limited propagation and differences in the clock buffers and sampling switches. Again, the errors take place with a period of $M*T_s$ and similar to gain mismatch, they are amplitude modulated with the input frequency Ω_o. The absolute errors are largest when the slope of the signal is high and lowest when slope is small or null. As a result, the error location again relies on the input frequency while its magnitude is reliant on input/signal frequency Ω_o and also dependent to the input signal's amplitude.

This is shown by the following equations and derivation of these equations is given in [9]

$$y(t) = \sum_{n=0}^{M-1} \sum_{k=-\infty}^{\infty} \left(x(t - \Delta t_n)\right) . \delta(t - kMT_s - nT_s) \tag{2.9}$$

$$Y(j\Omega) = \frac{1}{MT_s} \sum_{n=0}^{M-1} \sum_{k=-\infty}^{\infty} \left[\frac{A\pi}{j}\left(\delta\left(\Omega - k\frac{\Omega_s}{M} - \Omega_0\right) - \delta\left(\Omega - k\frac{\Omega_s}{M} + \Omega_0\right)\right) e^{-j\Omega_0 \Delta t_n}\right] e^{-jkn\frac{2\pi}{M}} \tag{2.10}$$

Therefore, the tones are located at:

$$\Omega_{error} = k\frac{\Omega_s}{M} \pm \Omega_0 \tag{2.11}$$

Where K= 1, 2, 3.....M and for the channel n: Δ_{tn} is the timing error. Ω_{error} is the frequency location of error tone.

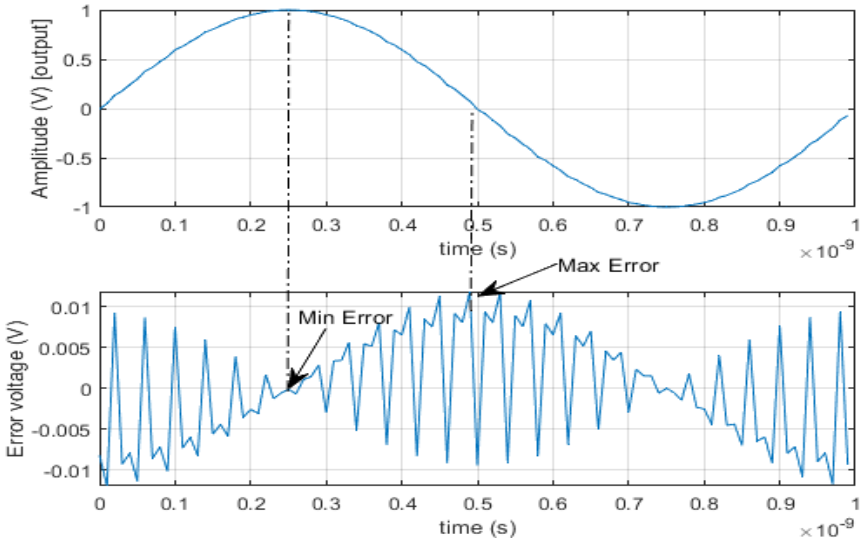


Figure 13 Output of Time-Interleaved ADC with timing mismatch.

Figures 14 and 15 show the simulations of the Time-Interleaved ADCs having timing mismatch across various signal/input frequencies.

Timing mismatch values for the four channel TI-ADC are d_{TS1} = -1.297e-12 s; d_{TS2} = -1.897e-12 s; d_{TS3} = 1.497e-12 s; d_{TS4} = -1.497e-12 s;

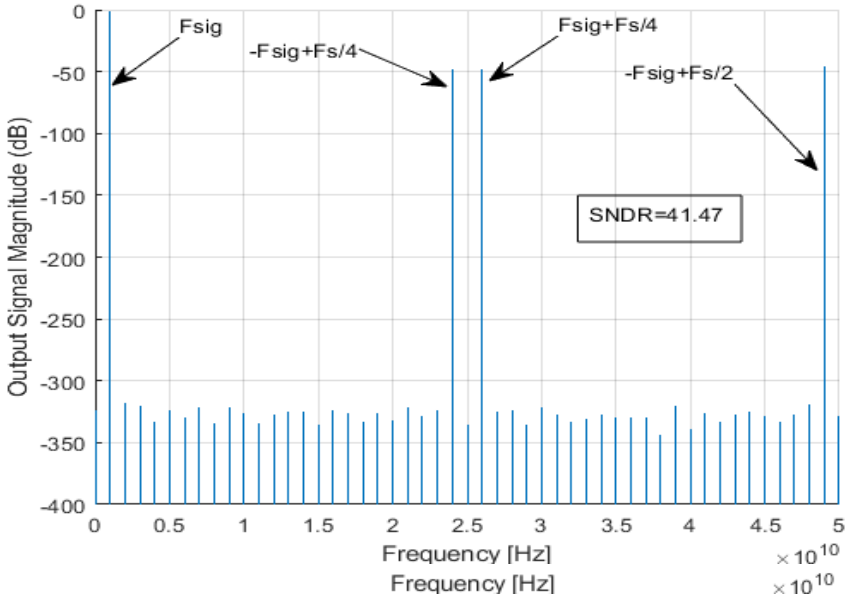


Figure 14 One sided spectrum of Interleaved ADC with Timing-mismatch and F_{sig}=1 GHz.

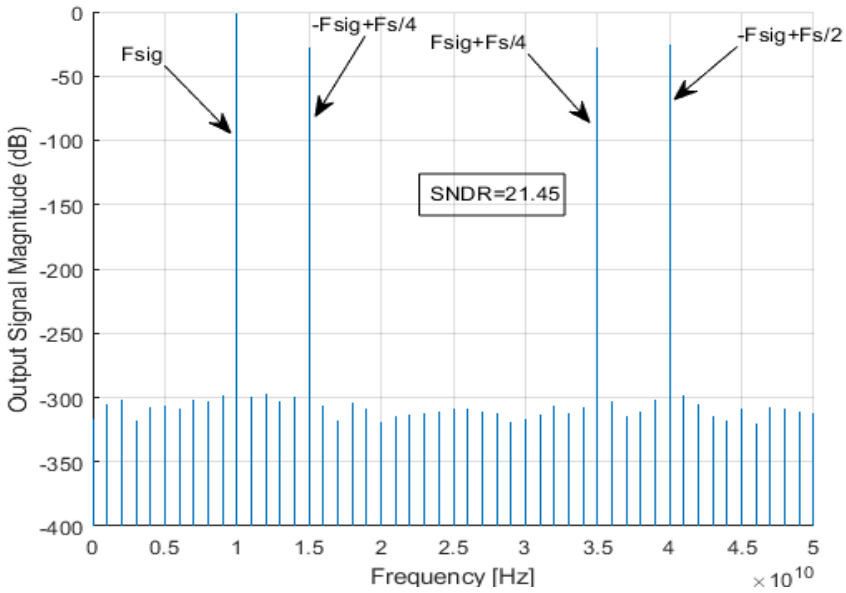


Figure 15 One sided spectrum of Interleaved ADC in presence of Timing-mismatch and F_{sig}=10 GHz.

The SNDR value in the presence of skew mismatch can be calculated using the formula given in [11].

$$\text{SNDR} = 20\log_{10}\left(\frac{1}{\sigma_{tn}2\pi f_{in}}\right) - 10\log_{10}\left(1-\frac{1}{M}\right) \tag{2.12}$$

Here M represents the net number of interleaved channels, σ_{tn} is standard deviation of skew mismatch and f_{in} is the frequency of the input signal. The results calculated through theory are matching with the results from MATLAB simulations.

The results of the simulation reveal that the frequency of the input signal has a significant impact on the location of the spurious tones and the SNDR is also input frequency dependent which is the same as explained in [10].

The timing mismatch error varies proportionally with the input frequency and dominates at greater speeds, therefore, to correct it with high accuracy, is a highly significant but a challenging task. The timing and the gain-mismatch spurs occur at the same frequencies but, they can be distinguished as the timing-mismatch are affected by the input/signal frequency and are more dominant at higher frequencies, on the other hand, the magnitude of the gain-mismatch does not depend on the input frequency, and it usually dominates at low frequencies.

2.4.4 Total mismatches (Offset+gain+timing)

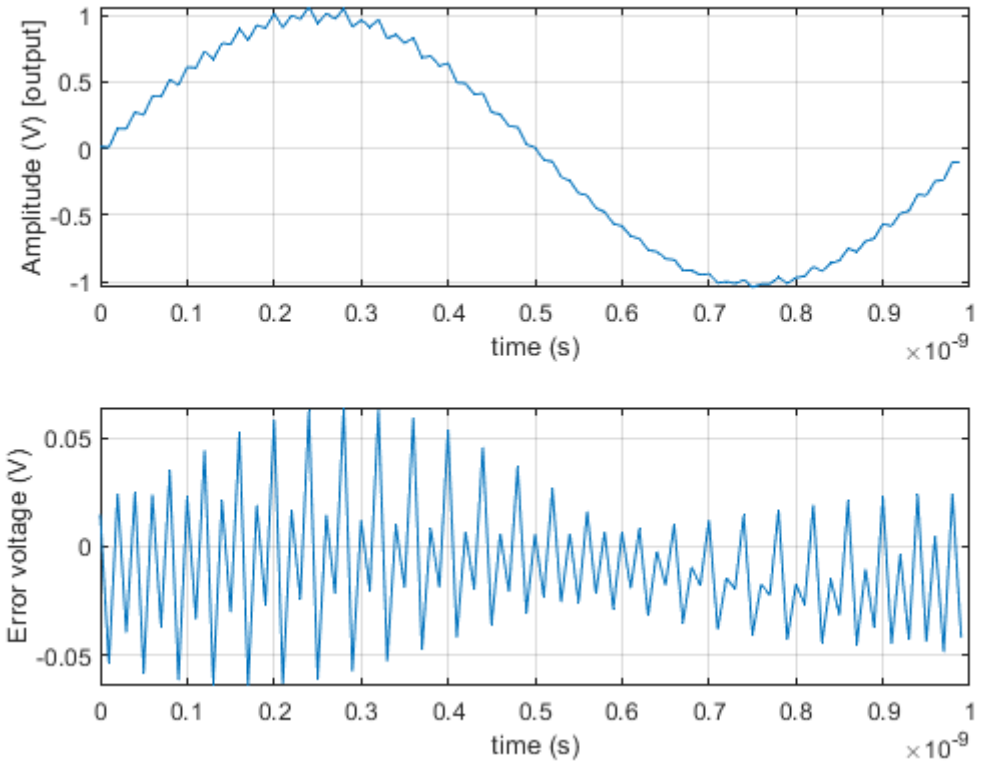


Figure 16 Output of Interleaved ADC having (Offset+gain+timing mismatch).

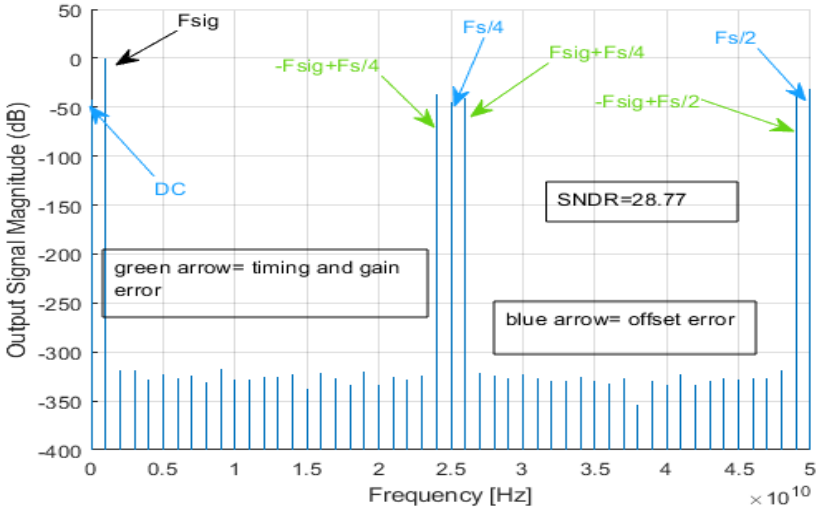


Figure 17 One sided spectrum of Interleaved ADC having (Offset+gain+timing mismatch) and F_{sig}=1 GHz.

2.5 Conclusion

Research on TI-ADCs have shown that a significant decrease in die size and power over flash type ADCs (for n >6) can be attained by using the Time-Interleaving technique, yet without sacrificing signal-to-noise ratio or bandwidth. Therefore, the Time-Interleaved ADCs are able to overcome the speed-power trade-off at a given resolution, by improving the sampling speed and decreasing the net power consumption. Nonetheless, mismatch between the lane-ADCs is a challenge for the data converter's designers since this can introduce undesired spurious tones in the output spectrum, subsequently degrading the overall performance of the Time-Interleaved ADCs [12].

Chapter 3: Single Transistor

The third chapter focuses on a comparative analysis of two advanced semiconductor technologies: 28-nm CMOS BULK and 22-nm FD-SOI CMOS technology.

3.1 Common Source Amplifier

The circuit illustrated in Figure 18 is designed in order to bias the drain voltage and drain current of transistors M_1 and M_2. The drain voltage is controlled using a feedback loop and drain current is controlled using a constant current source. The gate voltage for M_1 is derived from the output of an operational amplifier. This voltage is automatically adjusted using the feedback loop to ensure stability. Transistor M_2 receives the same gate voltage as M_1. This ensures that both transistors operate under identical conditions with the same drain voltage and same drain current. The right side of the circuit is basically a replica of left side, with the feedback loop which is effectively reducing the gain. When V_{GS} tends to increase, it also tries to increase I_D. The feedback loop adjusts the gate voltage to oppose this increase redirecting the current to ground, thus maintaining a stable I_D. That's why the output is taken at the right-side of the circuit which does not have any feedback loop.

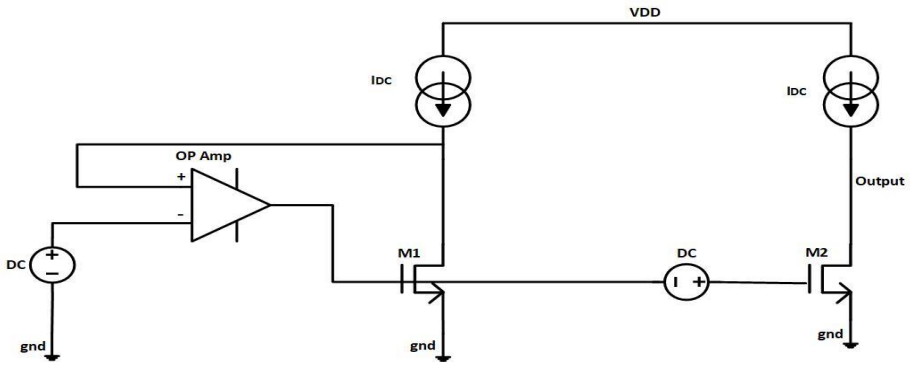


Figure 18: Common source amplifier with constant current source as a load

3.2 Results

3.2.1 Transconductance (gm)

The circuit is simulated using 28-nm Bulk and 22-nm FD-SOI CMOS technology to investigate the impact of varying design parameters such as length, width (L*100), and current density (I_D/W/L) on the gain, transconductance (g_m), output conductance (g_{ds}), -3dB bandwidth, and gain-bandwidth product of the amplifier. The length and width are adjusted so that the ratio of W/L is consistently 100. The drain current I_D is calculated as the product of current density and W/L.

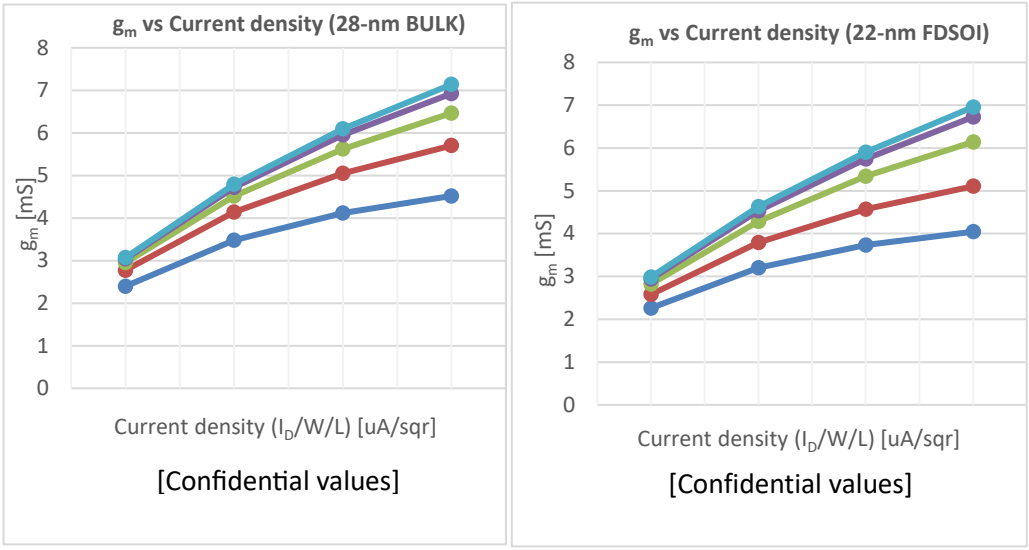


Figure 19: gm vs. Current density curves for different values of length and width

The graphs in Figure 19 illustrate the relationship between current density and transconductance g_m for various lengths and widths. It is observed that g_m increases as current density rises, as suggested by the MOSFET equation shown in [13].

$$g_m = \sqrt{(2.\mu_n.C_{OX}.\frac{W}{L}.I_D)} \tag{3.1}$$

When the current density doubles then

$$I_D \rightarrow (2 * I_D) \tag{3.2}$$

$$g_m \rightarrow \sqrt{2}\ .g_m \tag{3.3}$$

while all other parameters remain constant. Simulations indicate that g_m does not follow the trend precisely due to short channel effects.

3.2.2 Output conductance (g_{ds})

Figure 20 below shows the relationship between g_{ds} and current density for different lengths and widths. The output conductance equation in [13]:

$$g_{ds} = \frac{I_D}{L.V_E} \tag{3.4}$$

This equation demonstrates that g_{ds} increases as I_D increases, but due to short channel effects, the trend is not entirely observed as expected. This implies that when I_D is doubled, g_{ds} should also double; however, the observed g_{ds} does not double exactly, as shown in the figures below.

The comparison between 28-nm Bulk and FD-SOI 22-nm technologies reveals significant differences in how g_{ds} varies with current density. The 28-nm Bulk technology shows a more substantial increase in g_{ds} with current density, as compared to 22-nm FDSOI. But below graph in Figure 20 shows that 22-nm FD-SOI has higher ($r_{ds}=1/g_{ds}$) as compared to 28-nm Bulk technology.

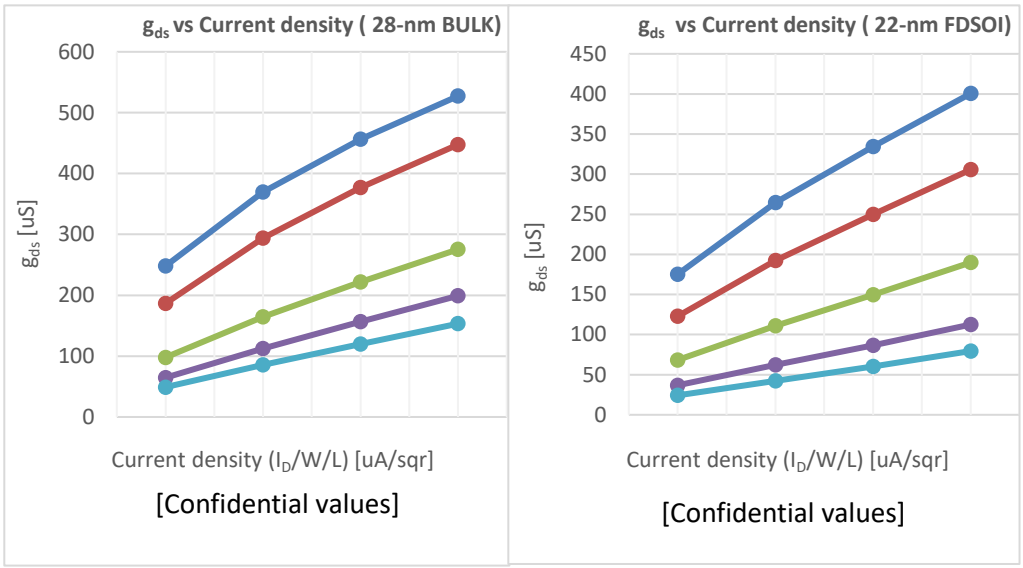


Figure 20 g_{ds} vs Current density curves for different values of length and width

3.2.3 DC Gain

Figure 21 illustrates the relationship between DC gain and current density for various lengths and widths of transistors. The graph indicates that as current density increases, the gain decreases, with higher values of length and width resulting in higher gain. This trend of decreasing gain with increasing current density aligns with the given equation (3.5)

$$\text{gain} = \frac{1}{\lambda}.\sqrt{\frac{(2.u_n.C_{ox}\,(\text{W.L})}{I_D}} \qquad (3.5)$$

The comparison between 28-nm Bulk and FD-SOI 22-nm reveals significant differences in how DC gain varies with current density. The 28-nm Bulk technology exhibits a more substantial decrease in DC gain with increasing current density as compared to 22-nm FD-SOI. But the 22-nm FD-SOI technology has higher intrinsic gain ($g_m.r_o$) as compared to 28-nm Bulk technology due to better transconductance (g_m) and higher output resistance (r_o).

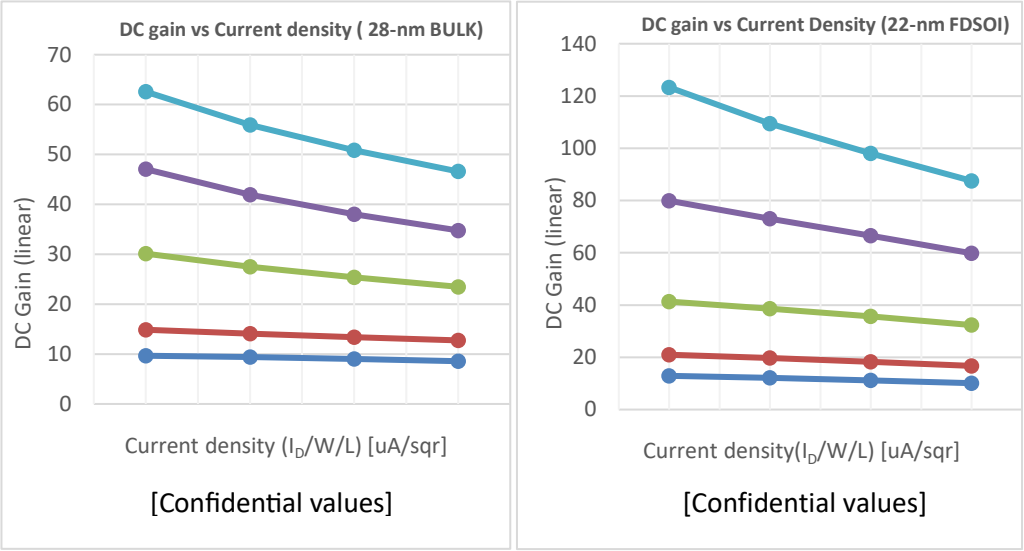


Figure 21 DC gain vs Current density curves for different values of length and width.

3.2.4 -3dB Bandwidth

Figure 22 illustrates the relationship between the 3dB bandwidth of a common-source amplifier and the current density.

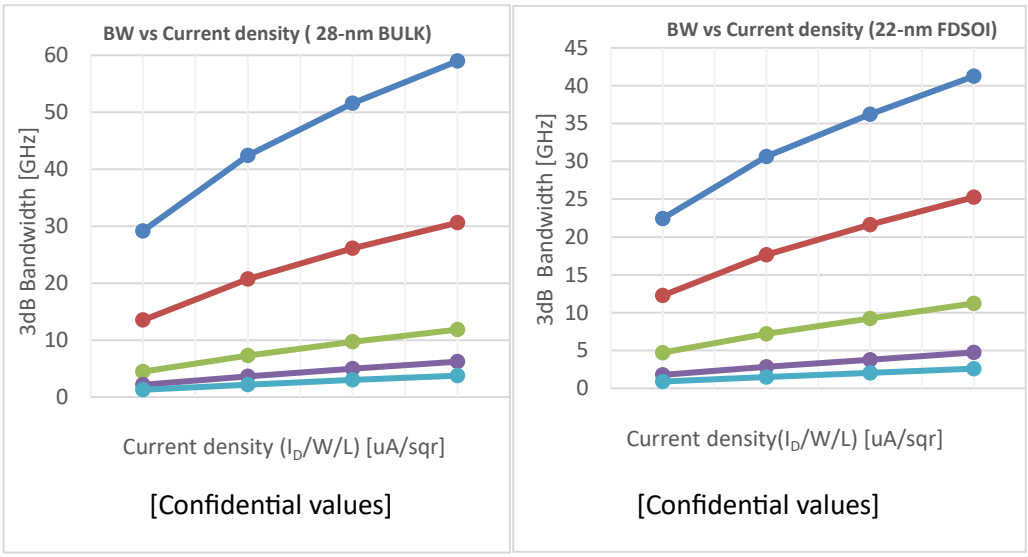


Figure 22 3dB bandwidth vs Current density curves for different values of length and width

According to the results, as current density increases, the 3dB bandwidth also increases. Furthermore, simulations show that transistors with smaller lengths and widths have higher bandwidths, as demonstrated in the figure 22 graphs.

The comparison between 28-nm Bulk and FD-SOI 22-nm technologies shows significant differences in how the 3dB bandwidth varies with current density. The 28-

nm Bulk technology exhibits a more pronounced increase in bandwidth with rising current density as compared to 22-nm FD-SOI technology.

3.2.5 Gain Bandwidth Product (GBW):

Figure 23 illustrates the relationship between the gain bandwidth product of a common-source amplifier and the current density.

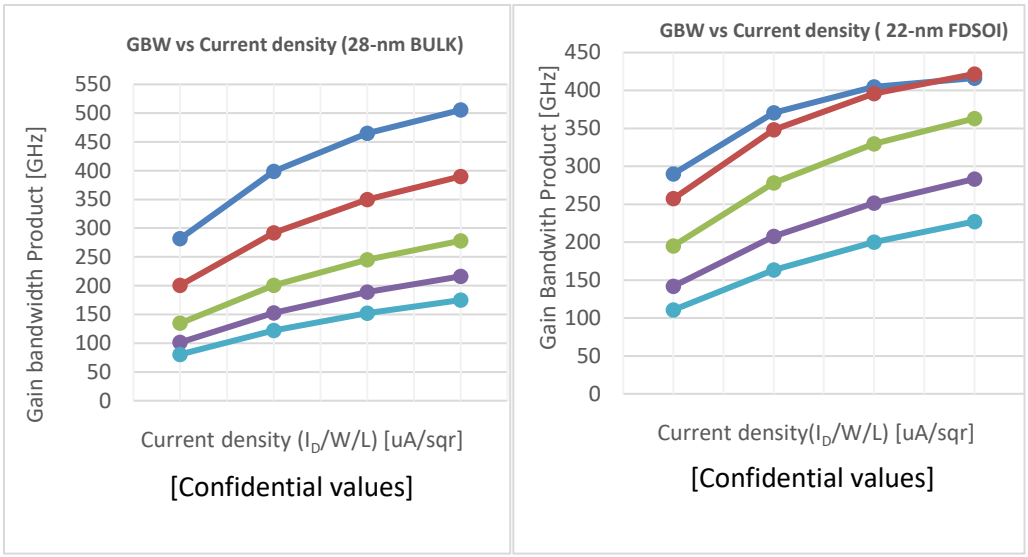


Figure 23 Gain bandwidth product vs current density curves for different values of length and width

The results indicate that as current density increases, the GBW also increases. Furthermore, simulations show that transistors with smaller lengths and widths have higher GBW, as demonstrated in the graphs. It has been observed that for higher values of length and width we can get better gain bandwidth product for 22-nm FD-SOI as compared 28-nm Bulk technology.

3.3 Conclusion

In summary, the 22-nm FD-SOI technology outperforms the 28-nm bulk technology in terms of gain and gain bandwidth product. Owing to various benefits of FD-SOI technology including better electrostatic characteristics, improved control of the random mismatch, lower junction leakage and capacitances, as well as easier manufacturing, this technology shows a better performance and offers improved area power and cost tradeoff as compared to 28-nm Bulk technology.

Chapter 4: Strong Arm Latch Comparator

4.1 Comparator

In an ADC system, a comparator is an essential component as it is responsible for comparing two analog signals and producing a logic output signal, thus functioning as a 1-bit ADC [14]. There are various types of comparators; however, the primary focus of this thesis is going to be the strong-arm latch comparator for ADCs particularly for TI-SAR ADCs.

4.2 Basics of comparator

The comparator has two analog inputs, one from the DAC as a reference signal and the other as the input to be measured, stated as $V_{in,n}$ and $V_{in,p}$ respectively. When $V_{in,p}$ is greater than $V_{in,n}$, the comparator will produce an output as a logic 1 or high. Conversely, if $V_{in,n}$ is smaller than $V_{in,p,}$ an output as a logic 0 or low will be generated. The figure 24(a) displays the operation of an ideal comparator. It compares the analog signal V_{in-p} with the reference signal V_{in-n}, producing a logic level for V_{out} based on this comparison. It also illustrates the general symbol for the comparator. Because of non-ideal nature of the components, the comparator's behavior is better represented in figure 24(b) where rise times causes an output delay. In case of dynamic comparators, the clock signal is used for carrying out the evaluation on one edge while reset is done on the other. Furthermore, two outputs are generated: one for the logic output and another one for its complementary, as explained in the figure 24(c).

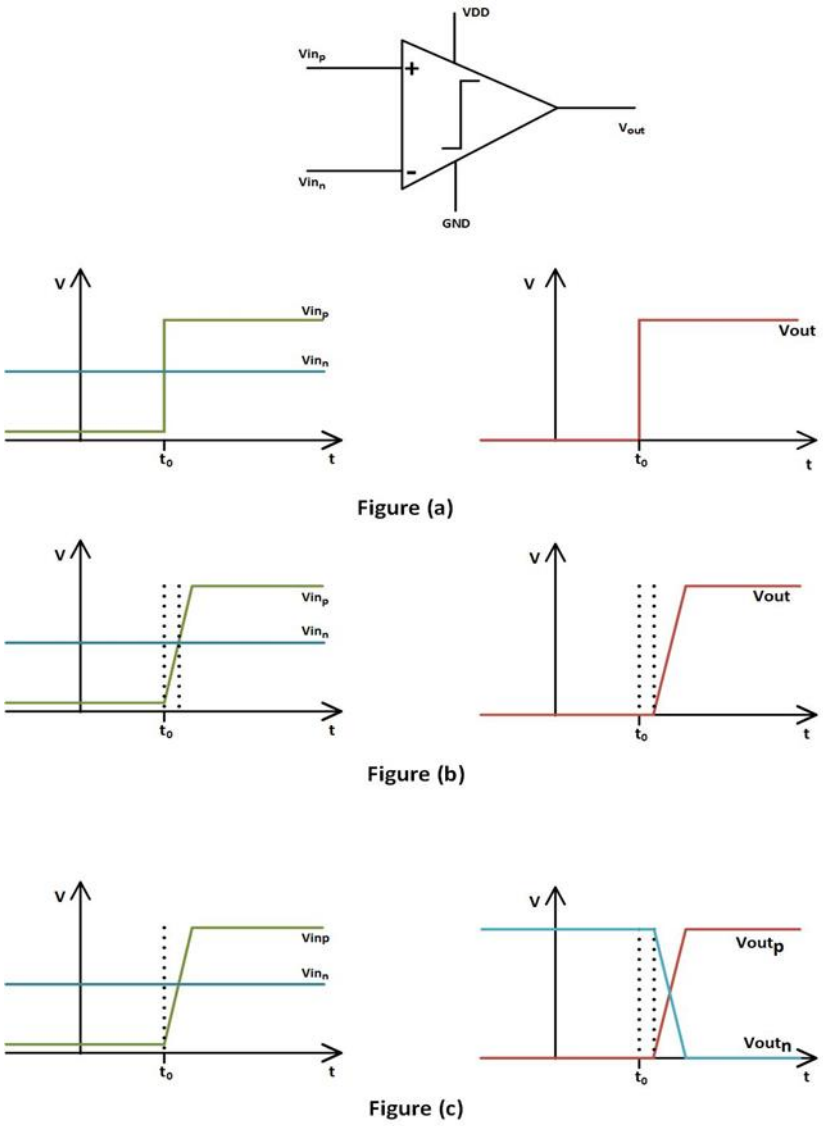


Figure 24 (a) Behavior in an Ideal Comparator. (b) Behavior in a non-Ideal Comparator. (c) A comparator with two outputs.

4.3 Comparator Phases

In a dynamic latched comparator, there are two distinct phases: namely the evaluation phase and the reset phase. During the evaluation phase, a comparison of the inputs is carried out by the comparator which then generates the logic output on the basis of which input voltage is greater. In the reset phase, the internal voltage levels are reset by the comparator. When the reset phase is not long enough, the internal voltage levels start acting as memory, potentially influencing subsequent comparisons.

4.4 Strong-Arm latch comparator circuit

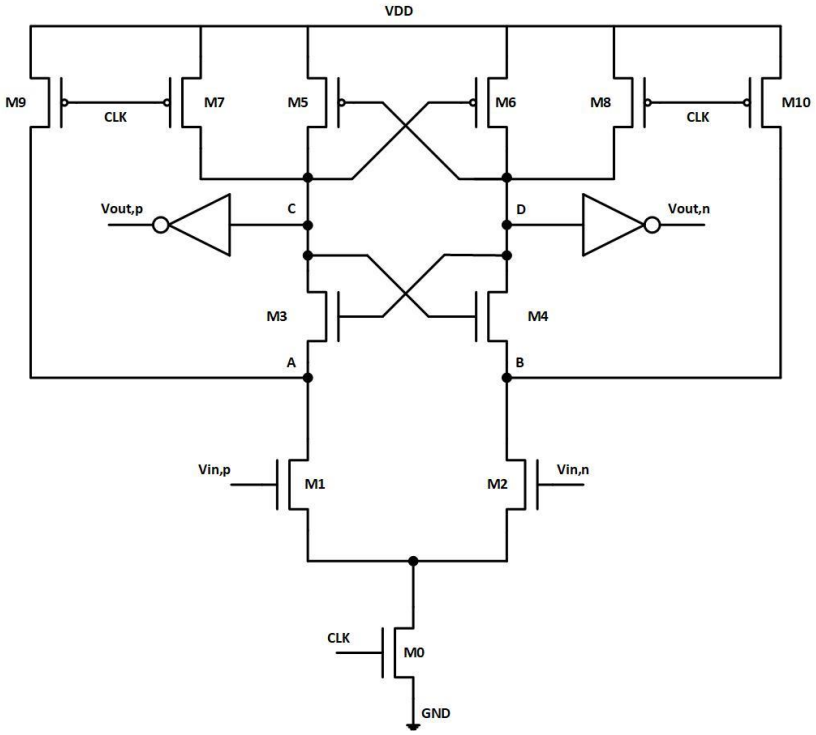


Figure 25 Strong arm latch comparator

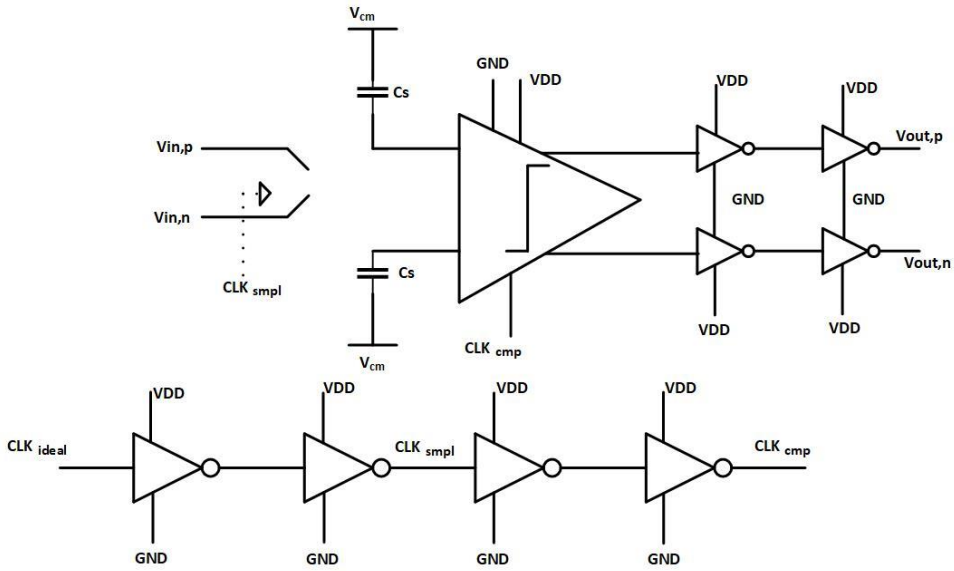


Figure 26 Strong-Arm-latch comparator test bench

4.5 Comparator Operation

When the clock is low or at logic level 0, then switches M_7, M_8, M_9, M_{10} are activated and they reset the node A, B, C, D to V_{DD}. It means that parasitic capacitances at these nodes are charged to V_{DD}. In this phase, the transistors from M_1 to M_6 and M_0 are off, and the circuit has no current flowing through it. It means that the strong-arm latch comparator does not have any static power consumption. This is one of the benefits of this type of comparator.

When the clock is high or at logic level 1, then transistors M1 and M2 are turned on and node A and B start discharging. Transistors M_1 and M_2 start drawing differential drain current based on the differential input voltage $V_{in,p}$ and $V_{in,n}$. If $V_{in,p}$ is greater than $V_{in,n}$ then M_1 will draw more current than M_2. When the parasitic capacitances associated with the nodes A and B are discharged to V_{DD}-$V_{th3,4}$ then transistors M_3 and M_4 are turn on.

If I_{NP} (current flowing through M_1) is greater than I_{NN} (current flowing through M_2) then node C will discharge faster than node D which will bring node C to V_{DD}-V_{th} at a higher rate. This will turn on M_6 while M_5 during this time will be off. It means one output will be at V_{DD} while the other will be at ground. If $V_{in,n}$ is greater than $V_{in,p}$ then circuit operation will operate the same in the opposite direction. This operation is also very well explained in [15].

The test bench for the comparator is shown in Figure 27. Input switches in a comparator test bench are used to select or sample the input signals. The clock signals control these switches to sample the input voltage at specific times. The smpl_ctrl signal is used to control the sampling switches. When smpl_ctrl is high, the input signals are sampled and stored on capacitors connected to the inputs of the comparator. This ensures that the comparator is comparing stable voltages rather than continuously varying signals. After sampling, the control signal smpl_ctrl deactivates, opening the switches. The comparator then compares the voltages stored on the capacitors and on the basis of this comparison, it sets its output accordingly.

4.6 Comparator Sizing for Noise

To get an idea how we should size our comparator in terms of input referred noise. Let's take a common source amplifier having PMOS as the current source load as indicated by the figure 27.

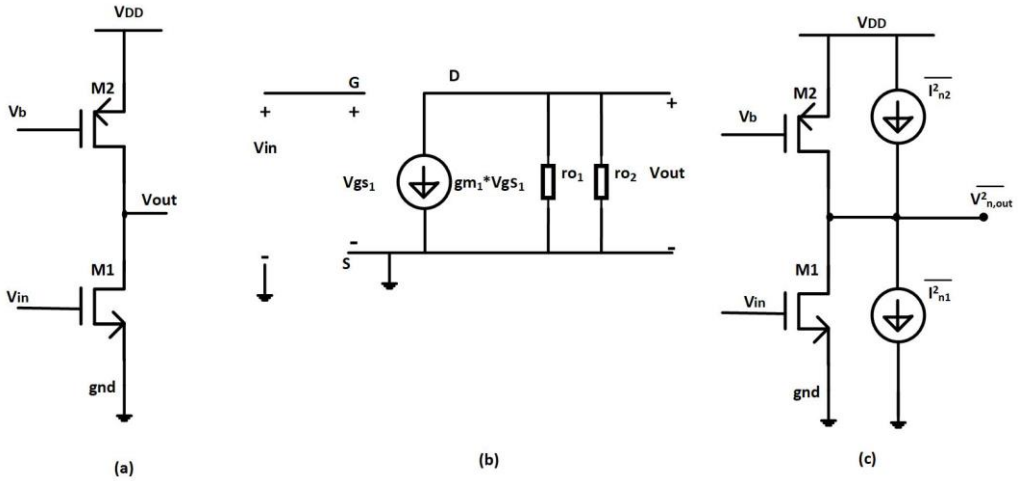


Figure 27 Common source amplifiers having PMOS transistor as the current source load

In a common source amplifier using a PMOS transistor as the current source load, the primary source of noise is the thermal noise generated by the NMOS transistor channel and the PMOS current source load. There is also a flicker noise, but it is dominant at low frequencies only.

Let's consider the thermal noise only,

$$I^2_{ntot} = I^2_{n1} + I^2_{n1} \tag{4.1}$$

$$I^2_{n,tot} = 4kT\gamma(g_{m1} + g_{m2}) \tag{4.2}$$

The output referred noise can be calculated by

$$V^2_{n,out} = I^2_{ntot}.(ro_1||ro_2)^2 \tag{4.3}$$

Or

$$V^2_{n,out} = (4kT\gamma(g_{m1} + g_{m2}))(ro_1||ro_2).^2 \tag{4.4}$$

Total output referred noise in case of thermal noise is given by the following equation.

$$V^2_{n,out,tot} = (4KT\gamma(gm_1 + gm_2))(ro_1||ro_2)^2 \tag{4.5}$$

The following formula can be used for calculating the input referred noise:

$$V^2_{n,inp,tot} = \frac{V^2_{n,out,tot}}{Av^2}$$

$$V^2_{n,inp,tot} = \frac{(4KT\gamma(gm_1 + gm_2))(ro_1||ro_2)^2}{(gm1(ro1||ro2)^2}$$

$$V^2_{n,inp,tot} = 4KT\gamma(\frac{1}{gm_1} + \frac{gm_2}{(gm_1)^2}) \tag{4.6}$$

The above equation (4.6) suggests that for decreasing the input-referred thermal voltage noise, gm_1 needs to be increased and g_{m2} must be decreased since M_2 serves as a current source instead of a transconductor. It might be asked why M_1 and M_2 in figure 27 exhibit different noise effects. Since noise currents of both transistors flow through $r_{o1}||r_{o2}$, why g_{m1} is needed to be maximized while g_{m2} should be minimized? The reason behind is that when g_{m1} increases, the output noise voltage increases in proportion to $\sqrt{g_{m1}}$ however the voltage gain of the stage increases in proportion to g_{m1}. Consequently, the input-referred noise voltage decreases. Such a trend does not apply to M_2. Nevertheless, increasing g_m will increase the power so there is a tradeoff between power and noise. This equation also suggests that devices operating at low temperature exhibit low thermal noise as temperature has a direct relation with the input referred voltage noise [13].

The Signal-Noise ratio for the input is explained by following equation:

$$SNR_{inp} = \frac{V^2{}_{inp}}{4KT\gamma(\frac{1}{gm_1} + \frac{gm_2}{(gm_1)^2})} \tag{4.7}$$

On the other hand, for the output this ratio is obtained via following equation.

$$SNR_{out} = \frac{(Av.V_{inp})^2}{(4KT\gamma(gm_1 + gm_2))(ro_1||ro_2)^2} \tag{4.8}$$

The explanation given above with the help of the equations can help us in sizing the transistors for the comparator in terms of noise. One can easily understand that for getting low input rms referred noise, the g_m of the PMOS needs to be lower while it should be higher for NMOS.

4.7 Important parameters

Various parameters should be taken into account while designing a comparator. These are mentioned below:

4.7.1 Delay

Delay is considered as the most essential parameter in a comparator design. It is generally measured when the clock signal reaches 50% of its rising edge to a point where difference between $V_{out,p}$ and $V_{out,n}$ on the rising edge becomes 50% of V_{dd}. The comparator must complete its signal comparison in one clock cycle and produce a stable output before the next cycle starts. This comparison slows down when the difference between V_{in-p} and V_{in-n} decreases, leading to an increased delay of the comparator. The derivation for calculating such delay in strong-arm latch comparator is explained in [16]. Comparator delay decreases as the common mode voltage increases or the g_m of the transistors increases.

4.7.2 Power consumption

Achieving low power consumption is an essential goal in nearly every electronic design. The strong-arm latched comparator is beneficial in one way that it consumes no static power, assuming the leakage currents are ignored.

Equation 4.10 given below can be used for calculating the average power used from the supply voltage during one comparison cycle:

$$P_{avg} = \frac{1}{\mathrm{T}} \int_0^{\mathrm{T}} V_{DD}.I_D \, \mathrm{dt} \tag{4.9}$$

Here, T symbolizes the period of the clock signal while $\mathrm{I_D}$ indicates overall current drawn from supply voltage. Thus, the above formula can be expressed as follows:

$$P_{avg} = \mathrm{f_{clck}}.V_{DD} \int_0^{\mathrm{T}} \mathrm{I_D} \, \mathrm{dt} \tag{4.10}$$

A more interesting parameter is energy per cycle, which can be computed as

$$\mathrm{E_{cycle}} = \frac{P_{avg}}{\mathrm{f_{clck}}} \tag{4.11}$$

4.7.3 Offset

For a comparator, an input offset voltage is defined as the voltage at which the output undergoes transitions from one logic state to another. Such offset results from the device mismatches, where symmetrical transistors are not completely identical and consequently having slight differences in their threshold voltages. Thus, their behavior differs, resulting in an offset between the input pairs. When the gate voltages of the input transistors become identical, one transistor is inclined to draw somewhat larger current, making its drain node to move more rapidly and generating an incorrect output. Even though other transistors also contribute to the offset, the primary source is the input pairs owing to their higher gain as compared to the other transistors that activate afterward. [13]. To calculate the comparator offset a binary search method was used which is explained in [17]. In another method to measure the offset voltage, you will apply a voltage staircase to the input of the dynamic comparator and the input voltage level that causes the output to change is recorded. This input voltage where comparator output is flipped will be the offset voltage.

4.7.4 Input-referred noise

Similar to offset, the input pair transistors are the major component of the input-referred noise [14]. In order to calculate this noise, we have to determine the output noise and then divide it with the voltage gain,

$$\overline{\mathrm{Vin^2}} = \frac{\overline{\mathrm{Vout^2}}}{\mathrm{A_v}} \tag{4.12}$$

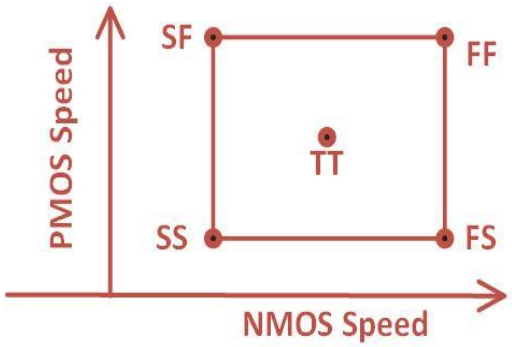
However, we cannot use this formula with a transient simulation since the comparator generates a digital output. An alternative technique used to determine the input-referred noise is based on conducting an extended transient simulation with a steady input. Even though this approach offers better accuracy, it is a very time-taking process, that is why it is usually advised not to be used during optimization. Instead, a more efficient technique involves running a Periodic Steady-State (PSS)+Pnoise simulation

to compute the gain and output-referred noise, followed by estimation of the input-referred noise with the previously mentioned formula in equation (4.12). A thorough explanation of this approach is given in [17].

4.7.5 Process Corners

MOSFET fabrication is not perfect; As a result, parameters undergo changes from one wafer to another, within a single wafer and even across the same chip. Consequently, different chips demonstrate different performance, and it is highly important to take this problem into account to ensure that the yield is acceptable [13].

The rectangle in the following figure shows the speed of PMOS and NMOS. The middle point of the rectangle is TT (typical corner) while the corners indicate various process corners for instance FF (fast-fast), SS (slow-slow), FS (fast-slow) and SF (slow-fast).



It is important to make sure that the transistors on the produced chip fall within the area inside the rectangle. For this, different tests are carried out across different corners to ensure the chip can handle the fabrication variations. Moreover, the chip's testing must also be performed over different temperature ranges and also at different supply voltages, known as PVT (Process-Voltage-Temperature) corners.

4.8 Results

In this section results are presented for the strong-arm latch comparator simulated using 28-nm CMOS technology and are taken from the parasitic extracted view.

4.8.1 Common mode sweep

Comparator is simulated over different common mode voltages to see how change in common mode voltage affects the working of the comparator regarding its offset, noise, delay and power consumption.

4.8.1.1 Delay

The common mode voltage is swept systematically in order to investigate the design response at different inputs. As figure 28 shows that with an increase in the input common mode voltage, the delay decreases. The tail transistor's current substantially affects the delay. As the common-mode voltage increases, the tail current also rises which results in a decrease in delay. A detailed derivation for the calculation of delay is given in [18]. As expected, the ss corner is the worst corner for delay and the ff corner is

the best one. We can also see that the delay is higher at -40°C and lower at 120°C. In terms of supply voltage, it has been observed that as the supply voltage is decreasing the delay has started increasing. Therefore, the delay has an inverse relation with the supply voltage as shown in figure 28(c).

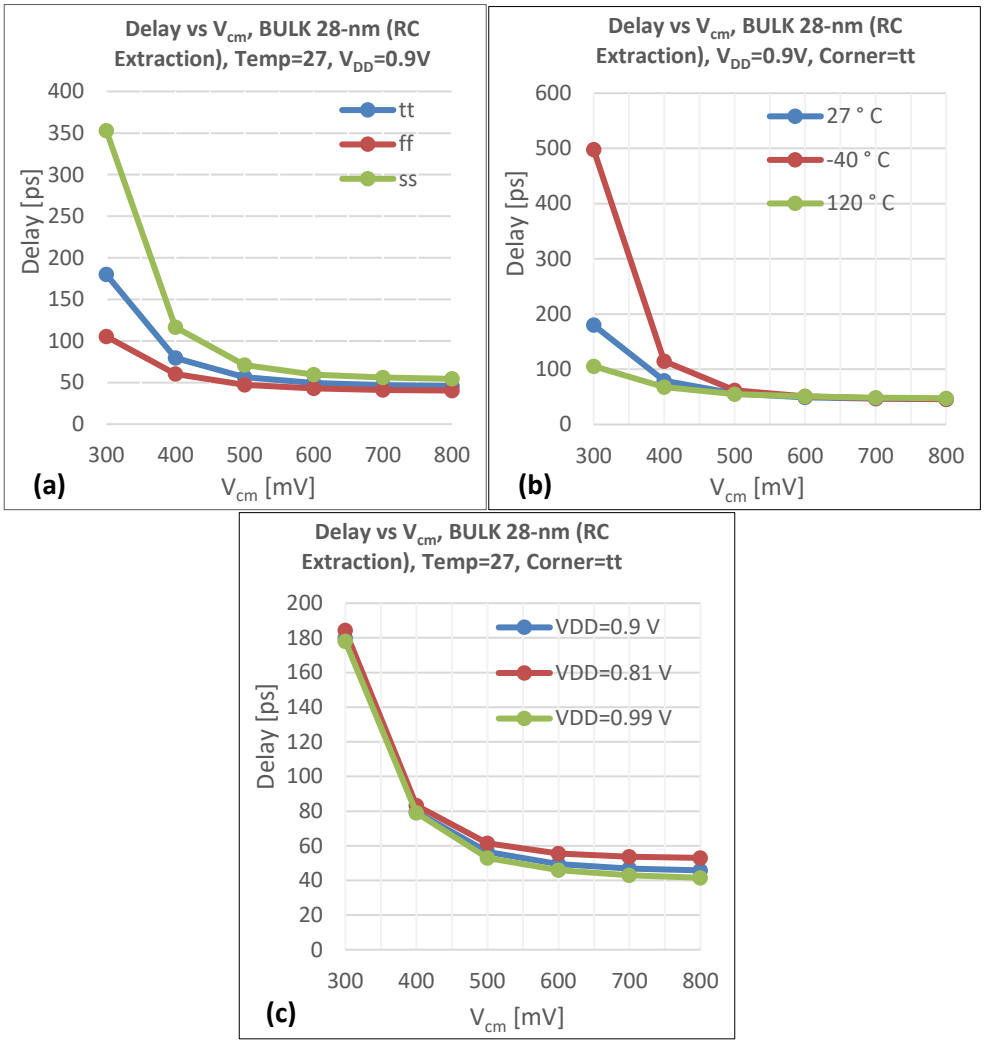


Figure 28 Delay vs Common mode voltage for V_{in}=Offset-Input Referred noise (RMS) and Fclock=1 GHz

Figure 28 shows that a lower common mode voltage implies a higher delay because of the lower tail current. Thus, a very low differential drain current is flowing, and the input transistors takes a longer time to make a comparison between two input voltages to produce an output either 1 or 0. When the common mode voltage starts increasing, the tail current increases as well. An increased tail current leads to a higher differential drain current which means more current is available to charge and discharge the internal nodes. Faster charging and discharging leads to quicker transitions between logic states, thus reducing the comparator delay. It should be noted that the minimum delay is not obtained at $V_{cm} = V_{DD}$. This is because an excessively large V_{cm} prolongs the duration of the latch regeneration phase because of the reduction in gain [19].

4.8.1.2 Energy/Cycle

The comparator power strongly depends on the common mode voltage. As V_{cm} increases, the power consumption increases due to increased short circuit current. Higher V_{cm} results in a higher tail current, leading to larger transistors switching currents leading to a higher power consumption. An interesting term is energy per cycle defined by equation (4.11). The energy per cycle versus common mode voltage over different corners is given below in figure 29(a).

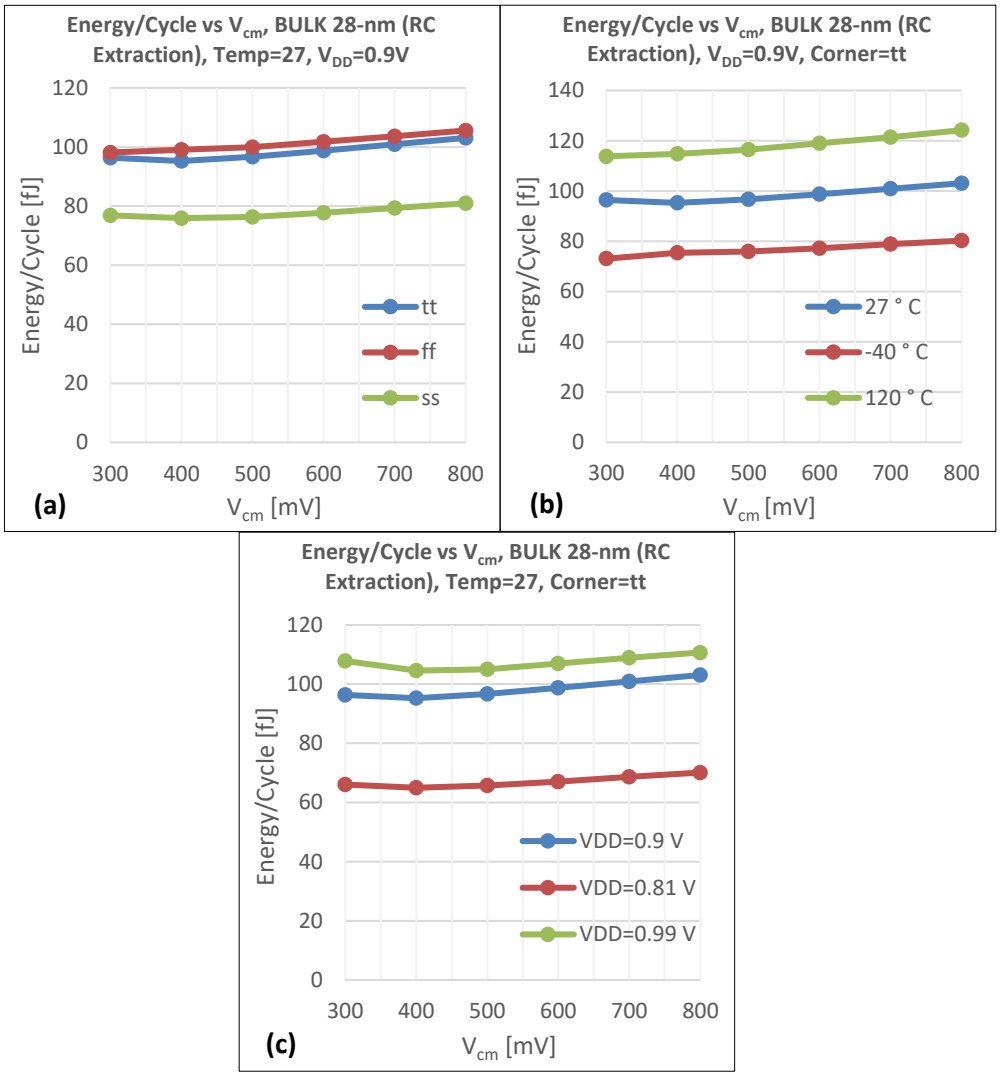


Figure 29 Energy/cycle vs Common mode voltage for V_{in}=Offset-Input Referred noise (RMS) and Fclock=1 GHz

It is observed from the figure 29(a), that the ff corner is the worst and the ss corner is the best one in terms of energy/cycle. The comparator is also simulated for different temperatures as shown in figure 29(b). We can see that the energy/cycle has a direct relationship with temperature with a highest energy/cycle for temp=120°C. The comparator is also simulated for different supply voltages. As expected, the energy/cycle is decreasing with decreasing supply voltage as shown in figure 29(c).

4.8.1.3 Offset

The g_m/I_D of the input transistor is determined by the input common-mode V_{cm} which significantly impacts the gain. A small V_{cm} is preferred for increasing the gain and reducing the offset. The input referred offset can be modeled as $\sigma_{os,\ preamp}$ during the pre-amplification phase, where its major source is $V_{Tn1,2}$ mismatch in the input pair transistors M_1 and M_2. During the latch phase, the initial offset referred to the output nodes can be modeled as $\sigma_{os,latch}$, with $V_{Tp5,6}$ being its major contributor, mismatch in the PMOS cross coupled pair transistors, M_5 and M_6 [19]. Thus, the root-mean-square input referred offset of the whole comparator, σ_{os}, can be denoted by the equation given below (4.13)

$$\sigma_{os} = \sqrt{\sigma_{os,pre\ amp}{}^2 + \frac{\sigma_{os,latch}{}^2}{G^2}} \tag{4.13}$$

This offset highly depends on the gain of the differential input pair, referred to as the pre-amplification gain. As the common mode voltage increases, the gain of the input pair transistor decreases, leading to an increase in the offset which is also seen in the figure 30 below.

Comparator is simulated for different corners, different temperatures and at different supply voltages to see how the offset is changing under different operating conditions. It has been observed that comparator has lowest offset at ss corner and offset is maximum for ff corner as shown in figure 30(a). Temperature variation also effects the offset of a comparator as in figure 30(b). It is also observed that variation in supply voltages around ±10% does not affect the comparator offset a lot as shown in figure 30(c).

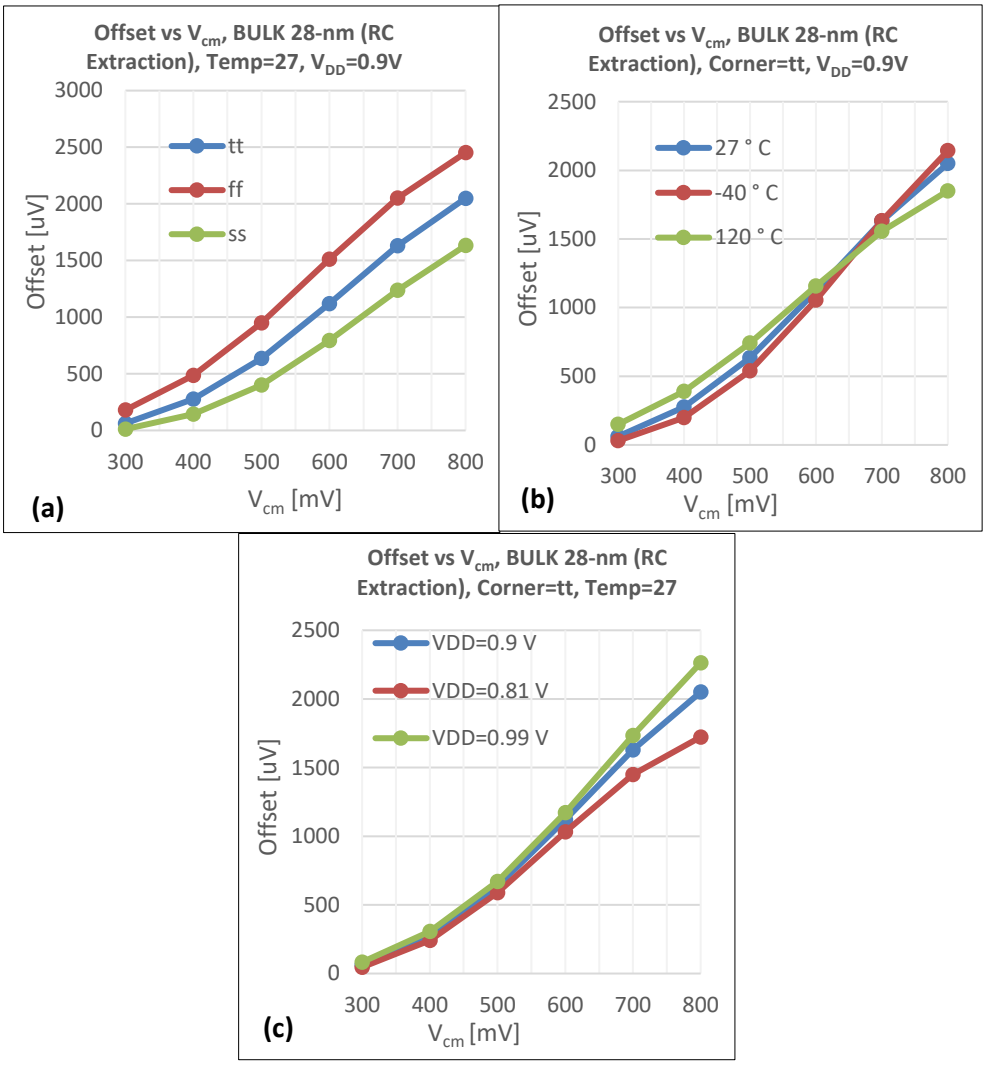


Figure 30 Offset vs Common mode voltage

4.8.1.4 Input referred noise

As explained in the given equation (4.14) the gain and the input referred noise of the comparator have an inverse relationship with each other. If common mode voltage increases gain declines so if the gain is decreasing the input referred noise will increase [19].

$$\sigma_n = \sqrt{{\sigma_{n,\text{pre amp}}}^2 + \frac{{\sigma_{n,\text{latch}}}^2}{G^2}} \tag{4.14}$$

Figure 31 illustrates the impact of the common mode voltage on the input referred noise.

A comparator is simulated across various process corners, different temperatures and at different supply voltages to see how the input referred noise is changing under different operating conditions. It has been observed that comparator has lowest input referred noise at ss corner and it is maximum for ff corner as shown in figure 31(a).

Temperature variation also strongly affects the comparator noise that can be seen in figure 31(b). Moreover, it is observed that variation in supply voltages around ±10% also significantly affect the comparator noise as shown in figure 31(c).

While a small common mode voltage is ideal for achieving lower offset, small noise and reduced power consumption, it results in slower speed. This shows the trade off in choosing the optimal common mode voltage.

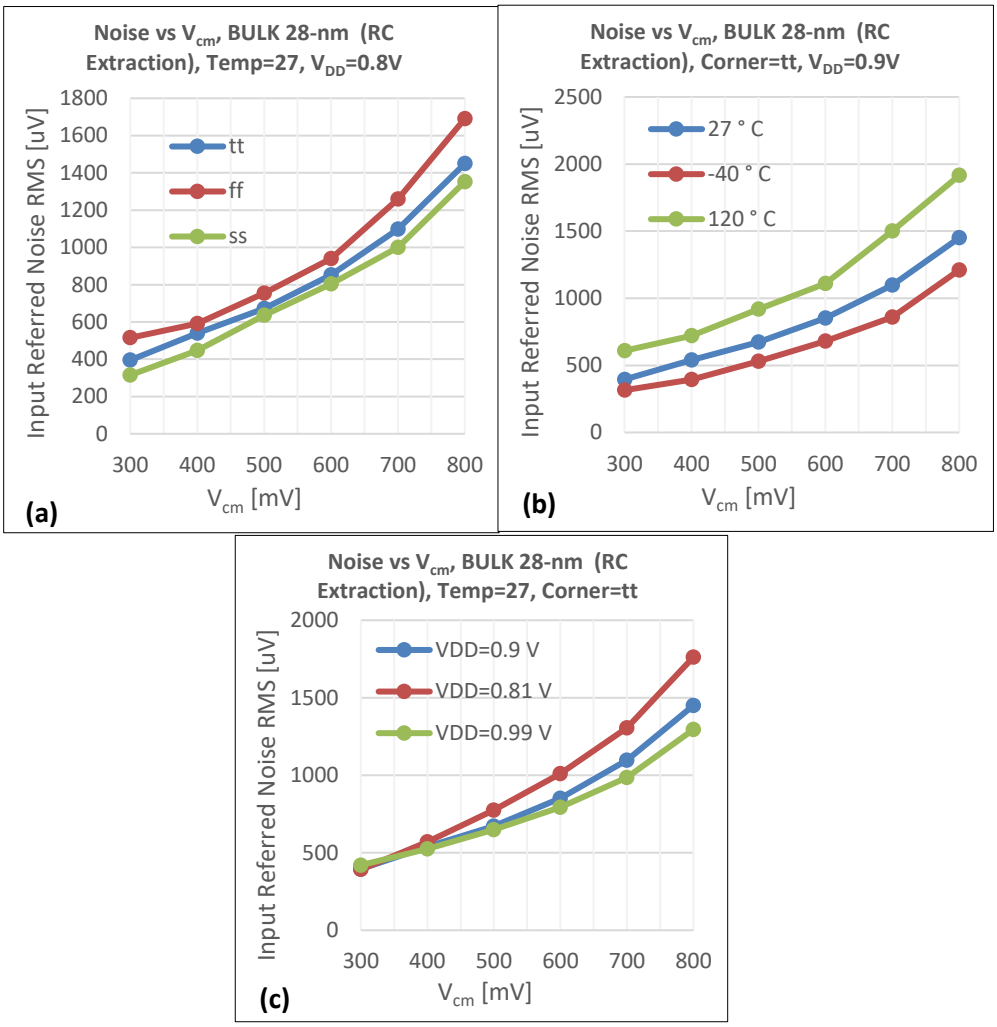


Figure 31 Input referred noise versus common mode voltage

4.8.1.5 Figure-of-Merit (FOM)

In order to evaluate the comparator performance comprehensively, a figure-of-merit is defined [20] which considers noise, delay and energy/cycle. The optimum figure of merit is obtained around V_{cm} =0.4 V which is more than 8 times better than at V_{cm}=0.9 V. This suggests that at this 0.4 V, the comparator finds an optimal balance between noise, speed and power consumption.

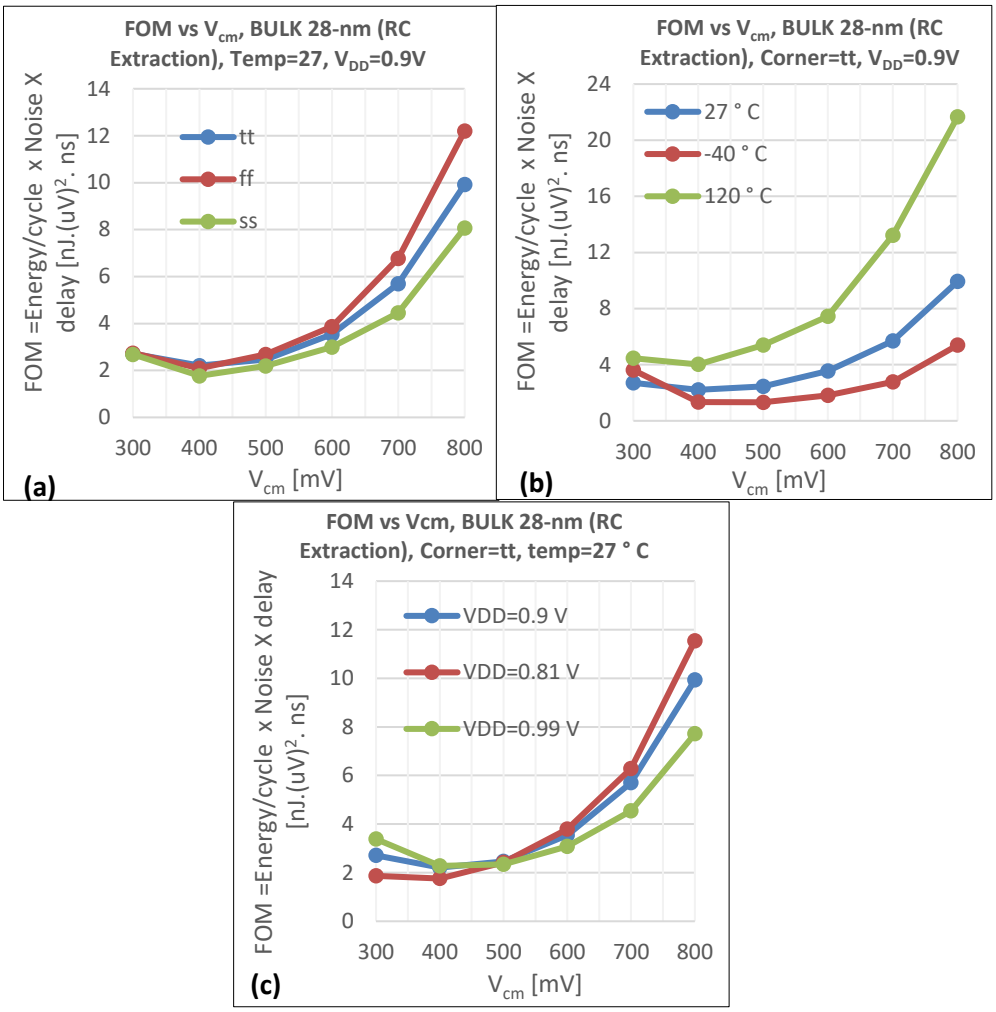


Figure 32 Figure of merit vs Common mode voltage

4.8.2 Differential mode sweep

It is interesting to see how the strong-arm latch comparator behaves with respect to delay and power or energy/cycle over different corners, when we are sweeping the differential input voltage. The results for 28-nm CMOS BULK technology are explained below.

4.8.2.1 Delay

As expected, the delay of the strong-arm latch comparator is decreasing when we are increasing the input differential voltage. The simulations are done over different corners, and we can see that the ss corner is the worst corner in terms of delay and the ff corner is best one for delay. The comparator is also simulated over different temperatures. Figure 33(b) shows that temperature has an inverse effect on the delay of comparator. It means as the temperature is decreasing the delay is increasing. It is also evident that the delay is increasing as the supply voltage decreases as shown in figure 33(c).

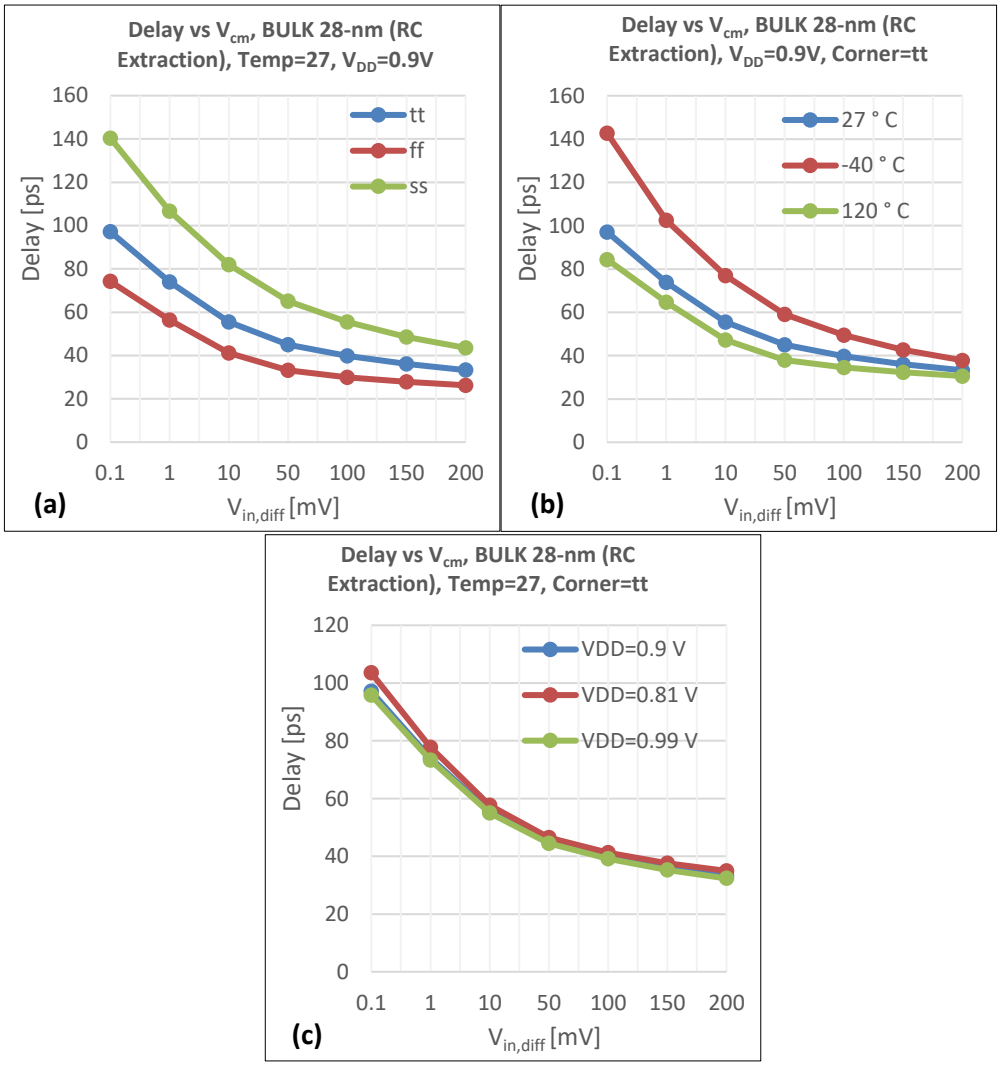


Figure 33 Delay vs differential input voltage at Vcm=0.4 V and Fclock=1 GHz

4.8.2.2 Energy/cycle

For a strong-arm latch comparator, the power consumption is decreasing with increasing differential input voltage. As expected, the ss corner is the best corner for the power consumption while the ff corner is the worst one. The comparator is also simulated for different temperatures as shown in Figure 34(b). The energy/cycle has a direct relationship with temperature and for temp=120°C the comparator has higher energy/cycle. The comparator is also simulated for different supply voltages. As expected, the energy/cycle is decreasing with decreasing supply voltage as shown in Figure 34(c).

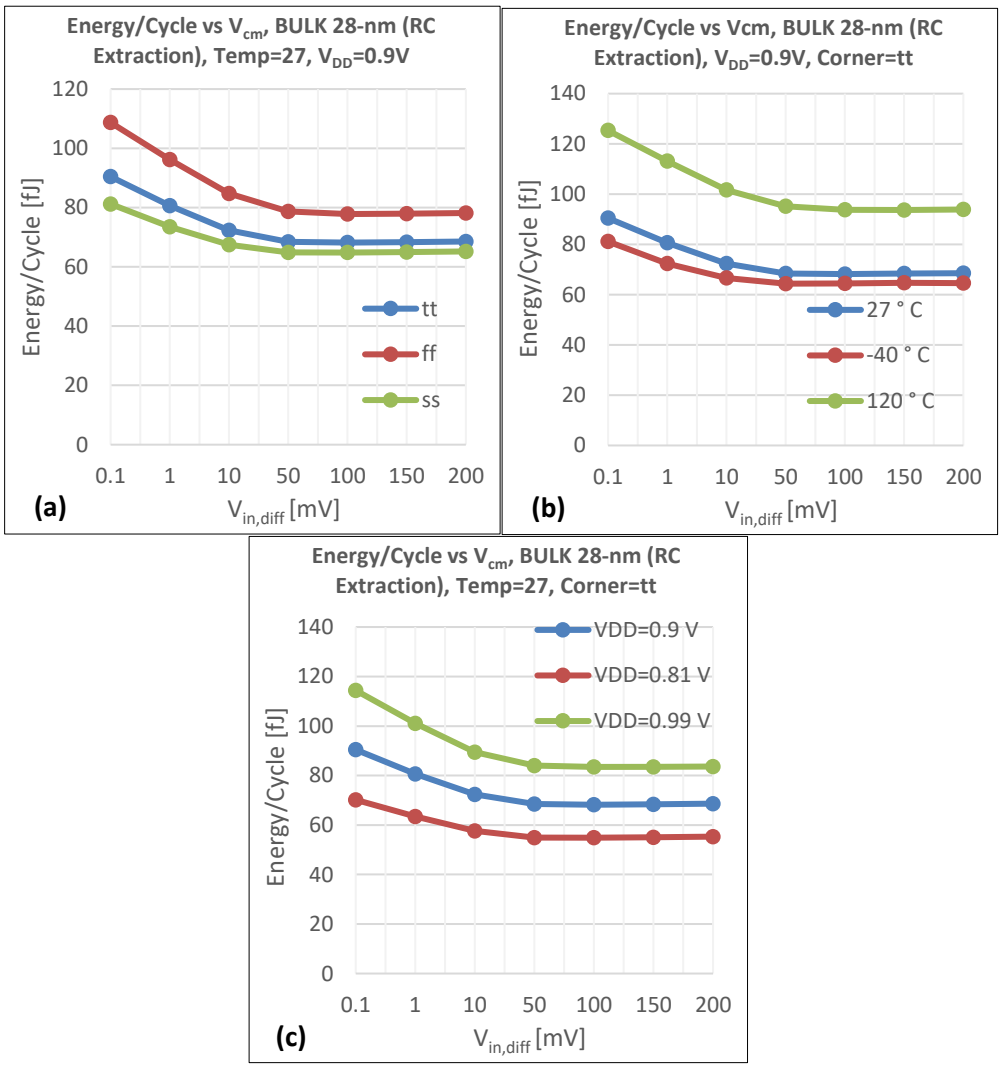


Figure 34 Energy/cycle vs differential input voltage for Vcm=0.4 V and Fclock=1 GHz

Chapter 5: Porting comparator to 22-nm CMOS FDSOI

The Strong-Arm latch comparator, originally designed in 28-nm CMOS bulk technology, was ported to 22-nm CMOS FD-SOI technology. During this process, key design parameters were adjusted to ensure a fair and accurate comparison between the two technology nodes.

5.1. Technology Scaling

The original comparator in 28-nm technology utilized the minimum channel length of 30-nm. In the 22-nm FD-SOI process, this length was reduced to 20-nm, representing a approximately 30% decrease in length as compared to 28-nm BULK. To maintain consistency and fairness in the comparison, the transistor widths were also scaled down by 30%. For example, if the width in the 28-nm design was W_{28} the width in the 22-nm FD-SOI design was adjusted to $W_{22} = 0.7^* W_{28}$.

5.2. Floor Plan Considerations for Layout

The layout design in 22-nm FD-SOI technology retained the same floor plan as used in the 28-nm CMOS bulk design. This approach ensures that any differences in performance are due to the technology change itself rather than variations in the physical layout, which could introduce additional parasitic effects.

5.3 Results:

5.3.1 Common mode sweep

Comparator is simulated over different common mode voltages to see how change in common mode voltage affects the performance of the Comparator in terms of offset, noise, delay and power consumption.

5.3.1.1 Delay

The comparator was simulated across various process corners, temperatures, and supply voltages to analyze how these factors influence the delay as shown in figure 35.

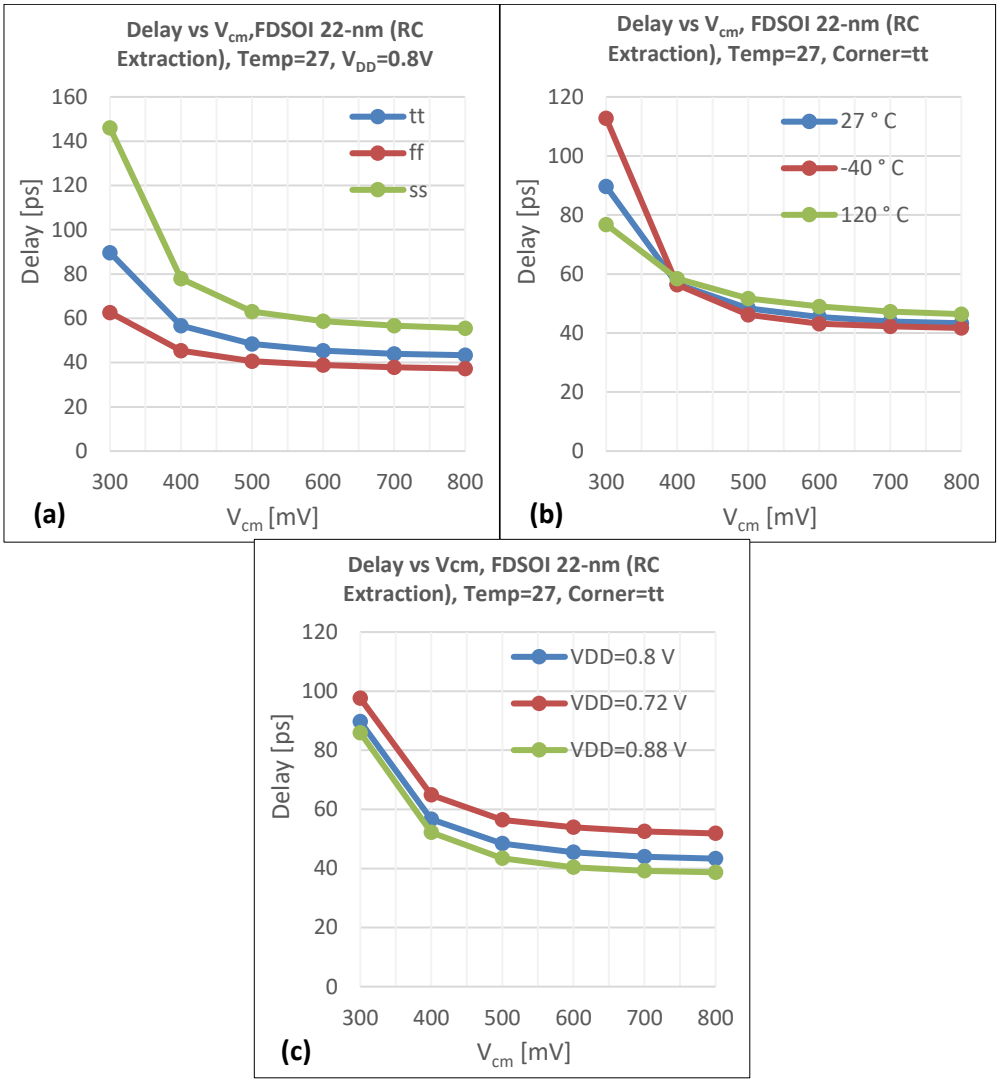


Figure 35 Delay vs Common mode voltage for Vin=Offset-Input Referred noise (RMS) and Fclock=1 GHz

As expected ss corner is the worst corner for delay, and ff corner is the best one. In terms of supply voltage as the supply voltage is decreasing the delay has started increasing. An interesting thing has been observed when comparator was simulated for different temperatures. At lower common mode voltage delay was higher for -40 ° C and it was lower at 120 ° C. When common mode voltage is greater than 0.4 V this trend has flipped and -40 ° C becomes better temperature for delay than 120 ° C as shown in figure 35(b).

5.3.1.2 Energy/Cycle

The comparator was simulated across various process corners, temperatures, and supply voltages to analyze how these factors influence the energy/cycle as shown in figure 36.

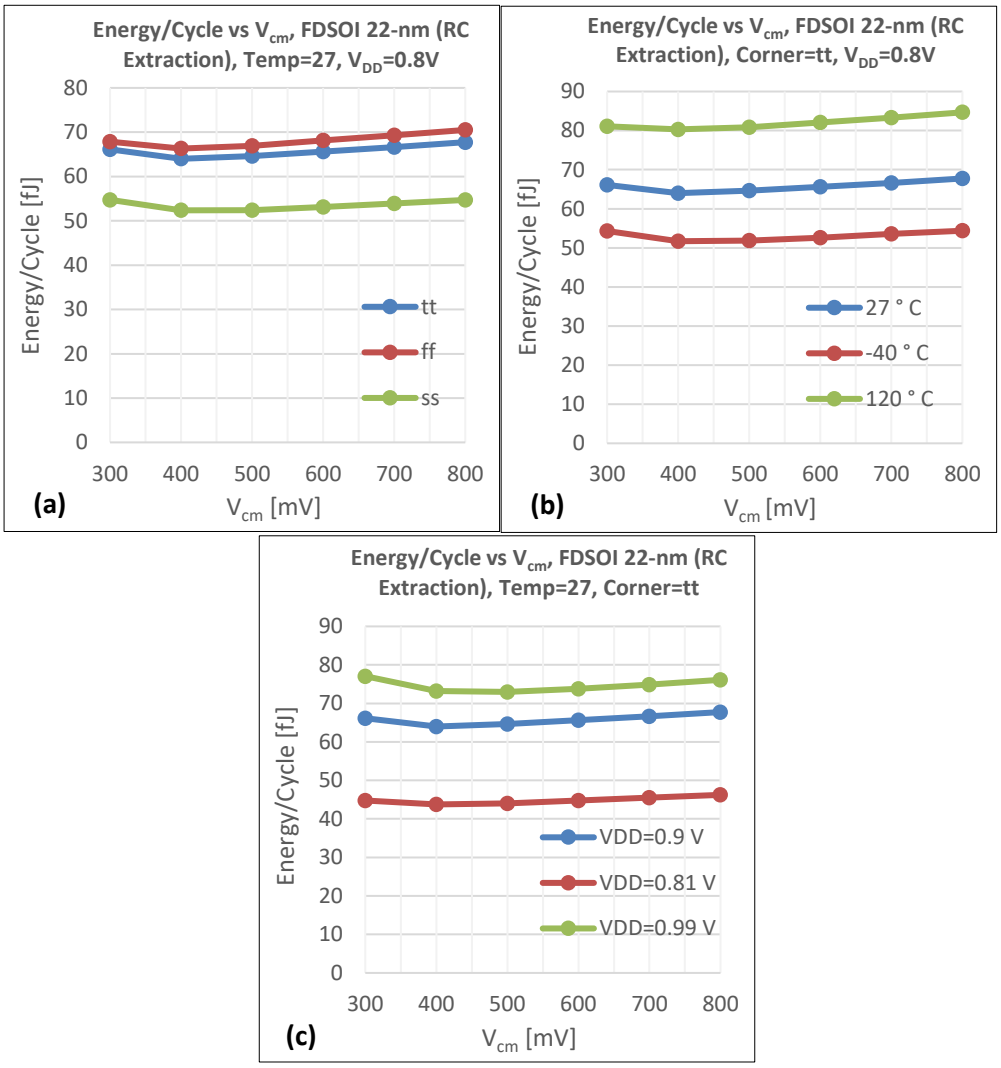


Figure 36 Energy/Cycle vs Common mode voltage for Vin=Offset-Input Referred noise (RMS) and Fclock=1 GHz

It is observed from the figure 36(a), that the ff corner is the worst and the ss corner is the best one in terms of energy/cycle. The comparator is also simulated for different temperatures as shown in figure 36(b). We can see that the energy/cycle has a direct relationship with temperature with a highest energy/cycle for temp=120°C. The comparator is also simulated for different supply voltages. As expected, the energy/cycle is decreasing with decreasing supply voltage as shown in figure 36(c).

5.3.1.3 Offset

The comparator was simulated across various process corners, temperatures, and supply voltages to analyze how these factors influence the comparator offset as shown in figure 37.

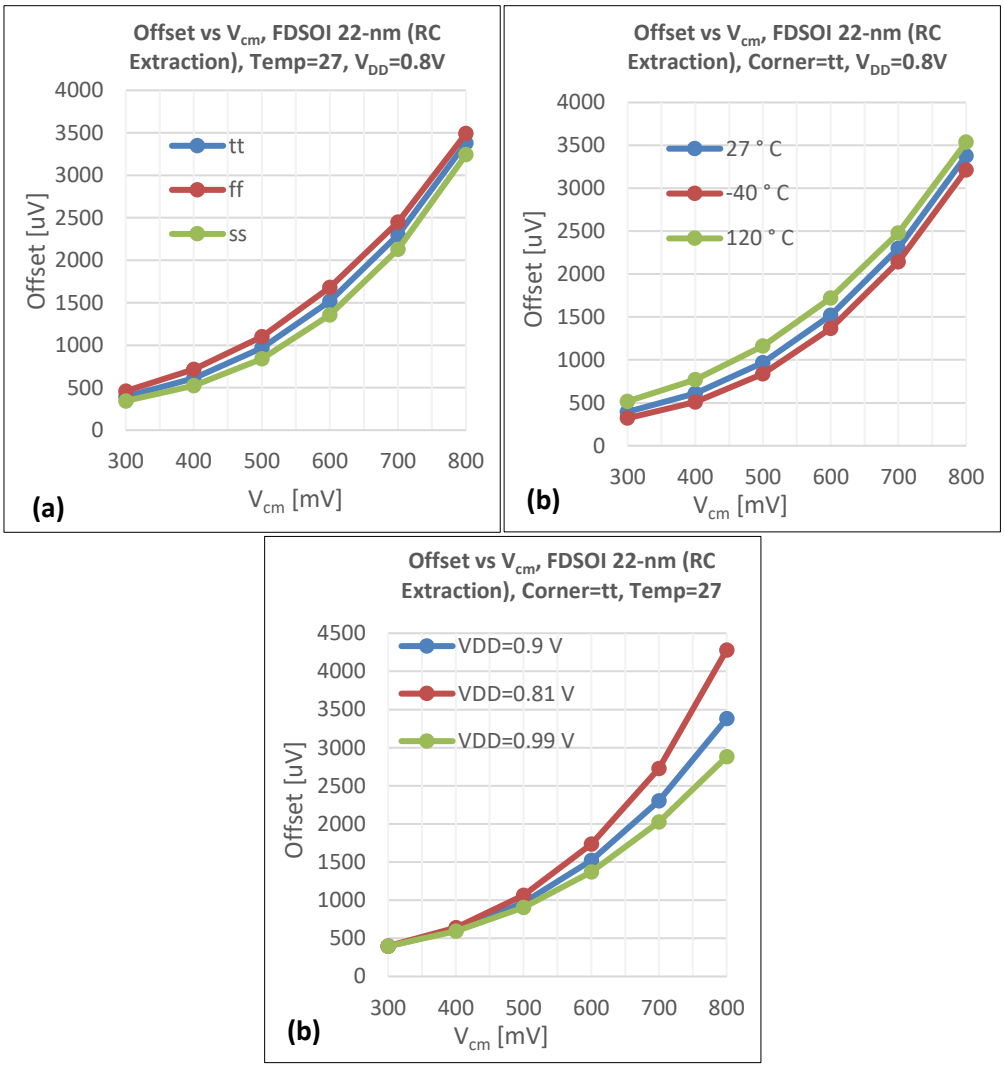


Figure 37 Offset vs Common mode voltage

5.3.1.4 Input Referred Noise

The comparator was simulated across various process corners, temperatures, and supply voltages to analyze how these factors influence the comparator noise as shown in figure 38.

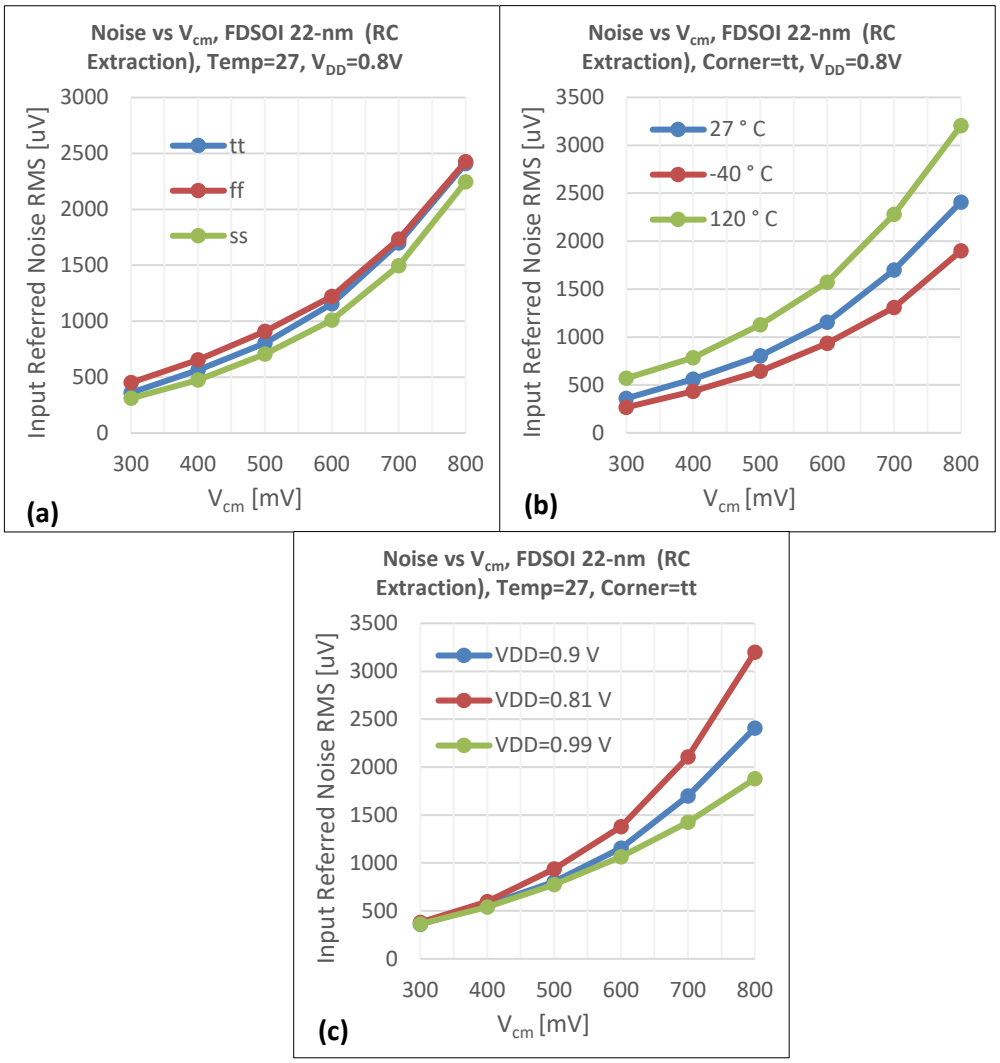


Figure 38 Input Referred Noise (RMS) vs Common mode voltage

5.3.1.5 Figure-of-Merit (FOM)

A figure-of-merit is defined for evaluating the comparator performance comprehensively [20] which considers noise, delay and energy/cycle. It has been observed that lower the common mode voltage, better are figure of merits as shown in figure 39.

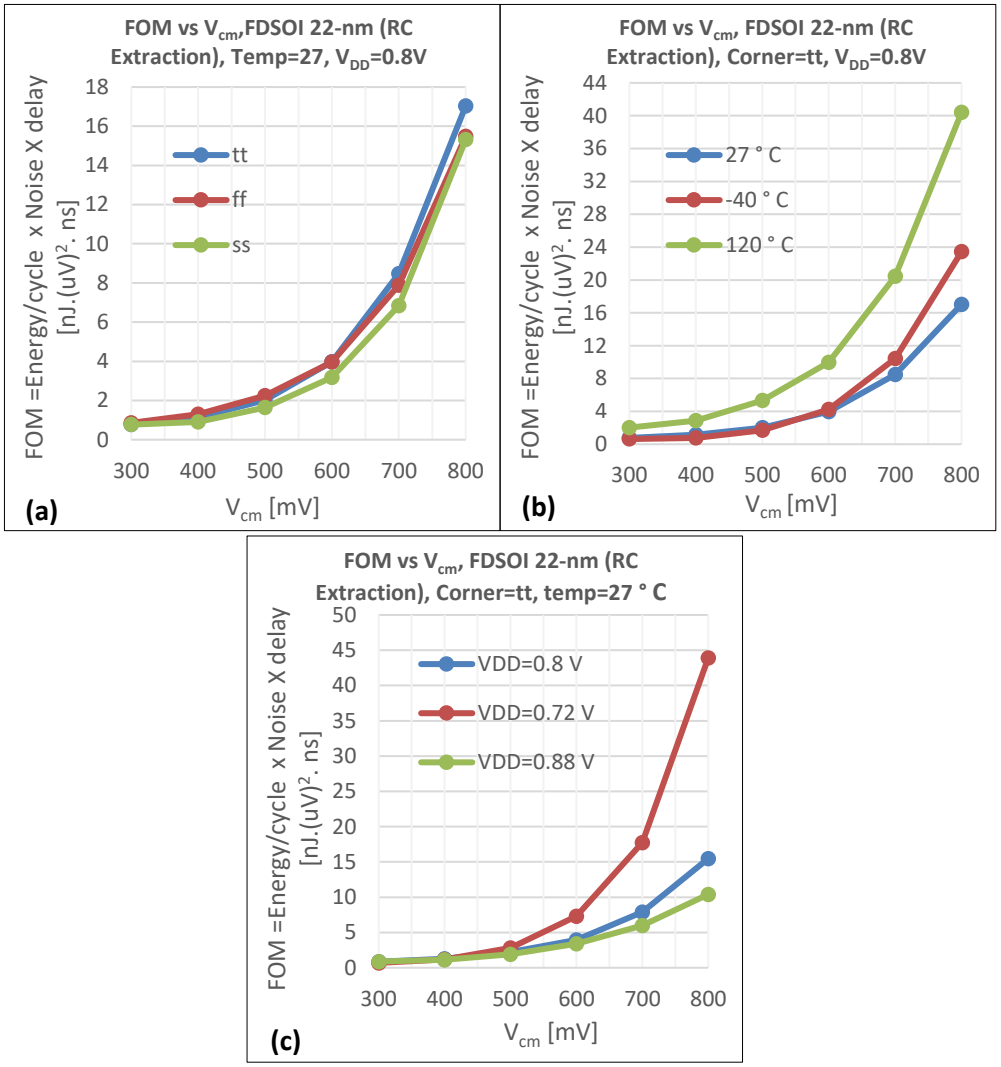


Figure 39 Figure of merit vs Common mode voltage

5.3.2 Differential mode sweep

It is interesting to see how the strong-arm latch comparator behaves with respect to delay and power or energy/cycle over different corners, when we are sweeping the differential input voltage.

5.3.2.1 Delay

The comparator was simulated across various process corners, temperatures, and supply voltages to analyze how these factors influence the comparator delay as shown in figure 40.

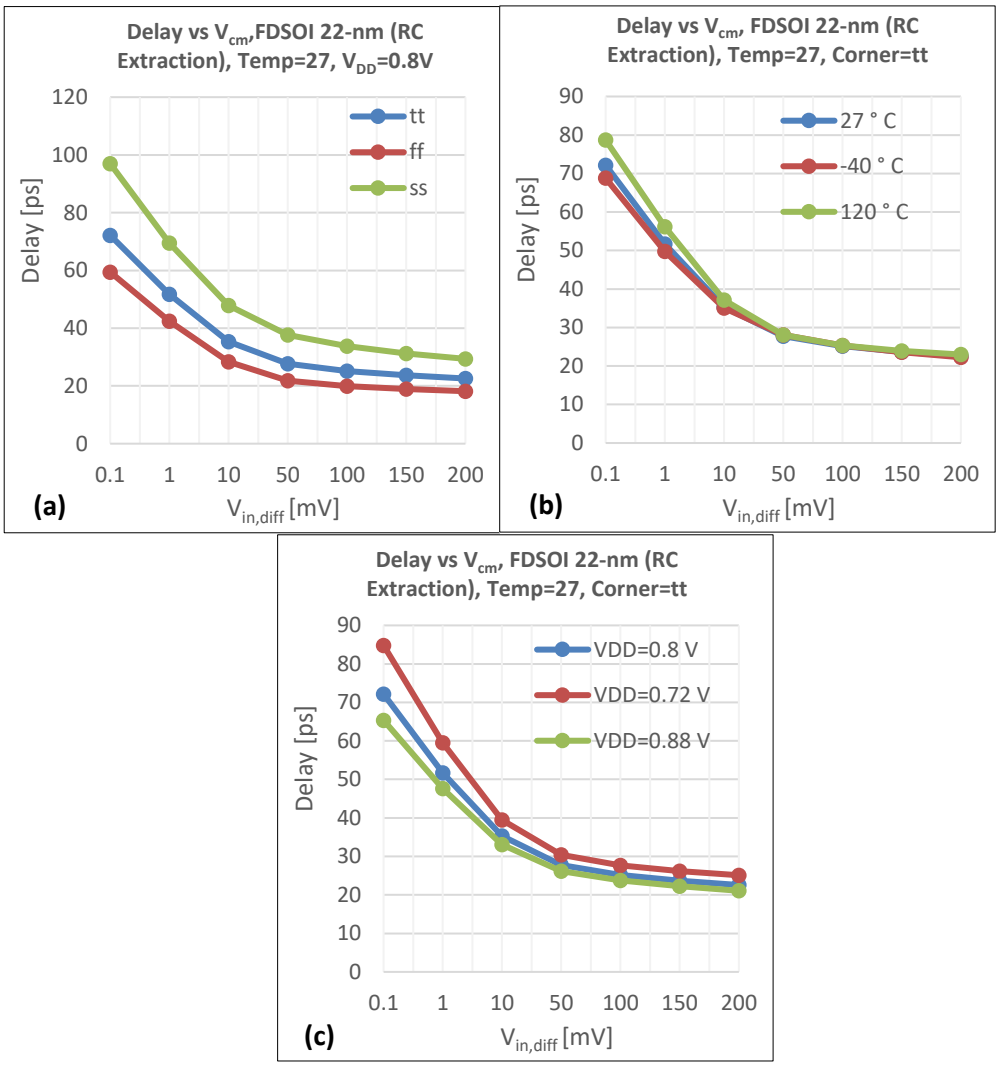


Figure 40 Delay vs differential input voltage at Vcm=0.4 V and Fclock=1 GHz

5.3.2.2 Energy/Cycle

The comparator was simulated across various process corners, temperatures, and supply voltages to analyze how these factors influence the comparator energy/cycle as shown in figure 40.

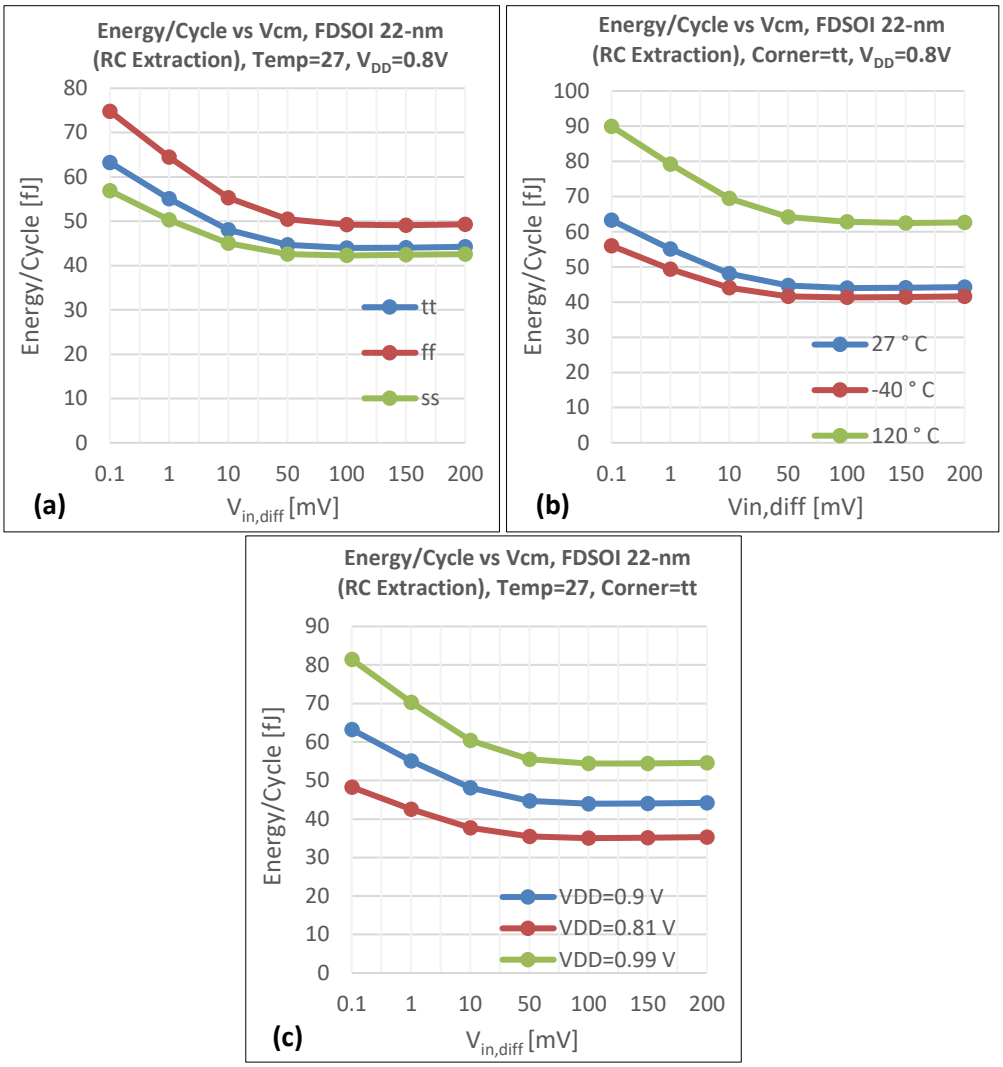


Figure 41 Energy/Cycle vs differential input voltage at Vcm=0.4 V and Fclock=1 GHz

5.4 Comparison between 28-nm BULK and 22-nm FDSOI technology

To make a comparison between 28-nm BULK and 22-nm FDSOI technology, figure of merits was calculated which takes noise, energy/cycle and delay into account. Figure of merits are calculated for different corners, supply voltages and temperatures to see how these parameters affect the performance of strong-arm latch comparator.

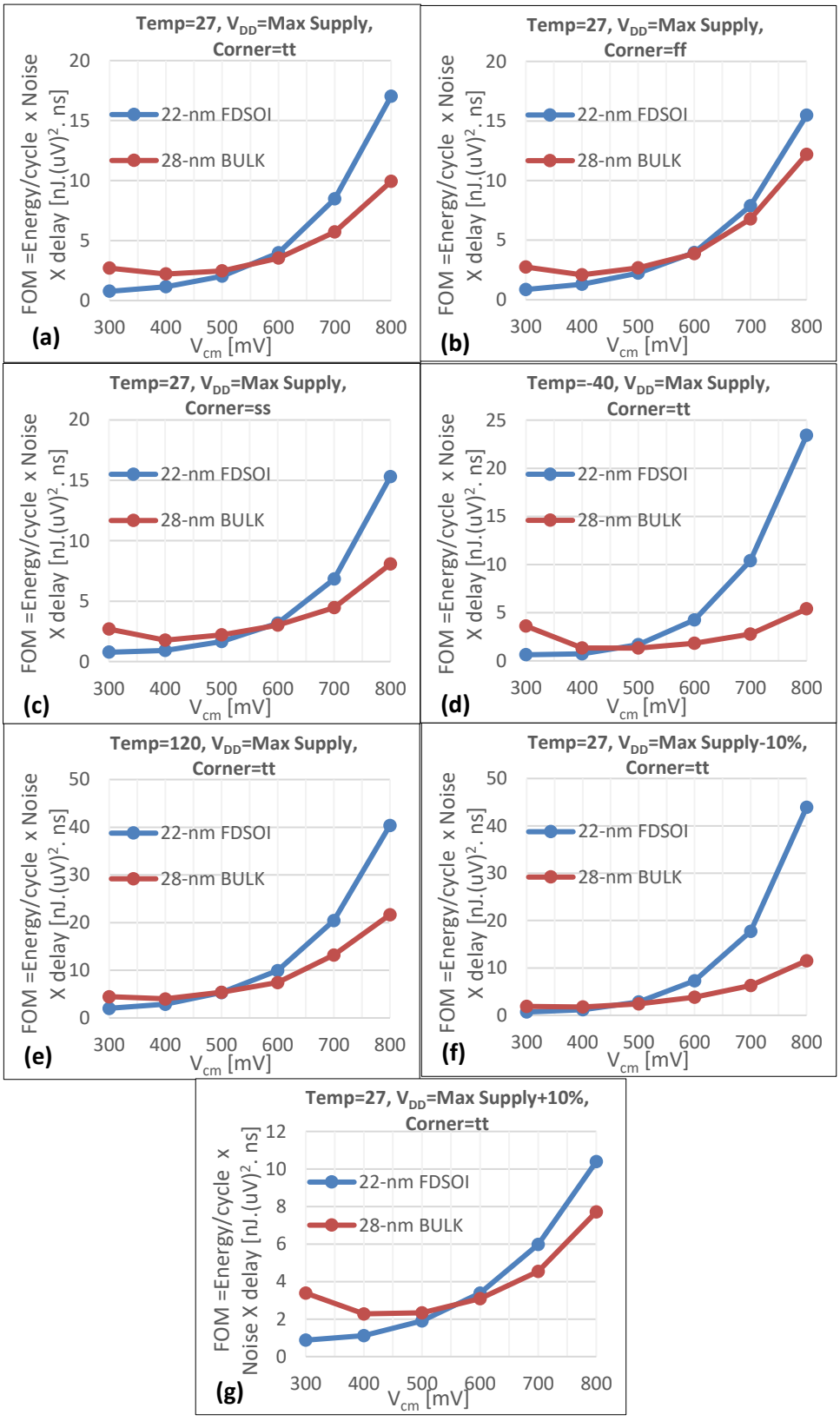


Figure 42 Comparison between 28-nm BULK and 22-nm FDSOI technology

5.5 Comparison between different comparators

To compare our strong-arm latch comparator with other comparators, a Figure of merit method proposed by Harijot in [20] was used which considers noise, energy/cycle and delay.

				Low Power Comparators			High-Speed Comparators		
parameters	This work		Bindra ISSCC [20]	Elzakker JSSC [21]	Dynamic Bias JSSC [22]	Inverter amplifier comparator [23]	Schinkel ISSCC [24]	Ramkaj ISSCC [25]	Goll ISSCC [26]
CMOS tech. [nm]	28	22	22	65	65	180	90	28	65
VDD [V]	0.9	0.8	0.8	1.2	1.2	1.2	1.2	1	1.2
Measured noise, $\sigma_{v,rms}$(mV) @Vcm=VDD/2	0.630	0.56	0.174	0.45	0.4	0.046	1.5	1.1	4.5
Energy/cycle [fJ]	95.39	64.30	75	88	34	1100	110	163	185
F_{clock} [GHz]	1	1	1	0.050	0.050	Not mentioned	1	13.5	5
Delay [ns] , Vin,diff ≈$\sigma_{v,rms}$@Vcm=VDD/2	0.064	0.056	0.28	0.68	1.2	18	0.1	0.035	0.06
FOM =Energy/cycle X Noise X delay [nJ.$(uV)^2$.ns]	2.42	1.1	0.6	12.1	6.5	42	24.7	7	224

Table 1 comparison between state-of-the-art comparators

5.6 Conclusion

From the figure of merit calculation and benchmarking the designed comparator with different state of the art comparators, we can conclude that the strong-arm latch comparator is still a valid choice for GS/s Time-Interleaved SAR ADCs. One major advantage of the strong-arm latch comparator is that unlike other comparators, it does not consume static power and is thus suitable to be used as a fast, low power comparator for Time-Interleaved SAR ADCs with low to medium resolution ranging from 6 to 10 bits for moderate noise performance.

Chapter 6: Conclusion and future work

The 22-nm FD-SOI technology is better than the 28-nm Bulk technology in terms of gain and gain bandwidth product as we have seen in chapter 3 for a single transistor. Based on the simulations conducted on the strong-arm latch comparator in chapter no 4 and 5 across two different technologies 28-nm Bulk and 22-nm FD-SOI, the results clearly indicate that 22-nm FD-SOI technology is better than 28-nm Bulk technology in terms of both speed and power efficiency. Specifically, the figure of merit (FOM), which incorporates comparator noise, energy per cycle, and speed, demonstrates that the 22-nm FD-SOI technology is superior, particularly at low common mode voltages. This performance advantage is likely attributed to the inherent benefits of FD-SOI technology, including reduced parasitic capacitance and enhanced electrostatic control, leading to improved overall efficiency. FD-SOI technology typically exhibits lower leakage currents due to the presence of a thin buried oxide layer, leading to improved power efficiency. FD-SOI offers a steeper subthreshold slope, which results in better performance at reduced operating voltages. FD-SOI's ability to implement body biasing enables dynamic adjustment of the transistor threshold voltage, providing opportunities to optimize the performance-power trade-off. Therefore, it can be concluded that for applications requiring high-speed and low-power comparators, 22-nm FD-SOI technology offers significant advantages over the traditional 28-nm Bulk technology.

For future work, one potential avenue is to run an optimizer to further enhance the performance of the comparator. This optimization process could involve fine-tuning design parameters, such as transistor sizing, biasing conditions, and layout considerations, to achieve an even better trade-off between speed, power consumption, and noise performance. By refining these parameters, the comparator's efficiency and robustness can be maximized, making it more suitable for demanding applications.

Following the optimization, the next logical step would be to prepare for a tape-out.

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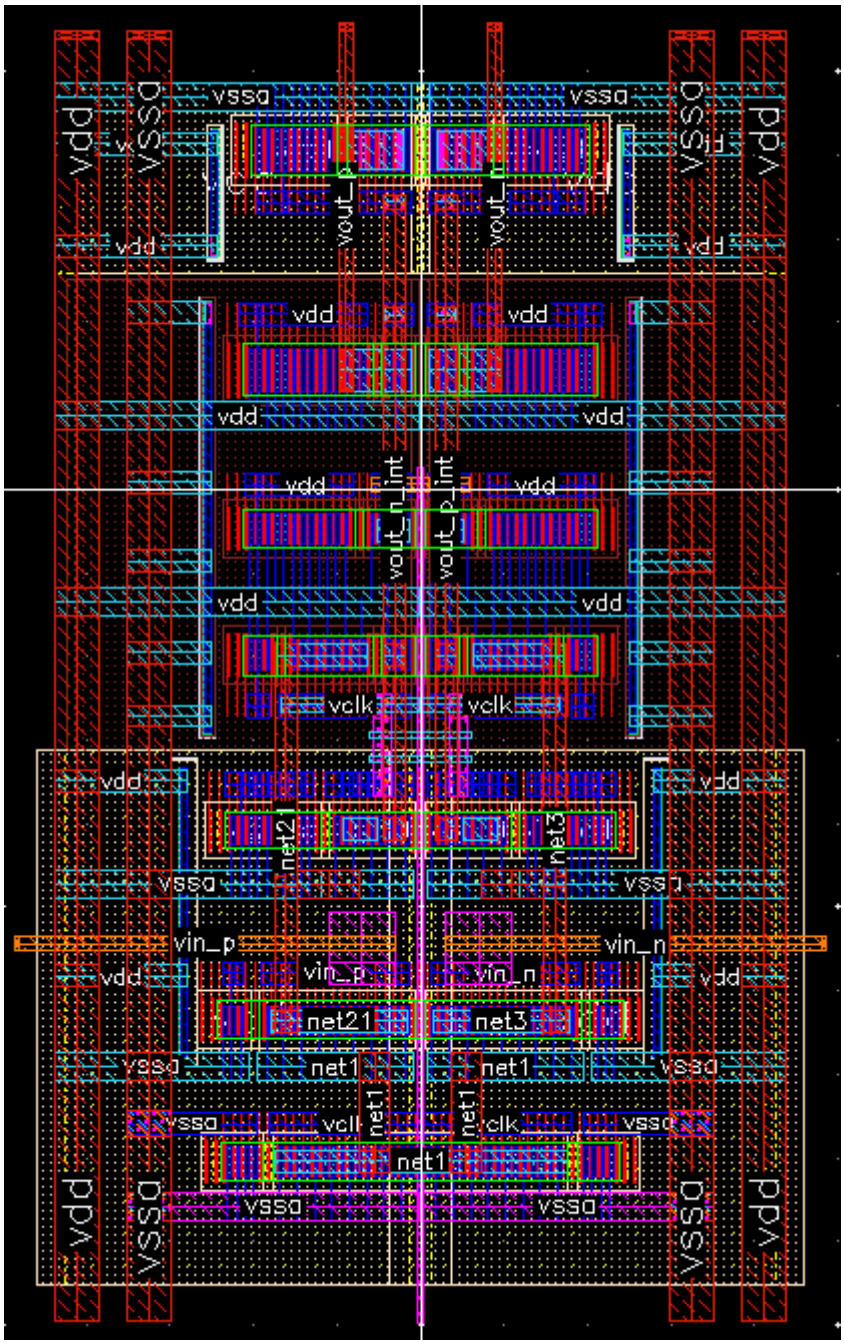
Appendix: Comparator layout



Appendix: MATLAB Model Code

First part of this code models ideal 4 channel Time interleave ADC!

Later on we introduce some offset error, gain error and skew mismatch to see how they effect the ideal 4 channel TI ADC performance!

```
clear all;

clc;

Fs=100e9; %sampling frequency

Ts=1/Fs;  %sampling time

LFFT=100; %number of FFT points!

Tmax = (LFFT-1)*Ts;

t=0:Ts:Tmax; % time vector

M=1; %First Bin.

%Fsig=1e9;

Fsig=M*(Fs/LFFT); %signal frequency

fbin=Fs/LFFT; %bins frequency
```

This corresponds to the frequencies represented by each bin in single sided spectrum.

```
freq = fbin*(0:1:LFFT/2);
```

Enable following lines to disable error due to input offset error

```
% VOS1 = 0;

% VOS2 = 0;

% VOS3 = 0;

% VOS4 = 0;
```

Enable following lines to enable error due to input offset error

```
 VOS1 = 0.023;

 VOS2 = -0.041;

 VOS3 = 0.015;

 VOS4 = -0.032;
```

Enable following lines to disable gain mismatch

```
A1 = 1;

A2 = 1;

A3 = 1;

A4 = 1;
```

Enable following lines to introduce gain mismatch

```
% A1 = 1.04;

% A2 = 0.98;

% A3 = 1.0;

% A4 = 1.009;
```

Enable following line to disable timing mismatch

```
dTS1 = 0;

dTS2 = 0;

dTS3 = 0;

dTS4 = 0;
```

Enable following line to enable timing mismatch

```
% dTS1 = -1.297e-12;

% dTS2 = -1.897e-12;

% dTS3 = 1.497e-12;

% dTS4 = -1.497e-12;
```

These below lines create time vector for each of the four interleave ADCs. Each starts at a different point in the sampling period to simulate time interleaving sampling.

```
t1 = 0:4*Ts:Tmax-3*Ts;

t2 = Ts:4*Ts:Tmax-2*Ts;

t3 = 2*Ts:4*Ts:Tmax-Ts;

t4 = 3*Ts:4*Ts:Tmax;
```

This line generates the input signal (sine wave) with amplitude 1. which is an ideal signal.

```
V_ideal = sin(2*pi*Fsig*t);
```

v1 simulates the output of the first ADC channel, applying gain, time skew and offset to the input signal . similar expressions apply for v2,v3,v4 which are representing other ADC channels.

```
v1 = A1*sin(2*pi*Fsig*(t1+dTS1))+VOS1;

v2 = A2*sin(2*pi*Fsig*(t2+dTS2))+VOS2;

v3 = A3*sin(2*pi*Fsig*(t3+dTS3))+VOS3;

v4 = A4*sin(2*pi*Fsig*(t4+dTS4))+VOS4;
```

This line reshapes the outputs from the 4 Channel ADC into a single vector. It interleaves the samples from each channel, mimicking the operation of a Time Interleave ADC.

```
V_TI=reshape([v1;v2;v3;v4], 1,LFFT);
```

This operation here performs FFT of ideal signal and interleave signal to convert it from time domain to frequency domain and then do normalization by making the signal independent of number of FFT points!

```
fft2_ideal = fft(V_ideal)/LFFT;

fft2_TI = fft(V_TI)/LFFT;
```

This operation takes the first half of the FFT result, which is all you need due to the symmetric nature of the FFT of real signal.

```
fft1_ideal = fft2_ideal(1:(LFFT/2)+1);

fft1_TI = fft2_TI(1:(LFFT/2)+1);
```

The below operation doubles the amplitude of the frequencies excluding the DC and Fs/2 frequency in the single sided spectrum! this step compensate for the loss in the two sided spectrum! since fft result is symmetric the energy of each frequency component is spread accross both negative and positive frequencies! By doubling the ampliude of positive frequencies we effectively account for this energy and obtain a correct magnitude for each frequency component!

```
fft1_ideal(2:end-1) = 2*fft1_ideal(2:end-1);

fft1_TI(2:end-1) = 2*fft1_TI(2:end-1);
```

This operation is performed to get a value in dB

```
fft1dB_ideal = 20*log10(abs(fft1_ideal));

fft1dB_TI = 20*log10(abs(fft1_TI));
```

This line calculates which index (position) in your FFT result corresponds to the frequecy of your input signal.

```
% signal_index=round(M+1);
```

Signal power is calculated based on the single sided FFT.

```
 Signal_power_TI= abs(fft1_TI(M+1))^2;
% Signal_power_ideal= abs(fft1_ideal(M+1))^2;
```

This line calculates the total power of all frequencies in the output signal excluding the DC component which is at index 1. It does this by squaring magnitude of each frequency component (to get power) and summing these values up.

```
Total_power_TI= sum(abs(fft1_TI(2:end)).^2);
% Total_power_Ideal= sum(abs(fft1_ideal(2:end)).^2);
```

Total noise in case of ideal and interleave signal is calculated below to get a SNDR value later on.

```
Total_Noise_TI= Total_power_TI-Signal_power_TI;
 % Total_Noise_Ideal= Total_power_Ideal-Signal_power_ideal;
```

Signal to noise and distortion ratio is calculated below in dB.

```
SNDR_TI= 10* log10(Signal_power_TI/Total_Noise_TI)
 % SNDR_Ideal= 10* log10(Signal_power_ideal/Total_Noise_Ideal)

% disp(['SNDR_dB =',num2str(SNDR_dB), 'dB']);
```

Effective number of bits calculated below based on the SNDR value!

```
ENOB_TI= (SNDR_TI-1.76)/6.02
 % ENOB_Ideal= (SNDR_Ideal-1.76)/6.02
% disp(['ENOB =',num2str(ENOB),]);
% figure (1);
% subplot(2,1,1);
figure;
% stem (freq,fft1dB_ideal,Marker="none", BaseValue=-400);
```

```
% xlabel('Frequency [GHz]');
% ylabel('Input Signal');
% grid on;
hold on;
% subplot(2,1,2);
stem(freq,fft1dB_TI,Marker="none", BaseValue=-400);
xlabel('Frequency [Hz]');
ylabel('Output Signal Magnitude (dB)')
hold on;
```

```
grid on;
```

Plot the error signal which is basically the difference between the output (interleave signal) and ideal signal.

```
% figure(2);
q = V_TI-V_ideal;
% subplot(2,1,1);
```

Plot the interleave signal.

```
figure;
% subplot(2,1,1);
%   plot(t,V_ideal);
%   hold on;
subplot(2,1,1);
plot(t,V_TI);
xlabel('time (s)');
ylabel('Amplitude (V) [output]');
grid on;
% hold on;
 subplot(2,1,2);
```

```
 plot(t,q);
 xlabel('time (s)');
 ylabel('Error voltage (V)');
grid on;
```