Master RADMEP

Master *Radiation and its Effects on MicroElectronics and Photonics Technologies* (RADMEP)

Ultra-High Doses Tests on 28nm CMOS technology for high energy physics application

Master Thesis Report

Presented by

Geoffrey Ciachera

and defended at

University Jean Monnet

11^{th} September 2024

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Erasmus+ UNIVERSITÉ JEAN MONNET SAINT-ÉTIENNE JYVÄSKYLÄN YLIOPISTO UNIVERSITY OF JYVÄSKYLÄ KU LEUVEN UNIVERSITÉ DE MONTPELLIER

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Ultra-High Doses Tests on 28nm CMOS technology for high energy physics application

Declaration

Hello,

I hope you are doing well,

After a bachelor degree in university Jean Monnet, I apply in an Erasmus mundus master degree program called RADMEP which stand for: Radiation and its Effect on Microelectronic and photonics technologies.

This program is divided in 4, the first semester was in Jyväskylä in Finland where we study semiconductors physics, basics electronics and irradiation tools. The second semester was in Belgium and we study at KUL. This second semester was focus on electronics engineering; we study from analogic electronic to computer architecture including radiation effect. Finally, the last semester was in France in university jean Monnet. The French semester is divided in two specialty and mine was radiation effects on photonics. During this semester we study radiation effects on optical fibers, RPL, lubricant, and did some Montecarlo simulation with Phits.

Finally, at the end of the program we have to do an internship, and I apply at CERN in "Ultra high dose test on 28 nm technology for high energy physics application" and luckly, I got selected.

This report contains the most interesting part of the results we (me and my local coordinator) we obtain during the internship. I declare that the content of this report is from me and was review by my coordinator.

Student name:

Geoffrey Ciachera

Abstract

This work is about the qualification of next generation of electronics detectors for high energy physics application. A new upgrade of the Large Hadron Collider, designated as High Luminosity Large Hadron Collider, is scheduled for completion around 2030 and applications specific integrated circuits will be exposed to new ultra-high radiation radiations levels. In comparison to the Large Hadron Collider, where the maximum expected total ionizing dose is limited to a few tens of Mrad after 10 years of experiment, while the high luminosity maximum radiation dose is predicted to be significantly higher for certain chips, reaching above 2.5 Grad. This total ionizing dose is approximately a hundred times greater and reaches new horizons in radiation electronics engineering.

In this study, the 28nm complementary metal-oxide semiconductor has been subjected to testing thanks to specific chip that allow to irradiated single diode or transistors. In Chapter 3, three tests were conducted on diode inside field oxides field effect transistor structure. The first test reaches a 1Grad total ionizing dose while the other two only 100Mrad. The second and third test were made at different biases and temperatures respectively. Results of these tests indicate that the damage to the diode is greater when the applied voltages and temperature conditions are higher.

The second test was conducted on transistors, and different transistors sizes i.e. W/L = 100/30 nm and W/L = 3/0.03 μm and W/L = 0.1/1 μm where W and L stand for the width (W) and the length (L) of the transistors respectively. These transistors were subjected to irradiation at a total ionizing dose of 5 Grad with the objective of evaluating their survivability. As a result, all n-doped and p-doped metal oxide semi-conductor transistors survived i.e. a significant current from drain to source is flowing, except the long and narrow p-doped devices which reached a degradation of 99%. Finally, n-doped device got a strong increase in the leakage current between 10 thousand to 1 million more than the pre-irradiation one.

Overall, the 28 nm complementary metal oxide semi-conductor is a promising technology to make application specific integrated circuits for new detectors generation for high energy physics applications. However, this report is not exhaustive and a lot of more tests are needed.

Keywords: Ultra high doses (UHD), 28nm CMOS technology, High dose rate, High energy physics (HEP).

Acknowledgements

I would like to express my sincerest gratitude to Giulio Borghello for welcoming me into the team and for his invaluable guidance. Despite my expertise in photonics and initial project which … as a nice French expression said “Tombé à l’eau”, I felt part of the team right from the start. Additionally, during this thesis, I encountered a large number of problems external to the work and even with difficulties, there was a great respect for which I will be forever grateful.

I would also express my gratitude to Gennaro Termo, that I annoy definitely too much while he was writing his PhD thesis. Grazie mille per la vostra pazienza 😊.

I would also say special thanks to Federico Faccio, Stefano Michaelis, Georgios Bantemist, Jerome Alozy, David Porret, Maxence Ledoux and Pinelopi Christodoulou for all the time you took to give advice and more generally help a newcomer, even if I was only staying 6 months.

I want to say thank you to all the team especially during the lunch time where there was funny and various conversation.

I would also say thank you to Sylvain Girard and Arto Javanainen for their guidance through all the meeting we have done.

I also say thank you to my RADMEP colleague with who I share the office for 5-months David Peninon-Herbaut for all the discussions and ideas we shared.

Finally, I would say thank you to my girlfriend Louise Gabion that encourage me until the very beginning of the thesis even though the situation was difficult sometimes.

Thank you everyone for your contributions to maintaining a positive and productive work environment. 😊

List of Acronyms

ASICs	Application Specific Integrated Circuit
CERN	Conseil Européen pour la Recherche Nucléaire
CMOS	Complementary Metal Oxide Semi-conductor
ESD	Electro-Static-Discharge
FCC	Future Circular Collider
FOXFET	Field Oxides Field Effect Transistor
HEP	High Energy Physics
HL-LHC	High Luminosity Large Hadron Collider
IPOL-5V	Integrated Point-Of-Load- 5V
LHC	Large Hadron Collider
nMOS	n-doped Metal Oxide Semi-conductor
p.r.	Pre-Radiation
pMOS	p-doped Metal Oxide Semi-conductor
RINCE	Radiation Induced Narrow Channel Effect
RISCE	Radiation Induced Narrow Short Effect
SMU	Source Measurement Unit

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Chapter 1: Introduction

CERN, i.e., Conseil Européen pour la Recherche Nucléaire in French or European organization for nuclear research in English, is one of the largest physics laboratories in the world. This organization was founded in 1954 between France and Switzerland, in the Geneva area. The particle accelerators at CERN give physicists the possibility to explore the uncharted territories of the infinitely small world of particles. CERN hosts the biggest particles accelerator in the world, the Large Hadron Collider (LHC). Thanks to the LHC the existence of the Higgs boson, long predicted by standard model theory, has been demonstrated. For the next generation of the LHC, called high-luminosity LHC (HL-LHC), some chips will be exposed to extreme doses, up to few Grads after 10 years of experiment. In order to design application-specific integrated circuits (ASICs) capable of withstanding these ultra-high doses (UHD), it is essential to conduct a thorough evaluation of the radiation response of the commercial CMOS technologies employed.

This work focuses on the 28nm CMOS technology selected to be the main CMOS process used for the next generation of ASICs for the particle detectors of the HL-LHC.

To test the radiation response of CMOS technologies, specific test chips have been designed by the Microelectronics section (ME) of CERN. These chips allow to measure isolated, i.e., with all terminals accessible and measurable, metal-oxide-semiconductor (MOS) transistors. The test chip and the methodology used to irradiate and measure it will be described in Chapter 2.

Chapter 3 focuses on TID effects on the reverse leakage current of PN junctions in the 28nm CMOS process. This study was undertaken in response to the unexpected TID-induced failure of a DC-DC converter designed by CERN. The DC-DC converter, named IPOL-5V, was irradiated to a total dose of 1 Grad (SiO_2), showing a failure mechanics compatible with an increase in leakage current of some PN junctions in the circuit. To verify this hypothesis, irradiations on PN junction devices in different conditions of bias and temperatures have been carried out. These experiments helped to better understand the phenomenon and to define design strategies to mitigate or remove it for next iterations of the converter and, in general, for the next ASICs.

In addition, in Chapter 4 a 28nm chip with different transistor sizes was irradiated up to an extreme total dose of 5Grad and then annealed at different temperatures. This is the first experiment at such high dose for the 28nm CMOS process used at CERN. The necessity for this test arises from the fact that ASICs situated in close proximity to the interaction point in some HL-LHC experiments may be required to withstand total doses exceeding 2.5 Grad. This unique test revealed surprising features of the radiation response of the 28nm technology, and provided designers with information needed to develop ASICs for such extreme radiation environments.

Finally, Chapter 5 includes the conclusion and potential future work.

1.1 Radiation environment

As mentioned, this report contains two experiments. Regarding the Chapter 3, IPOL-5V is a circuit that will be used in every CERN experiment for the HL-LHC. This chip will be placed in different position leading to a different expose. The worst-case scenario for IPOL-5V will be a TID of 1Grad after 10 years of experiment.

Regarding the Chapter 4, a chip will be place as close as possible to the particle collision leading to a unprecedent total ionizing dose for electronics devices. The chip will be expose to 5Grad after 10 years of experiment in the HL-LHC. Prior to the fabrication of the chip that will be exposed to the considerable radiation levels, an electronic technology must be validated. In this report, the 28 nm technology is undergoing evaluation.

1.2 State of the art

In consequence of the decision to employ the 28nm CMOS technology as the principal process for the next generation of chips for particle detectors, an intensive investigation of its ultra-high-dose response has been conducted [2-6]. The general conclusion is that the degradation of nMOS transistors is relatively limited, except for the radiation-induced increase in leakage current. Regarding pMOS transistors, their performance degradation can be more important, with an evident reduction in their maximum drain current. As for older technologies like, e.g., 130nm and 65nm nodes [1], the 28nm process suffers from radiation-induced narrow channel effects (RINCE). This phenomenon, related to charge trapped in the shallow trench isolation (STI) oxides, makes narrow devices, i.e., devices with a small channel width, more sensitive to ionizing radiation. While 28nm is sensitive to RINCE, it appears to be immune to radiation-induced short channel effects (RISCE) [2]. On the contrary, devices with small channel lengths appear to be more radiation tolerant. This reduced sensitivity of short channel devices has been attributed to the presence of the Halo implantations [6-7]. The overlap of halos in short channel devices creates a high-doped region under the channel, which results in a better TID response even at UHD levels.

Chapter 2: Materials and Methodology

2.1 Chip connection

The primary goal of this work is to irradiate and measure custom-made test chips to verify the radiation tolerance of the devices included in the chip. All tested chips have been designed by the microelectronics section of CERN. This chapter describes the methodology used to manipulate and measure the chips for all the experiments reported in this document.

Layout and Array: Figure *1* illustrates the chip utilized in this thesis. This 2.4mm×2.4mm chip was designed for the purpose of studying the effects of radiation on MOS transistors in 28nm CMOS technology. Each of the gray pads visible in Figure *3* is connected to a terminal of a MOS transistor, allowing for the evaluation of the effect of TID on the voltage-current characteristics of the device. The chip contains 256 pads arranged in eight arrays (or structures) of two columns of 16 pads each. The devices are physically placed between the two columns of 16 pads in each structure. Each structure is designed to study a specific aspect of TID effects. This thesis focuses only on two of the eight available structures: one designed to study the effects of bias on the TID response, and one containing Field-Oxide-FETs (FOXFETs) devices.

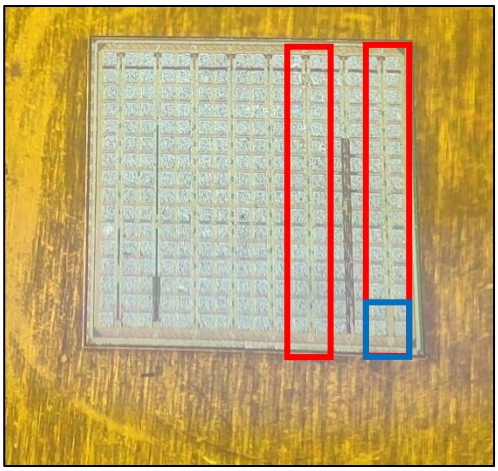

Figure 1 - Picture of a chip

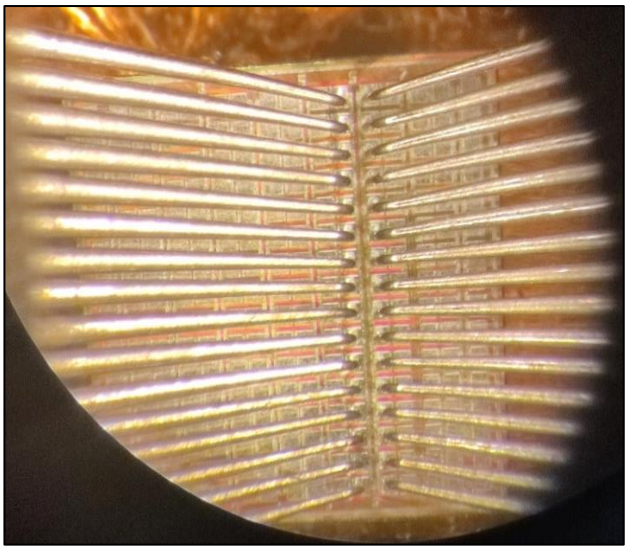

Figure 2 - Connection of an array

Chip connection: A custom probe card is used to measure the chip. The probe card is installed inside the x-ray machine, giving the possibility to measure the devices while irradiating. Each needle is connected to the corresponding pad of the structure, as shown in Figure *2*.

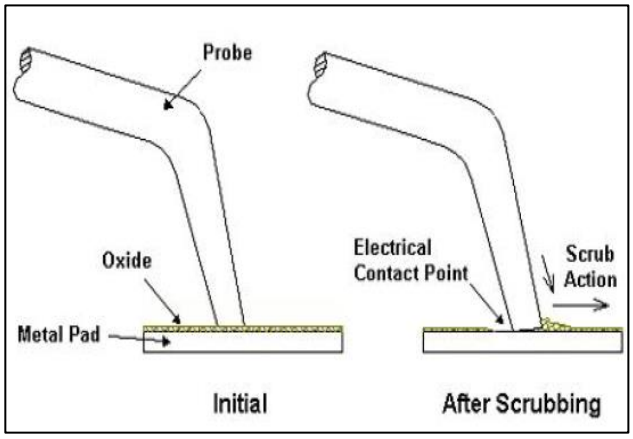

Figure 3 - Needles connection diagram *[3]*

Needles contact: When the needle touches the pads, they scratch a thin layer of oxides as depicted in Figure *3*. Once the electrical contact has been created, the chip can be measured.

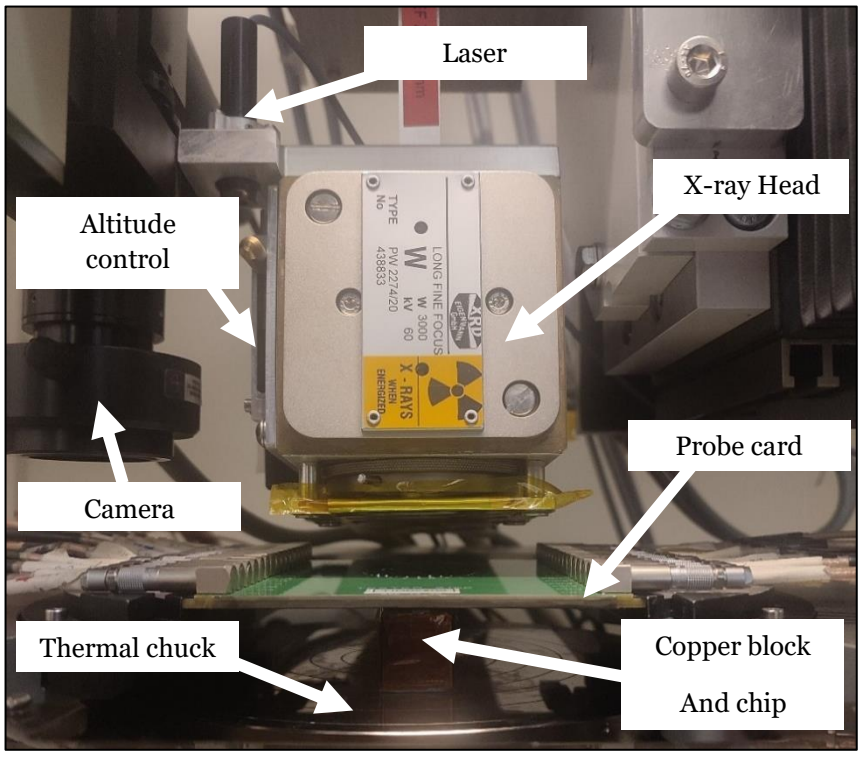

Figure 4 - X-ray machine set up inspired by *[3]*

2.2 X-ray cabinet and head positioning

Figure *4* shows the inside of the radiation chamber, where the probe card, the thermal chuck, the camera, and the laser are indicated. The laser is used to control the X-Y position of the camera and the X-ray head (containing the X-ray tube). The altitude of the X-ray tube with respect to the probe card is verified thanks to the "altitude control" visible on the Figure *4*. The altitude of the beam from the chip is an important parameter as it determines the dose-rate. The altitude control is exactly 2cm high, meaning that when it touches the prob card, the X-ray head is at 2cm form the chip plus the thickness of the prob card and the relief of the needles, i.e., 2.68cm in total. The beam can then be vertically moved with a precision of 0.1mm thanks to a mechanical control (stepper). This simple solution allows to precisely position the beam at the desired altitude.

2.3 X-ray tube characteristics

The Figure 5 show the X-ray fluence as a function of photon energies of a tungsten source operated at 50 mA current and a potential difference between the cathode and the anode of 40 kV. [4] describe how an X-ray tube works. The spectrum shows in Figure 5 is not the one employed during the subsequent test; rather, it is a schematic illustration of the methodology used to generate X-rays for the aforementioned test. Also note that an aluminums filter of 0.15mm is used to remove the low energies X-rays below 5kev as it is visible in Figure 5.

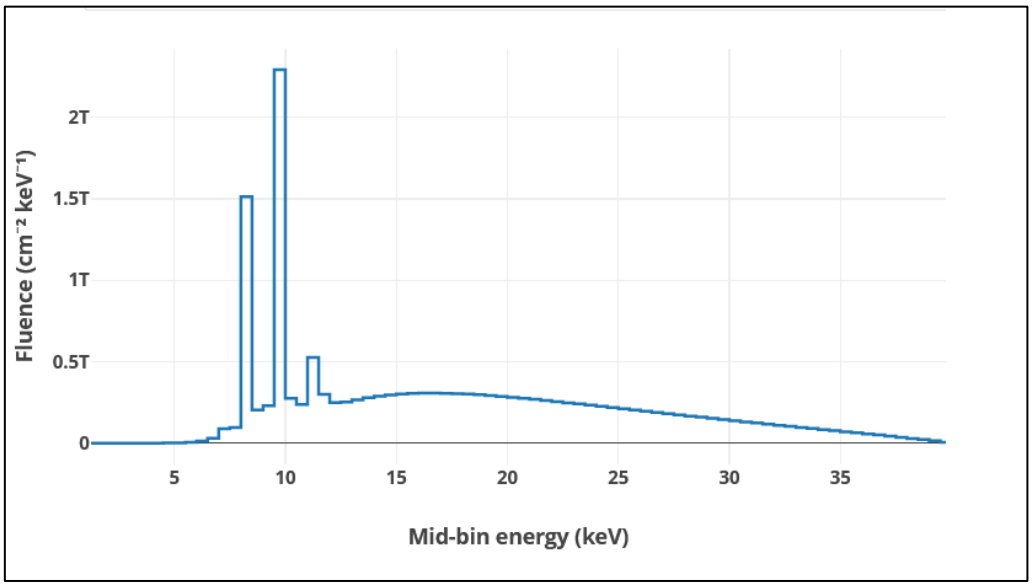

Figure 5 - X-ray spectrum of a tungsten source powered at 50mA and 40kV [5]

The discernible peaks in Figure 5 correspond to the characteristic X-ray of tungsten. The generation of these particular X-rays is elucidated by the electron (4) depicted in Figure 6. In this process, an incident electron collides with a core electron (e.g., a K or L electron) in the deep electronic layer of a tungsten atom, resulting in the ejection of the core electron. The vacancy created by this interaction allows an electron from a higher energy level to fill the resulting "hole," leading to the emission of a characteristic X-ray.

With regard to the X-ray spectrum, it should be noted that other X-rays are emitted. This phenomenon is known as bremsstrahlung interaction, or in English, "braking radiation" [4]. This is the point at which electrons reach the anode, or target, and do not interact with other electrons (X-ray characteristics), resulting in their braking due to the electrostatic forces exerted by atomic nuclei, as illustrated in Figure 6, 1 and 2. Stronger the break is and higher the energy of the X-ray will be. Ultimately, the maximum X-ray energy, namely 40 keV for illustrative purposes, corresponds to the collision between incident electrons and the nucleus, represented by number 3 in Figure 6.

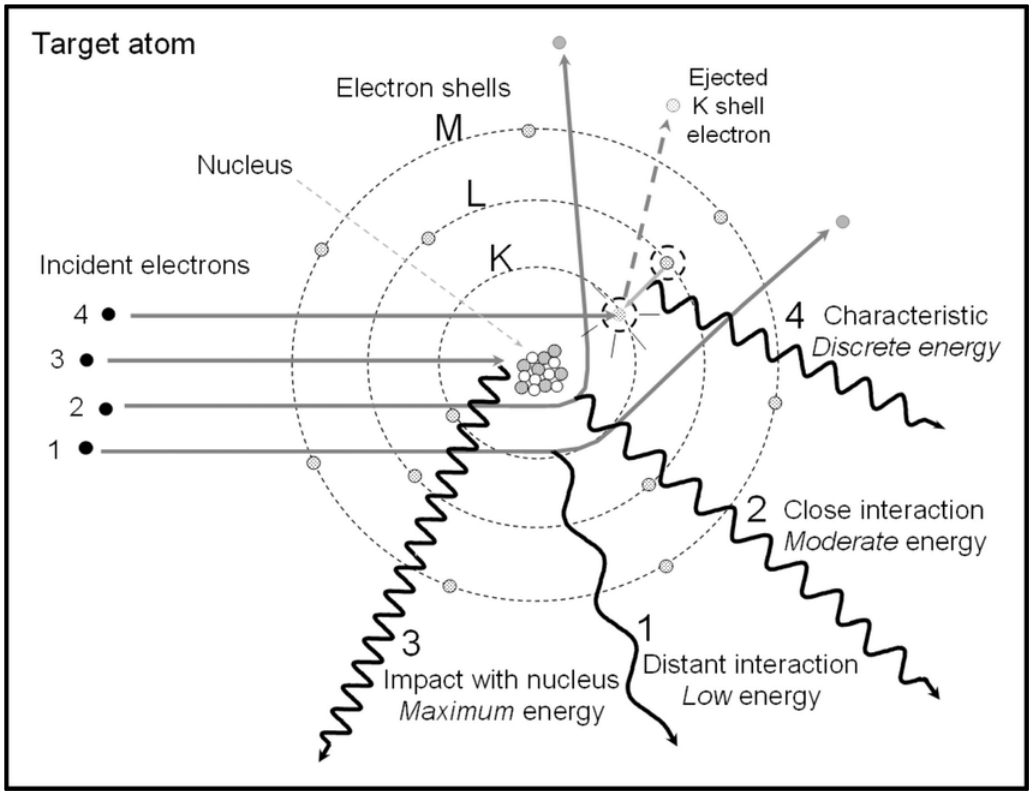

Figure 6 - X-ray production *[4]*

2.4 Dose rate distribution

The X-ray beam is not perfectly uniform in space, meaning that the dose-rate decreases from the center of the beam. To assure a correct calibration and to have a consistent TID for each irradiated transistor on the chip, it is fundamental to map the spatial distribution of the dose rate. Figure *7* shows an example of a calibration map. The map reports the dose-rate in Mrad(SiO_2)/h at different X/Y positions with respect to the [0.0, 0.0] position identified by the laser. The X/Y are reported in mm on the top and at the left of the map, respectively. Note that the center of the map [0.0, 0.0] does not correspond with the center of the beam, which is around the [1.5, -1.0] position. This however does not impair the placement of the chip in the beam, as also the position of the chip is taken using the laser as a reference. Finally note the dose rate distribution of the Figure *7* is done at low current. In [4] they explain that dose rate fluence and injected current is proportional.

Mrad(SiO_2)/h										
Y \ X	-2.0	-1.0	0.0	1.0	2.0	3.0	4.0	5.0	6.0	7.0
3.0	0.01	0.06	0.13	0.15	0.14	0.12	0.07	0.03	0.01	0.01
2.0	0.06	0.19	0.26	0.27	0.27	0.26	0.23	0.14	0.05	0.02
1.0	0.14	0.26	0.27	0.27	0.26	0.26	0.27	0.23	0.12	0.03
0.0	0.20	0.26	0.26	0.26	0.24	0.24	0.26	0.25	0.17	0.05
-1.0	0.22	0.25	0.25	0.22	0.24	0.23	0.24	0.23	0.20	0.06
-2.0	0.21	0.23	0.23	0.23	0.23	0.23	0.23	0.22	0.20	0.06
-3.0	0.19	0.21	0.21	0.22	0.21	0.21	0.21	0.21	0.17	0.04
-4.0	0.14	0.19	0.19	0.20	0.20	0.19	0.19	0.19	0.12	0.02
-5.0	0.03	0.13	0.16	0.17	0.17	0.17	0.17	0.15	0.05	0.01

Figure 7 – Dose rate distribution

The dose-rate decreases rapidly from the center of the beam, reaching relatively low-dose-rates after only 2 mm in each direction. In other words, the chip must be accurately placed. On this map, the chip should be located between [-1.0, 0.0] and [5.0, -2.0] in X/Y coordinates.

2.5 Block Diagram connection

Once the chip is connected, a measurement is run. The entire connection diagram for the irradiation setup is despite in Figure *8*. For the annealing test, another semiconductor analyzer named 4155B is used.

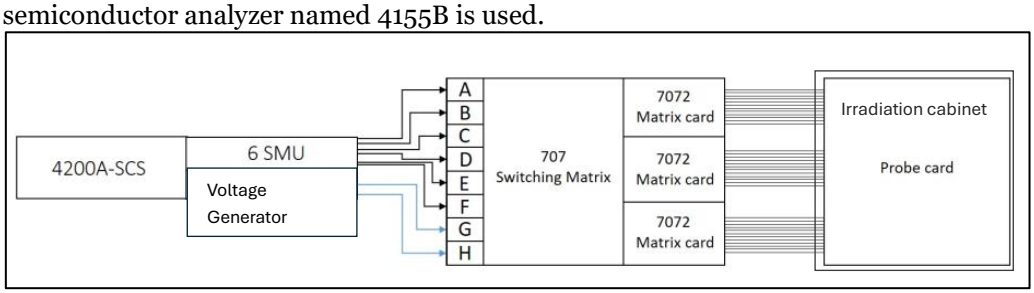

Figure 8 – Overview of the experimental setup *[3]*

The semiconductor analyzer shows thanks to the box 4200A-SCS in Figure *8* is an instrument used to measure I-V characteristics of transistors and diode. The semiconductor analyzer is connected to the switching matrix with 6 cables. Each cable is connected to a source-measure unit (SMU) of the 4200A. The switching matrix

connects each SMU to the desired 6 of the 32 cables going from the three 7072 matrix cards to the probe card. In this way, the SMU are connected to the pads of the chip and therefore to the terminals of the transistor. This allows to perform I-V measurements of the devices and retrieve the current flowing in all connected terminals. The G and H terminals of the switching matrix are connected to a voltage generator. Channel G is connected to ground, while channel H is at a high voltage, typically the VDD of the technology tested. Channels G and H are used to bias the transistors during irradiation. The entire system is controlled by a custom-made LabVIEW software that automatizes the measurements and the test routine described in the next section.

2.6 Test routine and data analysis

Figure 9 shows a typical test routine. The first measurement is always taken at 25°C, and it is used as a reference for the entire test. If the irradiation must me carried at a temperature different form 25°C, the chip is brought to the desired temperature and the test starts with a measurement of the chip. After that, the test is typically constituted by a series of irradiation steps, each of them followed by a measurement of the chip.

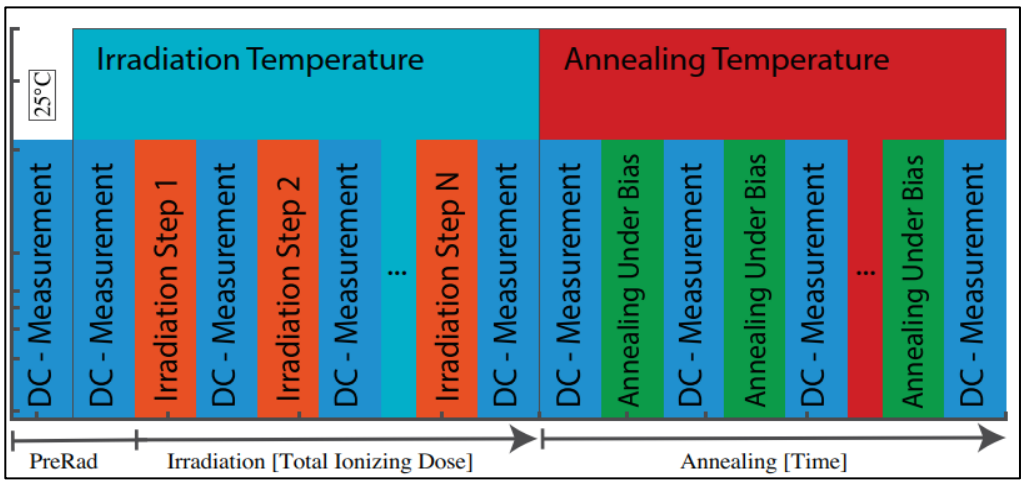

Figure 9 – Typical measurement procedure *[3]*

A typical measurement can take up to 5 min for the experiments discussed in Chapter 3 and from 15 to 20 min for those in Chapter 4. The post-irradiation behavior of the radiation response is monitored through a sequence of measurements separated by a certain amount of time. This phase of the test is called annealing. During both irradiation and annealing the chip is kept under bias. The specific biases, temperatures, and times used in the various tests described in this thesis will be outlined in the corresponding chapters. The result of each measurement is stored in a .txt file. A set of MATLAB functions allows to quickly read and visualize the result of the measurements.

Chapter 3: Ultra High doses effect on PN structure

3.1 IPOL-5V failure and test descriptions

This chapter discusses the TID-induced increase in leakage current of PN junctions in 28nm CMOS technology. This work has been carried out to understand the mechanisms behind the radiation-induced failure of the IPOL-5V DC-DC converter designed at CERN. IPOL-5V is a resonant DC-DC converter that step down the voltage from 5V (indicated by the '5V' of its name) to 0.9V. In early May 2024, the chip failed during an X-ray irradiation test. The chip stopped working properly between 10Mrad and 150Mrad. After 150Mrad, the chip resumed normal functionality and continued to operate without issues up to 1 Grad. Given that the chip is composed of three identical stages operating under different voltage domains as depicted by the block diagram of Figure *10*, it is possible that a failure may originate from any one of these three stages, This failure is visible in Figure *11* and Figure *12* by an inconsistent voltage increase and drops respectively. However, the primary suspect in the failure was determined to be a leakage current path between the $N_{WELL} - P_{SUB}$ junction of pMOS transistors which bulk connection was not to power rail of the top stage but to their source, as illustrated in Figure *13* . To confirm this hypothesis, an irradiation campaign with 3 tests at UHD was conducted on PN junctions in 28nm CMOS technology [6].

3.1.1 IPOL-5V presentation and layout

IPOL-5V is a state-of-the-art DC-DC converter based on resonant stacked-tank topology designed in a 28nm CMOS technology. IPOL-5V consists of three basic stages each one stacked on top of the other. The voltage domain of the top stage is 5V into 3.7V, the middle stage 3.7V to 2.3V and the bottom stage 2.3 to 0.9V shown as red, blue and green in Figure *10*. Each stage consists of two pair of switches connected in the middle with an LC resonant tank. Which explain why 9 voltages are visible in Figure *11* i.e. 3 voltage per stage.

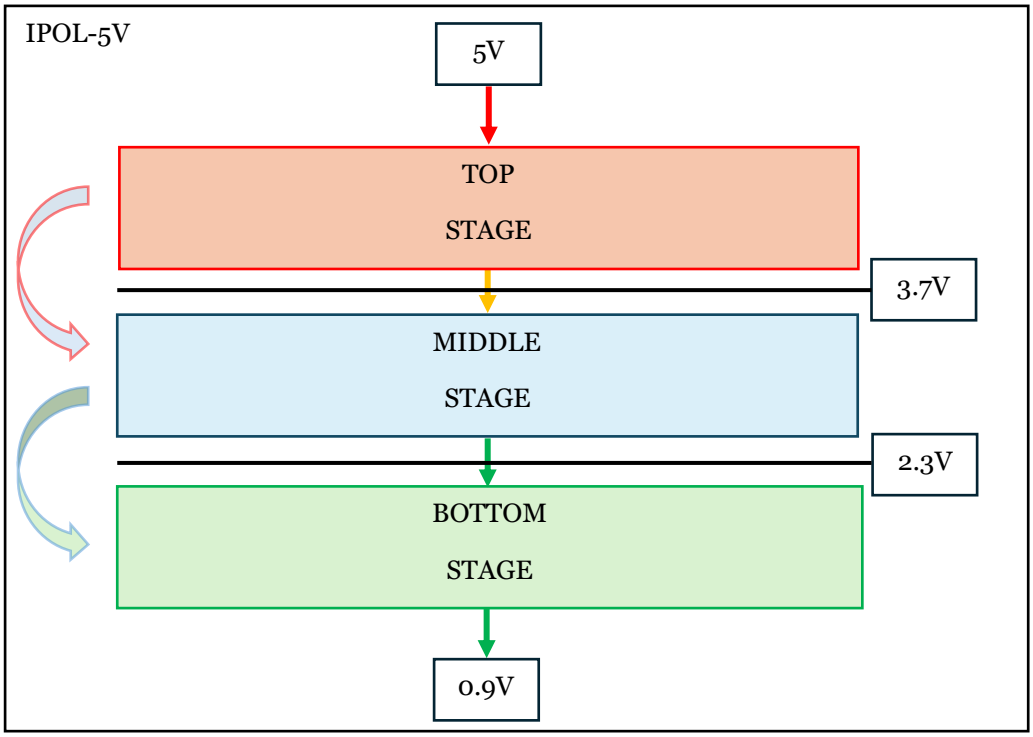

Figure 10 - IPOL-5V structure

In order to enhance efficiency and radiation hardness only core devices were used rated 0.9V. To achieve that and maintain safe operation, intermediate voltage domains of 0.9V were created with the use of linear regulators for each stage. It is noteworthy that the red arrows, which were used to indicate a potential failure.

3.1.2 IPOL-5V under test and "low dose failure"

Figure *11* is the measure of every IPOL-5V voltages for every stage during irradiation except the input voltage which is stable and equal to 5V. The top, middle and bottom stage are represented in red blue and green respectively as in Figure *10*. The flat voltage for every measure from 0 to 11Mrad is the "normal" behavior. A voltage jump is clearly visible when the TID reach 11Mrad. The purple bar represents when the X-ray tube was disactivated. Given that the dose rate is 2 Mrad/h, a straightforward calculation demonstrates that it requires approximately 15 minutes to reach the jump-down value.

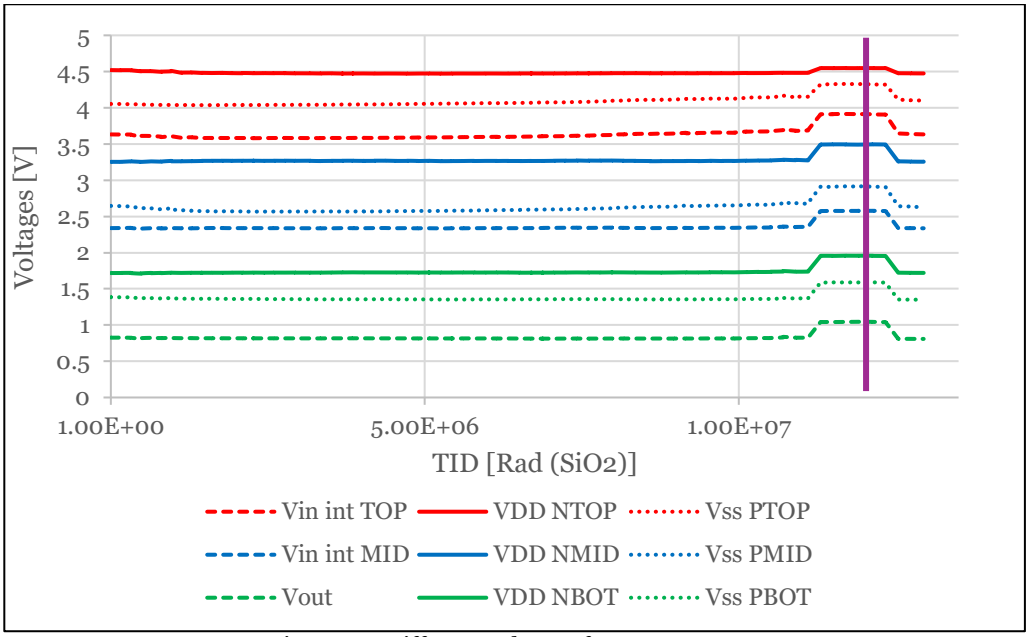

Figure 11 - Different voltage of IPOL-5V stages

The circuit used pair of nMOS and pMOS switches stacked on top of each other; this is the rationale behind the designation of some curves as "NTOP" or "PTOP" for the top stage and similar named for the middle stage. Note that Vin int TOP and MID and Vout are the intermediated voltage i.e. top and middle stage respectively and the final output voltage i.e. Vout.

Finally, as it is visible, the jump up voltage is similar around 30mV for every curve of every stage except the VDD NTOP which is 5mV.

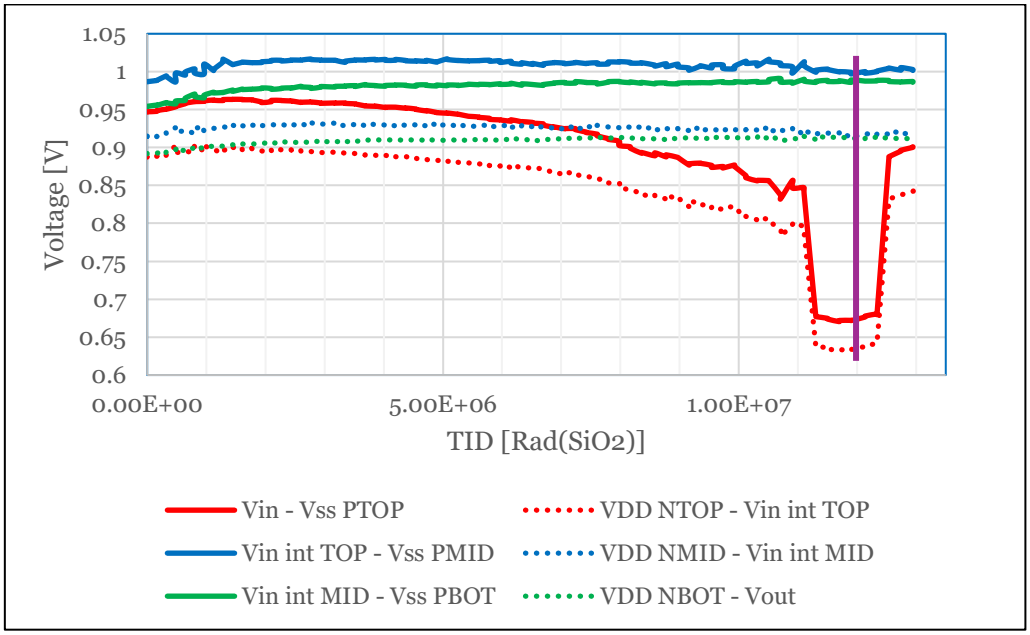

Figure 12 -Subtraction between input by every intermediate voltage

The color code is identical in Figure 12. Regarding the top stage, after the difference of the input voltage which is constant to 5V by the Vss PTOP which has a voltage increase at 11Mrad, the difference is not constant. As previously stated, the two voltages i.e. VDD NTOP and Vin int TOP do not have the same voltage increase (i.e. ~5mV instead of 30mV respectively) with the TID, resulting in an unequal difference at the output of the circuit. The aforementioned voltage drop is the underlying cause of IPOL-5V failure.

3.1.3 Failure mechanism

As previously stated, the failure of IPOL-5V is likely attributable to a voltage drop in the top stage. An abrupt increase in leakage current through a N_{well}-P_{sub} junction of a pMOS transistor may be a contributing factor to this voltage drop.

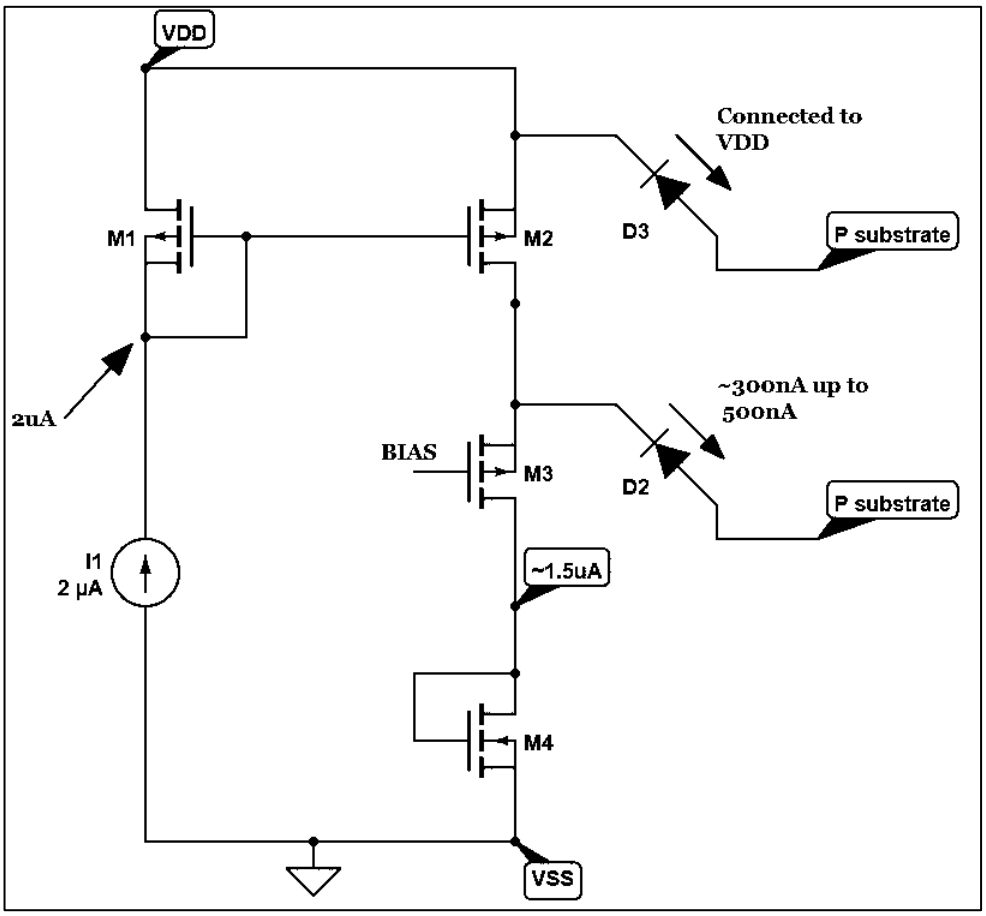

Figure 13 - Internal circuit one branch of a resonant stacked-tank

The diagram in Figure *13* shows a part of the current reference used in the three stages of IPOL-5V. This circuit includes 3 pMOS, named M1, M2, and M3 and 1 nMOS, called M4. The two top transistors, i.e. M1 and M2, form a current mirror, which copies the current from one side to the other. In this case, the 2µA of the left branch are copied to the right branch.M3 transistors is the hypothetical source of the circuit failure. The inclusion the D2 and D3 diodes indicates the leakage current of the N_{well}-P_{sub} junctions. As displayed in Figure *13*, M2 and M3 are part of the same branch, meaning that the current flowing in this branch is 2µA. If the D2 leakage current reaches a sufficiently high value with respect to the total available current, the current on the branch may drop from 2uA to a lower value and the circuits that are using this reference current may fail operating as expected. In the example depicted in Figure *13*, the D2 leakage current is 500nA, meaning that the remaining available current for M4 is only 1.5µA. Given that current and voltage are proportional, a reduction in one will result in an increase in the other parameter.

3.1.4 Simulations

The effect of an increased leakage current in the N_{well}-P_{sub} junction of M3 has been simulated at circuit level by injecting a current in the suspected sensitive node. Since the irradiation campaign did not give any information on the value of the leakage

current, simulations at increasing levels of N_{well}-P_{sub} current were carried out. Nothing was observed until reaching the critical value of 300nA, which represents the 15% of the total current given by supply. Note that this leakage value is only achievable in the top stage. The other two stages do not have sufficient voltage to generate this amount of leakage current. An accurate model of the PN junction leakage current can be find in [7]

3.2 Irradiation campaign on PN junction and FOXFET layout

In order to test the hypothesis set out in Section 3.1.3, an irradiation campaign was carried on FOXFET devices [8]. FOXFET devices are transistors but the gate is made of STI and is thicker than a standards transistors gate. In this case this is nFOXFET transistors. They are used for this experiment they are structurally close to the suspected N_{WELL} leakage current of the pMOS describe in 3.1.3. As mentioned in 3.1.2, the top stage recovers quickly after the radiation is stopped. This indicates that a rapid annealing process is occurring. To observe this phenomenon, a dedicated experiment, illustrated in Figure *13*, was designed. "Before" and "After" are identical measurements, separated by a fixed "Wait" time. The purpose of the "After" measurement is to be able to quantify the annealing after 5 min without any radiation.

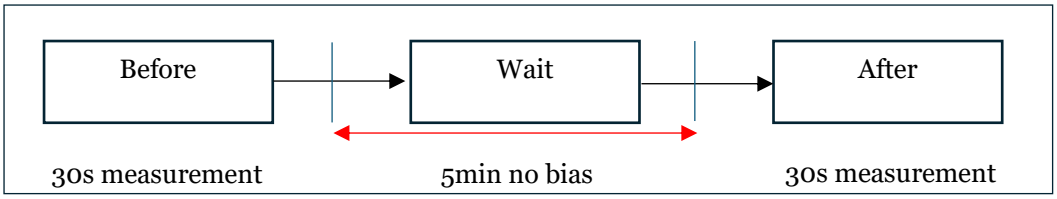

Figure 14 - PN junction measurement procedure

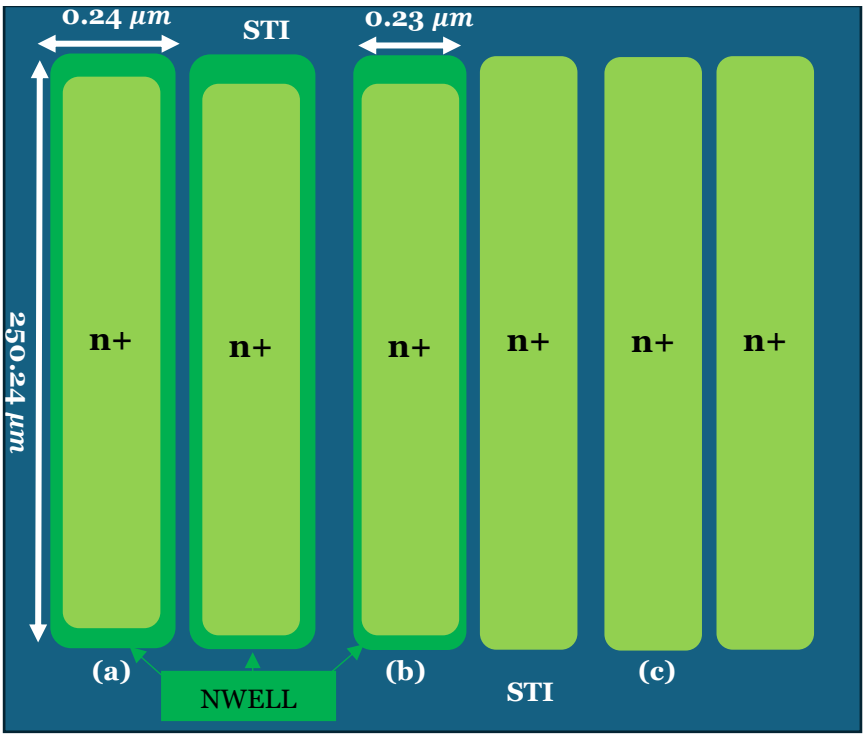

Figure 15 - FOXFETs top view

Figure *15* show the top, of the three FOXFET transistors used. Labels (a), (b), and (c) in Figure *15* corresponds to the labels (a), (b), and (c) in Figure *16*. The chip contains 3 different structures: Nwell-Nwell, Nwell-Nplus and Nplus-Nplus, where Nplus is more

doped than Nwell. These names refer to the n-type wells used as drain and source in the FOXFETs. Since the purpose of the test was to measure the TID response of the current flowing in PN junctions, only the drain-to-substrate current was measured, leaving the other terminals floating. The drain terminal of all FOXFET is not connected to any electrostatic discharge (ESD) protection, giving the possibility to bias and measure the PN junctions at voltages higher than VDD. This configuration allows to measure two $N_{WELL} - P_{sub}$ diode and one $N_{PLUS} - P_{sub}$ diode (Nwell-Nwell and Nwell-Nplus being identical on the drain side). Figure *16* show the side view of the 3 different FOXFET layouts included in the chip. Note that to connect an Nwell, an n+ diffusion is needed. The purple circle in Figure *16* indicates the region of the STI/PN junction corner that is suspected to be the source of the radiation-induced leakage current. This "leakage corner" will be described in further detail in section 3.4.

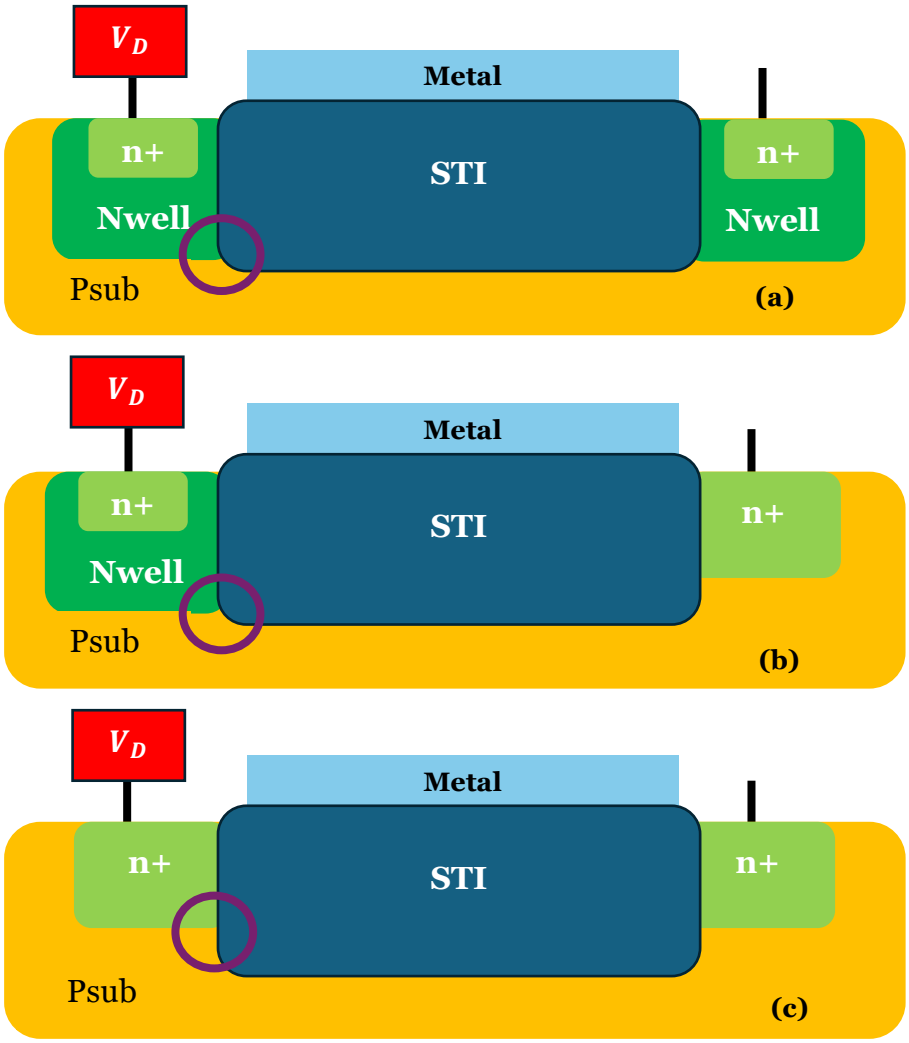

Figure 16 – FOXFETs side view

3.3 Measurement and bias during irradiation

The measurement of the PN junction was done by sweeping the voltage from 0 to 5V on the V_D terminal, keeping the substrate at 0V. It should be noted that the VD i.e. diode voltage, (or V_{PN} i.e. PN junction voltage) terminal was biased in 2 different ways during the subsequent experiment. The first is VD_{MEAS} and the second is VD_I. VD_{MEAS} is the

leakage current value at a specific "measured" voltage e.g. the current measure at 5V. In the following results, VD_{MEAS} is symbolize by a marker. While the VD_I represent the value of the bias of the VD terminal during the irradiation. VD_I corresponds to the line between two markers.

3.4 Results and discussions

In this Section three test results will be discuss. The initial test was conducted at a dose of up to 1 Grad at room temperature. 1Grad is highest dose that IPOL-5V should receive following a 10-year experimental period in the LHC. As said in Chapter 2 the dose rate is 6Mrad (SiO_2)/h, this experiment took 1 week and is an "exploration test" to observe UHD effect on PN junctions. After the first experiment it was conclude that 100Mrad test was sufficient reducing the irradiation time from 1week to 17H. The measurement setup remained identical, the experimental conditions varied according to the bias (second test) and temperature (last test). Finally, the reader should be aware that every result shown in section 3.4 are normalized with the perimeter of each well. The perimeters have been chosen here because the STI has it is visible in Figure *15* is all around every well i.e. the leakage current is all around the well. Perimeter calculation is shown in equation (2) for Nwell -Nwell structure and equation (3) and (4) for Nwell-Nplus and Nplus-Nplus structure respectively. Note that on the chip 11 wells of each type are in parallel.

$$Well_{\text{perimiter}} = Well_{\text{Number}} \times 2 \times (W + L) \quad (1)$$

$$(NW - NW)_{\text{perimiter}} = 11 \times 2 \times (250.24\ \mu\text{m} + 0.24\ \mu\text{m}) \quad (2)$$

$$(NW - NP)_{\text{perimiter}} = 11 \times 2 \times (250.24\ \mu\text{m} + 0.23\ \mu\text{m}) \quad (3)$$

$$(NP - NP)_{\text{perimiter}} = 11 \times 2 \times (250.24\ \mu\text{m} + 0.23\ \mu\text{m}) \quad (4)$$

Where, equation (1) shows the general method to calculate the perimeter, where $Well_{number}$ is the number of wells in the structure and $2 \times (W + L)$ is the perimeter of every well.

Along the results part, several coefficients have been created to simplify the analysis. Equations (5) and (6) shows these coefficients.

$$\alpha = \frac{I_{D_{TID(t)}}}{I_{D_{p.r}}} \quad (5)$$

Where $I_{D_{TID(t)}}$ is the leakage current measure at a specific TID after different interval of time t and $I_{D_{p.r}}$ is the leakage current before radiation

$$\gamma = \frac{I_{D_B}}{I_{D_A}} \quad (6)$$

Where I_{D_B} is the leakage measurement in the "Before" dataset shown in Figure *13* and I_{D_A} is the leakage current in the "After" dataset.

3.4.1 Irradiation effect

Figure *17* shows $I_{PN} - V_{PN}$ characteristics at four different levels of TID. Blue curves represent the leakage current before radiation (p.r.), the black curve show the current at TID = 1 Mrad(SiO_2), the red curves represent the maximum leakage current, reached at 30 Mrad(SiO_2), and the pink curve represents the leakage current at the maximum TID, i.e. 1 Grad(SiO_2).

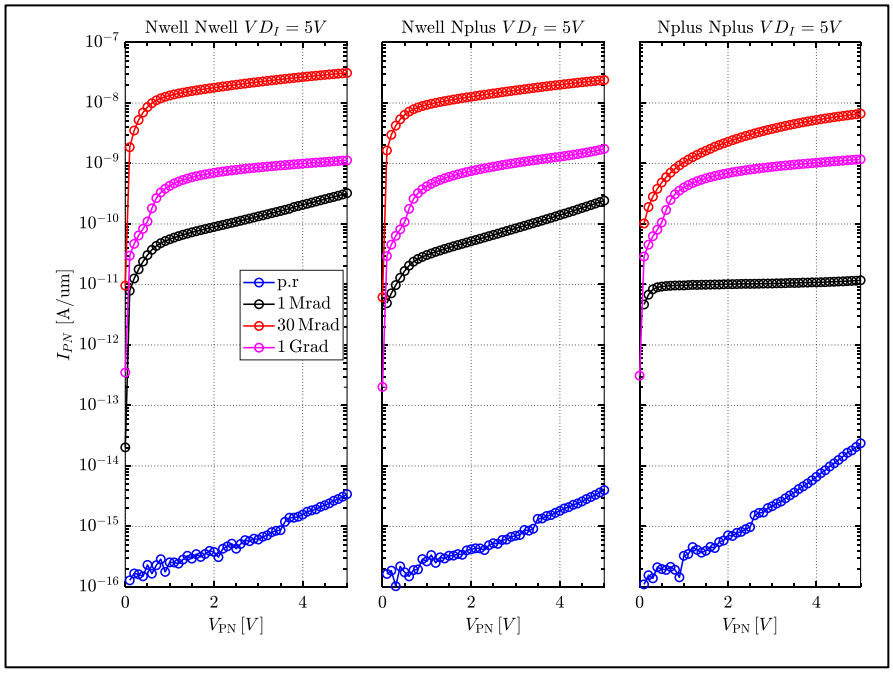

Figure 17 - I-V curve of a PN junction located on a FOXFET device

The current increases by more than 4 orders of magnitude from p.r. to 1 Mrad reaching a leakage current of $3 \times 10^{-10} A$ at 5V and increases until a leakage current peak of $3 \times 10^{-7} A$ at 30Mrad. After 30Mrad, the decrease in leakage current is clearly discernible, as evidenced by the pink curves. For the two Nwells, this decrease is approximately a factor of 30, while for the Nplus structures it is approximately a factor of 10.

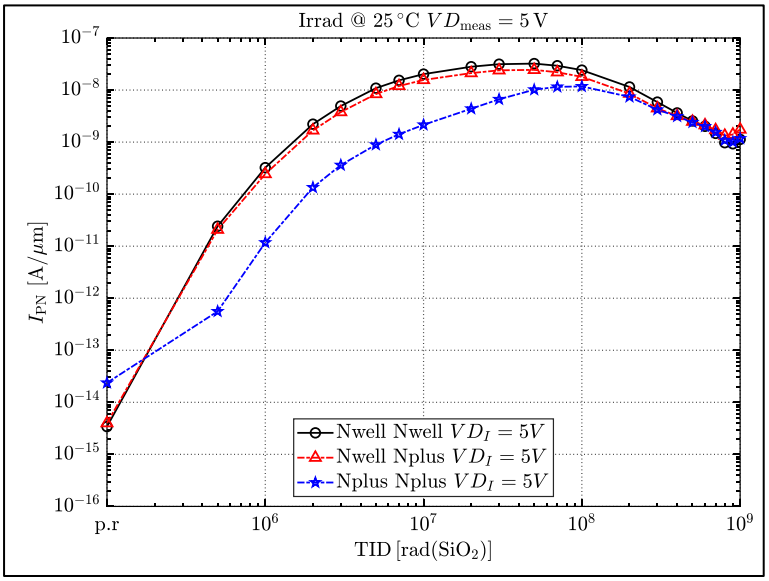

Figure 18 - Results of 3 wells bias and measure at 5V after a 1Grad irradiation

Figure *18* shows the evolution of leakage current measured at $V_{PN} = VD_{meas} = 5V$ with respect to TID. The leakage current peaks around 30 Mrad, and then slowly decreases until 1 Grad. This result strongly correlates with what measured in IPOL-5V, where the converter stopped working in the 10 Mrad – 150 Mrad range and recovered functionality at higher doses. The increase in leakage current appears to be greater for less doped structures i.e. Nwells. This is the first indication that the only relevant doping for the increase in leakage current is the one facing the STI oxide since Nplus doping is present also in Nwells (see Figure 15). The ratio between the TID reached at each measurement and the p.r. value is shown in Figure *19* by the evolution of the α coefficient defined in (5). Consequently, the sensitivity of Nwells with the dose even above 300Mradis greater, even when the leakage current appears to be comparable as shown in Figure *18* with Nplus wells.

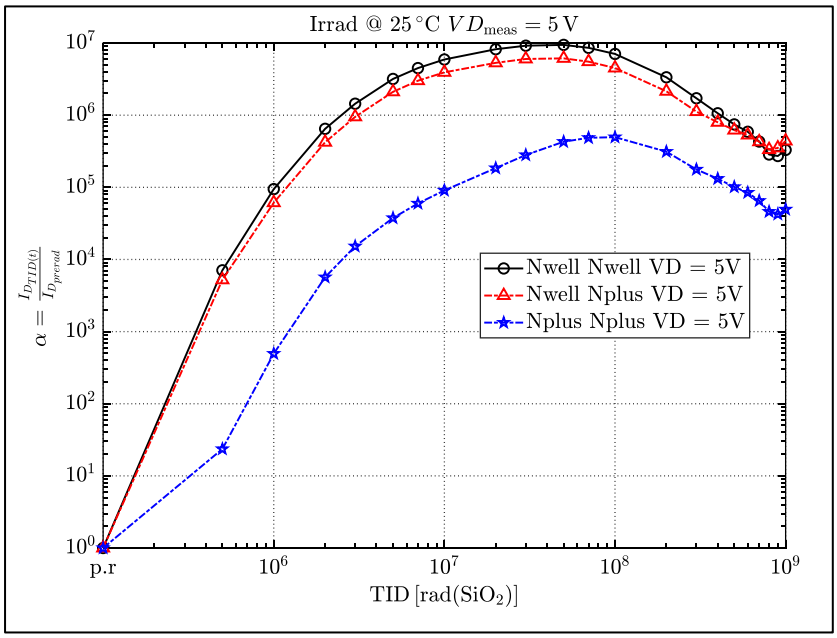

Figure 19 - leakage current increase normalized to the p.r. value

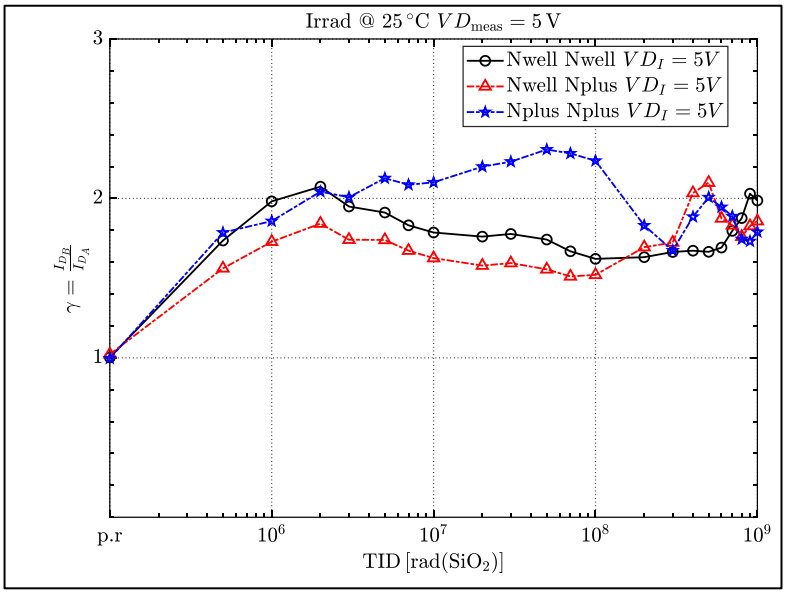

Figure 20 - Ratio of Before over After measurement

As shown in *Figure 14* , two identical measurements separated by 5 minutes are taken for each TID level. The two measurements are called “before” and “after”. Thanks to the γ coefficient defined in (6), the leakage current ratio of the before to after measurement is calculated for each well. The ratio is stable around 2, indicating that the leakage current in the “before” measurement is twice as large as in the “after” dataset. This result is consistent with the fast annealing measured in IPOL-5V, where the converter was quickly recovering its functionality once the beam was stopped. This is a strong indication that the mechanism causing the increase in PN junction leakage is related to the failure mechanism measured in DC-DC converters.

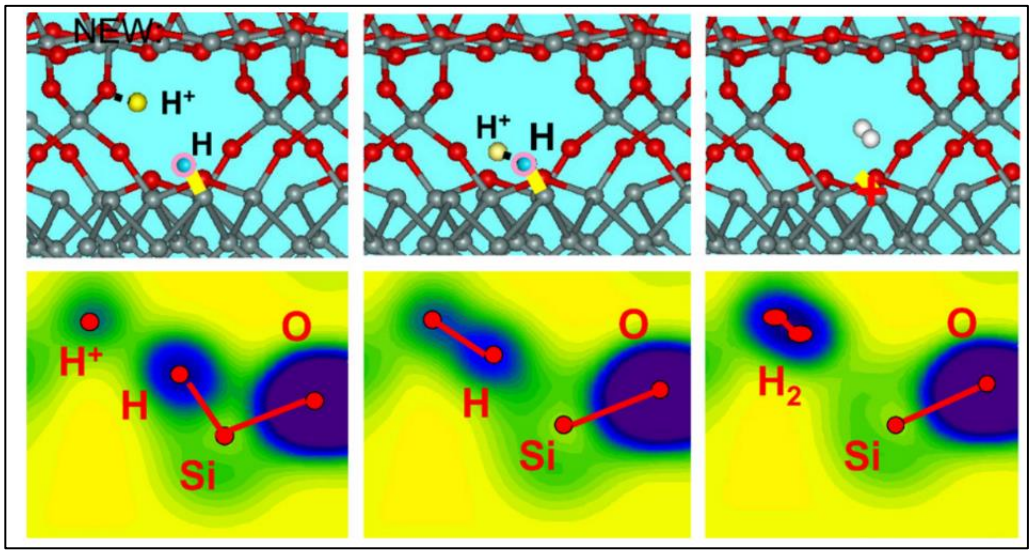

Figure 21 - Depassivation of dangling bonds at the interface. Darker regions in the figures on the bottom row correspond to a higher electron density *[9] [10] [11] [12] [13] [14] [15]*

As mentioned, after the leakage current peak at 30Mrad, the leakage current recover despite irradiation until 1Grad. *Figure 21* show the depassivation of dangling bonds i.e.

activation of interface traps which physically act as a "OFF" button (see Chapter 4) for the current flowing through the transistor channel due to the threshold voltage increase. This effect seems to be also observable in Figure *18* and Figure *19* after the leakage current peak at 30Mrad. The depassivation is a long time effect especially at high dose rate, because hydrogen ions need to be brought to the $Si - SiO_2$ interface as shown in the left side picture but holes act as a shield for H^+ ions [16]. When one hydrogen ion reaches the interface symbolize by red H^+. The hydrogen atoms bonded to the SI atoms symbolized by red H will form a bond with the hydrogen ions arriving at the interface. This is how a dangling bond is created [15] [17] i.e. an interface trap is created. Activation of interface traps tend to increase the 1/f noise which can be problematic at circuit level [17] [18]. Generally, trapped holes in oxides have fast effect on the device, and interface tend to arrive later [16].

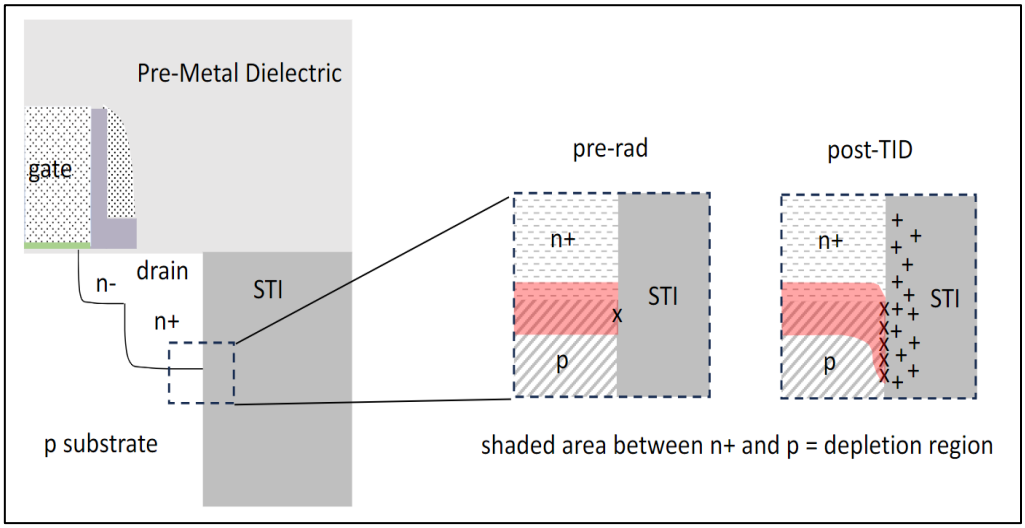

Figure 22 - Conceptual illustration of the influence of TID on the depletion region of a n+ drain diffusion in the substrate. Figure from the NSREC 2024 short course accessed with permission

Figure *22* illustrates the physical mechanism causing the increase in leakage current in PN junctions in CMOS technologies. The Figure *22* shows the drain of an nMOS transistor, which is conceptually analogous to the FOXFETs examined in this work. The red rectangle highlights the depletion region of the PN junction on both side, when a bias is applied. The crosses (X) indicate the interface traps present at the interface between the PN junction and the STI. These traps are created thanks to the depassivation of dangling bonds as describe with Figure *21*.These interface traps act like generation recombination centers and increase the surface (see perimeter above) where the current can flow i.e. reverse current know in this case as leakage current. The presence of defects is expected also before irradiation because the interface between the PN junction and the STI is poorly arranged. These defects contribute to explain the p.r. leakage. After irradiation, an important number of defects e.g. E' point defects have been introduced within the STI where a considerable quantity of hole represented by "+" markers are trapped. Holes electric field interact with the PN junctions and modify the shape of the depletion region symbolize in red. This seems to be the primary mechanisms of the important increase of the leakage current and can have dramatic consequences of the chip behavior [8] [19].

The following explanation is based on the NSREC 2024 short course, which was accessed with permission.

3.4.2 Bias effect

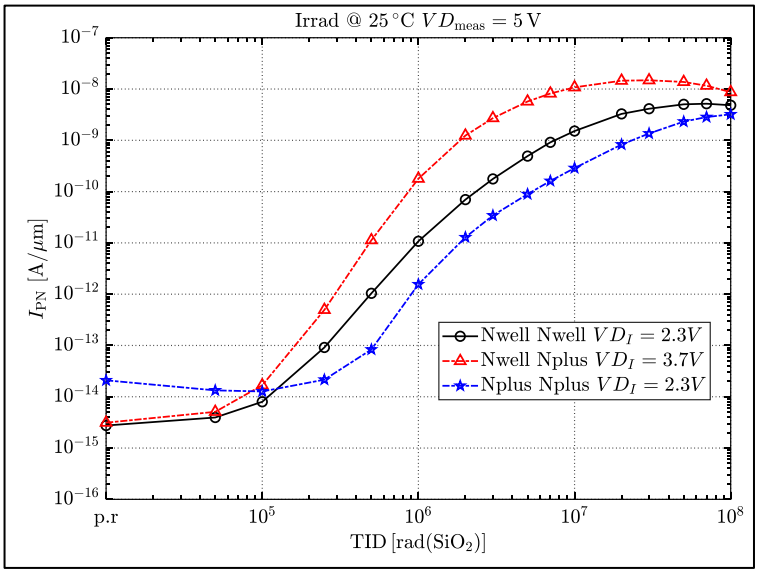

Figure 23 - Results after a 5V measurement and different biases during irradiation on a fresh device

The second test was at the same temperature, and measurement structure, only the bias during irradiation of the PN junction was change. A comparable phenomenon can be observed, namely a significant rise in the leakage current prior to saturation, followed by a decline. A clear bias effect can be observed e.g. Nwell bias at 2.3V exhibits a comparatively weaker increase in leakage current in comparison to the 3.7V measurement. Nplus leakage is even weaker for doping reasons describe in the previous paragraph. The conclusion is that the general behavior does not depend of the diode bias. The only noticeable effect that have the bias is in the maximum point which is higher with 5V approximately 30nA at 30Mrad than 3.7V and 2.3V which are at 10 nA and 7 nA respectively. Finally, the time needed to reach the leakage current peak seems also smaller for higher voltages. Figure *23* show this effect between the 2 Nwells structures, where the maximum leakage current peak seems to be 30Mrad at 5V and 3.7V meaning the maximum voltage of the DC-DC, however the maximum peak at 2.3V bias during irradiation seems to be reach at 60 or 70Mrad (circles markers).

3.4.3 Temperature

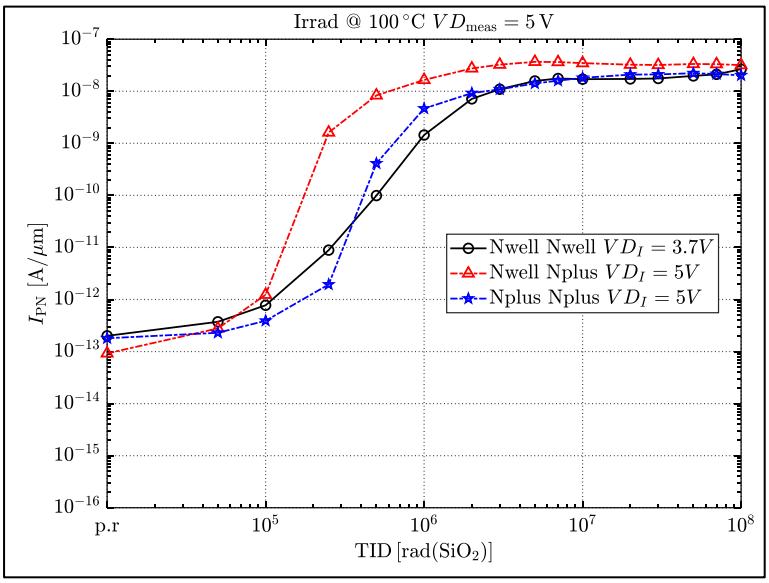

Figure 24 - Results after 5V measurement and with different temperature during irradiation on a fresh device

As illustrated in Figure *19* and Figure *23* the worst-case scenario is Nwells structure with 5V or 3.7V bias during irradiation, so this is why the third test was conducted with the highest possible bias. Figure *24* illustrates the results of an irradiation of the same test structure as described in the preceding two tests. The only parameters that change here is the temperature during irradiation. First, the purpose of this test was to understand if high temperature has a positive or a negative effect on the junction. Figure *24* show that the 100°C irradiation is definitely the most unfavorable outcome and change the behavior of what has been observed at 25°C. Instead of having the "classic" behavior of a strong increase, a peak and a decrease in a leakage current, a plateau is observed following the attainment of the maximum peak. Furthermore, the maximum value of the leakage is reach well before the classic case which in function of the bias is between 30-60Mrad. At 100°C test the maximum value of leakage is reach after ~2Mrad, meaning that the high temperature has a double negative effect. This effect seems to tells that 28nm technology might be sensitive to "true"dose rate effect.

Indeed, these isolated PN junction were irradiated at higher temperature to investigate the potential competition between charge generation-recombination but also dose rate sensitivity. Temperature increase is really important to simulated "low dose rate" equivalent experiment because the time to reach UHD with a low dose rate is time consuming. The isolated PN junction were instead irradiated at different biases (shown in Figure *23*) and temperatures in Figure *24*. Elevated temperature irradiation is a technique used to evaluate the presence of true DR effects in electronic components through high dose-rate tests [20]. Finally some more information on "true" dose rate effect will be published in RADEC 2024 with [21]

3.4.4 Annealing

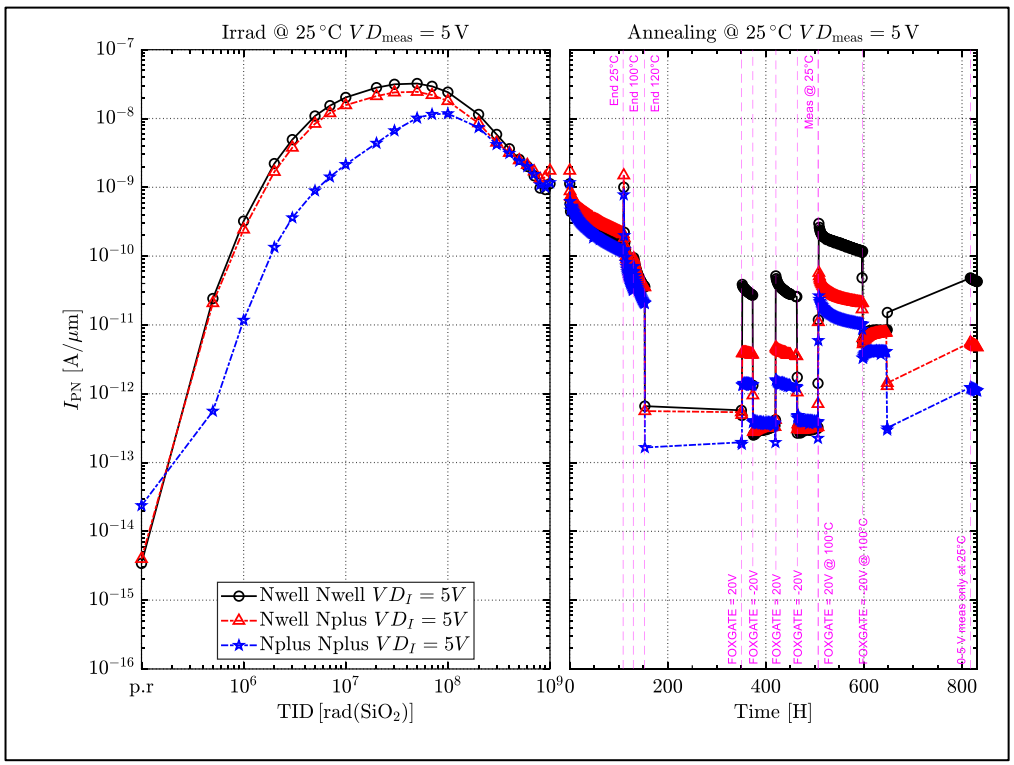

Figure 25 - 1Grad Irradiation of a PN junction and annealing at different temperature and bias configuration during ~800H

The right side of Figure *25* show the annealing experiment after irradiation. The first point of the annealing corresponds to the last point of irradiation. As it was for the irradiation test, each marker corresponds to a measure and each line corresponds to a space in time which here is called annealing. From the first point of annealing to the "end 25°C" purple line there is 109H and every measurement are separated by 1H. From these 109h, it is clear that the annealing process is slow. Right after the "end 25°C" the temperature is increase from 25°C to 100°C and a jump in the leakage current is observed. This increase in the leakage current of the diode was already observed in the p.r. value in Figure *24*, this is a temperature related effect. The 100°C duration was 20h and then there was 1 day at 120°C. As a result, the leakage current for the Nplus is less than one order of magnitude above p.r. value leakage meaning that the Nplus almost completely recover. For the two Nwells the result is different, there is approximately two order of magnitude difference between the p.r. leakage and the end of annealing where the last point is taken at 25°C and is located just after the "end 120°C". Two observations can be made in this state: The first observation is that with a temperature in the range of 100-120°C the annealing is much faster than at 25°C which is expected. The second is that there is a doping effect which allows highly doped material to recover faster than the less doped ones as it was mentioned earlier.

After temperatures annealing, a bias annealing test was done. Note that this test was done approximately 1 week after the temperature annealing one, which explain the important gap between the two measurements. The first point of the bias test and the last point of the temperature test are done in the same temperature and bias condition which confirmed the fact that the annealing at 25°C is slow. In the bias annealing test, the bias at the gate is 20V or -20V and the measurement (see *Figure 14*) is untouched. When the bias during the annealing is 20V at the gate, a jump in the leakage current is

observable in Figure *25* and the opposite effect is visible when the gate is at -20V. This test was done to understand in a deeper way the physics of the defect located in the STI as shown in Figure *26* and at the interface. The bias test duration was approximately 1 week long. The second part was to do the same test but at 100°C which is the third increase in leakage current that is visible in the Figure *25* which start at ~500h and finish at ~650h. It is also important to observe the shape of the Nwell black curve, which seems to decrease with the time seems to be instable recovery, because the last measurement point at 650H approximately is at the same level than the one at 150h before any treatment.

Finally, the last measurement of Figure *25* are only a 5V measurement and this was done to confirmed that the measurement bias even if this is short ~10s per well has an influence on the leakage current. The bias of the PN junction for the last measurement which start after 800h only take two values 0V and 5V. The value of the leakage corresponding to the 5V measurement is $\sim 6 \times 10^{-11}$ A/µm. However, for the measurement which has a progressive bias at the PN junction with a start at 0V with 100mV step increase until 5V the value of the leakage current is almost 10 times higher $\sim 5 \times 10^{-10}$ A/µm and this means that the measurement has an effect. Furthermore, it is crucial to highlight that this observed phenomenon is not a consequence of annealing between two points over time, because in Figure *25* it is visible that the point taken in the same bias condition and temperature at ~650H are in the same order or magnitude for each well in comparison with the one at 150H. The conclusion is that the bias has strictly no influence on the recovery even after weeks at +/- 20V at the gate.

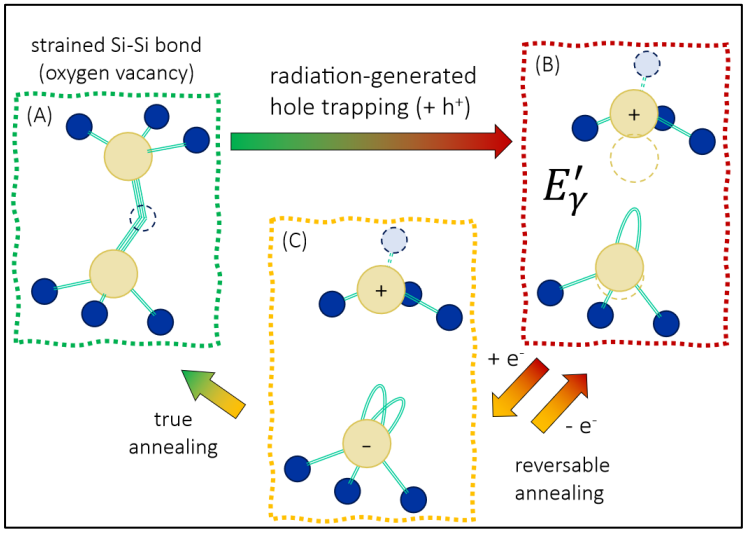

Figure 26 - Reinterpretation of a similar figure produced by Lelis and co-workers in *[22]*.

Regarding the non-annealing effect of the bias even at +/-20V at the gate the preferred hypothesis is that of reversable annealing as it is shown in Figure *26*, where few part of the STI are incomplete and looks like (A) before any radiation. In (A) the structure has a design defect i.e. an oxygen is missing leading to an $Si - Si$ covalent link. This link is anormal in amorphous glass, in theory, every Si atoms are connected to 4 oxygens atoms. These two Si atoms are then far away from each other. When this $Si - Si$ covalent link is irradiated and broke as shown in (B), the energy needed to "repair" the link (B) → (A) is important in the microscopic scale. During the experiment of Figure *25*, even with 20V at the gate and 100°C was not enough energy to make a stable covalent link, leading to think that the recover structure was looking like (C) only, where one Si atom become an ion Si^- and the global structure is neutral because the other ion is Si^+.In other words, instead of having a "true annealing" with a covalent bond between the two Si atoms, the hypothesis is to have "reversable annealing" with 2 non stable Si ions.

Ultimately, as mentioned black and red curves are identical devices, but have a different "bias" response. This is why another test bench was run with a voltage sweep at the gate from -35V to 35V and a hysteresis curve was observed, this hypothesis is discussed in future work Section of Chapter 5.

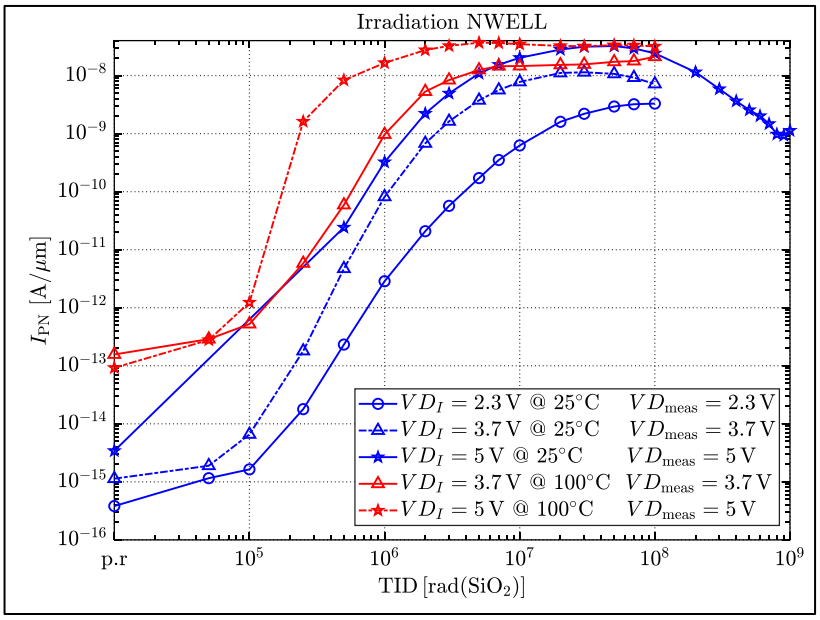

Figure 27 - 1Grad and 100Mrad test at different temperature and bias configuration

Figure *27* show the evolution of the leakage current in function of the TID at different bias and temperature during irradiation. Every results describe earlier are visible on Figure *27*, however the measurement point is different. Indeed, in this case the measurement value (VD_{MEAS}) is the same as the irradiation bias value (VD_I), which is important, because the purpose of a DC-DC converters is to deliver a constant continue bias. In other words, except if the DC-DC broke, it is not possible to bias at 5V in the middle and bottom stages and vice versa. To give a simple example, measuring at 5V the 2.3V bias Nwells during irradiation will just give a worst-case scenario of what can happen if the measurement was at 2.3V, but has no chance to happen physically in the IPOL-5V device. Even with the real condition measurement show in Figure *27*, the trend is the same i.e. lower bias induced less leakage and higher temperature induced more leakage. The blue curves represent the leakage current evolution at 25°C in function of the TID of the $N_{WELL} - P_{SUB}$ of the FOXFET structure. To obtain the leakage current flowing in the device, which has been identified as the potential failure cause of IPOL-5V, the curves will be normalised with the real perimeter of the $N_{WELL} - P_{SUB}$ pMOS transistors. This normalization is possible because the leakage current from one structure to the other is proportional to the perimeter as shown in Equation (8).

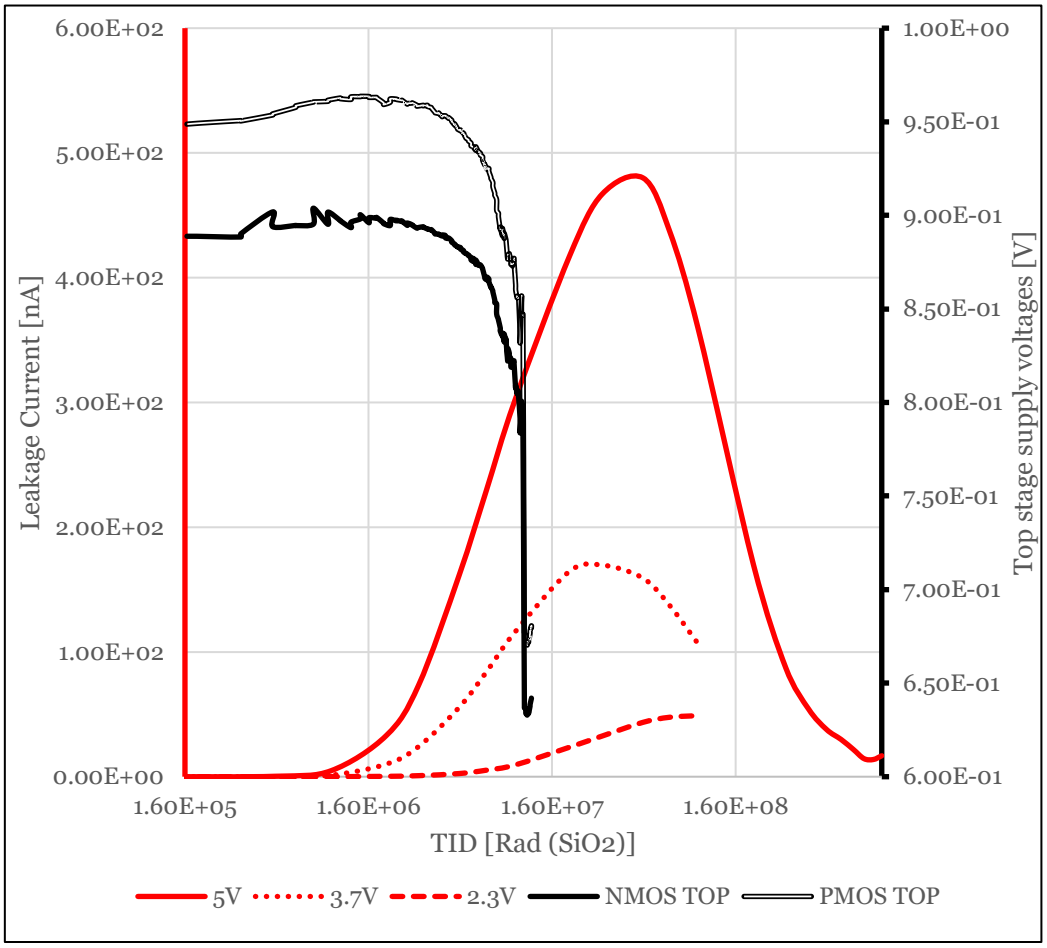

Figure 28 – Conversion between the normalized current of the irradiated PN junction of Figure 29 with the transistor perimeters of IPOL-5V

As mentioned, each of the irradiation results of the PN junctions described below is normalized by a perimeter given in (2) (3) and (4). This perimeter is specific to the diode, however the perimeters of the N_{WELL} and N_{PLUS} of IPOL-5V are different. It is therefore possible, using the irradiation data from the PN junctions, to transpose the exact well of the IPOLs using (8).

$$\frac{I_{\mathrm{PN}}}{L_{\mathrm{PN_{perimiter}}}} \times L_{\mathrm{IPOL_{perimiter}}} = I_{\mathrm{IPOL}} \qquad (8)$$

Where I_{PN} is the leakage current of the PN junction irradiated in Figure *18*, Figure *23* and Figure *24* from $N_{\mathrm{WELL}} - P_{\mathrm{sub}}$. $L_{\mathrm{PN_{perimiter}}}$ is the perimeter of the diode defined in (2), (3) and (4) for every structure. $L_{\mathrm{IPOL_{perimiter}}}$ is the perimeter of the well structure in IPOL-5V. and finally I_{IPOL} leakage current between $N_{\mathrm{WELL}} - P_{\mathrm{sub}}$ in IPOL-5V.

As a consequence of (8), it is possible to normalize the PN junction current with the perimeter of the leaky pMOS transistor, which is contained in IPOL-5V. The pMOS leakage is shown thank to every red curves. The continue, dotted and dashed lines represent the leakage current of the N_{WELL} pMOS at 5V, 3.7V and 2.3V respectively. The black curve represents the voltage drop visible in Figure *12*. It is clear that if the leakage

current between $N_{\mathrm{WELL}} - P_{\mathrm{sub}}$ above 300nA, an important voltage drop of 300mV for the 5V bias curve is observed. In Figure *28*, the 300nA of leakage current is reached approximately at 10Mrad, which corresponds to what has been observed during IPOL-5V irradiation campaign. Moreover, the 5V bias during irradiation transposed curve allows to better understand why the IPOL-5V irradiation recovers after 150 Mrad. The leakage current failure only occurs above 300 nA, but after 150 Mrad the leakage current is below 300nA, the chip "recover" and work properly.

The conclusion of Chapter 3 is that after an irradiation campaign of IPOL-5V and several simulations a critical point was suspected to be the reason of the failure. This suspected point was the $N_{\mathrm{WELL}} - P_{\mathrm{sub}}$ structure located inside a pMOS transistor. After an irradiation campaign on $N_{\mathrm{WELL}} - P_{\mathrm{sub}}$ structures located in FOXFET transistor and transposition of the leakage current of the irradiated diode to the $N_{\mathrm{WELL}} - P_{\mathrm{sub}}$ of the pMOS, results show that the irradiation induced leakage current i.e. above 300nA can cause an important drop of 300mV leading to a failure of the chip. The correlation between the experimental data and the suspected structure provides evidence that this pMOS $N_{WELL} - P_{SUB}$ structure is sensitive to radiation and may result in the failure of IPOL-5V for use in the HL-LHC.

Chapter 4: Ultra High Doses on 28nm CMOS technology

In this chapter, an UHD experiment to test the survivability of the 28nm CMOS technology is reported. This experiment was the most time-consuming because the final TID was 5Grad, and the annealing test was about 2010h at different temperatures i.e. from 25°C up to 100°C. Knowing the dose rate and the measurement time, from Chapter 2, the irradiation time can be easily calculated: 833.3 h, which corresponds to ~35 consecutive days. Moreover, they were 54 irradiation steps of approximately 20min each, which increased the duration of the first step of this experiment by 18 h, in the end this irradiation campaign lasted almost 36 days non-stop. Regarding the annealing, it lasts 2010h with the exact same measurement, the annealing took ~84 days and they was 517 measurements, meaning ~7 days of measurement. Finally, this experiment lasted ~127 days. Furthermore, for UHD test in 28 nm, the RINCE and halo effects appear to be the most prominent, whereas the RISCE effect is nearly undetectable. In general, in 28 nm technology, the STI exerts a considerable influence[23][24][25] .

4.1 Transistor layout and biases

4.1.1 layout

A simplify 3D representation of transistors that have been irradiated are depicted in Figure *29*. The most important point is that every chip is surrounded by STI, and this will have a really important effect in leakage current increase with the TID. Secondly, there are two highly doped regions called n+, they are identical and represented the drain and the source. The two other regions called LDD are low n-doped regions with several advantages describe in [26]. In addition, there are also spacers but they have a negligible influence for 28 nm technology. Finally in light grey there are halos. Halos are made to reduce the leakage current of transistors, short channel effect ,and tend to increase the threshold voltage of the transistor [27] . Note that the chip represented in Figure *29* is a long device i.e. halos are far from each other. In the case of a short device, halos from the drain and the source can overlap leading to a highly p-doped region in the middle of the channel and vice versa for a pMOS as shown in Figure *30*. [24]

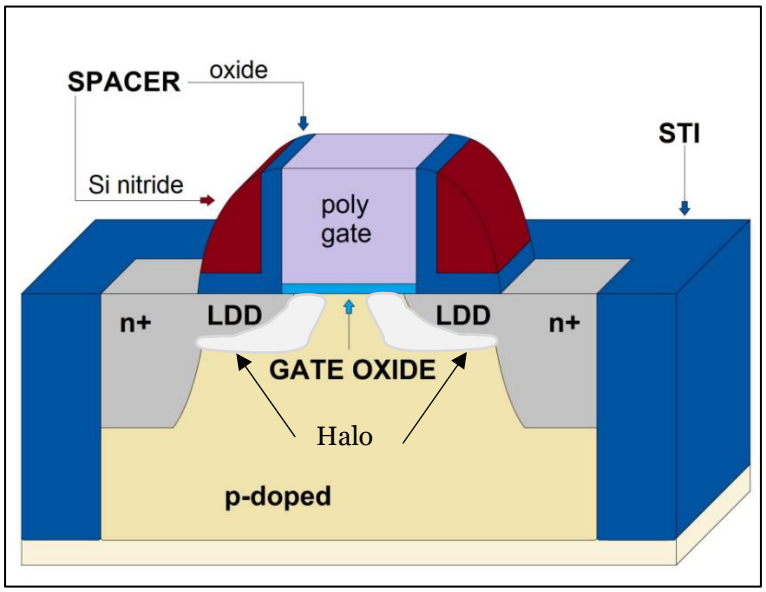

Figure 29 – Schematic representation of a nMOS transistor. *[3]*

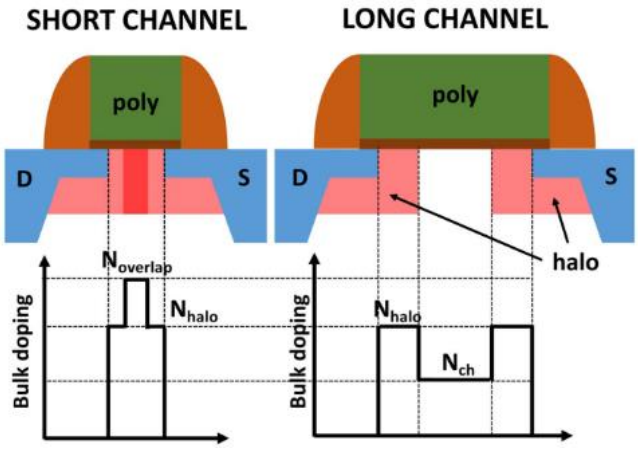

Figure 30 - 28-nm pMOSFET structure with nonuniform doping distribution of the bulk due to the halo implantations. In the short-channel transistor, the drain halo can overlap with the source one, whereas in the long-channel transistor, halos are confined in the lateral regions of the channel. Diagram from *[24]*

4.1.2 Experimental bias and analysis parameters

This test was done on 10 nMOS and 10pMOS of different sizes as described earlier in Chapter 2. However, all the transistors were biased either in diode configuration, i.e. with the gate and drain biased at 0.9V and the source grounded, or in onlyVGS configuration with only the gate biased at 0.9V, and the drain and source grounded.

As only transistors have been subjected to irradiation, data analysis is conducted using ID-VG as depicted in Figure *31*. The two-color bar represents the bias value at which the leakage current and the on-state of the transistors have been measured.

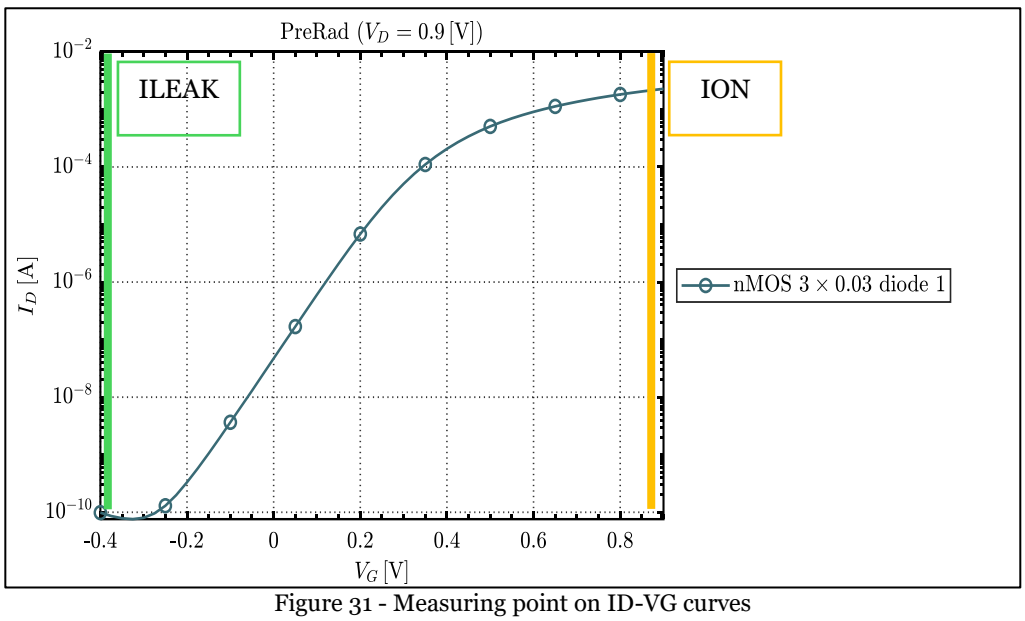

Figure 31 - Measuring point on ID-VG curves

In addition, Figure *31* shows 3 regions. First, between -0.4V to -0.2V which corresponds to the off-state of the transistor. The second described by Equation (9) corresponds to the linear region from -0.2V to 0.3V. The last described by Equation (10) corresponds to the saturation region between 0.3V to 0.9V.

$$I_D = \frac{W}{L} \times \mu_n \times C_{ox}(V_{GS} - V_{Th}) \times V_{DS} \quad (9)$$

$$I_D = \frac{W}{2L} \times \mu_n \times C_{ox}(V_{GS} - V_{Th})^2 \times (1 + \lambda V_{DS}) \quad (10)$$

Where W is the channel width, L is the channel length, μ_n is the mobility of electron, C_{ox} is the capacitance of the oxides, V_{GS} is the gate source voltage, V_{Th} is the threshold voltage of the gate, V_{DS} is the drain-source voltage and finally λ is the channel length modulation coefficient.

Finally, for nMOS devices, 4 parameters will be analyzed: ILEAK, ION, ΔV_{th} and gm. 3 parameters for pMOS devices: ION, ΔV_{th} and gm. ION and ILEAK are shown in Figure *31*. ΔV_{th} is the absolute value of the threshold voltage shift and $gm = \frac{\partial I_{DS}}{\partial V_{GS}}$.

Note that, ILEAK is not analyzed for pMOS. Indeed, pMOS are, by structure, resistant to leakage current induced by radiation. In nMOS the leakage current is due to an accumulation of positive charges in the STI as shown in Figure *32*.

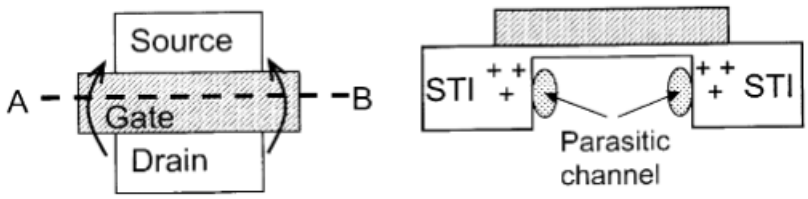

Figure 32 - Top view of an open-layout NMOS transistor (left). On the right, the same transistor is viewed from the source or drain. *[8]*

Positive charges act like a positive voltage source on each side of the transistor, and the STI acts like a gate for the parasitic transistor. When enough positive charges are accumulated in the STI, the silicon crystals become inverted and current can flow from drain to source. These transistors are called parasitic transistors and the gate voltage is controlled by the TID. In other words, if the dose is increased, the leakage path will continue to expand and becomes stronger, and saturation is not anticipated. [28].

However, in pMOS devices, the charge flowing from the drain to the source are holes. These holes are already positive, so when there is an accumulation of positive charges in the STI due to irradiation, the parasitic path is more “off” and acts as a stronger barrier to the hole from the drain. As there is a negligible leakage current for pMOS transistors, this parameter is not analyzed.

4.2 Results and discussions

This section will present nMOS and pMOS results after a 5Grad test. As said in Chapter 2, there are different transistor sizes i.e. W/L = 100/30 *nm* and W/L = 3/0.03 μm and W/L = 0.1/1 μm nMOS and pMOS. In this section RINCE and radiation effect on halo are observed.

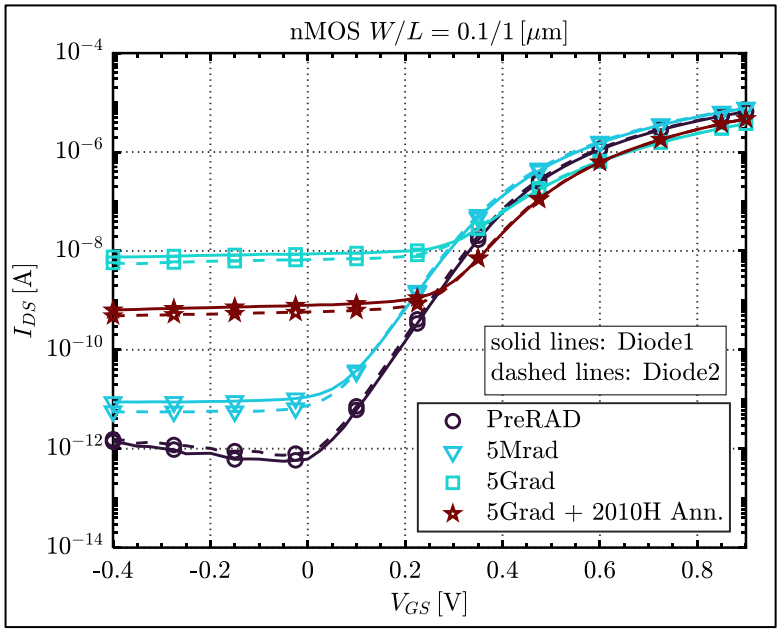

Figure 33 - Long and Narrow ID-VG curves of a nMOS in function of the TID and annealing time

Figure *33* and Figure *34* show an ID-VG curve representing the worst-case scenario per CMOS type i.e. the W/L = 0.1/1 μm size of nMOS and pMOS transistor in diode configuration.

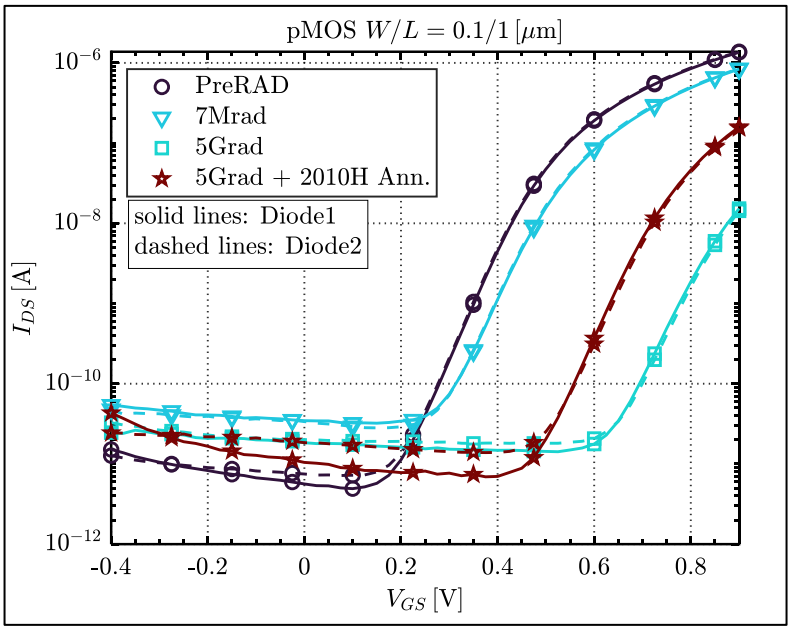

Figure 34 – Long and Narrow ID-VG curves of a pMOS in function of the TID and annealing time

4.2.1 Results nMOS: ILEAK, ION, gm and V_{TH} shift

1- Transistor dimensions: $W/L = 3/0.03\ \mu m$

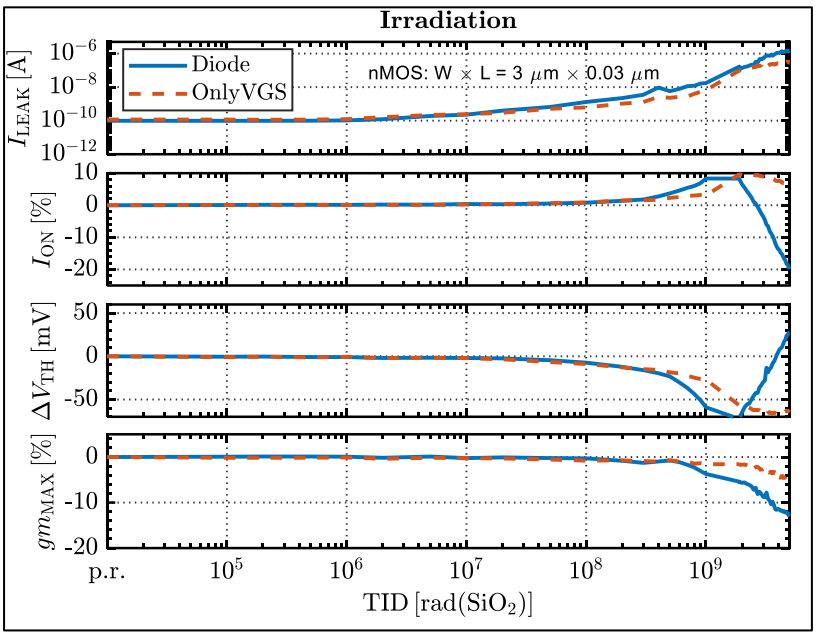

Figure 35 - nMOS maximum width and minimum length 5Grad irradiation in two different bias configurations

Figure *35*, show the irradiation results of 5Grad of the $3\mu m/0.03\mu m$ transistors biased onlyVGS and diode configuration described in Section 4.1.2. First the leakage current monotonically increase until the maximum doses of 5Grad. Moreover, the amount of leakage between diode and onlyVGS is comparable, meaning that there is a limited bias effect for the leakage current.

Regarding the ION, or the current flowing through the channel when the gate is biased at 0.9V, a clear bias effect is visible. The diode configuration in blue, shows 3 regions. The first one, from 0 to 500 Mrad during which the ION is constant around the p.r. value. The second region start at 500Mrad, the ION increases from 0% to 10% until reaching ~1Grad, this phenomenon is probably due to the positive charges present in the gate oxide or the High-k material, which act as additional voltage sources on top of the voltage at the gate. This effect seems to be confirmed by looking to the ΔV_{TH} curves. When the threshold voltages decrease the ION increase while the gm remains constant or varied by 1% even at 1Grad The ION increase between 0 to 1Grad is clearly due to threshold voltage shift the two curves are symmetric.

In addition, the plateau seen in the ION graph between 1-2Grad for the diode configuration device is not a physical effect, but it is due to a measurement failure. The measurement is then correct from 1.9Grad to 5Grad, the chip was disconnected and connected again.

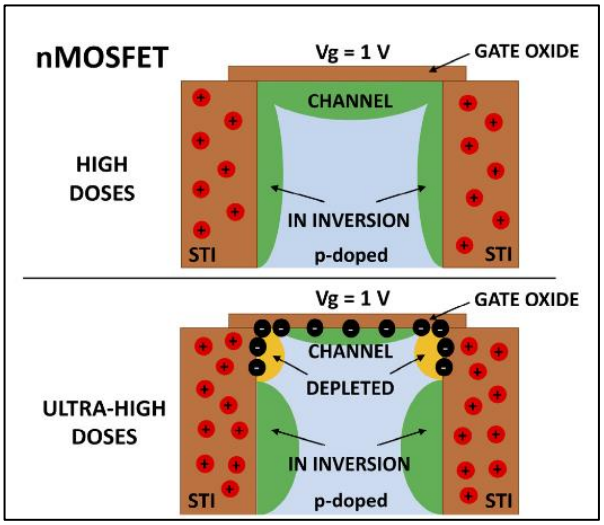

Figure 36 - Conceptual cut view of a nMOS transistor with the STI sidewall at the edge of the channel. *[28]*

After 2 Grad still for the diode configuration, there is a strong decrease in the ION. The prevailing hypothesis is that activation of interface traps as explain in Figure *21* play a dominant role. Interface traps exhibit a distinctive signature effect, namely an increase in the threshold voltage and a reduction in transconductance shown in Figure *36* by the yellow region. This yellow region is supposedly responsible of the effective channel width degradation [28].

Ultimately, onlyVGS and diode configuration appears to exhibit a similar behavior, characterized by three distinct regions in the ION, ΔV_{TH} and gm. Initially, there is an increase in the ION, accompanied by a decline in the threshold voltages. This is followed by a subsequent rise and fall in the ION, and a similar but opposite oscillatory pattern is observed in the threshold voltage. Nevertheless, the aforementioned regions are shifted, necessitating a larger dose to observe the same effect between only VGS and diode bias configuration. This leads to the conclusion that the diode configuration represents the worst-case scenario. Quantitatively, there is approximately 25% difference between ION and onlyVGS configuration.

2- Transistor dimensions: $W/L = 0.1/0.03\ \mu m$

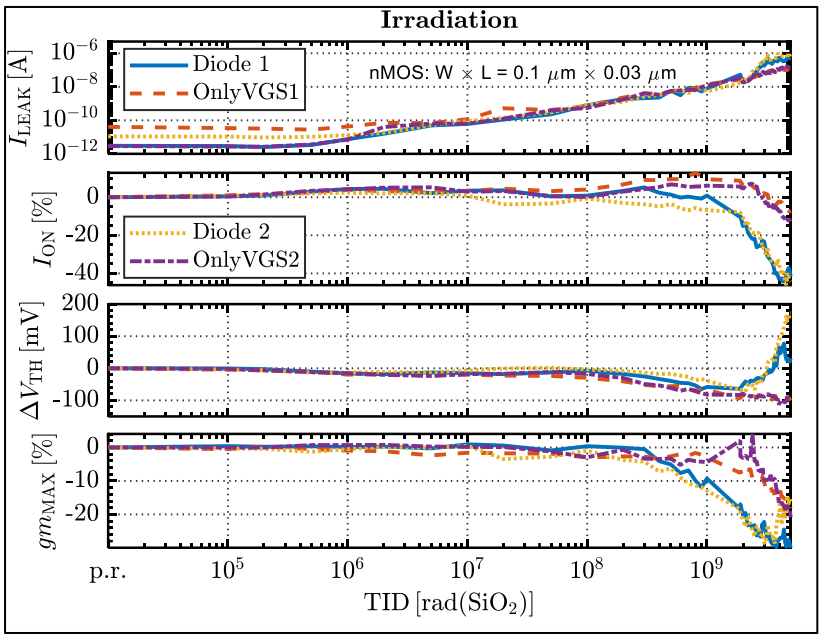

Figure 37 - nMOS minimum size irradiated at 5Grad at different bias configuration

The observations made of the maximum W and minimum L are also evident in the minimum size transistors depicted in Figure *37*. First, leakage current monotonically increases for the same reason. Leakage current between diode and onlyVGS reach the same order of magnitude after 5Grad i.e. the influence of the bias during irradiation is negligible. Second, ION and ΔV_{TH} has opposite behavior, the decrease of the threshold voltage is due to oxide trap while the increase of the threshold voltage and decrease of *gm* is due to the activation of interface trap explained in Figure *21*. Finally, the gm, ΔV_{th} and ION are much worst for the diode configuration than onlyVGS one. The conclusion is the same for the minimum size, diode configuration is the worst-case scenario.

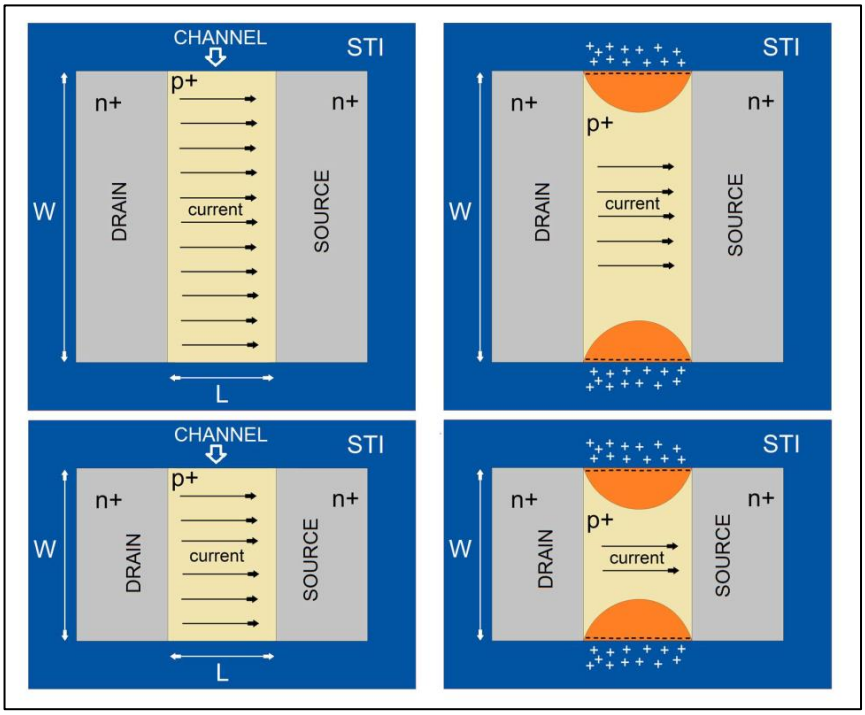

Figure 38 - Top view of a transistor, on the left side of the figure is depict the normal behavior of the transistor. On the right side the RINCE effect is shown by the orange part by the reduction of the channel width because of charges traps in the STI *[3]*.

RINCE, occurs when the transistor width is small [1] [3], in this case the transistor width is 100nm. Figure *38* shows top views of transistors of different width but identical length. The top left diagram of Figure *38* shows a transistor type similar to the one in Figure *35*. The top right transistors show the same transistor in which after a certain TID. Holes trapped in oxides traps induced by radiation are represented by a "+" symbol. These holes close to the channel tend to invert a part of the channel symbolized in orange with "-"symbol. For thick transistor, the ratio between the orange region and the full width of the transistor is close to 0 i.e. the RINCE effect is negligeable. However, when the thickness W of the transistor is too small, the ratio between the orange zone and the full channel W becomes non-negligible. As the current can only flow in the non-orange region, it can no longer flow properly from drain to source.

3- Transistor dimensions $W/L = 0.1/1\ \mu m$

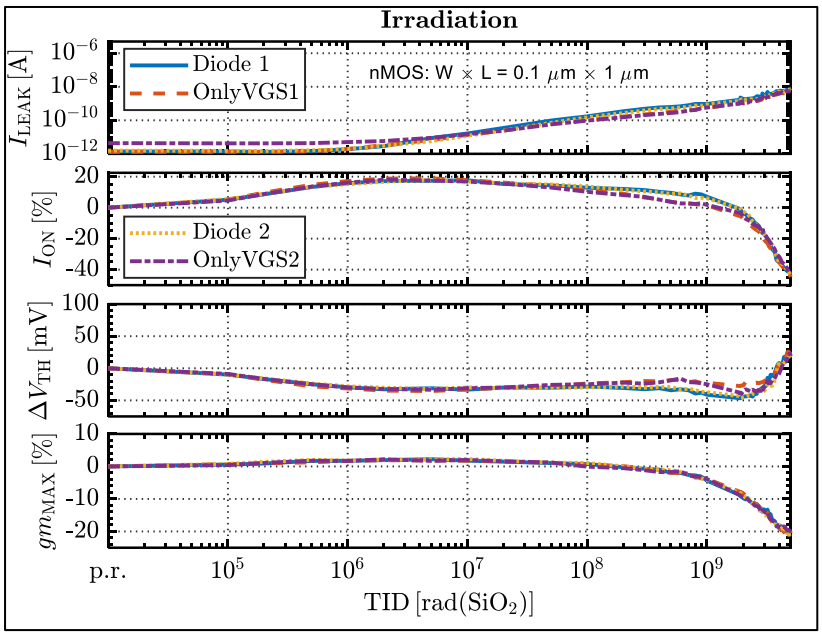

Figure 39 -nMOS minimum and width maximum length 5Grad irradiation in two different bias configurations

Every observation regarding the leakage current made for other devices are valid for long and narrow device illustrated in Figure *39*.However, the increase in the ION happens much faster than in the 2 previous devices i.e. 10krad instead of 1Grad. There is still a correlation between $\Delta V_{TH}, gm$ and ION i.e from 10krad to 10Mrad there are a lot of holes trapped in the oxide that increase the current value flowing through the channel. Then from 10Mrad to 2Grad there is a clear decrease in ION while ΔV_{TH} seems to be stable around its minimum value -40mV and gm is also stable, excepted from 1 to 2 Grad where a 10% decrease is visible. As a result, the dominant effect for this portion of the curve seems to be RINCE. Finally, ION and gm decrease monotonically from 2Grad to 5Grad until reaching -40% for ION and -20% for gm, while ΔV_{TH} increases from -40mV to +40mV independently of the bias configuration, indicating for this curve portion a dominant effect of the activation of interface traps. Finally, this led to the conclusion that there is no bias effect during irradiation for long and narrow devices.

The general conclusion for nMOS devices, regardless of size, is that the maximum degradation on the ION is -50%, i.e. every transistor survives even at 5Grad.

4.2.2 Results pMOS: ION Transconductance and threshold voltage shift

1- Transistor dimensions $W/L = 3/0.03\ \mu m$

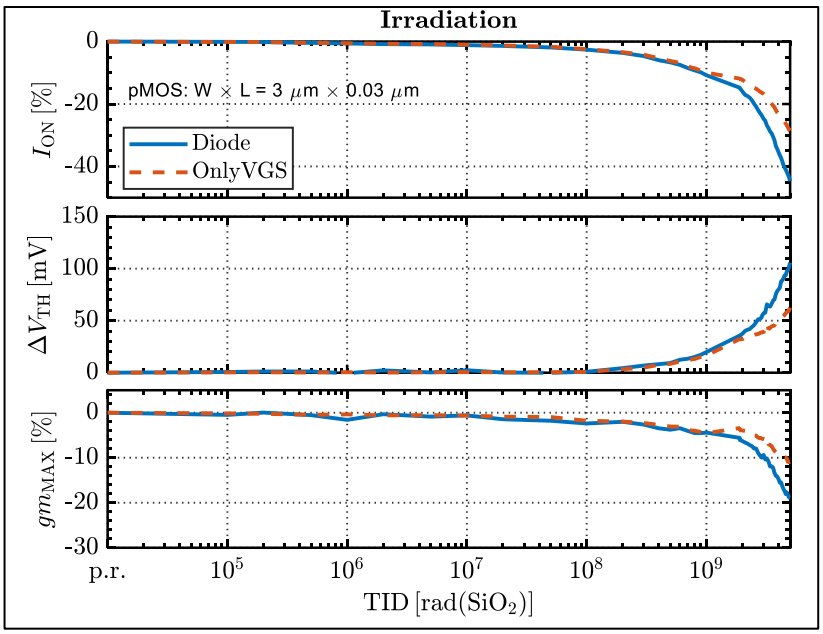

Figure 40 - pMOS maximum width and minimum length 5Grad irradiation in two different bias configurations

2- Transistor dimensions $W/L = 0.1/0.03\ \mu m$

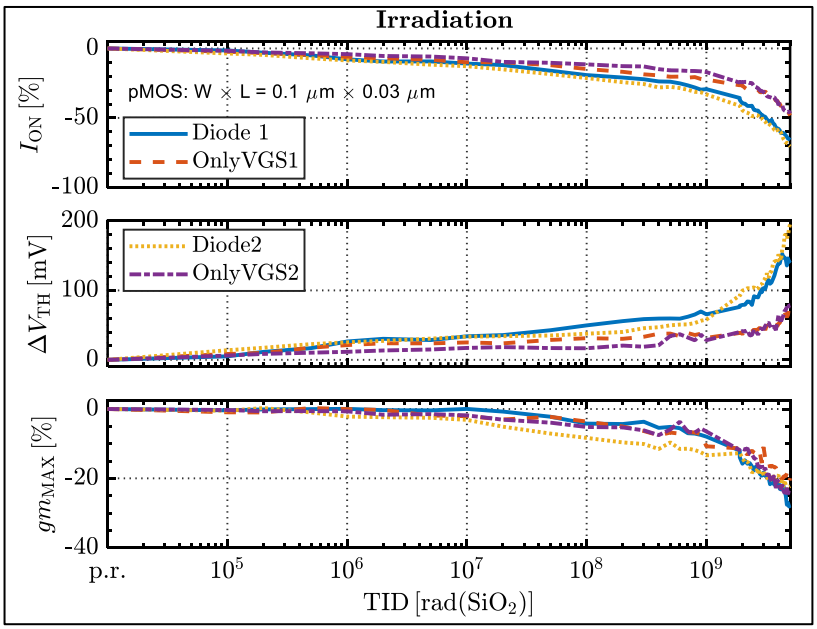

Figure 41 - pMOS minimum size length 5Grad irradiation in two different bias configurations

3- Transistor dimensions $W/L = 0.1/1\ \mu m$

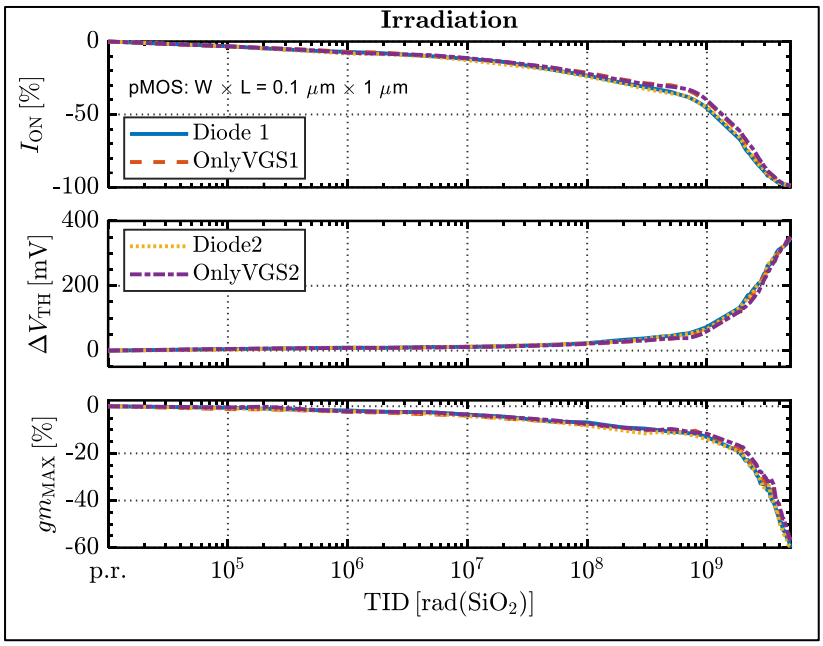

Figure 42 - pMOS minimum and width maximum length 5Grad irradiation in two different bias configurations

Regarding the pMOS, every size and bias configuration follow the same trend i.e. a monotonic decrease in the ION and *gm* while ΔV_{th} increases as shown in Figure *40*, Figure *41* and Figure *42*. The best-case scenario seems to be the short and thick transistor in the Figure *40*, the ION value decrease from 0% to -45% and -30% for diode and onlyVGS configuration respectively. The worst-case scenario is the long and narrow and device which reaches a degradation of 99% from Table *1*. Transistors length seems to have an impact i.e. short channel tends to have a worst case in degradation which is the diode, while the long channel reaches the same degradation level independently of the bias configuration as depicted in Figure *42* and in Table *1*. Finally, the important increase in the ΔV_{TH} and opposite effect for ION and *gm* between 1 to 5Grad is due to a scale effect.

pMOS transistors do not have a rebound effect due to positive charges (holes) as observed in nMOS. Indeed, instead of having a beneficial effect by combining the effect of the gate voltage and the holes trapped in the oxide, the effect will be the opposite: holes will act as a “brake” on the negative gate voltage. So, the voltage, which was originally -0.9V for pMOS, will for instance, after 5Grad be equal to -0.8V for the diode configuration for the maximum width transistor discussed in Figure *40*. Moreover, hydrogen transportation is impossible. In fact, all voltages in pMOS are opposite to the one in nMOS. If in nMOS protons are able to travel to the interface, this is mainly due because the voltage at the gate pushes the positive charges to the interface i.e. protons or holes [16]. However, in pMOS, the protons will be attracted by the gate which is negatively biased i.e. depassivation is not possible. This is why pMOS transistors have an ION degradation twice as high as for nMOS transistors of the same dimensions.

4.2.3 Annealing

Table 1 resume the p.r. 5Grad irradiation and end of annealing results. This part will mainly be focus on the annealing effect.

Type	Size ($W \times L$)	Bias	Meas point	p.r.	5 Grad	End of Ann	ILEAK 5Grad/ ILEAK Ann
nMOS	0.1 μm × 0.03 μm	Diode	ILEAK [A]	7.07 × 10^{-11}	7.08 × 10^{-7}	5.76 × 10^{-7}	1.23
			Ion [%]	0	-43.05	-10.21	
		Only VGS	ILEAK [A]	2.18 × 10^{-11}	1.09 × 10^{-7}	2.07 × 10^{-7}	0.52
			Ion [%]	0	-9.92	7.27	
	3 μm × 0.03 μm	Diode	ILEAK [A]	9.85 × 10^{-11}	1.50 × 10^{-7}	3.03 × 10^{-7}	0.50
			Ion [%]	0	-19.83	-16.89	
		Only VGS	ILEAK [A]	1.17 × 10^{-10}	2.88 × 10^{-7}	7.68 × 10^{-8}	0.37
			Ion [%]	0	5.94	4.20	
	0.1 μm × 1 μm	Diode	ILEAK [A]	1.46 × 10^{-12}	6.66 × 10^{-9}	5.60 × 10^{-10}	11.89
			Ion [%]	0	-43.37	-29.19	
		Only VGS	ILEAK [A]	2.83 × 10^{-12}	5.40 × 10^{-9}	3.23 × 10^{-10}	16.7
			Ion [%]	0	-42.76	-27.85	
pMOS	0.1 μm × 0.03 μm	Diode	Ion [%]	0	-68.23	-70.11	
		Only VGS	Ion [%]	0	-47.54	-39.56	
	3 μm × 0.03 μm	Diode	Ion [%]	0	-44.75	-55.58	
		Only VGS	Ion [%]	0	-28.60	-29.46	
	0.1 μm × 1 μm	Diode	Ion [%]	0	-98.92	-88.51	
		Only VGS	Ion [%]	0	-98.68	-90.47	

Table 1 – Table showing the full leakage currents for nMOS at p.r. maximum TID and after more than 2000H of isothermal annealing cycles lasting several days at different temperatures ranging from 25°C to 100°C. Note also that the ratio between maximum TID and the end of annealing is shown in the very last column on the right.

First, the annealing test has a complex structure. After the radiation stop, approximately 3 weeks of annealing were one under bias at 25°C before changing the position of the chip to the annealing setup (see Chapter 2) and start an isothermal annealing. The first step of the isothermal annealing was to increase the temperature from 25°C to 40°C. This step last for 1 week. Then, the temperature was increase to 40°C to 50°C for one week and so on until 80°C. Note that from 80°C to 90°C and from 90°C to 100°C the test was reduced to half a week. The objective of the experiment was to ascertain whether holes trapped in silicon dioxide are capable of recovery following exposure to 5Grad. Finally, for minimum size and maximum length, 2 transistors were irradiated with the same bias configuration i.e. 2 in Diode and 2 in onlyVGS configuration. Values on Table *1* are the average of the two.

Table *1* shows the p.r. 5Grad and after annealing result. Let's first focus on the leakage current in green for the nMOS devices. The last column shows the ratio between max TID. Following the conclusion of the annealing process, the maximum reduction in leakage current was observed to be approximately 15 times less than the 5Grad leakage current after 2010 hours of annealing with temperature variations. In other words; leakage current anneals slowly even in the best case.

Annealing for nMOS ION is able to recover by 33% for diode configuration 20% for $W/L = 0.1\ \mu m \times 0.03\ \mu m$. Regarding $W/L = 0.1\ \mu m \times 1\ \mu m$ the annealing is about 15% for both bias configurations. However, the diode and onlyVGS configuration of the $W/L = 3\ \mu m \times 0.03\ \mu m$ transistors recovers 3 and 1.5% respectively.

For pMOS transistors, the ION annealing is around 10% for $W/L = 3\ \mu m \times 0.03\ \mu m$ in diode configuration but also for $W/L = 0.1\ \mu m \times 1\ \mu m$ transistors in both bias configurations and for $W/L = 0.1\ \mu m \times 0.03\ \mu m$ onlyVGS configuration. Regarding $W/L = 0.1\ \mu m \times 0.03\ \mu m$ transistors, the recovery of diode configuration is negligeable i.e. 2% like $W/L = 3\ \mu m \times 0.03\ \mu m$ onlyVGS case.

The general conclusion regarding the annealing of transistors after an irradiation at 5 Grad is that it is extremely slow for both types, i.e. nMOS and pMOS. The chips will be at a temperature of -30°C in the HL-LHC, so annealing should be even slower in real operating conditions.

Overall, several points have to be noted for this experiment. First, 28nm CMOS technology seems to be really radhard, because even after 5Grad of radiation only the long and narrow ION pMOS was 99% degrade. Secondly, even after a long post TID thermal treatment at different temperature, the annealing remains small for the ION of both transistor type. Finally, nMOS seems to have negligible annealing for the leakage current in comparison with the important increase induced by the TID.

Chapter 5: Conclusions and future works

Over the thesis, two different experiments were done for two really accurate purposes. The first, described in Chapter 3, was about a DC-DC converter called IPOL-5V. IPOL-5V will be used at different locations within the HL-LHC but the maximum expected dose is around 1Grad. During an irradiation campaign IPOL-5V fails between a certain doses range, i.e. 10 Mrad to 150 Mrad, before it starts working again up to 1Grad. Following the completion of the irradiation campaign, a simulation campaign was initiated. This involved the injection of several currents, which were empirically determined, with the objective of simulating the TID effect in multiple nodes of the three-stage of IPOL-5V. Simulation campaign shows that, the internal circuit of IPOL-5V has several sensitive nodes especially some Nwell of pMOS transistors. This injected current was simulating $N_{\text{well}} - P_{\text{sub}}$ leakage and once it reaches 300nA a voltage drop was observed. It was hypothesized that the voltage drop was the cause of the IPOL-5V failure. As previously stated in Chapter 3, the 300nA is a leakage value that was only attainable due to the higher voltage of the IPOL-5V top stage. Following the hypothesis of a leakage current increase between $N_{\text{well}} - P_{\text{sub}}$, an irradiation campaign was initiated on the PN junction inside a FOXFET transistor which has the same $N_{\text{well}} - P_{\text{sub}}$ structures to confirm that the cause of the IPOL-5V failure is coming from this pMOS.

During the irradiation campaign 3 chips were irradiated. As previously stated in Chapter 3, the chip is composed of 33 wells, including 22 with a lower doping level, designated as Nwell, and 11 with a higher doping level, designated as Nplus. In addition, every measured leakage currents were normalized with the perimeters of each well. The first chip was irradiated at 25°C and up to 1Grad bias at 5V i.e. the same irradiation condition of the top stage of IPOL-5V. The result of this experiment was to confirmed that the leakage current between $N_{\text{well}} - P_{\text{sub}}$ can increase by several orders of magnitude. Experimental data show for $N_{\text{well}} - P_{\text{sub}}$ the leakage current demonstrates an increase from a few femto-amperes to tens of nano-amperes with at a dose of only 10Mrad bias with a bias at 5V. This first experiment also shows that a leakage current peak is reached at 30Mrad before starting an annealing until 1Grad.

Then a second test was done at 25°C and up to 100Mrad with a bias that simulated the bottom and middle stages of IPOL-5V i.e. 2.3V and 3.7V. The behavior of the leakage was similar i.e. a peak was reached at 30Mrad for 3.7V and 60Mrad for 2.3V bias during irradiation. Then, a decrease was observed from 30Mrad or 60Mrad to 100Mrad respectively. The only difference was simply in the value of the maximum peak which was, as expected, lower at 2.3 and 3.7V than the one at 5V (see Figure *17*).

The last experiment was an irradiation test up to 100Mrad at 100°C and bias at 5V and 3.7V. However, the leakage current reached a maximum at only 2Mrad instead of 30Mrad and did not decrease until 100Mrad, i.e. a plateau was observed around the maximum value of the leakage current after 2Mrad. This experiment led to the conclusion that the $N_{\text{well}} - P_{\text{sub}}$ leakage is sensitive to the dose rate effect [20][21]. Although further investigations are required to fully characterize this dependence.

Finally, each normalized leakage current from the 2 irradiations at 25°C of the PN junction structure was normalized to the real perimeter of the Nwell pMOS that was believed to be the cause of the failure. The leakage current data adapted to the IPOL-5V shows that at around 10Mrad a leakage of 300nA is observed leading to the voltage drop previously simulated, the chip was not responding until 150Mrad because the leakage current of the $N_{\text{well}} - P_{\text{sub}}$ was above 300nA. However, as mentioned above, after 150Mrad, the leakage current reaches a value below 300nA, and then, start to operate

again normally. Chapter 3 provides comprehensive evidence to elucidate the underlying causes of IPOL-5V's failure within a specific dosage range and identifies the precise point of failure.

In the Chapter 4, another completely different experiment was done, which aimed to test up to 5Grad the survivability of 28nm CMOS technology to make ASICs for HL-LHC application. This test was necessary for CERN because electronic components and circuits will be exposed to higher doses in function the positioning of the chip inside the particle accelerator experiment. These doses will be greater than 2.5Grad.

This experiment lasted 4 months with almost 1000h of irradiation with measurements and more than 2000h of isothermal cycle annealing. On the tested chip, 20 transistors, 10 nMOS and 10 pMOS with different sizes were irradiated. These transistors were bias following two different configurations i.e. Diode and onlyVGS

The results of this experiment for both bias configurations demonstrate that for the shortest nMOS, the leakage current (ILEAK) exhibits a notable increase from a few pico-amps of leakage at the p.r. value to 1µA of leakage after 5Grad. This signifies a considerable augmentation in the leakage current, with the p.r. value exhibiting a factor of 1 million. The rise in leakage current for the long transistors is observed to increase from pico-amps 10 nano-amps for both configurations, representing a factor of 10 thousand between the p.r. leakage current value and the post-irradiation. Annealing is slow and is about 15 times less current for the best case after 2010h annealing i.e. long and narrow transistors (see Table *1*).

Regarding ION, ΔV_{TH} and gm, several differences were observed. First, short transistors (i.e. L = 30nm) have bias influence, i.e. diode configuration shows a greater ION and gm degradation and a higher ΔV_{TH} increase which was not the case for long (i.e. L=1μm) and narrow configuration. In addition, nMOS transistors, regardless of size, follow the trends of an initial increase in ION due to the holes accumulation in oxide traps and then a decrease due to the activation of interface traps (see Figure *21*). It has been noted that ΔV_{TH} behaved in the opposite way and gm tends to fall after 1 Grad independently of bias configuration and transistors size.

Overall, every nMOS transistors independently of the size and the bias survives to the 5Grad irradiation. The most damaged nMOS for the ION curves was the minimum size diode configuration and long and narrow transistor both bias configuration with a degradation at around -42% after 5Grad. The less damaged one was the short and large in onlyVGS configuration with almost 6% of current increase in comparison with the p.r. value.

As said in Chapter 4, pMOS transistors are generally 2 times more damaged that nMOS for the same doses. pMOS transistors follow exactly the same trends independently of the size i.e. a monotonical decrease from p.r. to 5Grad irradiation. Short pMOS survive to 5Grad irradiation with a maximum ION decrease at -70% for minimum size diode configuration instead of -40.3% in average of onlyVGS configuration and maximum width transistors regardless the bias. Long and narrow pMOS were at -99% ION degradation after 5Grad, leading to the conclusion that the transistors were always off and not usable. Note that for all pMOS, no leakage current increase is reported.

Regarding the behavior of ΔV_{TH} and gm for pMOS transistors, these two parameters followed exactly the same trend, i.e. ΔV_{TH} increased to a maximum at 5 Grad and gm decreased to a minimum due to the build-up of holes in the oxide.

Finally, annealing can be considered as very slow or inefficient for pMOS transistors.

Future works

Hysteresis

Regarding Chapter 3, several experiments can be done to have a better understanding of why the leakage current does not anneal with a significant bias of 20V to 35V at the FOXFET gate. As said in Chapter 3 the favorite hypothesis is that the annealing is not "real" annealing but only correspond to the appearance of a local neutral structure inside the SiO_2. This neutral structure behaves like "real" annealing but when a bias is applied, electrons that are not stable can travels inside the SiO_2 resulting in a strong increase of decrease in the $N_{WELL} - P_{SUB}$ leakage current.

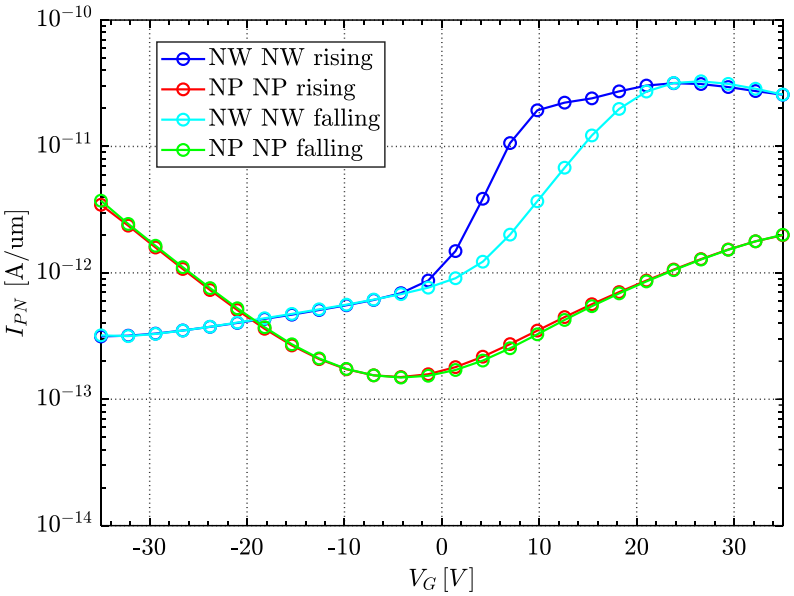

Figure 43 - Sweeping from -35V to 35V and then from 35V to -35V in the gate voltage of two FOXFET transistors, one doped as Nwell and the second doped as Nplus. A hysteresis curve is visible for the Nwell-doped transistor.

The test of Figure *43* was carried out because the red and black curves in Figure *25* behave differently with +20V at the FOXFET gate, even though they are the same two PN connections. This means that the gate, even when it is off, has an effect on the measurement and that the order of the measurement is therefore important. Figure *43* show that with a sweep from -35V to 35V and vis versa, a hysteresis curves is observed for the Nwell. The same effect is visible with gate sweep from -20V to 20V but less pronounced.

Figure *43* seems to be in line with the hypothesis described in the Figure *26* but further investigations are needed.

UHD Variability

For the Chapter 4, a unique test has been carried out. [26] It is not uncommon for electronic components to exhibit markedly disparate behavior, despite originating from the same company, laboratory and production batch. In this case, these irradiated transistors are a very well mastered technology, because they are a commercial device. As previously stated, the objective of this experiment was to investigate a different region at an ultra-high dose However, the fact that a single test has yielded a particular

result does not necessarily indicate that the technology in question will behave in the same manner under all circumstances.

Several other tests can be done to have a better idea of what can happen to 5Grad. However, there may be some time constraint problems, 28nm seems to be sensitive to the dose rate effect, i.e. low dose rate degrades more than high dose rate as explained in Chapter3. The 5Grad irradiation is probably a worst-case version of what will happen at -30°C in real condition in the HL-LHC but further investigation is needed.

As mentioned, the test took around 3000h, a way to reduced drastically the annealing is to do isochronal annealing i.e. i.e. to cycle the temperature from -30°C to 100°C for a few minutes to extract the activation energies of the defects created by radiation in 10-degrees increments, with a measurement at 25°C between each temperature increment. This test can decrease the annealing time from 2000h to 8h. A more detailed description of isochronal annealing is provided in [29] [30] [31].

FCC expected dose

In other hand, the expected dose for the FCC particle accelerator for proton-proton collision can reach 500Grad of radiation after 10 years as shown in *Figure 44*. With the actual irradiation setup install at CERN, 10 years are needed to reach this dose with a continuous irradiation at 6Mrad/h.

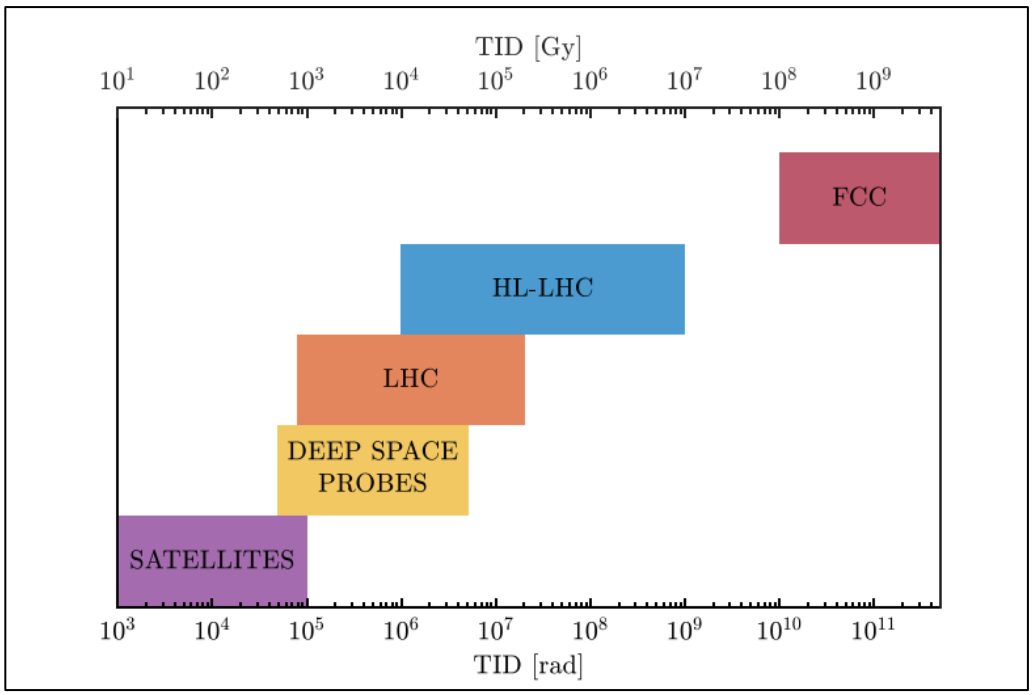

Figure 44- Comparison of TID levels in different radiation environments. The FCC is expected to reach unprecedented TID levels, 500 times higher than those expect in the HL-LHC [3]

The demands of the proton-proton collision for the FCC seem insatiable at the moment. However, new work on even smaller technologies, i.e. finfet transistors, could be significantly more radiation hard than the 28nm technology.

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