Master RADMEP

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TOTAL IONIZING DOSE ANALYSIS OF SAR ADC FOR SPACE APPLICATIONS

Master Thesis Report

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Abstract

This study investigates the performance of a Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) under Total Ionizing Dose (TID) conditions, identifying the TID-sensitive blocks and their impact on overall performance. TID models were developed to simulate two primary effects: threshold voltage shifts in the comparator and leakage current increase in the sampling and capacitor digital-to-analog converter (CDAC) switches. Models were developed based on experimental data from literature, and using a combination of Berkeley Short-Channel IGFET Model (BSIM) device modeling and circuit-level modeling. SPICE simulations, employing transient and spectral analyses, revealed that threshold voltage shifts in the comparator have minimal impact on noise characteristics and overall performance due to the comparator's robust design features. Conversely, leakage effects in the sampling and CDAC switches caused slight deviations in the output signal due to erroneous voltages generated through the switches, resulting in significant degradation in the ADC performance parameters. Combined TID effects revealed further performance degradation due to compounded errors resulting from erroneous voltages fed to the comparator and the TID-induced on-resistance variability of the sampling switches. Results from this analysis provide valuable insights into the SAR ADC's suitability for space applications and highlights the critical effects in the design blocks that significantly impact overall ADC performance under radiation.

Table of Contents

List of Figures

List of Tables

1 Introduction

Analog-to-Digital Converters (ADCs) are integral components in today's technologies, acting as a bridge between the analog and digital world [1]. This conversion is essential because in modern measurement systems, virtually all measured quantities are converted to the digital domain [2], but most real-world signals—such as sound, light, temperature, and motion—are inherently analog. ADCs convert these continuous signals into a digital format that electronic devices and systems can interpret, process, and utilize.

ADCs have been gaining significant ground, with their applications spanning several industries, including instrumentation, sensory-based systems, measurement and control systems, and communications [3]. As more industries continue to gear towards digital transformation, the demand for ADCs with higher precision, faster conversion rates, and lower power consumption, is only expected to rise [4], driving innovations and advancements in ADC design and implementation.

One particularly important area of ADC application is in space operations, in which the ADC is a critical component in the analog front-end of external sensors. The reliability of electronic components is vital for mission-critical operations since it is difficult to interfere with them once deployed [5]. Furthermore, environmental conditions in space are much harsher than on the ground. In addition to significant temperature changes, high levels of radiation present in space drastically affect circuit performance and lifetime [6]. Thus, radiation-hardness of electronics is a primary concern for space applications [7].

To address this concern, this study aims to evaluate the performance of an ADC design under radiation effects. By understanding the impact of ionizing radiation on its critical components, this study aims to ensure the effective application of the ADC in high-performance sensor systems, particularly to the unique challenges of space applications.

1.1 ASYGN

Founded in 2008, ASYGN is a semiconductor design company headquartered in Grenoble, France, with additional operations in Montpellier, France; Copenhagen, Denmark; and Atlanta, USA.

Initially, ASYGN began by building dedicated Design Automation Tools to streamline analog circuit system-level verification. By 2010, it began delivering chip designs to its first customers, until today, where the company has now expanded to providing chip design solutions across four main fields, summarized in Figure 1: radio frequency (RF), sensor interfaces, radio frequency identification (RFID) sensing, and green artificial intelligence (AI).

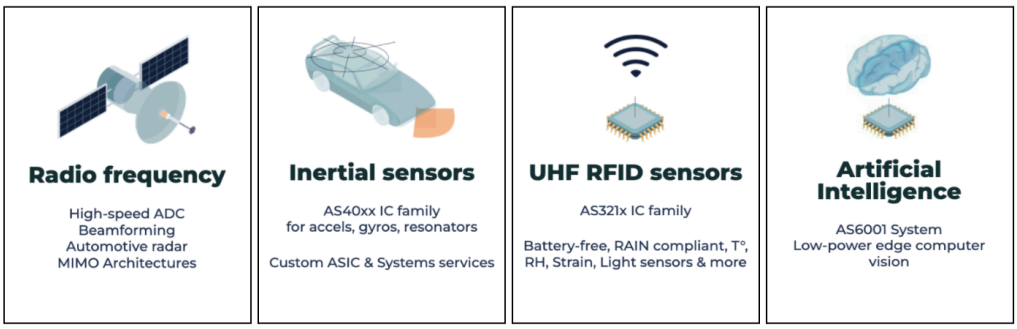

Figure 1. ASYGN's four main fields of chip design solutions

Source: Adapted from [8]

In the sensor interface design solution area, ASYGN provides electronics for high-performance, high-precision, or low-power inertial systems, as well as full-custom integrated circuits to interface with microelectromechanical systems (MEMS) such as accelerometers, gyroscopes, and resonators.

1.2 Context and Objectives

ASYGN's family of inertial sensors are employed in a wide array of applications, ranging from ground applications to aerospace and space operations. The robustness and reliability of these components in different environments, particularly in space where they are exposed to high levels of radiation, is a critical consideration which the company is beginning to explore and, perhaps in the future, thoroughly investigate and actively incorporate in the design.

Within a single system, each component exhibits varying levels of sensitivity to different types of radiation. Furthermore, naturally present radiation differs across various environments, and even within the space environment, multiple radiation effects must be considered, e.g. long-term permanent effects, or short-term instantaneous effects.

To define the scope of the research, this study focuses on the performance evaluation of the Successive Approximation Register (SAR) ADC in the sensor interface, which is responsible for converting analog signals from the MEMS devices into digital data that can be processed by electronic systems. The analysis is performed in the framework of space applications, particularly on long-term permanent Total Ionizing Dose (TID) effects.

The specific objectives of the study are as follows:

1. to identify the TID-sensitive blocks of the SAR ADC and their corresponding physical effects, based on previous literature;
2. to model these effects in SPICE, using both BSIM models and circuit-level modeling;
3. to investigate the individual impact of the critical blocks on the overall ADC performance, through SPICE simulations; and
4. to evaluate the SAR ADC performance under all combined TID effects, through SPICE simulations and spectral measurements.

1.3 Successive Approximation Register (SAR) ADC

The Successive Approximation Register (SAR) ADC is a high-performance, low-power ADC architecture, frequently used for medium to high-resolution applications, typically ranging from 8 to 18 bits, with samples rates under 5 megasamples per second (MSps) [9]. These features make them suitable for applications where minimizing area and power consumption is critical, such as battery-powered instruments, satellite controls, and data or signal acquisition.

Figure 2 illustrates the basic architecture of a SAR ADC. Its key components are a sample-and-hold (S/H) circuit, a comparator, a SAR logic control unit, and a digital-to-analog converter (DAC). This architecture uses a binary search algorithm to convert an analog input to digital data. The conversion process begins by sampling the analog input V_{in}, then comparing the sampled input $V_{S/H}$ with the DAC output V_{DAC}. In the first conversion, the SAR logic unit is initially set to mid-scale, that is 100…000, where the most significant bit (MSB) is set to 1. This sets the DAC output to $V_{ref}/2$ or half of the reference voltage provided to the ADC. If $V_{S/H} > V_{DAC}$, the comparator outputs a logic high (1) and the MSB remains at 1. Otherwise, if $V_{S/H} < V_{DAC}$, the comparator outputs a logic low (0) and the MSB is cleared to 0. In the subsequent cycle, the SAR logic unit moves to the next bit down, sets it to 1, then performs another comparison. This process continues sequentially until the least significant bit (LSB) is determined, resulting in an N-bit digital representation of the input.

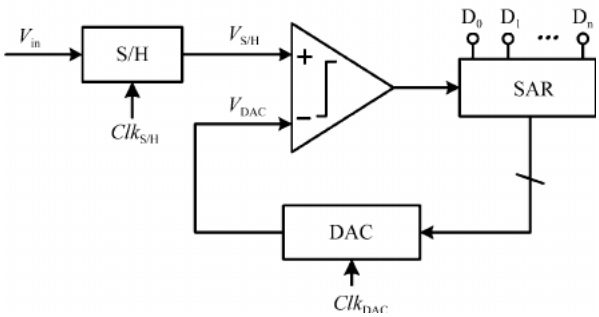

Figure 2. Basic architecture of N-bit SAR ADC

Source: Adapted from [10]

Figure 3 illustrates an example of this conversion, illustrating that an N-bit SAR ADC takes N clock cycles to convert an analog input into an N-bit digital output. The ADC sampling rate F_S, therefore, is only a fraction of the internal clock frequency F_{CLK} which drives the comparison cycles. Thus, while the SAR architecture is efficient in terms of area and power, it poses some limitations on speed and resolution [9].

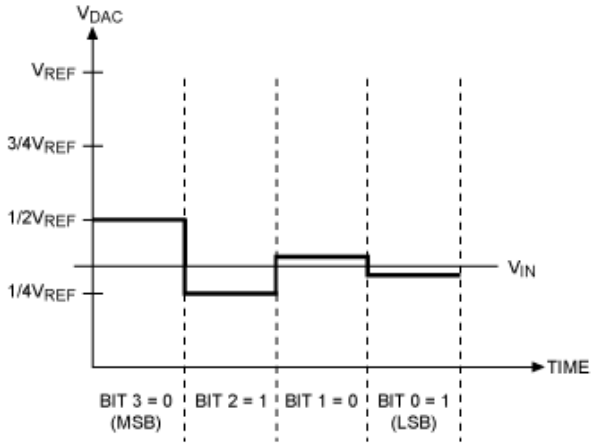

Figure 3. Example of 4-bit SAR ADC operation

Source: Adapted from [9]

1.4 Total Ionizing Dose Effects in Electronics

Electronic components can be subjected to various radiative environments composed of high-energy photons, protons, electrons, neutrons, and heavy ions – where the main particles at play are determined by the environment [11]. In the space radiative environment, these particles are mainly protons and electrons trapped in the earth's radiation belts, heavy ions from cosmic rays, and alpha particles emitted by the sun during solar activities. Depending on the incident particle, the radiation effects can be categorized under two main events: short-term (temporary) single-event effects (SEEs), caused by the interaction of a single particle, and long-term cumulative (permanent) effects due to continued exposure to radiation [7].

SEEs can be caused by a single high-energetic particle, mainly cosmic solar particles and trapped protons in the radiation belts, instantaneously inducing charges in the semiconductor regions of an electronic device. This may lead to temporary effects such as transient currents and bit flips [5]. It is also possible, however, that an SEE causes a hard error on the device and power-cycling is needed to recover it. In the worst case, it can be physically destructive to the device and cause permanent functional effects [12].

On the other hand, cumulative dose effects can be categorized into two: Total Ionizing Dose (TID) and Displacement Damage Dose (DDD). TID is mainly caused by trapped protons and electrons in the radiation belts. While SEE is induced by a single particle strike, TID is caused by numerous particles depositing energy into the device, creating electron-hole (e-h) pairs and trapping charges, typically in the insulator materials of the device, like SiO_2 . This results in variations in the device parameters, possibly leading to functional failure [12].

DDD has similar degradation characteristics as TID. However, it involves a different physical mechanism. It is caused by huge particles, mainly protons, that results in the displacement of nuclei in a material from their lattice position. Figure 4 illustrates the three main types of radiation effects, particularly on a metal-oxide-semiconductor (MOS) structure.

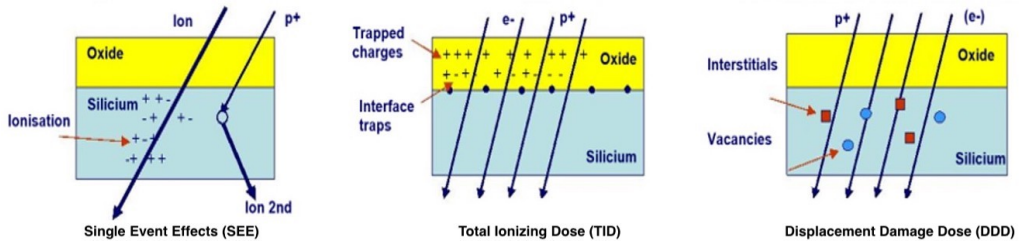

Figure 4. Types of radiation effects in MOS structure

Source: Adapted from [11]

In complementary metal-oxide-semiconductor (CMOS) devices, the energy deposited from TID creates defects in the device through four main physical processes [13], illustrated in Figure 5:

1. electron-hole (e-h) pair generation;
2. electron-hole (e-h) pair recombination;
3. transport of free carriers remaining in the oxide; and
4. formation of trapped charges or interface traps.

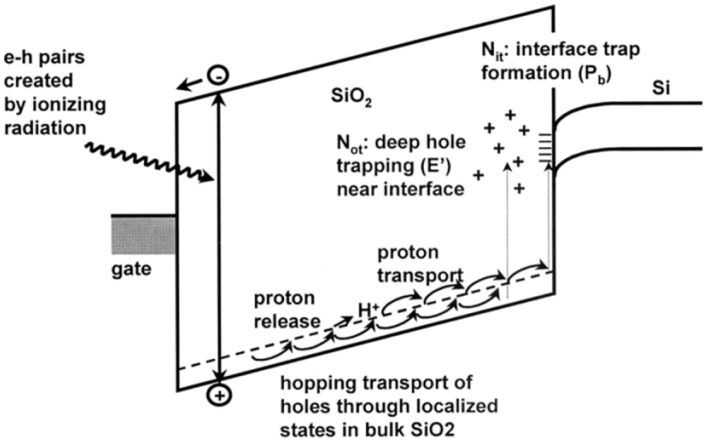

Figure 5. Main processes in TID damage of MOS structure

Source: Adapted from [14]

In CMOS devices, TID generates e-h pairs in the SiO_2 dielectric. These are formed along the tracks of particle strikes, with the e-h pair density being proportional to the energy transferred to the material. Thus, TID is typically expressed in grays (Gy), the SI unit denoting the energy absorbed per unit mass of material. For reference, 1 gray is equivalent to 1 joule of energy deposited per kilogram of the material. However, in the space community, TID is often still expressed in rads. To provide context, 1 rad is equivalent to 0.01 Gy.

Following the generation of e-h pairs, a fraction of these recombine within a small time window [15]. Due to the significantly higher mobility of electrons compared to holes, electrons are rapidly swept out of the oxide. The remaining holes migrate towards deep traps within the oxide bulk or to the Si-SiO_2 interface, resulting in the formation of trapped positive charges [13].

At the device level, this process leads to a negative shift of the transfer curve (drain current I_D vs. gate-to-source voltage V_{GS}) of both n- and p-channel metal-oxide-semiconductor field-effect transistors (MOSFET), as illustrated in Figure 6. Thus, for a fixed I_D, the presence of trapped positive charges shifts the V_{GS} bias point more negative. In NMOS, this manifests as a reduction in the threshold voltage V_{TH} and an increase in the off-state current I_{OFF}. In PMOS, the result is an increase in the magnitude of V_{TH} and a decrease in I_{OFF}.

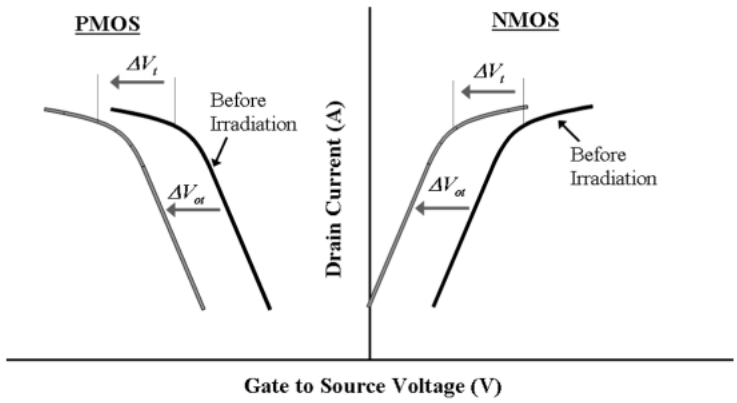

Figure 6. TID effect on MOS transfer curve

Source: Adapted from [13]

While a shift in the transfer curve contributes to the increase of I_{OFF}, radiation-induced leakage current is mainly attributed to the positive charges trapped in the shallow trench isolation (STI) oxide at the transistor edge. This accumulation eventually builds up an electric field that is high enough to create an inversion channel between source and drain through which leakage current can flow, as if it was flowing in two parasitic lateral transistors.

2 Methodology

Most studies on radiation effects on ADCs are conducted using real-life experimental setups, with the fabricated chip exposed under X-ray or gamma ray radiation. While actual tests provide more accurate results, it is challenging to isolate and analyze the effects of radiation on each ADC block separately. In some TID tests, the area to which radiation is applied cannot be controlled [5].

In this study, TID models are developed based on experimental data published in previous literature, in correspondence with the target technology and total dose associated with the application. A combination of device modeling using the Berkeley Short-Channel IGFET Model (BSIM) and circuit-level modeling is developed and introduced to the SAR ADC design to simulate its radiation response.

2.1 TID Effects in 130-nm CMOS Technology

To characterize the overall system response, it is necessary to investigate the TID response at the transistor level of the SAR ADC design, which is implemented in the TSMC 130-nm CMOS standard process.

Previous TID experiments on commercial, non-hardened 130-nm CMOS technology have provided valuable insights. In particular, [16] extends these results by performing measurements on both NMOS and PMOS devices manufactured by different foundries. X-ray irradiation was performed at room temperature, up to a TID of 200 Mrad(Si) in multiple steps, and at a dose rate of 25 krad/min. This dose is sufficient for space applications and, therefore, applicable to our analysis.

Results from [16] revealed a shift in the transfer characteristics of the irradiated NMOS devices, shown in Figure 7, highlighting two primary TID effects: a decrease in V_{TH} and an increase in I_{OFF}. These are mainly attributed to positive charges trapped in the gate oxide and STI oxide, respectively. The degradation values are summarized in Table 1.

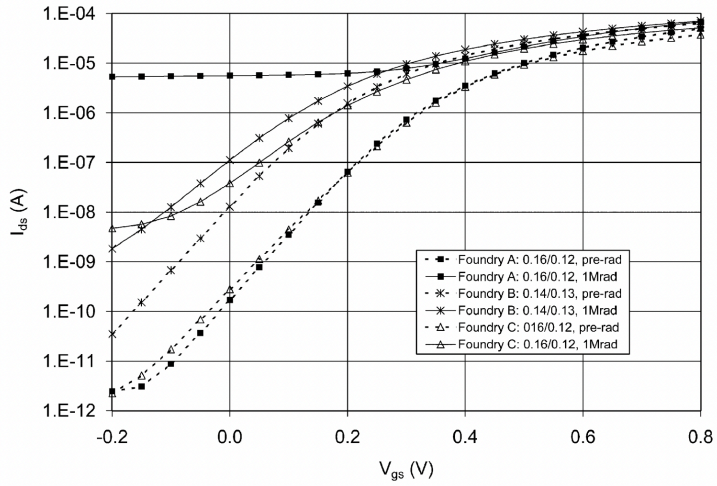

Figure 7. NMOS transfer curve from different foundries, pre- and post-radiation (1 Mrad)

Source: Adapted from [16]

Foundry	TID at max degradation (Mrad)	$\Delta V_{TH,max}$ (mV)	I_{OFF} increase
A	$1-5$	-135	10^4 ×

Table 1. Maximum TID-induced degradation in NMOS

Source: Adapted from [16]

In contrast, tests on PMOS showed only marginal effects under TID, with no leakage current degradation observed and only a negligible shift in the threshold voltage. This is attributed to the PMOS gate bias which is usually negative, resulting in fewer charges being trapped, most of which are far from the Si-SiO_2 interface. Thus, no significant parasitic inversion regions are formed.

Given these results, TID models are developed for two main effects:

1. decrease in threshold voltage V_{TH}; and
2. increase in off-state leakage current I_{OFF}.

Since PMOS transistors have shown negligible effects under TID, these models are only employed in the NMOS transistors of the SAR ADC design, where TID effects are more critical.

Reference TID values for voltage and current are obtained from Table 1, which are in correspondence with the technology and dose applicable to this study.

2.2 Threshold Voltage Shift Model

The V_{TH} shift in the transistor is modeled using the Berkeley Short-Channel IGFET Model (BSIM), a family of MOS transistor models widely used in SPICE simulations for integrated circuit (IC) design [17]. Because it is based on simple device physics and can quickly reflect physical phenomena by automatically calculating device parameters, it is becoming a standard for IC design. Initially implemented in C language, newer BSIM models are now written in Verilog-A, enhancing their adaptability and integration in modern design workflows.

In the BSIM4v4.7 model version [18], applicable to the Process Design Kit (PDK) of the SAR ADC design, the threshold voltage V_{TH} for long and wide MOSFETs with uniform substrate doping is modeled by the equation:

$$V_{TH} = V_{FB} + \phi_S + \gamma\sqrt{\phi_S - V_{BS}} = V_{TH0} + \gamma\left(\sqrt{\phi_S - V_{BS}} - \sqrt{\phi_S}\right) \quad (1)$$

where V_{FB} is the flat-band voltage, V_{TH0} is the threshold voltage of the long-channel device at zero substrate bias, and γ is the body bias coefficient.

If the substrate doping profile is not uniform in the vertical direction, $N_{substrate}$ is defined to be the doping concentration (NDEP) at X_{dep0}, and V_{TH} is modeled by:

$$V_{TH} = V_{TH0} + \frac{qD_0}{C_{oxe}} + K1_{NDEP}\left(\sqrt{\phi_S - V_{BS} - \frac{qD_1}{\epsilon_{Si}}} - \sqrt{\phi_S}\right) \quad (2)$$

where $K1_{NDEP}$ is the body-bias coefficient and $N_{substrate} = NDEP$.

In both equations, a threshold voltage shift can be modeled by introducing a variable V_{tshift} to V_{TH0}, which offsets the V_{TH} of the NMOS by a user-defined value. In the simulator level, this creates a design variable in the SPICE simulation workspace that allows the user to set this value. To illustrate, Figure 8 shows the transfer curve of the NMOS component for V_{tshift} values set from -100 mV to 100 mV, in steps of 50 mV. By setting V_{tshift} to a negative value, the result is a negative shift of the transfer curve observed in actual TID experiments [13, 16].

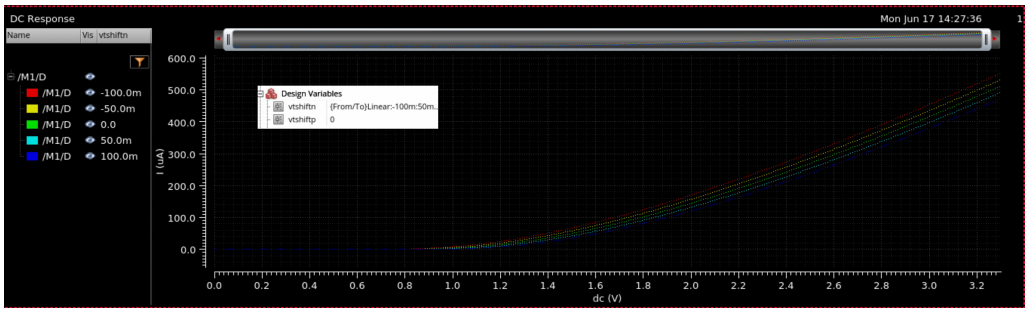

Figure 8. Transfer curve of NMOS for multiple V_{tshift}

In the V_{TH} shift model employed in the SAR ADC design, V_{tshift} is set to -135 mV, obtained from Table 1, corresponding to a TID of 1-5 Mrad.

2.3 Leakage Current Model

The off-leakage current, defined as the current flowing from the transistor drain to source when the gate is off, occurs when the transistor is not in strong inversion and no conducting channel is ideally present between the two terminals. This is often associated with subthreshold current since subthreshold is often the main factor [19].

Figure 9 shows the transfer curve in yellow of a minimum-size NMOS used in the SAR ADC design. At $V_{GS} = 0$, a small leakage current $I_{OFF} = 6.606$ pA is observed. When a radiation-induced threshold voltage shift is modeled by setting $V_{tshift} = -135$ mV, a slight increase in the off-state leakage is observed due to the reduced gate voltage required to invert the channel. However, radiation-induced leakage is primarily related to transistor edge effects, which must be modeled separately.

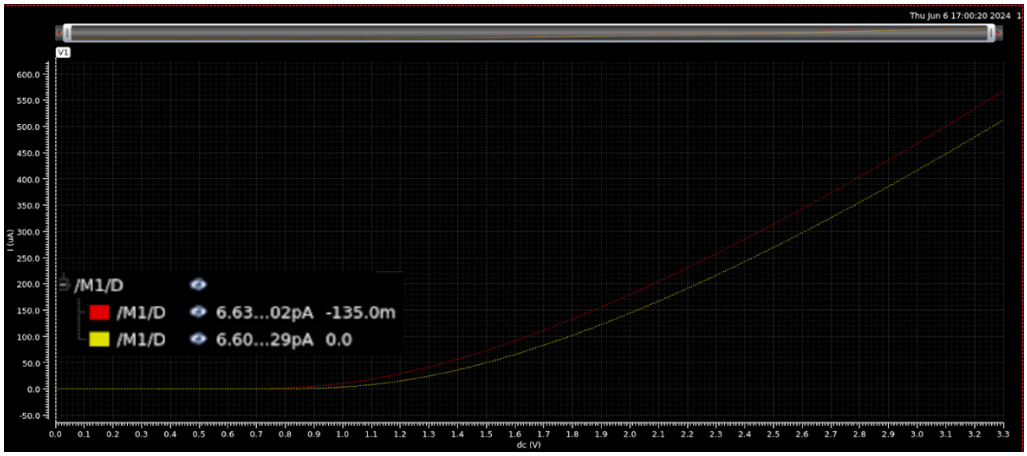

Figure 9. Transfer curve of minimum-size NMOS illustrating off-leakage current for pre-radiation device (yellow) and with $V_{tshift} = -135$ mV (red)

Radiation-induced leakage is modeled at circuit level by adding a DC current source between the nodes that form the leakage path [20, 21], i.e. in parallel with the drain and source of the transistor, as illustrated in Figure 10. Since the leakage current is highly dependent on the transistor size, an exact reproduction of the radiation-induced leakage, by simulation, is not possible. Instead, the radiation response of the device is approximated by adopting values compatible with experimental data reported in previous literature [16, 20], which is the methodology adopted for this model.

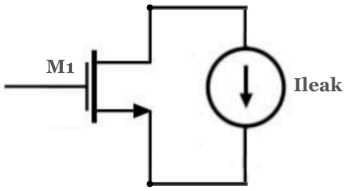

Figure 10. Modeling radiation-induced leakage current in NMOS with parallel current source

In the TID model for leakage, current values are calculated by taking the reported value in Table 1 as the baseline for minimum-size NMOS (W/L = 0.6µ/0.6µ). That is, I_{OFF} increases by 10^4 times, or to 66.06 nA. This value must be scaled linearly with the number of fingers and inversely with the transistor length such that a customized and more accurate leakage model is achieved for each transistor. However, since minimum length and finger number are used in the transistors where leakage is to be modeled, the base calculation, presented in Table 2, is applicable to the design. The calculation yields a leakage current value in the order of magnitude that is comparable with literature for the same technology under similar doses [22].

TID (Mrad)	Width (µm)	Length (µm)	TID leakage current (nA)
1-5	0.6	0.6	66.06

Table 2. Base calculation of TID leakage current in 130-nm CMOS technology

2.4 ASYGN SAR ADC Design

The ASYGN SAR ADC is a 16-bit, 1-MHz ADC with a common-mode voltage (V_{CM}) based switching method and a split capacitor digital-to-analog converter (CDAC) architecture.

Figure 11 shows the circuit diagram of this architecture, which consists of the dynamic comparator, CDAC, sampling switch, and SAR control logic. The ADC is designed using dynamic blocks which allows it to save on DC power consumption. It is high-resolution, medium-speed, high dynamic range, and low-power. While the input is sampled at a rate of 1 MHz, multiple comparison cycles are required to complete a single conversion. Hence, the ADC internal clock frequency is much higher at 80 MHz. To summarize, Table 3 lists the key parameters of the design.

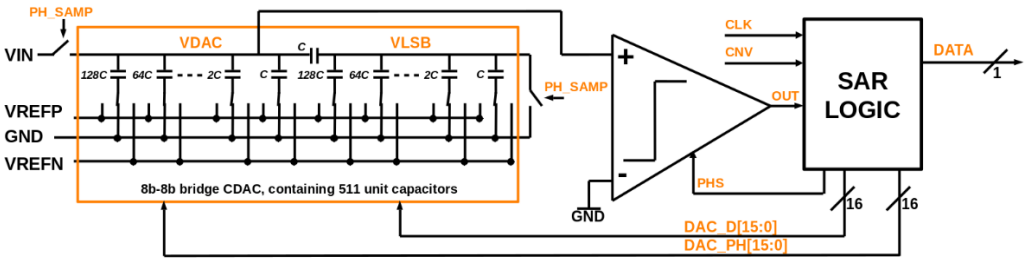

Figure 11. ASYGN SAR ADC circuit diagram

Source: Adapted from ASYGN

Parameter	Value	Unit
Resolution	16	bits
Sampling frequency	1	MHz
Master clock frequency	80	MHz
Supply voltage (V_{DD})	±2.5	V
Analog power consumption	0.26	mW
Digital power consumption	1.13	mW
Reference voltage (V_{REF})	±2.5	V
Full-scale input	10	$V_{pp-diff}$

Table 3. ASYGN SAR ADC design parameters

Figure 12 illustrates the working principle of the SAR ADC. During the conversion (CNV) phase, when $CNV = 1$, the sampling switches (PH_SAMP) close and the input voltage is charged into the DAC voltage (V_{DAC}). During the hold phase, when $CNV = 0$, the sampled input is held on V_{DAC}. In both phases, the output DATA is initially set to 1.

The first comparison is executed in the second rising edge of the clock (CLK) after $CNV = 0$. After some delay, PH_SAMP closes and the 128C bottom plate is switched to the negative reference voltage (V_{REFN}). This sets DAC_PH[15] to 1, making the first MSB conversion and changing the voltage at V_{DAC} to the DAC conversion. In this phase, DATA is set to 0, which signals the header bit of the data sequence.

In the next rising CLK edge, the 64C bottom plate is switched to V_{REFN}, making the $MSB - 1$ conversion. V_{DAC} is changed following this conversion and DATA is set to D15, indicating the MSB.

In the 16^{th} rising CLK edge, the 15^{th} comparison is executed. The 2C bottom plate is switched to the positive reference voltage (V_{REFP}) and the $LSB + 1$ conversion is made.

As with the previous comparison cycles, V_{DAC} is changed following this conversion and DATA is set to D2, indicating the LSB + 2 bit.

In the 17th rising CLK edge, the 16th and last comparison is executed. The C bottom plate is switched to V_{REFN}, making the LSB conversion. V_{DAC} is changed and DATA is set to D1, indicating the LSB + 1 bit.

In the 18th rising CLK edge, when the comparison cycles are completed, all bottom plate switches are set to GND. This restores V_{DAC} to the converted sampled voltage and DATA is set to D0, indicating the LSB.

The whole cycle restarts and the converted sample is held in V_{DAC} until the next CNV rising edge. During this time, DATA is reset to 1.

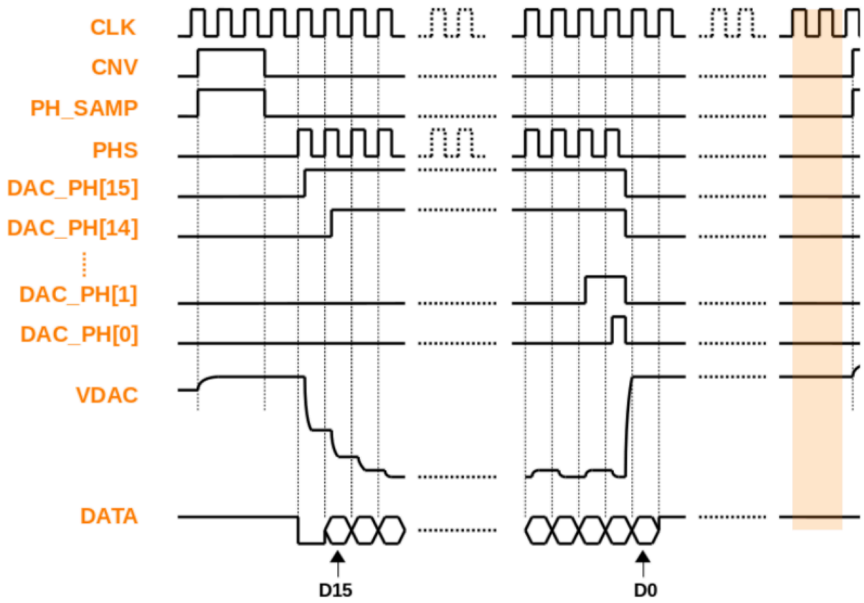

Figure 12. SAR ADC working principle

Source: Adapted from ASYGN

Figure 13 shows the top schematic of the design. A transient analysis of this illustrates an overview of the ADC operation, as shown in Figure 14. The simulation results show how each bit is determined and output sequentially, demonstrating the step-by-step conversion process of the SAR ADC.

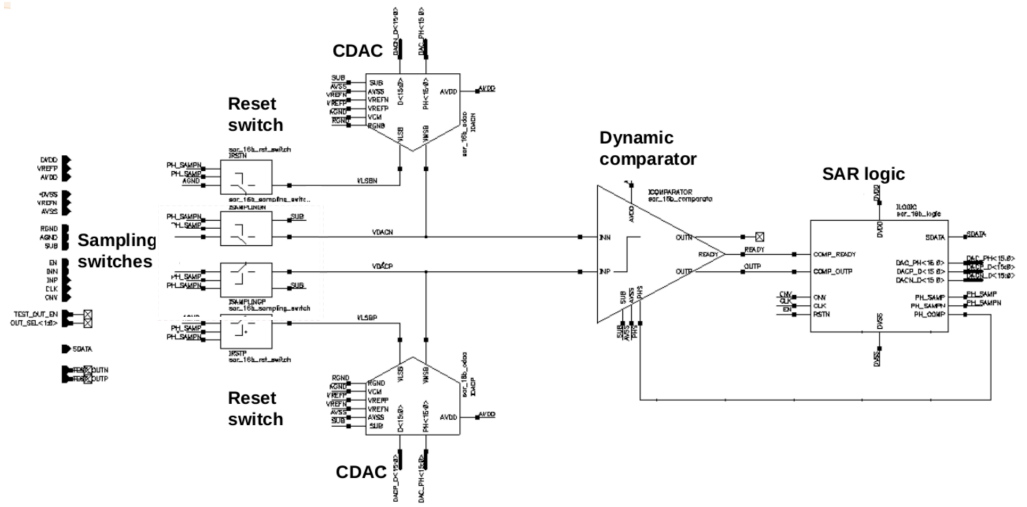

Figure 13. ASYGN SAR ADC top schematic

Source: Adapted from ASYGN

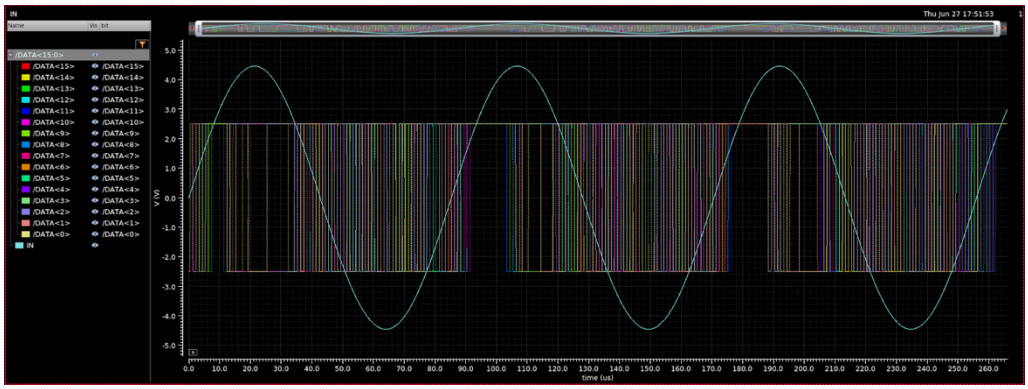

Figure 14. SAR ADC analog input and digital output

2.4.1 Comparator

The comparator is one of the main analog blocks of the SAR ADC. Its main function is to compare the sampled input with the DAC voltage and provide the logic level for the output based on the result. It is therefore fundamental in the binary search algorithm process and is a critical block in determining the ADC's speed and accuracy.

Figure 15 shows the schematic of the dynamic latched comparator in the ASYGN SAR ADC. This architecture is widely used in high-speed ADCs due to its high input impedance, full output swing, and high speed [23]. The differential input pair receives the input signals, with the current switch limiting the flow of current through it. An additional current switch degeneration further limits the sink current to reduce kick-back noise. The central latch then captures and holds the output state after the comparison phase, with the reset switches resetting it between comparisons. The output logic, which includes buffers, then drives the final digital output signals.

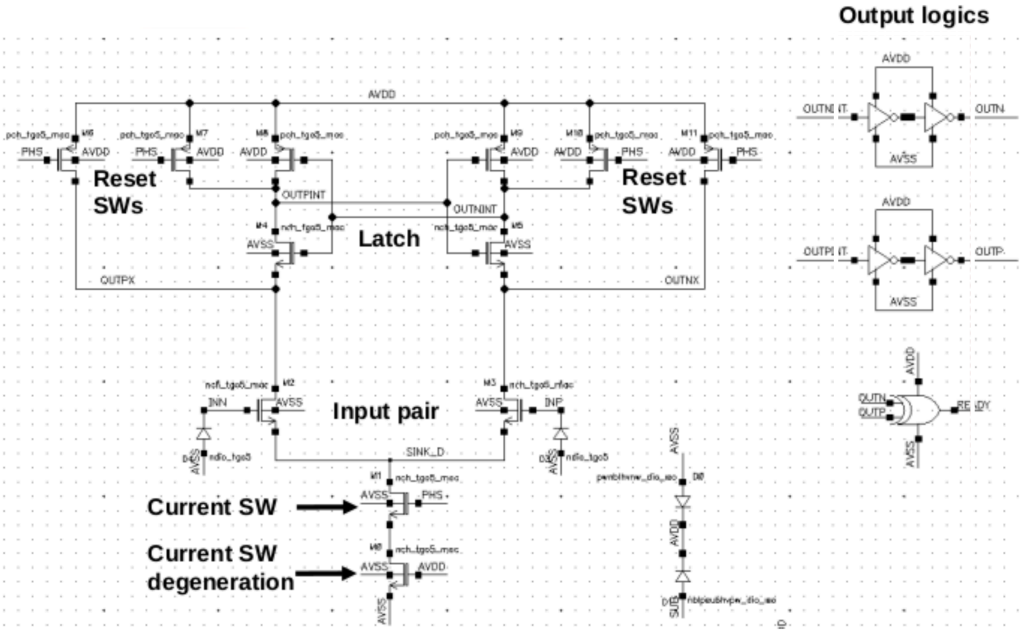

Figure 15. Dynamic latch comparator in ASYGN SAR ADC

Source: Adapted from ASYGN

Radiation studies on SAR ADCs [5, 7, 20] have identified the comparator as one of the critical components under investigation for TID effects, as continuous-time analog circuits have been shown to be particularly susceptible to TID [24]. In [5], simulations modeling radiation-induced offsets in the comparator resulted in bit flips in the DAC output code. In a separate study from [20], simulations modeling leakage, corresponding to doses of up to 1 Mrad(Si), in the NMOS devices of a latched comparator showed no significant effects, with negligible offset and settling time degradation. This is because, for transistors in saturation (or triode) region, leakage current effects are not critical.

Given these results, this study models the TID effects in the comparator by introducing the V_{TH} shift model, developed in Section 2.2, in its NMOS transistors, as shown in Figure 16. This approach allows for a focused evaluation of how V_{TH} shifts affect the comparator performance. Since there is not enough published data to sufficiently model variability, this model simply assumes a uniform V_{TH} shift across all NMOS.

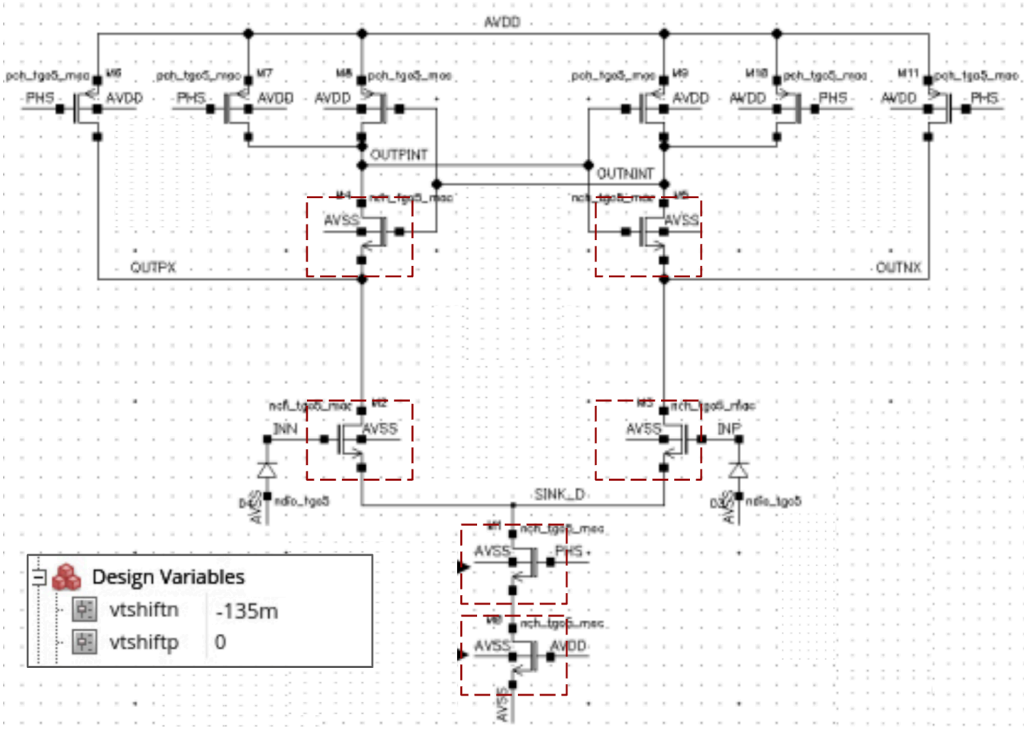

Figure 16. TID model in dynamic latch comparator

2.4.2 Sampling Switch

In the SAR ADC, the sampling switch connects the input signal to the capacitive matrix during the sampling phase, charging the capacitors to the input voltage. After the sample phase, the switch disconnects, isolating the capacitor and holding the sampled voltage steady. This held voltage is then used for the successive approximation conversion process. Thus, the precise operation of the sampling switch is crucial for maintaining the integrity of the sampled signal.

The sampling switch is often implemented as a bootstrap switch since the voltage at this node may reach values higher than the reference voltage provided. Figure 17 shows the schematic of the sampling switch in the ASYGN SAR ADC.

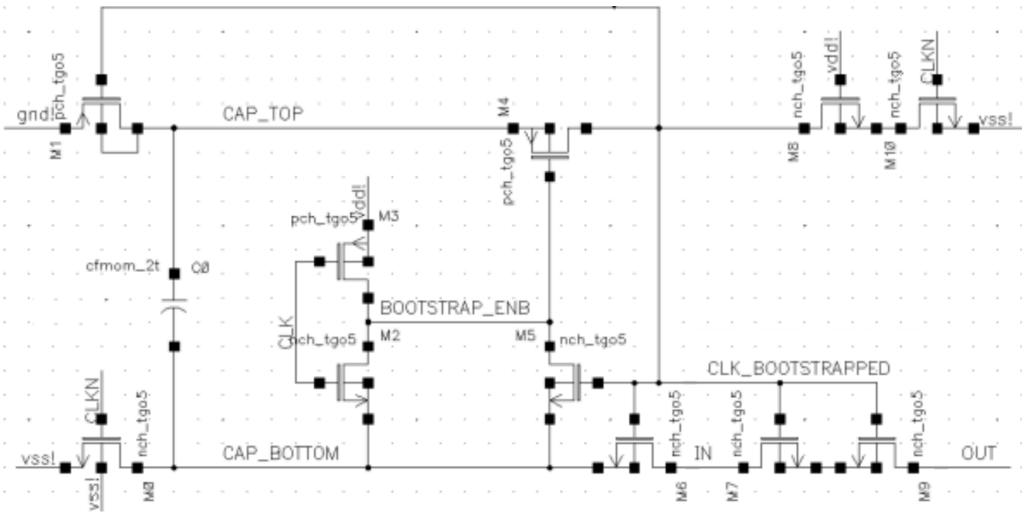

Figure 17. Sampling switch in ASYGN SAR ADC

Source: Adapted from ASYGN

In [20], the main failure mechanisms from TID irradiation were attributed to the sampling switch mainly due to radiation-induced leakage paths formed to the capacitor array - introducing errors in the generated output voltage and resulting in linearity degradation. Voltage errors were mainly observed in the top-plate sampling switch connecting the array to the input voltage V_{IN} (see Figure 11) as this causes charge to leak from/to the capacitors.

Given these results, the leakage current model developed in Section 2.3 is employed in the NMOS of the sampling switches, as shown in Figure 18, to model the TID-induced leakage in the sampling switch. The leakage value presented in Table 2 is used.

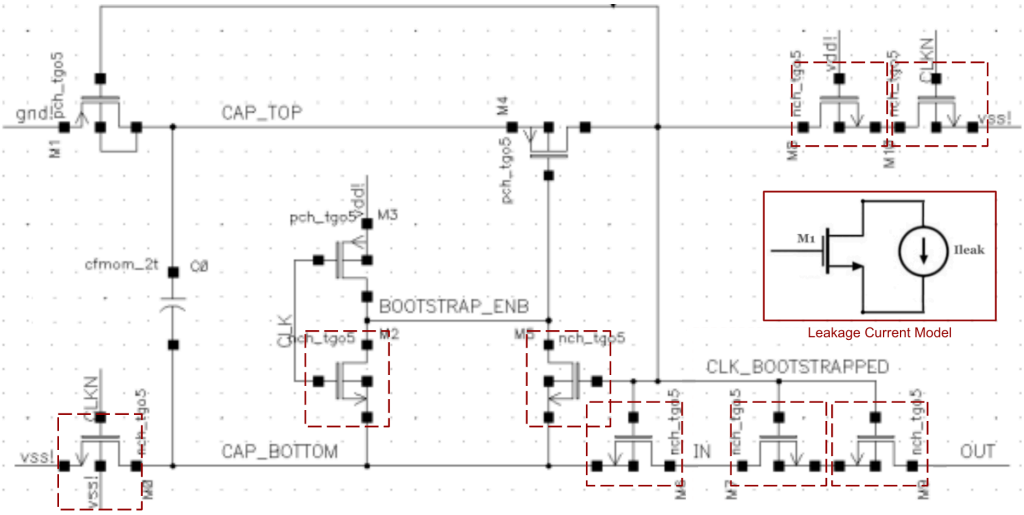

Figure 18. Leakage current model in sampling switch

2.4.3 Capacitor Digital-to-Analog Converter (CDAC)

The Capacitor Digital-to-Analog Converter (CDAC) employs the principle of charge redistribution to generate an analog output voltage provided to the comparator. Thus,

the SAR architecture requires that both the DAC and the comparator are as accurate as the overall system [9].

Figure 19 shows the schematic of the 16-bit single-end split CDAC of the ASYGN SAR ADC. The split CDAC is a popular DAC architecture that splits the conventional binary-weighted capacitor array into two branches that are connected through a bridge capacitor. This approach scales down the total capacitance value, reducing die area and improving speed [25].

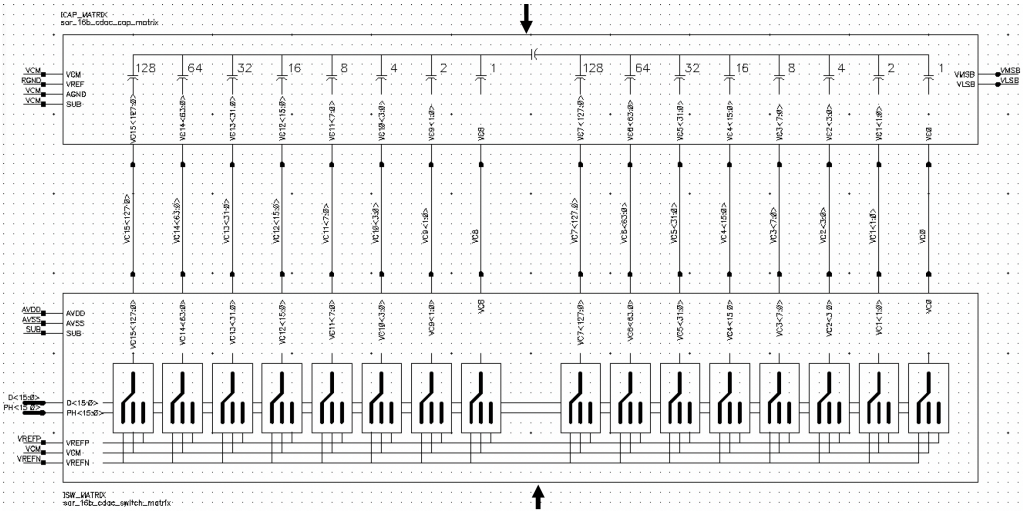

Figure 19. 16-bit single-end CDAC in ASYGN SAR ADC

Source: Adapted from ASYGN

CDAC simulations performed in [20] showed that the main failure mechanism originates at the capacitor array, with the capacitive dividers generating inaccurate voltages at each redistribution step. Apart from the sampling switch, leakage also affects several NMOS transistors of the CDAC switches in the bottom plate. Thus, as in the sampling switch, the leakage current model is employed in the NMOS transistors of the CDAC switch matrix, as shown in Figure 20.

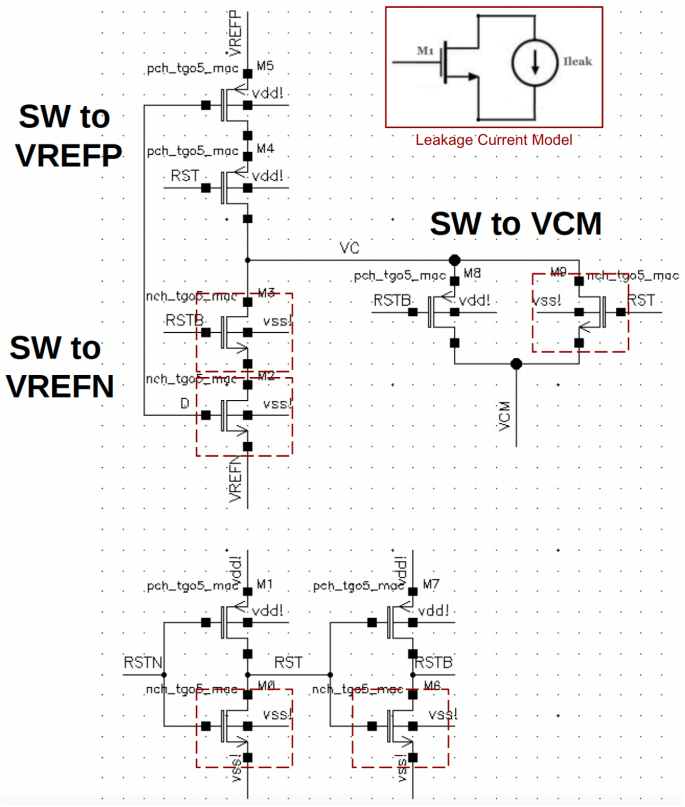

Figure 20. Leakage current model in CDAC switches

3 Results

The ASYGN SAR ADC is designed in Cadence® Virtuoso®, and simulated with Cadence® Spectre® and Mentor Eldo™. Four transient analysis simulations are performed highlighting different TID effects: (1) using the original, fault-free design, (2) modeling only the V_{TH} shift in the comparator, (3) modeling only the leakage in the sample and CDAC switches, (4) modeling all TID effects. Simulations exclusively modeling certain TID effects are performed to highlight their individual impact on the ADC performance, while the final simulation which models all these effects evaluates the overall ADC performance under radiation.

3.1 Pre-Radiation

To measure the key performance parameters of the SAR ADC, a transient simulation is performed, with the testbench schematic illustrated in Figure 21. At the input, a differential sine wave of -1 dBFS ($8.91\ V_{pp-diff}$) and frequency of 11.72 kHz is set. The serial output SDATA is fed to a serial-to-parallel converter with the same CLK and CNV as the ADC. The parallel output data DOUT is then generated from this block for post-processing. While the ADC operates at a sampling frequency (F_S) of 1 MHz, the clock frequency (F_{CLK}) is set at 80 MHz.

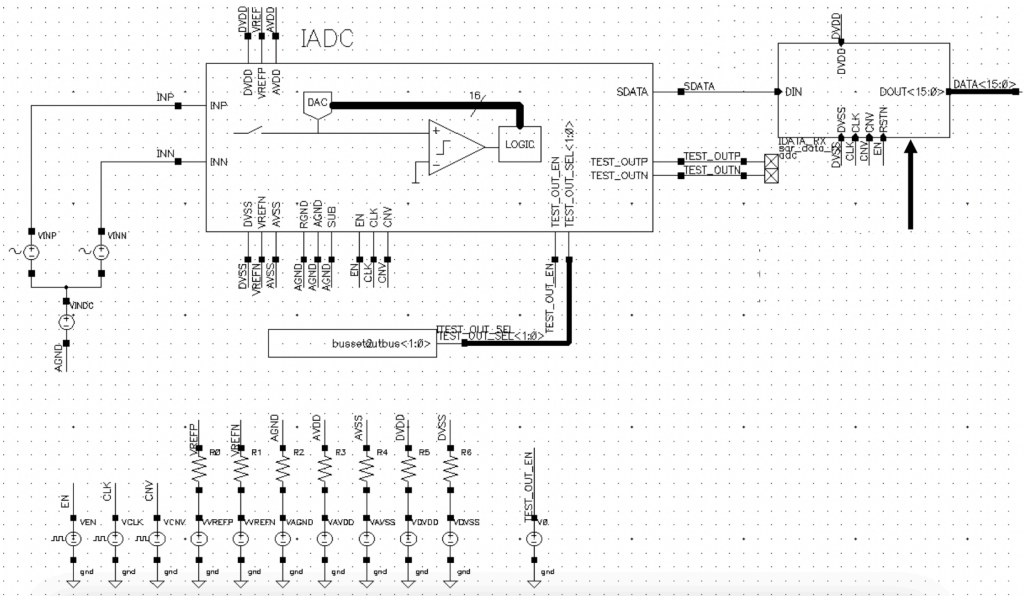

Figure 21. Testbench schematic of SAR ADC transient simulation

Figure 22 shows the input and output waveforms of the ADC simulation testbench. For the 16-bit ADC, $2^{16} = 65536$ divisions are available for producing a 1-V output, resulting in a quantization level of $1/65536 = 15.26\ \mu V$. Figure 22 illustrates how the ADC converts the input into a series of digital data of discrete values at discrete time intervals, approximating the input signal with fixed precision.

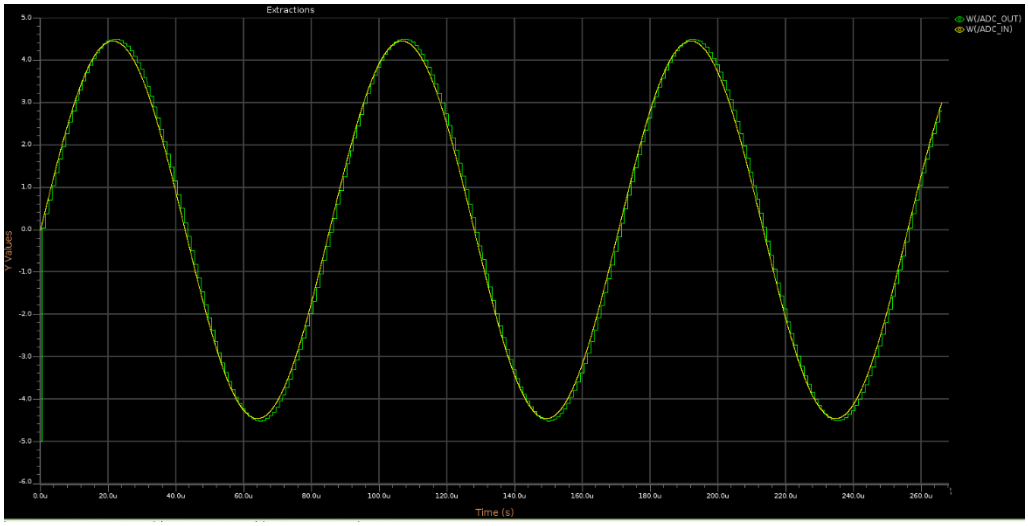

Figure 22. SAR ADC input (yellow) and output (green) waveforms, pre-radiation

In Figure 23, the DAC voltage is overlaid, representing the reference voltages generated by the DAC at each clock cycle.

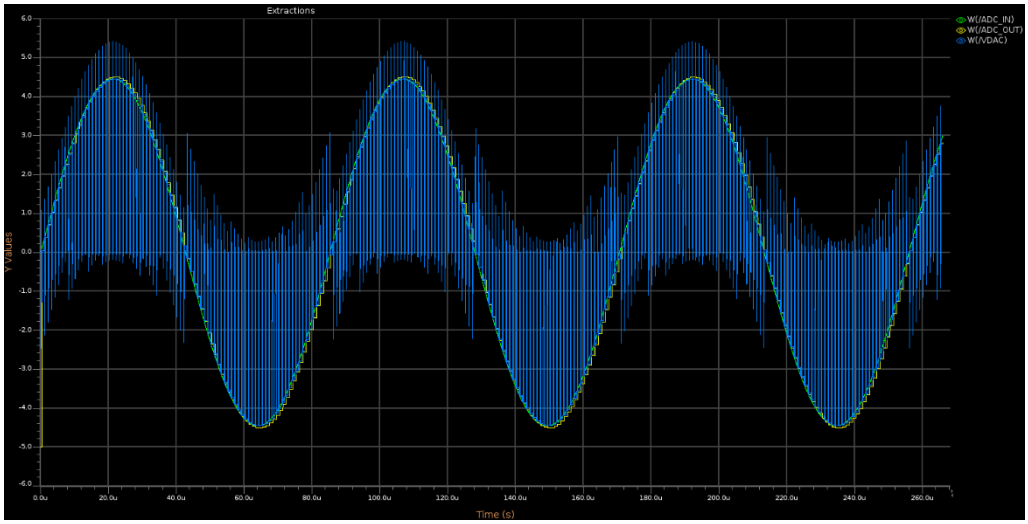

Figure 23. SAR ADC input and output waveforms with DAC voltage (blue), pre-radiation

While the time-domain representations are useful in verifying the ADC functionality and understanding its working principle, it is insufficient to measure the full performance of the ADC. To extract the key performance parameters, a signal processing technique called Fast Fourier Transform (FFT) is performed on the ADC output to obtain the frequency-domain plot, or spectrum. Considering trade-offs between accuracy, calculation time, and measurement repeatability, the number of captured samples is chosen to be 256, generating the ADC frequency spectrum shown in Figure 24.

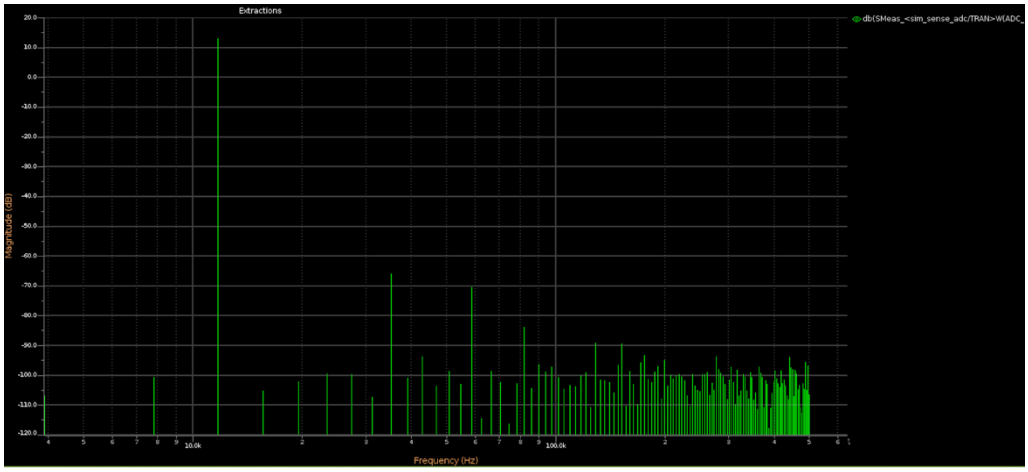

Figure 24. SAR ADC frequency spectrum, pre-radiation

The spectrum illustrates the magnitude of the signal frequencies through the converter, with the fundamental frequency at 11.72 kHz, or the frequency of the sine input signal. Harmonics below and above the signal are also present. Apart from enabling extrapolations on the fundamental frequency, harmonics, and noise floor, the output spectrum also allows for the calculation of key ADC performance parameters such as the Signal-to-Noise Ratio (SNR), Signal-to-Noise-and-Distortion Ratio (SNDR), Spurious Free Dynamic Range (SFDR), Effective Number of Bits (ENOB), and Total Harmonic Distortion (THD). Table 4 summarizes the performance metrics of the SAR ADC.

Parameter	Value	Unit
SNR	77.7	dB
SNDR	73.1	dB
SFDR	79.1	dB
ENOB	12.6	bit
THD	-77.7	dB

Table 4. SAR ADC key performance measurements, pre-radiation

The SNR is the ratio of the fundamental to the noise floor, excluding the power at DC and in the first five harmonics [26]. Measurements suggest that the design effectively differentiates the signal from the noise, with typical ADC SNR requirements ranging from 60 to 70 dB [27].

Similarly, the SNDR is the ratio of the power of the fundamental to the power of all the other spectral components including noise floor and distortion, but excluding DC [26]. The measured SFDR suggests good ADC sensitivity even in the presence of noise and distortion.

SFDR is the ratio of the power of the fundamental to the next highest spur, or harmonic. The measured value indicates the ADC's good ability to suppress spurious signals and harmonics relative to the main signal.

The ENOB indicates that the ADC provides a resolution close to 13 bits, where the maximum limit from the quantization noise is 16 bits.

THD is the ratio of the power of the fundamental to the power of the harmonics. In this calculation, up to 11 harmonics are counted in the THD and SNDR calculations. The measured THD indicates low harmonic distortion, ensuring minimal impact of the harmonics on the input signal.

Overall, the performance metrics indicate that the SAR ADC design demonstrates excellent signal fidelity, minimal distortion, high dynamic range, and precision in signal conversion.

3.2 Effects from V_{TH} Shift in Comparator

Figure 25 shows the results of a transient simulation performed on the SAR ADC testbench using the same parameters, but with the post-radiation model of the comparator introduced in the design. This isolates the contribution of the TID-induced threshold voltage shifts in the comparator to the overall ADC performance. Time-domain representations show no considerable effects on the output, with no visible offsets and settling time degradation observed.

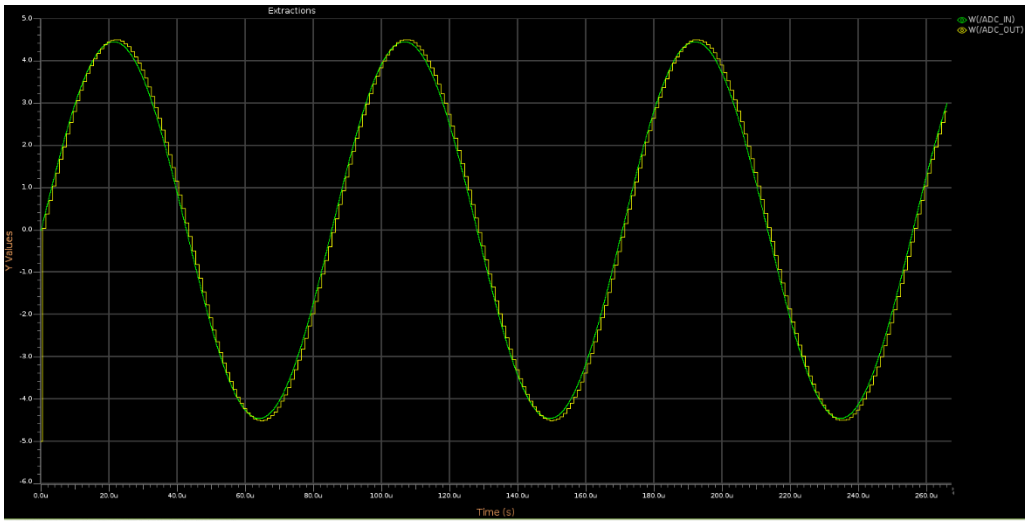

Figure 25. SAR ADC input (green) and output (yellow) waveforms, with V_{TH} shift effects in comparator

Spectral measurements presented in Table 5 however show some degradation in the ADC performance parameters, although quite negligible with values less than 1 dB. Thus, results indicate only minor changes in the comparator performance post-radiation.

Parameter	Pre-radiation	TID (1-5 Mrad)		Unit
		Comparator	Degradation	
SNR	77.693	77.457	-0.236	dB
SNDR	73.093	72.745	-0.348	dB
SFDR	79.105	78.970	-0.135	dBc
ENOB	12.613	12.574	-0.039	bit
THD	-77.702	-77.465	0.237	dB

Table 5. SAR ADC key performance measurements, with TID effects in comparator

To verify the comparator's performance, a separate noise simulation is performed on the component by setting a small DC voltage of 1 mV as input while it is clocked. Figure 26 illustrates the schematic of the comparator noise simulation testbench. This Periodic Steady-State Simulation (PSS) calculates the input-referred noise from the gain and output-referred noise of the comparator.

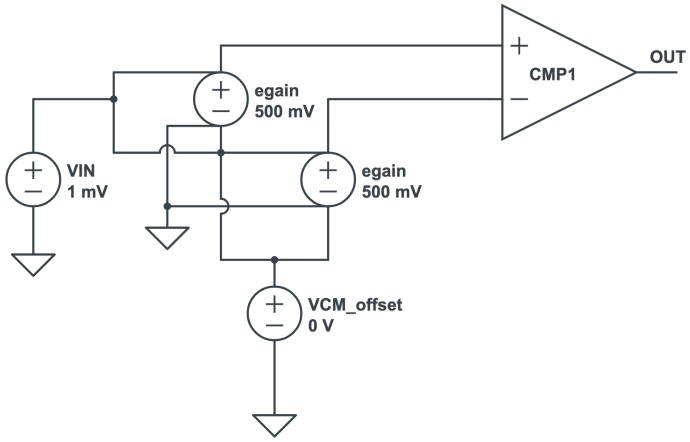

Figure 26. Testbench schematic of comparator noise simulation

The simulation parameters are shown in Figure 27. With the comparator sampling frequency set at 70 MHz, the noise frequency range is set from 0.1 Hz to 35 MHz (half of the sampling frequency). The maximum sideband count is set to 16, which showed a good tradeoff between simulation time and precision. The noise is probed at the output of the latch such that when the voltage reaches a threshold value of $V_{IN} \cdot A_V$, that is 1 mV · 10 = 10 mV, noise is generated at the output.

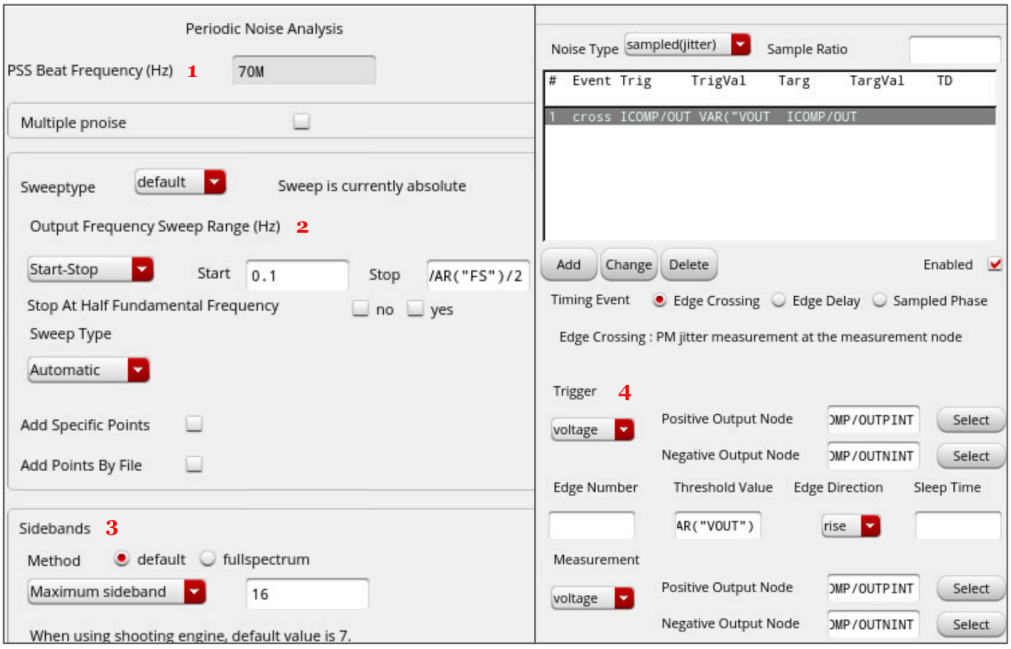

Figure 27. Simulation parameters of comparator noise analysis: (1) sampling frequency, (2) noise frequency range, (3) maximum sideband count, (4) noise type and trigger

Figure 28 illustrates the input noise spectral density of the comparator before and after introducing the TID-induced V_{TH} shift model. Only a negligible increase in the input-referred noise, measured at 10 kHz, is observed. This suggests that TID effects only have a minor impact on the noise characteristics of the comparator design. Due to the latch stage of the dynamic comparator which operates in a regenerative feedback mode, small V_{TH} variations are quickly overcome by the positive feedback. The reset switches, which periodically reset the latch and input nodes, also reduce charge accumulation.

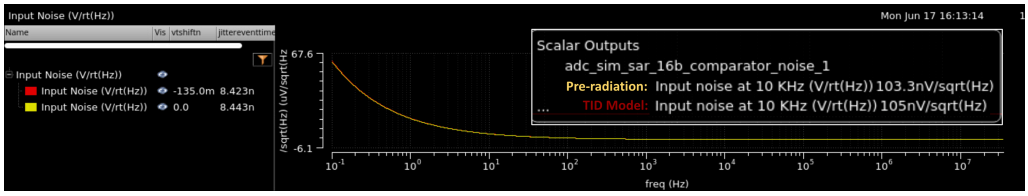

Figure 28. Noise simulation results of comparator, pre-radiation (yellow) and with TID (red)

In addition to the radiation-robust design, TID effects on SAR ADC comparators are also highly dependent on power consumption [20], which reflects the biasing of the transistors. Since the power consumption of the comparator design is 150 µW, it is considered low-power for an analog block. Ultra-low power analog circuits, with consumption in the order of nW, may be more sensitive to TID and present more distinct effects [21], depending on the dose values.

To further test this, Figure 29 shows the input noise spectral density of the comparator for increasing V_{TH} shift values. Even for a V_{TH} shift of -150 mV, which corresponds to the highest maximum degradation dose tested for the target technology, the comparator still exhibits good noise performance with minimal post-TID degradation of less than $1\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$.

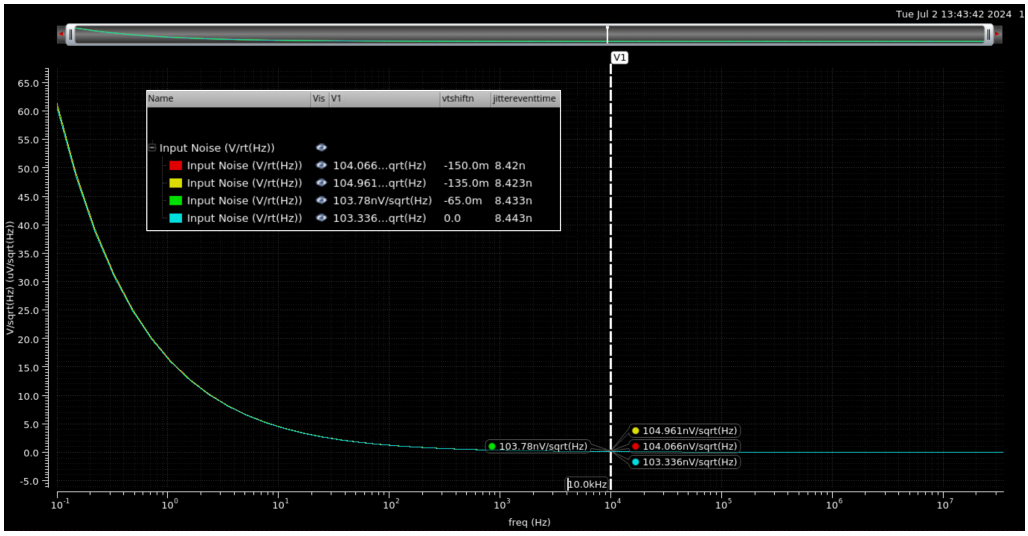

Figure 29. Comparator input noise with Vin = 0.1 mV, pre-radiation (cyan) and with TID-induced $V_{tshift} = -65$ mV (green), -135 mV (yellow), and -150 mV (red)

3.3 Effects from Leakage in Switches

To distinguish the contribution of leakage effects from the switches, Figure 30 shows the transient simulation results of the SAR ADC after introducing the leakage current model in the sampling and CDAC switches. While the output signal maintains a consistent sinusoidal shape following the input, noticeable deviations are observed particularly in regions where the slope of the sine wave changes rapidly. Visual inspection shows that the output does not smoothly track the input this time, with a slight phase shift observed between them. This may be attributed to delays introduced by leakage effects that affect ADC timing. Furthermore, a reduced amplitude is observed at the negative peaks of the output waveform, suggesting possible errors in the sampling and measurement of the input signal.

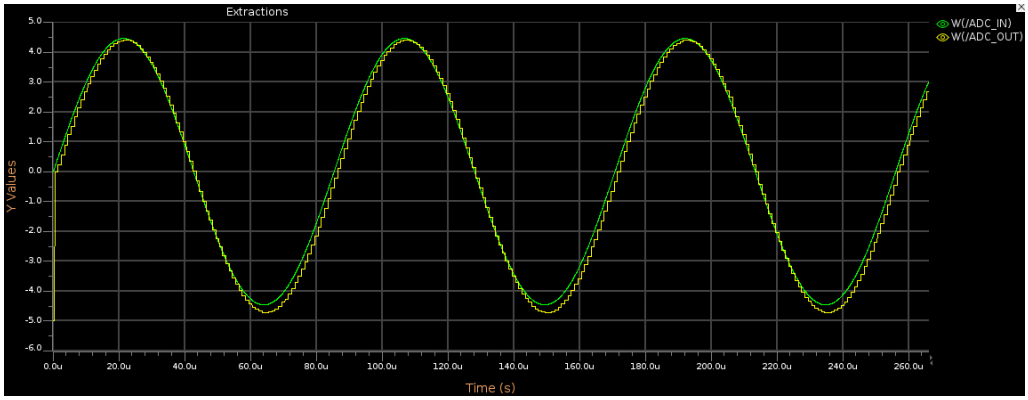

Figure 30. SAR ADC input (green) and output (yellow) waveforms, with leakage effects in sampling and CDAC switches

Performance measurements, presented in Table 6, reveal that leakage effects from the switches have a significantly larger contribution to the performance degradation of the SAR ADC design, which impacts the noise performance, resolution, and accuracy. Since leakage paths in the CDAC switches cause charges to leak through the capacitors, reference voltages generated at the capacitive divider for comparison are not accurately being formed. In addition to DAC voltage errors, leakage paths in the sampling switches also degrade their ability to preserve charge during the hold phase, resulting in an incorrect reading of the input. In particular, charges injected into the DAC when the sampling switch is closed can cause nonlinearities and degrade the SFDR [28], as seen in the results of the measurements performed. Since the SAR ADC operation is based on charge redistribution, TID effects within the set of switches that control the capacitor array can result in measurement errors, due to unintended charge redistribution which modifies the generated voltages.

Parameter	Pre-radiation	TID (1-5 Mrad)		Unit
		Switches	Degradation	
SNR	77.7	55.2	-22.5	dB
SNDR	77.7	55.2	-22.5	dB
SFDR	79.1	61.3	-17.8	dBc
ENOB	12.6	8.88	-3.72	bit
THD	-77.7	-59.8	17.9	dB

Table 6. SAR ADC key performance measurements, with leakage effects in sampling and CDAC switches

3.4 Combined TID Effects

After isolating the different TID effects from the individual ADC blocks and analyzing their individual impact on the overall ADC performance, a transient simulation is performed where all of the identified TID effects are modeled in the SAR ADC design: (1) V_{TH} shift in the comparator, and (2) increased leakage in the sampling and CDAC switches. By modeling all these effects which have been identified as the main TID effects in SAR ADC, the component's performance in radiative space environments can be simulated and analyzed. Figure 31 shows the result of the simulation. Visual inspection of the output in the time domain seemingly reveals the same non-idealities found in the simulation results modeling only the leakage effects, with the output deviating from the input at certain regions of the waveform.

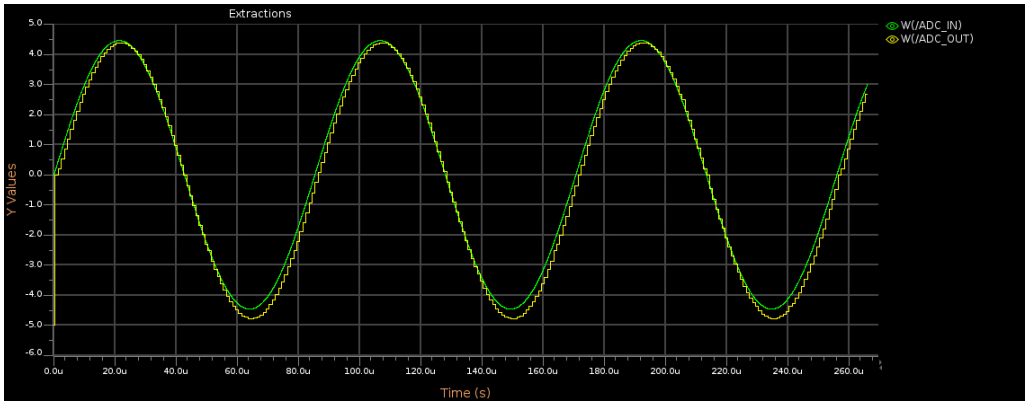

Figure 31. SAR ADC input (green) and output (yellow) waveforms, with TID effects in all critical blocks

Table 7 summarizes the performance metrics of the ADC for all three simulations performed. The first two simulations highlight the impact of individual TID effects while the third one combines all these effects, simulating the overall ADC performance under radiation. Results of the combined-effects simulation reveal further degradation of the ADC performance parameters. While TID-induced V_{TH} shifts in the comparator were shown to have a negligible impact on the ADC, with the comparator demonstrating robust performance under radiation, the same cannot be said when this model is introduced in combination with leakage effects in the switches. As seen in Table 7, the combined model results in additional degradation in the performance measurements that is non-negligible. As discussed in Section 3.3, leakage effects result in incorrect measurements of the input through the sampling switch and erroneous reference voltages generated at the DAC. These erroneous voltages, when fed to the comparator during the binary search process, introduce an increased offset. This offset effectively slows down the comparator, shifts the output codes, and results in bit errors or missing codes. Furthermore, combined effects in the sampling switch impact its on-resistance during conduction, making it more variable with the input signal. The variability in the on-resistance of the switch is particularly significant in the speed of the ADC [28], as the on-resistance is crucial for the quick settling of the comparator during the 16 comparison cycles. Increased on-resistance not only reduces the speed but also

degrades the overall accuracy of the ADC, as the comparator consumes a significant portion of the total conversion time.

Parameter	Pre-radiation	TID (1-5 Mrad)			Unit
		Comparator	Switches	All	
SNR	77.7	77.5	55.2	52.0	dB
SNDR	77.7	77.5	55.2	52.0	dB
SFDR	79.1	79.0	61.3	60.8	dBc
ENOB	12.6	12.6	8.88	8.34	bit
THD	-77.7	-77.5	-59.8	-55.1	dB

Table 7. SAR ADC key performance measurements, with TID effects in (a) comparator only, (b) switches only, (c) both

4 Conclusion

In this study, TID-sensitive blocks of the SAR ADC and their physical effects were identified, SPICE simulations were performed to analyze the impact of each component on the overall system performance, and the SAR ADC's performance was evaluated under TID conditions, providing insights into its resilience and suitability for high-radiation applications.

TID models were developed for two main effects: (1) threshold voltage shifts in the comparator, and (2) leakage current increase in the sample and CDAC switches. Using baseline data from previous literature, a combination of BSIM device modeling and circuit-level modeling were applied to simulate TID effects corresponding to the target technology and total dose associated with space applications.

TID models were introduced to the design and transient analysis simulations, as well as spectral measurements, were performed to evaluate the ADC performance. Simulations exclusively modeling certain TID effects were performed to highlight the impact of each effect or block, while a final simulation modeling all effects was performed to simulate the overall ADC response under radiation.

Simulation results, modeling threshold voltage shift effects in the comparator, showed minimal impact on its noise characteristics. No significant degradation was observed in the overall ADC performance, suggesting negligible effects in the comparator performance post-TID due to its low-power design, regenerative feedback mechanism, and periodic resetting which manages charge accumulation.

Simulation results modeling leakage effects in the sampling and CDAC switches, however, underscored the significant impact of leakage effects on the ADC performance. Slight deviations and inaccuracies, with respect to the input signal, were observed in the output, attributed to erroneous reference voltages generated at the DAC due to leakage paths from/to the capacitors, and incorrect input voltage readings from leakage in the sampling switch.

Simulation results modeling all combined TID effects revealed further degradation in the ADC performance, due to compounded errors when erroneous voltages from the DAC and sampler are fed to the comparator during the comparison phases. Increased offset in the comparator, as well as variability in the sampling switch on-resistance, contribute to bit errors, reduced speed, and accuracy degradation.

5 Future Work

While simulation-based analysis of radiation effects on electronics allows isolation and separate analysis of individual blocks, actual TID experimental setups still provide more accurate results, where the fabricated chip is exposed under X-ray or gamma radiation. Based on the results, a failure study can be carried out and the simulations results can be validated.

Currently, an irradiation testbench is in its early design phase to perform an X-ray radiation experiment on the ADC chip, which is to be fabricated in the future. As a substitute, the EVAL-AD7982-PMDZ 18-Bit, 1 MSPS PulSAR® ADC PMOD evaluation board from Analog Devices is used a provisionary board. This is mounted on a digital microcontroller test board from ASYGN via SPI, which in turn, is connected to a PC with a data logging and management tool via USB. The setup is shown in Figure 32.

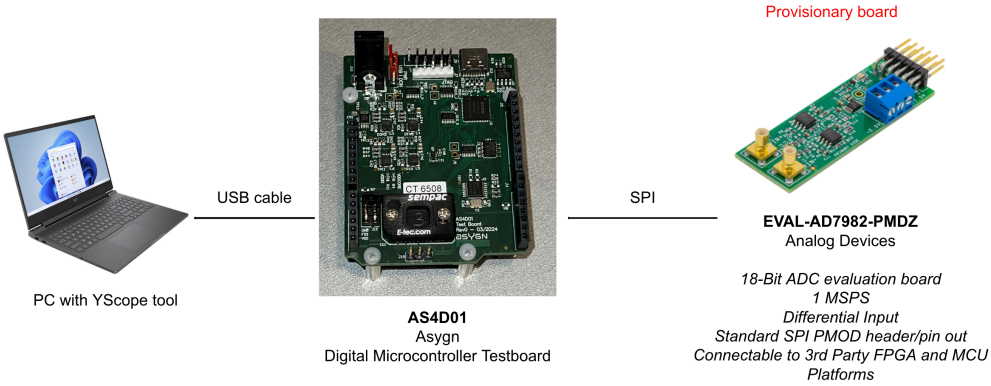

Figure 32. Testbench setup for X-ray radiation test of SAR ADC

Data communication between the components is validated by successfully acquiring and displaying the ADC output on an oscilloscope for a 10-kHz 1-V_{PP} sine wave differential input, as shown in Figure 33.

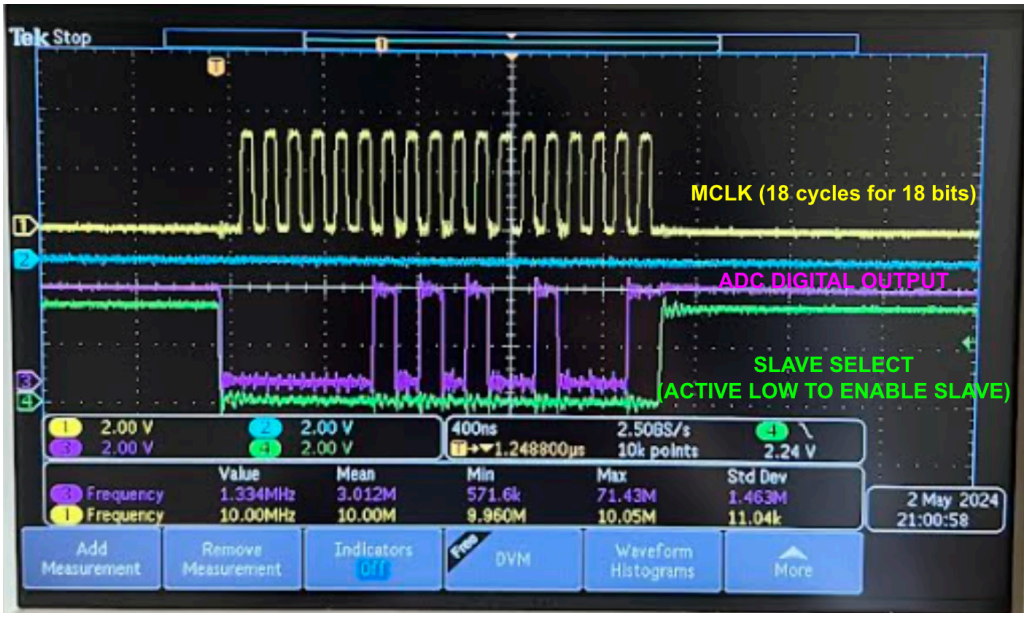

Figure 33. Master clock (CH1, yellow), ADC output (CH3, purple), and Slave Select (CH4, green) signals from test setup

Once the fabricated chip is ready, a Python script can be implemented to acquire the ADC output in hexadecimal values, and then imported to a signal processing tool such as MATLAB to extract spectrum measurements and evaluate the performance parameters.

In this study, a simplified TID model was developed by limiting the studied effects to V_{TH} shift and I_{OFF} increase. Other TID effects, such as the radiation-induced increase in variability between devices can also be modeled in future work. This is particularly relevant for the comparator, since our current model assumes a uniform V_{TH} shift across all NMOS, for a lack of published data to sufficiently model this effect. By incorporating device variability into the model, we might see greater impacts on performance. Beyond that, different process corners could also be explored. The impact of a possible increase in 1/F noise can also be studied. Aside from TID, the impact of SEE can also be investigated to provide a comprehensive analysis of the SAR ADC's performance under radiative space environments.

From the simulation results alone, radiation-hardened by design (RHBD) techniques can also be studied and implemented in the SAR ADC design, such as using Enclosed Layout Transistors (ELT) to cancel radiation-induced leakage currents.

RHBD layout-level techniques for mixed-signal layouts can also be studied and implemented, such as using interdigitated layout to improve matching of transistors and help reject SETs, implementing redundancy in the input and reference voltage traces, and implementing MOS devices based on edgeless transistors (ELTs) [7].

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