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DELAY LINE DESIGN FOR HIGH-RESOLUTION TIME-TO-DIGITAL CONVERTERS

Master Thesis Report

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Abstract

Microelectronic technology is constantly scaling towards more modern, advanced, smaller technology nodes, which allows higher operational speeds and more robustness to total ionising dose. However, the technology downscaling also lowers supply voltage, thus shrinking the available headroom for the voltage domain operations. That is why more and more attention is paid to the processing of the analog signal in the time domain, where zero crossings of a signal represent analog information. That is why time-to-digital converters (TDC) take the stage instead of analog-to-digital converters (ADC). Moreover, in order to withstand harsh environments to be able to operate in the field of high energy and nuclear physics and space, these devices have to be able to tolerate the ionising radiation effects, thus, radiation hardening is required to mitigate this degradation caused by these effects.

This thesis aims to thoroughly explore the fundamental architectures of TDC, and propose and compare more advanced system architectures for time-to-digital converters, which would allow to improve possible resolution and power consumption (which is the main bottleneck for space applications and battery-powered devices) in comparison to the existing designs.

Detailed analysis of the Lee-Kim and Maneatis delay cells is conducted, covering minimal achievable delay, power consumption, the effect of local mismatch on the performance, jitter and supply sensitivity, in two different technologies: UMC 180nm and TSMC 65nm. The performances of the cells have been compared and the best one was chosen for the design of the delay line for precise timing signal generation. The solution for delay cell enhancement to be suitable for specific architectures is given for enabling coarse-fine tuning.

The sub-gate delay resolution in the order of pico-seconds is discussed and is achieved by using local passive interpolation, feed-forwarding technique and their combination.

Additionally, the final design of a high-speed delay line is discussed, incorporating various improvements to ensure the correct operation of the delay line at high clock frequency in all process corners. The work concludes with a novel approach to mitigating supply sensitivity using active DAC control to amplify and counteract supply fluctuations, ensuring improved performance and reliability.

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List of Abbreviations

ADC	Analog-to-Digital converter
ADPLL	All-digital phase-locked loop
ASIC	Application-specific integrated circuits
CMOS	Complementary metal-oxide-semiconductor
CS	Current starving
DAC	Digital-to-Analog converter
DE	Delay element
DLL	Dleay-locked loop
DNL	Differential non-linearity
FB	Feedback
FF	Flip-flop
FPGA	Field-programmable gate array
HVT	High threshold voltage
IF	Interpolation factor
INL	Integral non-linearity
LET	Linear energy transfer
LIDAR	Light detection and ranging
LPI	Local passive interpolation
LSB	Least significant bit
LVT	Low threshold voltage
MSB	Most significant bit
NIEL	Non-ionising energy loss
PD	Phase detector
PET	Positron emission tomography
PLL	Phase-locked loop
PVT	Process, voltage, temperature
RO	Ring oscillator
SEE	Single-event effect
SEL	Single-event latch-up
SET	Single-event transient
SEU	Single-event upset
STI	Shallow-trench isolation
SVT	Standard threshold voltage
TDC	Time-to-Digital converter
TID	Total ionising dose
ToF	Time-of-Flight
VCO	Voltage controlled oscillator
VCRO	Voltage-controlled ring oscillator

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1. Introduction

Time-to-digital converters (TDCs) are a type of data converters, not dissimilar to analog-to-digital converters (ADCs), but instead of converting voltages to digital words – TDCs quantise time intervals, thus being the core of time-mode circuits. There are various architectures of TDCs, with further progress relying on novel design solutions and CMOS process scaling. The key points for further research and optimization are aiming for higher resolution; reduced power consumption, area and conversion time; increased linearity and input ranges; process, voltage and temperature (PVT) robust solutions, ability to withstand mismatch and even more importantly in our case – harsh environments. Additionally, more circuitry in the TDC architectures is made in digital CMOS logic, which facilitates the design and allows to benefit from CMOS downscaling especially.

The spectrum of TDC applications is quite wide: they are used in high-energy [1] and nuclear physics for precise measurements [2], and implementation in both ASICs and FPGAs [3, 4] found their applications in positron emission tomography (PET) [5] and other medical imaging techniques [6], time-of-flight (ToF) and light detection ad ranging (LIDAR)[7].

TDCs can be classified into sampling TDCs, noise-shaping TDCs, and stochastic TDCs [8], depending on the architecture, just like with usual analog-to-digital converters. Here, we will try to give a short overview of the architectures, considered for the multichannel TDC design.

1.1 Fundamental TDC architectures

One of the straightforward ways, which historically was also one of the earliest, to convert time intervals into digital words is using the **counter technique**: count the number of high-frequency clock cycles that fit in the duration of the interval between “start” and “stop” events [9, 10]. The advantage of the method is zero conversion time, since the result of the measurement is available almost immediately after the end of the time interval to measure. However, the digitizing of the same given time interval may result in two different codes due to the dependency of the reference clock phase with respect to the event signal. The downside of the counter-based TDC is limited by the reference clock resolution: for a (quite modest) resolution of 1ns a clock frequency of 1GHz is needed, thus, to achieve a more state-of-artish resolution around several picoseconds unreasonably high-frequency reference clock is required (>100 GHz). So, to achieve better resolution and still stay with a reasonable clock frequency, interpolation techniques are used: count the fractions of clock cycles, generated by a number of delay elements.

Another widely used architecture is a **delay-line TDCs** (Fig. 1.1(a)). In this case, the direct conversion of time intervals into digital words is based on delaying the signal, which goes through the chain of buffers, by a unit delay (T_{LSB}) with each next delay element (DE). The outputs of the delay cells are connected to distributional buffers (not shown on the diagram) and them in turn – to the flip-flops (FF), which are sampled at stop event arrival. The timing diagram is given in Fig. 1.1(b): by decoding the thermometer code, the time interval between start and stop pulses can be evaluated in terms of the number of unit delays (T_{LSB}).

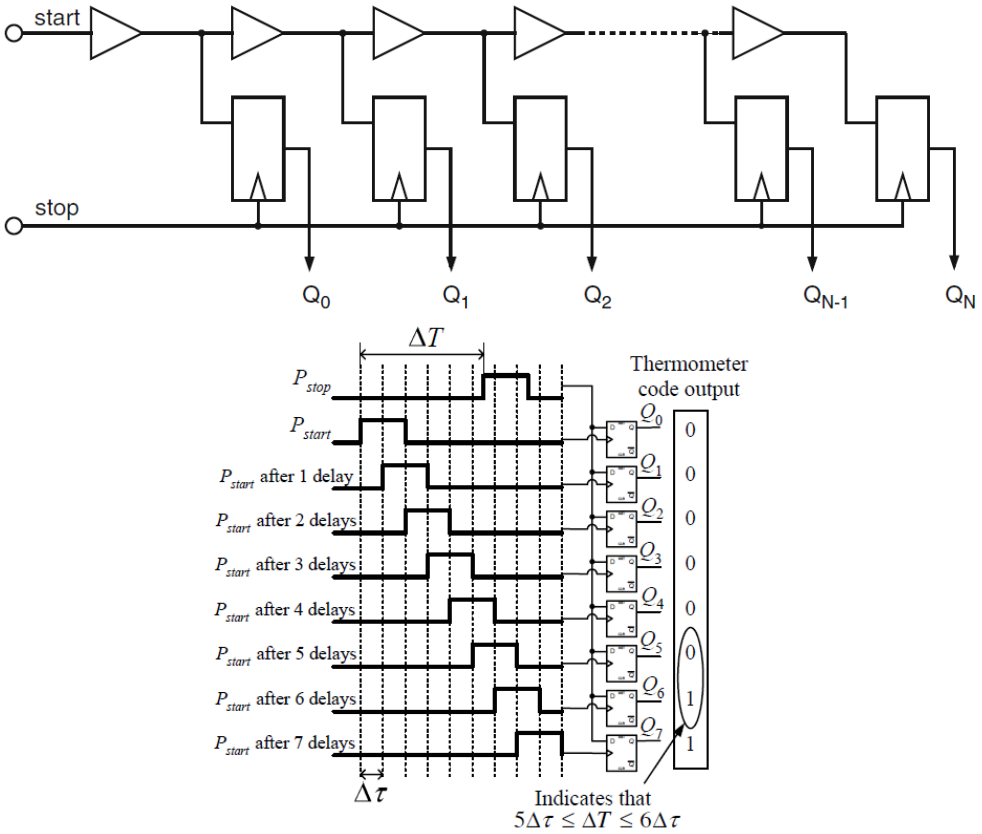


Figure 1.1 Block (a) [8] and timing (b) [11] diagram of a delay-line based TDC

The length of the delay line in this case determines the maximum time interval, that can be measured. Henceforth, for very long intervals the core of such TDC would take too much area. Thus, **looped architecture** was introduced: a short delay line is looped and a counter calculates how many times the start signal has passed the delay line, before TDC has been stopped [8, 12].

One of the drawbacks of the architecture is susceptibility to the impact of PVT variations on the precise timing calibration. Another downside is the accumulated inaccuracy of the delay, which directly translates to gain error (Fig. 1.2(c)) and integral non-linearity (INL) – deviation from either the best-fit line or the line, that connects the end-points of the characteristic, whereas local variations contribute to offset (Fig. 1.2(b)) and differential non-linearity – deviation of each step from its ideal value [8].

The measured interval can be estimated as:

$$T_{IN} = B_{OUT} T_{LSB} + \varepsilon \qquad (0 \le \varepsilon \le T_{LSB}), \tag{1}$$

where B_{OUT} is the output digital value (decoded thermometer code) and ε is the quantization error.

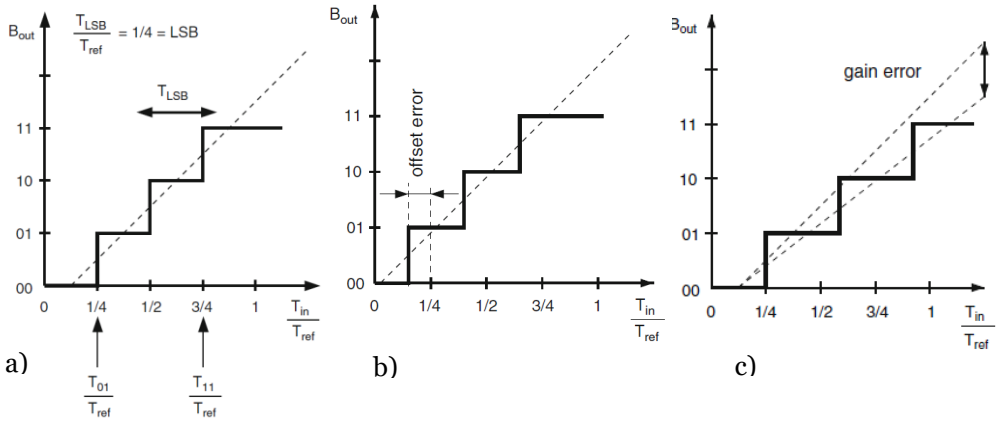


Figure 1.2 Ideal input–output characteristic (a) of time-to-digital converter interval, characteristic with offset (b) and gain (c) error [8]

As has been mentioned earlier, TDCs are greatly affected by PVT variations, degradation due to ageing and harsh environments, thus in a basic delay-line configuration can only qualitatively estimate the given time interval in terms number of unit gate delays. To achieve absolute measurement some sort of calibration of the delay line is required. To get a self-calibrated line delay- or phase-locked loops **(DLL/PLL) TDCs** are used (Fig.1.3).

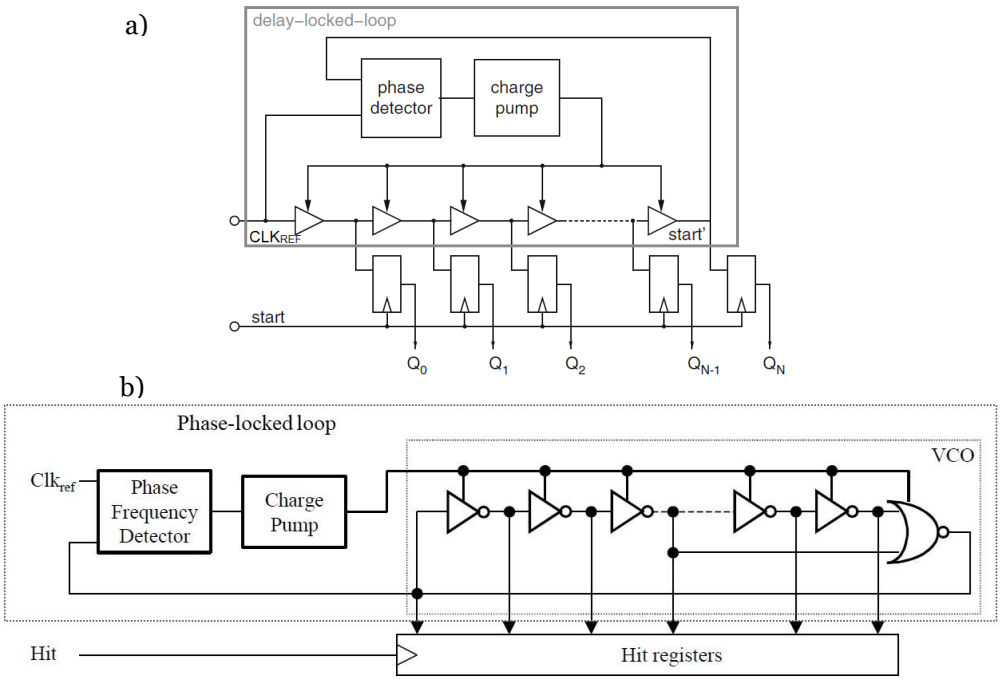


Figure 1.3 Block diagram of a) DLL-based TDC [8] and b) PLL based TDC [13]

The measurement of the time interval itself is the same, as in the case of delay line TDCs [8]. A separate channel for stop signal is used, thus calculating the difference between the start and stop measurements, the wanted time interval can be found.

To explain the self-calibration mechanism, let's assume, for simplicity, that approximately one period of reference clock fits in the delay line. The input and output of the delay line are fed into a phase detector (PD), which compares their phases. If they are equal – delay along the line is exactly one period (unit delay is then $T_{LSB} = T_{CLK}/N$, where N is the number of delay cells). If the rising edge at output node occurs earlier, than the rising edge of the reference clock at the input of delay line, the total delay of the line is smaller then the reference period, and vice versa. This data is used to control the delays of tunable delay elements (DEs). Due to the presence of high-frequency components at the output of the PD, it has to be followed by a low-pass loop filter. However, it should be mentioned, that the tuning of the delay reduces the TDC resolution since the linear operation of the control loop requires some space for tuning both ways: for slower and faster operation. More or less the same working principle is in the case of using PLL-based implementation of TDCs. In the latter case, when a delay line is used as a voltage-controlled ring oscillator, the loop filter needs an integrating component in order to eliminate the steady-state phase difference. This is usually implemented as a charge pump in combination with a phase-frequency detector, which adjusts the control voltage, that is applied to the tunable delay cells.

1.2 Architectural choices and system considerations in multichannel TDC design

With the project's evolution, the choice of the system's architecture has been carefully considered, taking into account the availability of other already-designed blocks, power consumption and calibration capability.

The initial idea for the system architecture was to use pre-designed an All-Digital Phase-locked loop (ADPLL). The timing information is to be obtained from the delay line, which is configured into a voltage-controlled ring oscillator (VCRO), in order to tune the delays of the VCRO we need a digital-to-analog converter (DAC) for providing control voltage (Fig. 1.4).

Figure 1.4 TDC architecture based on ADPLL, DAC and voltage-controlled ring oscillator

Here the reference clock provides the stable timing signal to the system, received by the ADPLL, which generates a high-frequency signal and ensures, that the output frequency is locked to the reference. ADPLL benefits from digital techniques for phase and frequency detection, making it more compact and power efficient. The PLL controls the DAC, which in turn uses its analog voltage output to modulate the delays of the delay elements and consequently, the frequency of the VCRO. The signals generated by the ring oscillator are used to obtain precise timing information for the TDC.

The advantages of this architecture are power efficiency and compactness due to the use of all-digital PLL.

The downside of the initial architecture (ADPLL-based) is the necessity to design an accurate digital-to-analog converter (DAC) to perform control over the ring oscillator and higher phase noise, the former being the main problem of the architecture. The requirements for the DAC make it challenging to design: it should allow high-speed operation and medium resolution at the least, it would be driven by a digital sigma-delta modulator. It would require precise analog components and advanced layout techniques to minimise noise, crosstalk, and other parasitic effects. Additionally, high-speed DAC consumes significant power, which overcasts the power efficiency of the rest of the architecture. As always, there is a constant trade-off between power consumption and performance (resolution and speed), optimising one aspect comes at the expense of the other.

A different option, which allows omitting the precise DAC, is using a PLL and LC oscillator for generating a clock signal for the delay line stabilized in a DLL, which would generate the timing signals for the flip-flops (Fig.1.5). An obvious advantage is lower noise due to generating the clock for the DLL with a low-jiiter LC-PLL. Nevertheless, the drawbacks are the complexity of the additional DLL design and the corresponding power consumption.

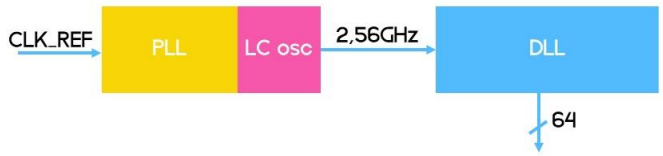


Figure 1.5 TDC architecture based on a PLL, LC oscillator and DLL

However, the question of whether we can digitally calibrate the line, using 3 or 4 bit DAC, to drop the DLL persists. The idea is to use a delay line in an open-loop configuration, which would receive a clock signal from the LC oscillator (Fig. 6). The calibration would be performed with a dedicated calibration channel, which uses the reference clock as start-stop signal. By observing subsequent 1->0 transitions in the delay line, which are separated by one period, the number of delay cells that fit in one period and thus the unit delay can be calculated and tuned via digital calibration, using the DAC. In this case a simple 4-bit R-2R ladder can be used as DAC.

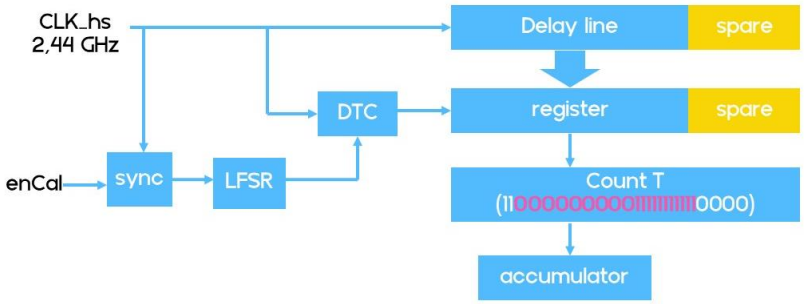


Figure 1.6 Open-loop architecture of TDC with calibration of delay line using dithered DTC

In order to reduce the quantization error in this measurement, a digital-to-time converter (DTC) is used to dither the input start-stop signal [14]. Here, the linear-feedback shift register (LFSR) generates a pseudo-random sequence, which causes the output delay to vary around the intended value, thus randomizing systematic (as in the case without dithering) and potentially large quantization error, averaging it out over multiple samples.

It is possible to have a flexibility in the desired resolution of TDC, initial goal for the resolution was set to be 5ps. That means, that to cover the whole reference clock period the number of cells needed can be calculated:

$$N = \frac{T_{\text{CLK\_REF}}}{T_{\text{LSB}}}. \tag{2}$$

So, for the delay line to cover the whole period with whatever resolution we choose, it has to be configurable. For example, extra buffers can be added to the line, which will ensure operation with higher resolution, but when the resolution can be lowered, these extra buffers can be separated from the line by switches. However, this configurability can be achieved by adding switches, which in turn will add more parasitics, that will degrade the delay propagation and therefore resolution.

Specific buffering is provided to enable multichannel operation.

As for the delay cells, that generate the precise timing information, then there are several possibilities, which can be generally divided into single-ended and differential cells. This way for the single-ended circuit, a loaded buffer can be used: two inverters with a capacitive load connected between them (Fig. 1.7(a)). To control the loading of this internal connection an NMOS transistor is used, this way by increasing the load, the slew rate of the signal will reduce and consequently, the propagation delay rises. The advantage of the cell is its simple topology, but the drawback is higher minimal delay and thus worse resolution due to the additional loading.

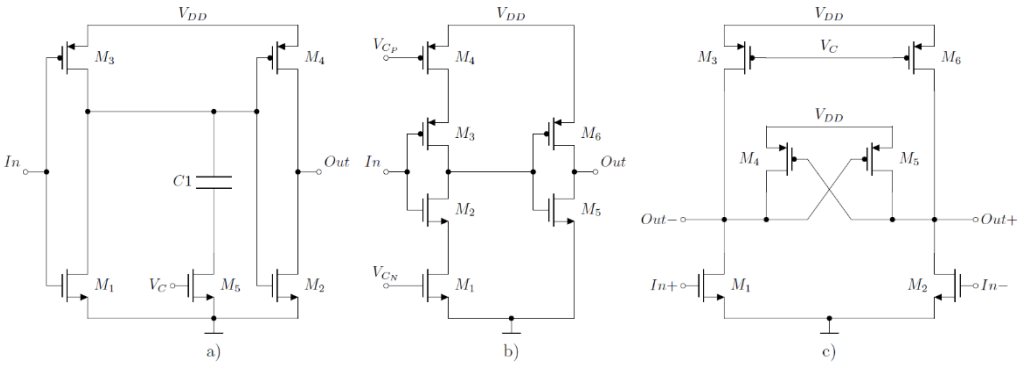


Figure 1.7 a) Single-ended loaded delay cell, b) current-starved single ended delay cell, c) pseudo-differential delay cell [15]

Another option for the single-ended delay element is to use a current-starved delay cell (Fig. 7(b)), the control over the delay is realized by limiting the current in the inverter stage, thus decreasing slew rate and increasing delay. However, the disadvantage of the topology is the pulse-shrinking effect due to the unbalanced current-starving devices,

the mismatch between which will additionally worsen (thus increasing the pulse-shrinking effect) due to ageing and harsh environment-caused degradation.

The advantage of using a differential or pseudo-differential delay cell is the delay propagation as of only a single inverter, thus allowing higher resolution. One of the examples of a pseudo-differential cell, which will be further analysed in depth, is the Lee-Kim cell (Fig. 7(c)), it consists of current starved cross-coupled inverters. The current-starving at the PMOS side affects the rising edge, which is compensated by the intra-cell cross-coupling and alternating connection between the cell in the delay line.

1.3 Ionising radiation effects in MOSFETs

The radiation effects on silicon electronic devices are divided into two main groups: ionising, which consists of long-term effects (cumulative) – total ionising dose (TID) and short-term effects – single-event effects, and non-ionising (also referred to as non-ionising energy loss – NIEL). NIEL includes displacement damage and nuclear interaction, the former being very significant for image sensors, as it significantly increases dark current, resulting in hot pixels, and noise. The effect of ionising radiation will be discussed in detail in this section as it has more impact on MOSFETs. For mitigation of the mentioned effects radiation-hardening techniques can be used.

1.3.1 Total ionising dose effects

The TID effects cause gradual degradation of the complementary metal-oxide semiconductor (CMOS) devices because of the charge trapping by the insulation layer (oxide) of the device, which causes, among other, threshold voltage shifts and leakage current [16]. The first phase of charge trapping is the generation of electron-hole pairs (the larger part of which will instantly recombine not causing any damage to the device) in the oxide due to the passing of ionising radiation. However, as the remaining electrons are much more mobile, than the holes, the former quickly escape towards the positive bias, whilst the latter migrate to the Si-SiO_2 interface using the localised states, where they can be trapped, thus forming positive oxide-trap charge [17]. Interface traps can also be generated in the Si-SiO_2 interface, trapping either negative or positive charges. Traps above mid gap behave like an acceptor dopant and are called acceptor like traps. They are neutral when empty and negatively charged when filled. Traps below mid gap behave like a donor dopant and are denoted donor-like traps. They are neutral when filled and positively charged when empty. For an NMOS device (p-substrate) the Fermi level at the interface is above the middle of the bandgap. Since the traps below the Fermi level can be considered filled the charges trapped above mid gap result in a net negative interface trapped charge. Naturally, the opposite is true for a PMOS device. Since both types of trapped charges are positive for PMOS (though interface charge build-up is slower in PMOS as it involves hole migration against the electric field in the gate oxide), the shift of the threshold voltage is more significant, than in the case of NMOS, where they partially compensate each other (Fig. 1.8). However, for the NMOS this is true in the long run, because the oxide traps form first, thus decreasing the threshold voltage, but later the interface traps start dominating, increasing the threshold voltage of the transistor [18]. Moreover these interface states contribute

significantly to the increase of 1/f noise and reduction of the mobility of charge carriers [15].

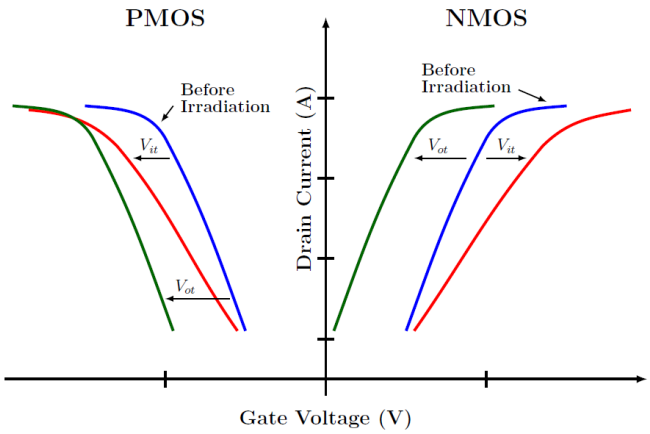


Figure 1.8 Threshold voltage shift of NMOS and PMOS devices, here V_{it} is the shift due to the interface traps and V_{ot} – due to the oxide traps [15]

Another manifestation of the TID effect is the increase of leakage current: for example, for NMOS the positive oxide charges can activate a parasitic electron channel between n-regions at the edges of the transistor, thus even when no voltage is applied to the gate, there's leakage current flowing (Fig.1.9). Additionally, trapped charges in the shallow-trench isolation (STI) reduce inter-transistor isolation.

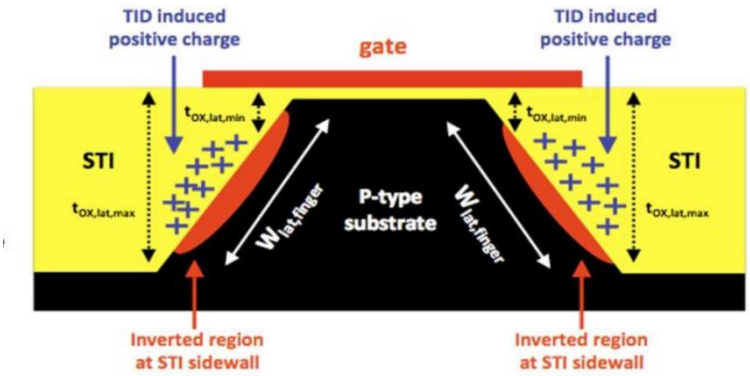


Figure 1.9 Lateral parasitic transistors caused by positive charges in STI

Due to technology scaling, the thickness of the gate oxide is decreasing, thus less charge can be generated in the gate oxide because of ionising radiation and, additionally, a larger part of the trapped holes can leave the oxide via a tunnelling mechanism. However, as gate oxide contributes less to the TID degradation, the STI traps become more significant, especially for narrow transistors.

1.3.2 Single-event effects

The discussed TID effects are cumulative, whereas the SEEs are instantaneous, being the result of the interaction of a highly energetic particle with silicon. A particle travelling in the substrate creates a certain amount (which depends on the linear energy transfer (LET)) of electron-hole pairs. Most of these electrons and holes are separated

by the electric field of the depletion region, as a result, the drift of the charge carriers causes current to flow for a brief time [19]. In general, SEEs can be either destructive or non-destructive.

A Single event upset (SEU) is a bit flip or a change of state, which occurs when a particle deposits enough energy in the critical circuit node (off-devices are sensitive). Sequential circuits suffer most because of the storage elements and typically small device sizes. Advanced technologies are more prone to SEUs, because as the technology gets smaller, less energy is needed for an upset.

Single event transients (SETs) are short voltage and current spikes, which can temporally disturb the circuit's signals. The impact of an SET on a system can be different and depends on the affected node and SET nature. In closed-loop architectures, SETs are generally compensated within the closed loop time constant. In combinatorial circuits, the duration of the SET pulse determines the effect on the circuit: if it's shorter, than the gate propagation delay, then it will fade out, but if it's longer, then it will propagate and can be captured by the sequential logic, causing an upset. Both SETs and SEUs are non-destructive, but the latter corrupts the data, which has to be fixed after.

Single event latch-up (SEL) may occur due to a highly energetic particle strike, which activates a parasitic thyristor PNPN structure [20] (Fig. 1.10). Triggering the structure causes a large latch current from the power supply to ground, thus potentially damaging the chip, which can be avoided by power cycling the device, when a latch-up is detected. To prevent SEL a larger number of well and substrate contacts is required to reduce the substrate resistance. Additionally, guard rings, isolating the PMOS and NMOS devices, can be used to improve the SEL robustness.

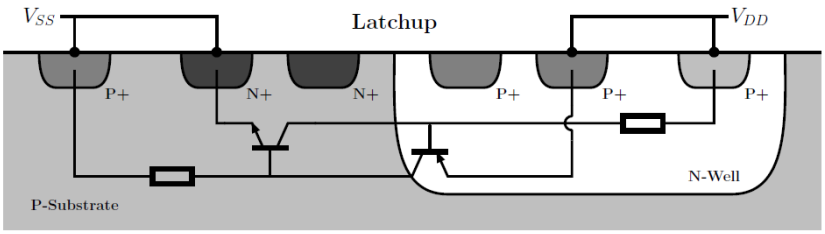


Figure 1.10 Cross-section of a CMOS structure with a parasitic thyristor shown

For designing circuits, that are meant for harsh environments, the afore-mentioned effects have to considered. With more advanced technologies being released the TID effects become less significant. Therefore, when designing a chip in technologies, such as UMC 180 nm and TSMC 65 nm, the latter will be more TID robust. While for the SEE the situation is the opposite, which is especially important for the digital parts. The single-event effects can be mitigated by using a silicon-on-insulator CMOS technology instead of bulk-CMOS, but the TID robustness would decrease, as more charges can be trapped in the buried oxide [21]. When using CMOS technology, a significant improvement of the radiation hardness can be achieved by design choices and by using a specific layout. For instance, the use of enclosed-layout transistors (ELT) significantly

reduces TID effects due to the closed gate separating the source and the drain regions, avoiding contact with the STI oxide. Since there are no gate edges, there are no parasitic transistors either. However, due to the ELT shape, the minimal size of a transistor is quite large, which results in higher power consumption. Additionally, studies have shown, that larger transistors are more robust to TID: they demonstrate lower leakage and threshold voltage shifts [22]. When comparing device types, NMOS transistors perform better, than PMOS, regarding drive-current degradation. To prevent SEL from the layout perspective, guard rings and deep n-wells are used. Some of these methods will be incorporated to protect the analog part of the TDC from the effects of ionising radiation.

For the digital part of the system triple modular redundancy (TMR) is used to prevent SEEs, since they can change the state of the logic, resulting in corrupted data. Basically, TMR is just triplicating all the logic cells: this way if data in one of them gets corrupted, the voter (also triplicated as they are sensitive to SEU, too) selects the two correct outputs, unaffected by the SEU. But, naturally, since all the cells are triplicated, then the area and power consumption are also increased proportionally [23].

2. Methodology of delay cell design analysis

A tunable delay cell is the core of the delay line based (including DLL and PLL-based) TDC. Its purpose is to create a precise and controllable delay, which allows us to compensate for the process, temperature and supply voltage variation (PVT variations), performance degradation due to ageing and, even more importantly in our case, total ionising dose in a harsh radiation environment.

Thus, to have a cell, whose architecture allows to have the least effect of the mismatch, PVT variations, jitter on the generated delay, and enough tuning range to compensate for the degradation we have to perform theoretical (analytical) and more practical (simulation) analysis.

The chosen delay elements (DEs) for the project are the Lee-Kim [24] and Maneatis cells [25].

2.1 Theoretical analysis of the delay cells

2.1.1 Lee-Kim cell

The Lee-Kim cell (Fig. 2.1 (a)) is a differential delay cell, which consists of an NMOS input pair, a cross-coupled PMOS latch, that provides positive feedback (FB), and a pair

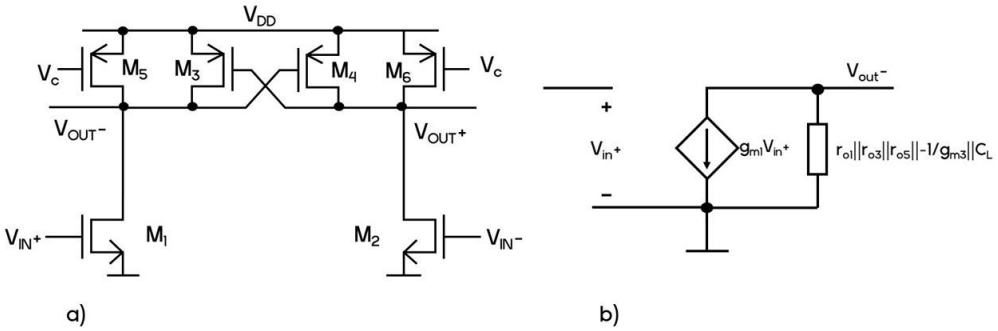


Figure 2.1 a) The schematics of a Lee-Kim delay element, b) small-signal model of the cell

of current-starving PMOS, that allows the control over the delay of the cell. In order to build a PLL-based TDC, we have to ensure, that the cell has enough small-signal gain to oscillate. Let us perform the small-signal analysis to understand, what would influence the delay and gain of the DE.

First, let's start with making a small-signal model of the cell and simplify it a bit (Fig. 2.1 (b)), then using common relationships, find the expressions for gain and oscillation frequency (hence the delay) of the cell. As we know, the gain of the circuit can be found as the product of transconductance and output resistance, in our case we can write (1).

$$A = G_M R_{OUT} = \frac{G_m}{G_{out}} = \frac{-g_{m1}}{\Sigma g_{ds} - g_{m3} + sC_L} = \frac{\frac{-g_{m1}}{G_{ds} - g_{m3}}}{1 + s\frac{C_L}{G_{ds} - g_{m3}}}. \quad (1)$$

So, we can see, that the DC gain equals:

$$A_0 = \frac{-g_{m1}}{G_{ds} - g_{m3}}, \tag{2}$$

and the cut-off frequency:

$$\omega_p = \frac{G_{ds} - g_{m3}}{C_L} \tag{3}.$$

The frequency of the oscillation for a ring oscillator, that would satisfy the Barkhausen criterion, is given (2).

$$\omega_{osc} = \tan\left(\frac{180^0}{N}\right)\omega_p = \tan\left(\frac{180^0}{N}\right)\frac{G_{ds} - g_{m3}}{C_L}. \tag{4}$$

To satisfy the second condition, the loop gain should be larger, than one (5).

$$\frac{\left(A_0\right)^N}{\left(\sqrt{1+\left(\frac{\omega_{osc}}{\omega_p}\right)^2}\right)^N} = 1 \Rightarrow A_0 = \sqrt{1+\left(\tan\frac{180^o}{N}\right)^2}. \tag{5}$$

To ensure the oscillation against PVT variations, we would have to provide a factor of 2…3 in gain margin. With a loop margin of 2.5 for a 16-stage ring oscillator, the DC gain of a cell should be equal to at least: A_o = 1.08, for 32 stages: A_o = 1.029, for 64 stages: A_o = 1.016.

So we see, that to increase the gain of the Lee-Kim cell, we have to increase the transconductance of the input NMOS and FB PMOS pair and increase the output resistance of the control and FB transistors, which can be done with proper sizing. But we need to balance a larger gain and a smaller delay. As we can see, from the frequency equation, the delay is proportional to:

$$t_d \sim \frac{C_L}{G_{ds} - g_{m3}}. \tag{6}$$

So the increase of output resistances and the transconductance of the latch would increase the delay directly, and an increase of the input pair width would for sure increase the drive and hence decrease the delay, but also increase the capacitive loading, thus, increasing the delay. So, the actual sizing can be found with the help of simulation.

We can control the current and thus the delay with the control voltage, which is applied to the gates of the current-starving PMOS. If the tuning transistors are in saturation, then we can say, that delay is inversely proportional to the control voltage squared of the PMOS.

2.1.2 Maneatis cell

The main difference between the Maneatis and Lee-Kim cell is the bias circuit, which is used for the former [25] (Fig. 2.2). This "boosted" biasing utilizes a traditional 5T OTA, which helps to reduce supply sensitivity, it detects changes in the replica bias due to VDD variation and adjusts the gate voltage of the NMOS current source (V_{BN}), thus keeping the output swing constant even with the tail current source with finite impedance. Copy of control voltage from a half-buffer replica (V_{BP}) biases the symmetric load, while the amplifier adjusts the gate voltage of the NMOS tail source accordingly [26].

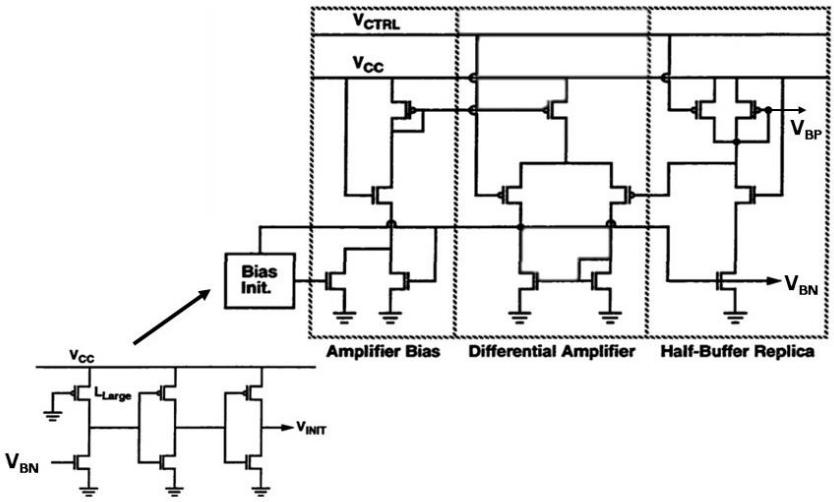


Figure 2.2 Bias circuit for Maneatis delay cell [25]

A similar analysis as with the Lee-Kim cell is done for the Maneatis cell (Fig. 2.3).

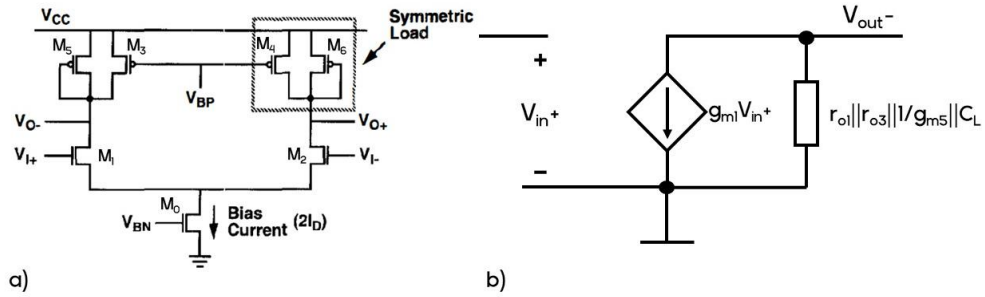


Figure 2.3 a) The schematics of a Maneatis delay element, b) small-signal model of the cell

The gain of the circuit can be found as:

$$A = G_M R_{OUT} = \frac{G_m}{G_{out}} = \frac{-g_{m1}}{\Sigma g_{ds} + g_{m5} + sC_L} = \frac{\frac{-g_{m1}}{G_{ds} + g_{m5}}}{1 + s\frac{C_L}{G_{ds} + g_{m5}}}. \quad (7)$$

Thus, the DC gain of the circuit equals:

$$A_0 = \frac{-g_{m1}}{G_{ds} + g_{m5}}, \tag{8}$$

and the cut-off frequency:

$$\omega_p = \frac{G_{ds} + g_{m5}}{C_L}. \tag{9}$$

So, the oscillation frequency can be found by (4):

$$\omega_{osc} = \tan\left(\frac{180^0}{N}\right)\frac{G_{ds} + g_{m3}}{C_L}. \tag{10}$$

The needed gain can be achieved by increasing the transconductance of the input NMOS, the output resistances of the transistors and decreasing the transconductance of the symmetric load. The buffer delay is proportional to:

$$t_d \sim R_{\text{eff}} C_{\text{eff}} \approx \frac{C_{\text{eff}}}{g_{m5}}, \tag{11}$$

where C_{eff} is the effective output capacitance of the buffer. The drain current of one of the symmetric pair transistors can be found as:

$$I_D = \frac{k}{2}(V_{ctrl} - V_{th})^2. \tag{12}$$

Therefore, the delay is defined as [25]:

$$t_d = \frac{C_{\text{eff}}}{g_{m5}(V_{ctrl} - V_{th})}. \tag{13}$$

2.2 Simulation of the delay cells

The methodology of the analysis of a single delay cell is described next (Fig. 2.4):

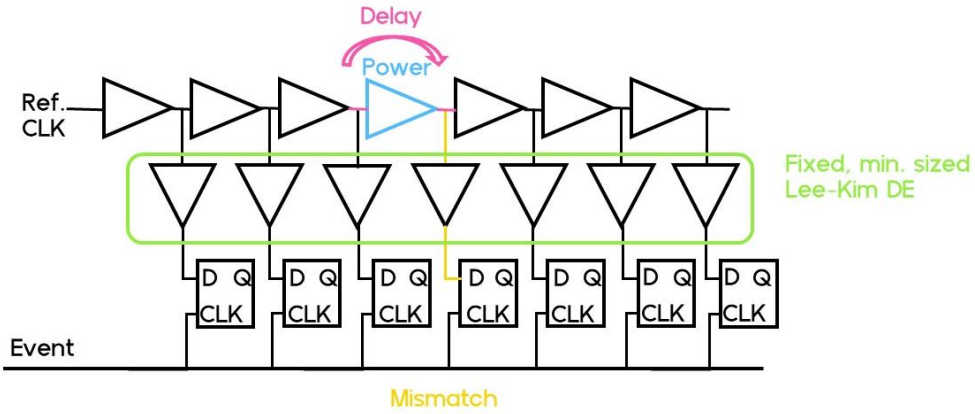


Figure 2.4 Methodology of single delay cell analysis

In order to simulate the circuit and optimize a delay cells with behaviour close to the one, in a delay line, we need to construct a short delay line: three buffers before and after the DE, which we are testing. Also, it is important to load each delay element of the

line with additional distributional buffers like in the actual DLL or PLL-based converter, this way we will have a more realistic delay and additional loading of the distributional buffers won't be underestimated. For the initial stages of the optimization we use minimal-sized Lee-Kim delay cells as distributional buffers, as the sampling registers rad-hard DICE flip-flops (FF) are used. In order to mimic a ring-oscillator behaviour, the steepness of the reference clock is set to be approximately the same as the last loaded delay cell. To analyse a certain design choice we simulate this test-bench to see its effect on the delay propagation and power consumption of a single cell. To evaluate the effect of the local device mismatch on the performance, we look at the standard deviation of the delay obtained in Monte Carlo analysis both at the output of the DE and at the input of the FF.

For jitter analysis, we have a different test bench, which consists of a single delay cell (to avoid accumulated jitter), which is loaded with its copy and a distributional buffer (Fig.2.5). To find jitter we run a long transient analysis with noise and then find the standard deviation of the delay. In the case of jitter analysis, the slope of the signal is crucial, so to get a reliable result, the slope of the reference clock is set to be the same as the last loaded delay cell, this way once again imitating RO operation.

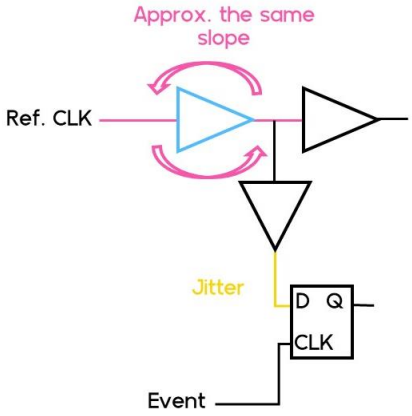


Figure 2.5 Methodology of jitter analysis

3. Results of single-cell analysis

This section is dedicated to the discussion of the analysis results, which has been outlined in the previous chapter. The goal of the analysis was to find the optimum sizing of the buffers, which would satisfy the trade-offs between power, delay, mismatch and jitter, which would ensure a wide enough tuning range to be able to reach the lock at the goal frequency in all the PVT corners and with the degradation due to ageing and radiation. The analysis has been done in two technologies: UMC 180nm and TSMC 65nm, the lengths of the transistors have been set to minimum, unless stated otherwise. The supply voltage for 180-nm technology is 1.8 V and for 65-nm it is 1.2 V.

3.1 180 nm CMOS

3.1.1 Lee-Kim delay cell

The optimization of the delay cell starts with the attempts to minimize the delay using the circuit parameters, such as the transistors' sizing. Naturally, when it comes to speed one wishes to make the transistors wider, thus, getting into one of the new designer's pitfalls, because it will also increase the loading. Another Mr. Hyde to this Dr. Jekyll is increased power consumption, crucial for space or battery-powered applications, where power is the bottleneck.

As can be seen from the previous analysis, we should be able to decrease the delay by making the input NMOS wider. Let's see the effect of the sizing of NMOS and current starving (CS) PMOS on the delay and power (Fig. 3.1), and of the FB PMOS (Fig. 3.2). The analysis is done at the control voltage: Vc = 0.3 V.

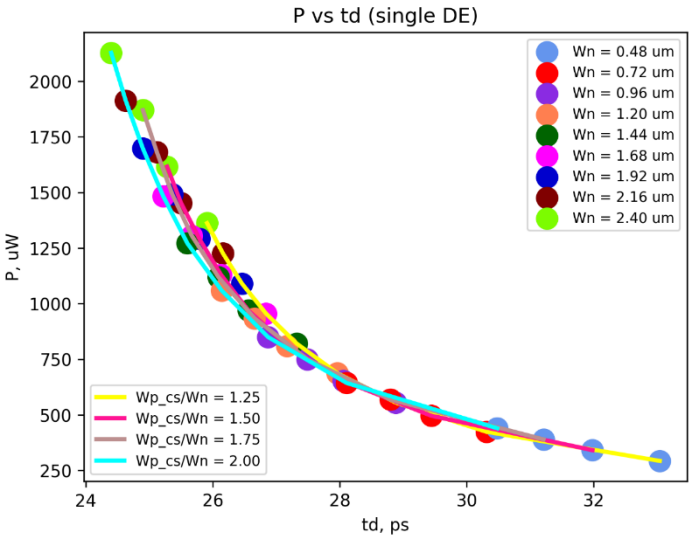


Figure 3.1 Delay vs power consumption of Lee-Kim cell (180 nm) at different width of NMOS (W_n) and ratios of width CS PMOS to NMOS (W_{p_cs}/W_n)

Conclusion:

- the width of NMOS is critical for the delay, but we have to compromise with power: stick to a reasonably small (regarding possible radiation effects, mismatch and noise) NMOS width (around 0.72 µm to 0.96 µm)

- the ratio of CS PMOS to NMOS width has to be chosen regarding compromise delay/power (but the effect is less pronounced, than in the case of NMOS width): around 1.5 seems reasonable
- the ratio of FB PMOS to NMOS is better to be chosen smaller (for both delay and power), so it's best to have latch PMOS two times smaller, than input NMOS.

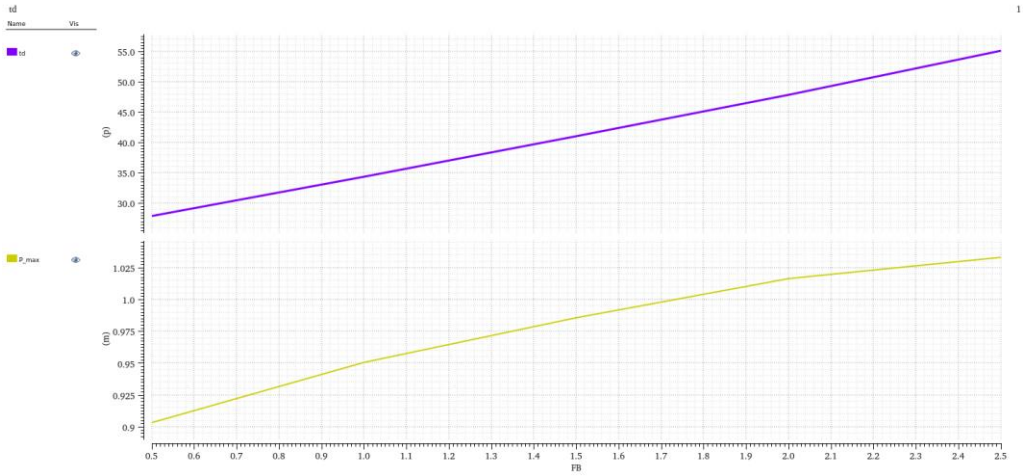


Figure 3.2 Delay and power consumption of Lee-Kim cell (180 nm) vs width ratio of FB PMOS to NMOS (FB)

Next, increasing the width of the FB transistors will improve the power supply (PS) immunity of the circuit, as has been shown in the literature [27]. However, according to the small signal analysis (and common sense) making the latch stronger will increase the delay, so we have another trade-off: PS sensitivity and delay (Fig. 3.3).

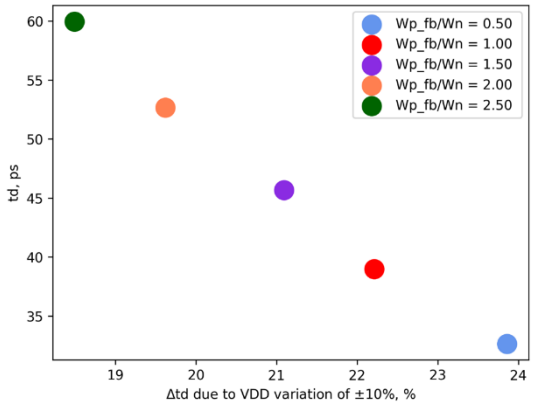


Figure 3.3 Delay variation of Lee-Kim (180nm) due to VDD change (1.62...1.98V) vs delay for different width ratios of FB PMOS to NMOS

Since the ratio of FB PMOS width to NMOS affects the immunity to V_{DD} variation only mildly, but crucially – the delay: we have to prioritize minimizing the delay, so latch PMOS two times smaller, than NMOS is still the optimum choice.

To see, how the mismatch between transistors would affect the delay of the cell, we run a Monte Carlo analysis and take the standard deviation of the delay, which we will try to minimize. As the mismatch is more pronounced [28] in smaller devices, and wider devices draw more current, again we foresee a power and delay deviation trade-off. The effect of circuit parameters on the mismatch is given in Figure 3.4.

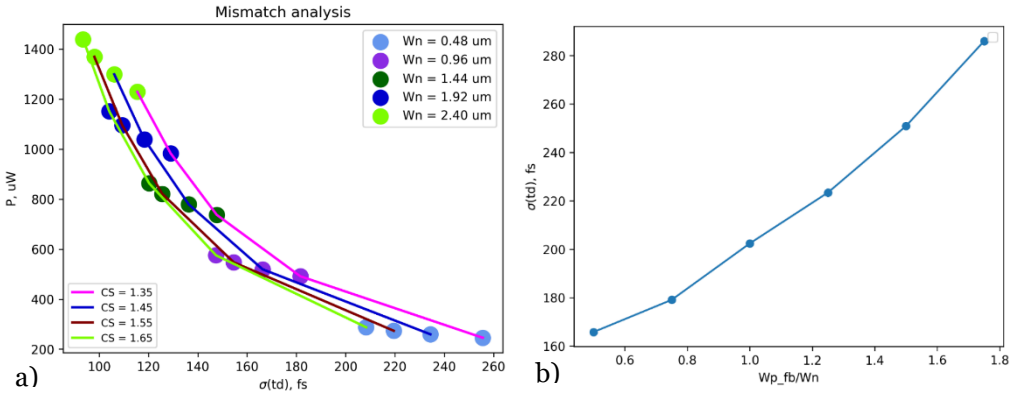


Figure 3.4 a) Delay deviation due to local mismatch of Lee-Kim cell (180 nm) vs. power consumption at different NMOS and CS PMOS widths, b) Delay deviation due to local mismatch vs FB PMOS to NMOS width ratio

Conclusion:

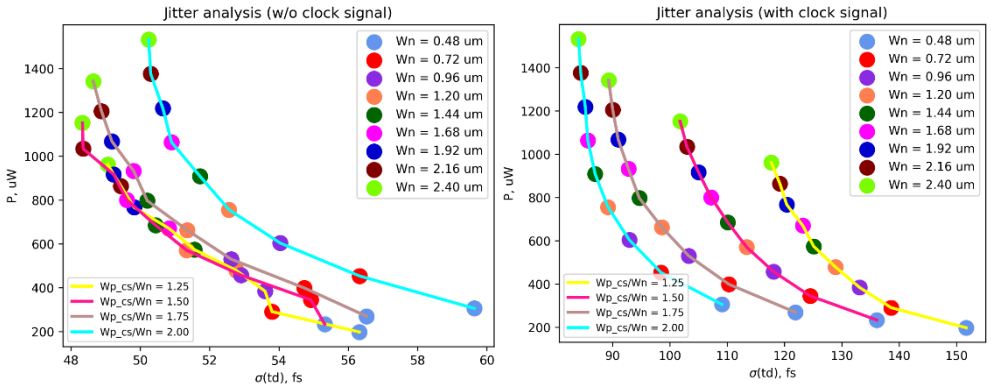
- For smaller deviation we have to choose a smaller FB PMOS (as a bonus we also have lower power consumption and smaller delay)
- For optimum deviation the CS ratio should be around 1.35…1.75 (small difference in both delay and its deviation).
- Smaller delay deviation in case of mismatch favours larger widths of NMOS (bonus: significantly smaller delay), but is limited by power budget.
- Since the delay deviation is negligible (around 200 fs in case of NMOS width of 0.72 µm and CS PMOS of 1.08 µm) compared to one LSB (around 29 ps), it's better to prioritize power and settle for reasonably small transistors.

Next, to perform a jitter analysis, we run a long transient with added noise and calculate the standard deviation of delay in each cycle. We have slightly different results, in the case when there's an event coming to the clock input of FF (Fig. 3.5(a)) (when we actually sample an event) and in the case, when no event is coming (Fig. 3.5(b)). This is due to the fact, that the clock signal, which arrives at FF, can either help or hinder our timing signal from the delay cell, depending on the time of the arrival (coinciding of edges).

Thus, for smaller jitter:

- it's better to have larger input transistors (up to 1.2 µm, the further increase doesn't yield much improvement), which corresponds to theoretical considerations as jitter increases for lower current levels and longer delays [29], thus correlating with the delay analysis results;

- a larger ratio of CS PMOS to NMOS (which also ensures a smaller delay, that is directly translated into lower jitter) and smaller FB PMOS.
- but since jitter is much smaller, than one LSB, and is not significantly affected by tuning the circuit parameters, it's more reasonable to go for a low-power solution.



a) b)

Figure 3.5 Jitter analysis of Lee Kim cell (180nm). Delay deviation vs power consumption: a) no event arrives at FF, b) with an event arriving at the CLK input of FF

As the final step of the analysis, we have to check the chosen design of the delay cell for tuning range in different corners. Since the circuit has to acquire a lock at a certain frequency for DLL or PLL, we need to make sure, that the same delay is reachable in all PVT corners, at the (Fig. 3.6) we can see simulated corner process, while voltage and temperature variation will be examined for the final design.

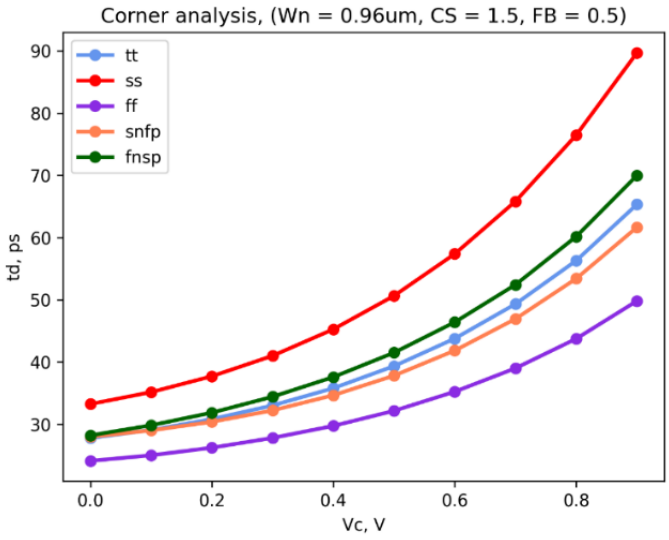


Figure 3.6 Corner analysis of Lee-Kim cell (180 nm)

3.1.2 Maneatis cell

The same analysis, as in the case of the Lee-Kim cell, is performed to optimize the Maneatis cell (Fig. 3.7).

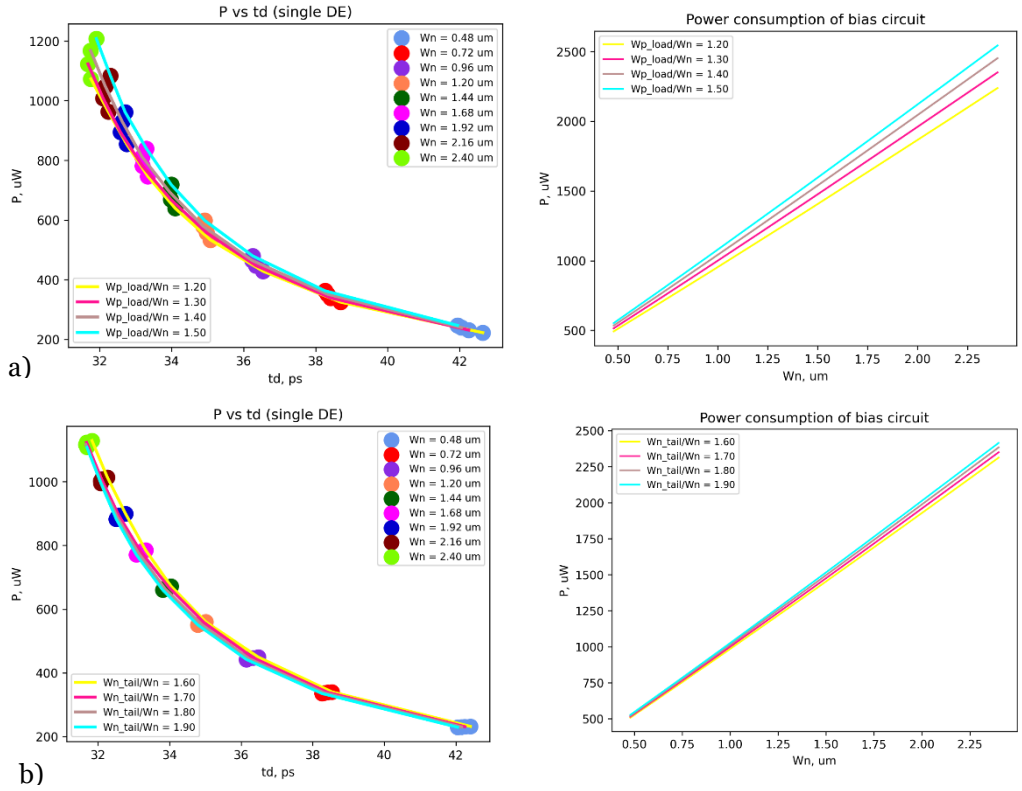


Figure 3.7 Delay vs power consumption of Maneatis cell (180nm) and power consumption of bias circuit for different NMOS width and a) ratio of widths of load PMOS to NMOS; b) ratio of widths of tail current source to input NMOS

Analysing, the simulation results, we can make the following **conclusions**.

- For a smaller delay, a wider input NMOS is better, but the minimum delay, that can be reached is limited by the power budget of the circuit, so it's better to choose a reasonably small W_n (around 0.96 to 1.44 μm) for the optimum in power↔delay trade-off.
- The ratio of load PMOS width to input NMOS (W_{p_load}/W_n) almost doesn't affect (in the vicinity of the optimum) either power consumption or delay; the best ratio is proved to be around 1.3.
- The ratio of current source width to input NMOS (W_{n_tail}/W_n) also has a limited impact on the delay, which improves with increasing the width of the tail current source. In the simulations, the channel length of the current source was set to be twice the minimal length (360 nm) to minimise the influence of supply variations, which is manifested due to the finite output resistance of the current source. So indefinitely increasing the width of the tail NMOS would counteract the attempt to increase supply immunity. Considering those, it's reasonable to set the width of the tail source to be 1.7 times larger than the input NMOS.

As mentioned earlier, the sensitivity of the circuit to supply variation can be minimized, if the current source resistance is increased. To find the optimum value for the channel length of the tail current source we perform simulations of delay variation due to VDD change of ±10% (1.62 V – 1.98 V) compared to nominal at different channel lengths of the tail NMOS (Fig. 3.8). As we can see, the curve reaches a plateau, so there's no point in making the transistor longer, than 360nm, as it was set initially based on theoretical considerations.

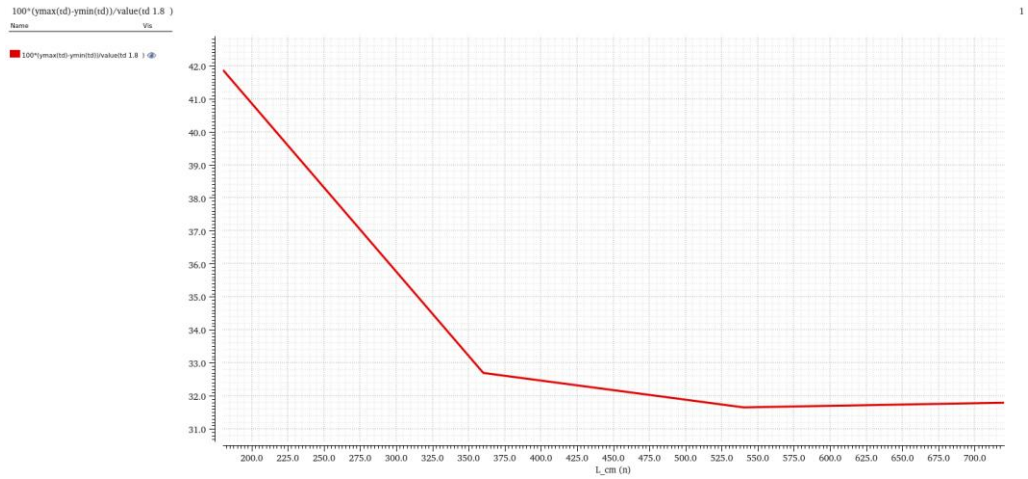


Figure 3.8 Delay variation of Maneatis cell (180nm) due to VDD variation of ±10% (1.62V...1.98V) vs tail current source channel length

Next, we perform a series of Monte Carlo analyses to determine the parameters of the circuit, which is the most robust concerning local mismatch (Fig.3.9).

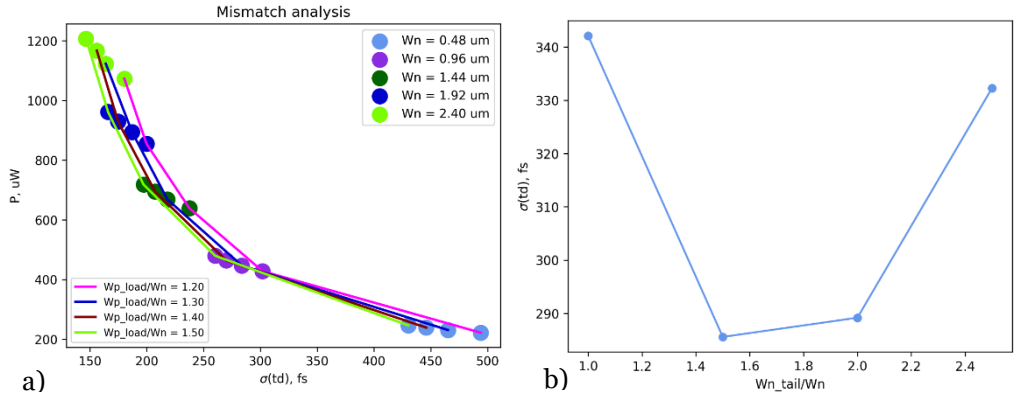


Figure 3.9 Mismatch analysis of Maneatis cell (180 nm). a) Standard deviation of delay due to local mismatch vs. power at different input NMOS width (W_n) and widths ratios of load PMOS to input NMOS (W_{p_load}/W_n); b) standard deviation of delay vs. ratio of tail source width to input NMOS (W_{n_tail}/W_n)

Conclusions:

- For smaller deviation, the width of input NMOS should be larger (bonus: smaller delay), but as the deviation of mismatch is extremely negligible to LSB (around 300 fs of deviation at the LSB value of 36 ps).

- Increasing the W_{p_load}/W_n ratio is beneficial for smaller mismatch, but the effect is rather small.
- For the width ratio of tail source to input NMOS there's a clear optimum value of around 1.7.

The jitter analysis demonstrates the difference in jitter values for the case, when an event is arriving at the FF and is being sampled (Fig. 3.10 (b)), and the case, when no event arrives at the FF, so it stays idle (Fig. 3.10 (a)). Since we are more interested in jitter, that would be in the way of an accurate measurement, the case with the event arriving at the FF is more representative. In both cases, it's best to have a large input NMOS due to greater current and smaller propagation delay, as follows from theory [29].

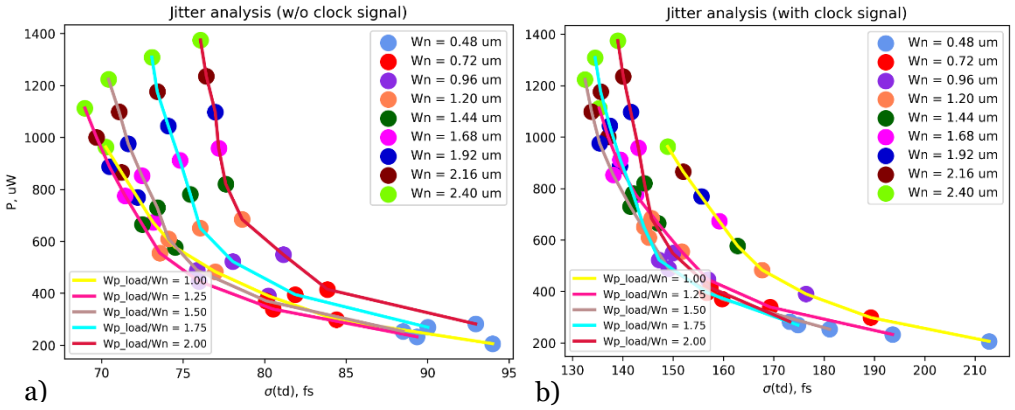


Figure 3.10 Jitter analysis of Maneatis cell (180nm). Jitter vs power at different circuit parameters a) no event arrives at FF, b) event arrives and is sampled by FF

In addition, it seems to be best to keep a W_{p_load}/W_n around 1.5-1.75 (depending on input NMOS width) and a smaller W_{n_tail}/W_n ratio. However, it should be noted, that in either case, the influence of circuit parameters on the jitter is not significant. Therefore, this analysis cannot be decisive.

Another thing worth mentioning is that the control voltage limits the swing of the delay cell: the output voltage cannot go lower, than the control one. This is a significant drawback, especially, when higher delays are needed and control voltage is increased.

Corner analysis is essential to ensure the correct operation of the circuit at the aimed frequency despite process variations (Fig. 3.11). We can see, that, unfortunately, this delay cell cannot reach the same delay in all corners, specifically, for the slow-slow and fast-fast lots.

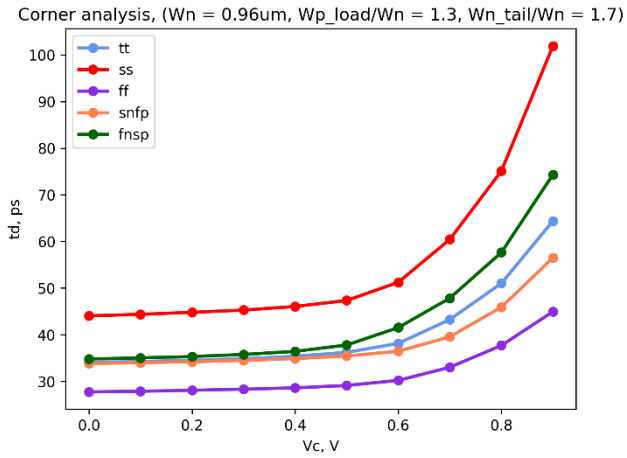


Figure 3.11 Corner analysis of the Maneatis cell (180 nm)

3.2 65 nm CMOS

With the transition to a newer, smaller technology we expect a reduction in both propagation delay and power consumption. The same analysis methodology is applied here. The low threshold voltage (LVT) transistors are chosen to reduce the delay.

3.2.1 Lee-Kim cell

First, we want to see the trade-off between minimum possible delay and power consumption (Fig. 3.12), where we expect approximately the same trends as in 180-nm technology.

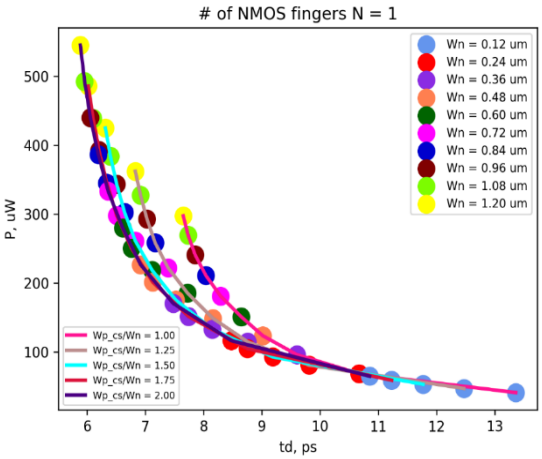


Figure 3.12 Delay vs power consumption of Lee-Kim cell (65 nm) at different width of NMOS (W_n) and ratios of width CS PMOS to NMOS (W_{p_cs}/W_n)

We can see that our anticipations were, indeed, correct. The LSB value dropped from approximately 29 ps to 9 ps. Again, increasing the drive strength by putting wider input transistors is beneficial for the delay to a point, when the parasitic capacitances provide too much load, so the larger NMOS becomes a detriment, instead of an improvement. Naturally, we are limited by the power budget, so the optimum point seems to be on the

bending of the curve: this way both the power consumption and delay are kept reasonably low. Therefore, the optimal width of NMOS is about 240-360 nm.

It is better for minimising the delay to have a larger CS PMOS to NMOS width ratio, but making these transistors too wide would compromise the gain. From the simulations, it has been found, that the value of W_{p_cs}/W_n, which would provide enough gain to satisfy the Barkhausen criterion for all the widths of input NMOS: A_0 = 1.08 for a 16-stage oscillator (this includes a loop gain margin of 2.5), is 1.5.

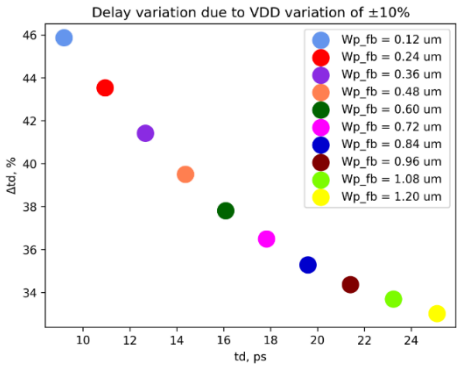


Figure 3.13 Delay variation of Lee-Kim (65 nm) due to VDD change (1.08...1.32 V) compared to nominal (at 1.2 V) vs delay for different widths of FB PMOS

The width of feedback PMOS devices, that create the latch, has a direct impact on the delay and power supply immunity (Fig. 3.13). The effect on supply sensitivity is quite limited, but the delay of the cell skyrockets, so it is best to keep it minimal sized.

To investigate the impact of local mismatch on the delay, a Monte Carlo analysis is performed (Fig. 3.14). To keep delay deviation due to mismatch smaller, we need to go for larger NMOS (at least, not minimally sized, increase of the width beyond 360 nm is not beneficial), large CS PMOS to NMOS widths ratio (Fig. 3.14(a)) and smaller width of FB PMOS (Fig. 3.14(b)).

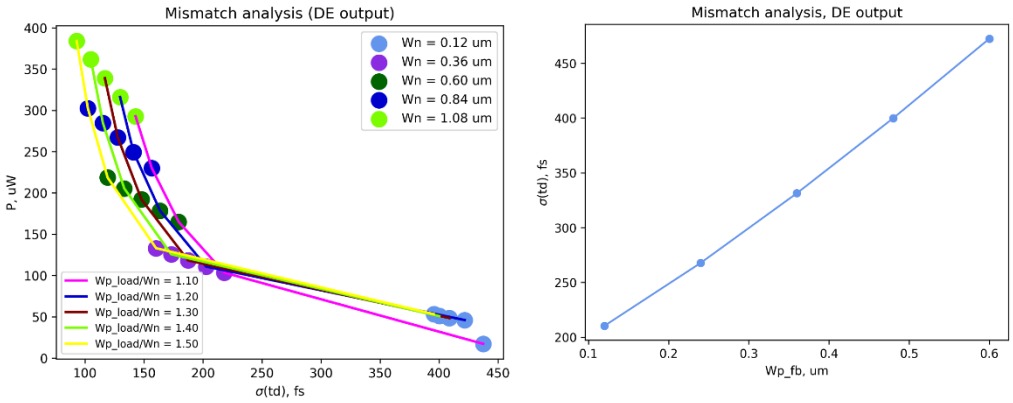


Figure 3.14 a) Delay deviation due to local mismatch of Lee-Kim cell (65 nm) vs power consumption at different NMOS and CS PMOS widths, b) Delay deviation due to local mismatch vs FB PMOS width

As the jitter, seen at the input of the FF has a large contribution from distributional buffers, we want to check it both at the DE output (distributional buffer input) and FF input (distributional buffer output), as they may show different trends (Fig. 3.15). We can see a trend, which seems counterintuitive, at the FF input (the case of an event being sampled), it seems, that for a smaller jitter, we would have to have a smaller input NMOS, but the effect of transistors' sizing on jitter here is quite insignificant (25 fs of difference). Therefore, it's best to aim for lower jitter, which is seen at the output of the delay cell, and when those are designed – design distributional buffers for lower jitter at their output. If we consider jitter at the output of our delay cells, then wide NMOS (up to 600nm, same as we still have improvement of delay) is better for jitter, while CS PMOS to NMOS widths ratio doesn't have much impact, as for FB PMOS it's best to have it minimally sized (as a bonus we also get smaller delay).

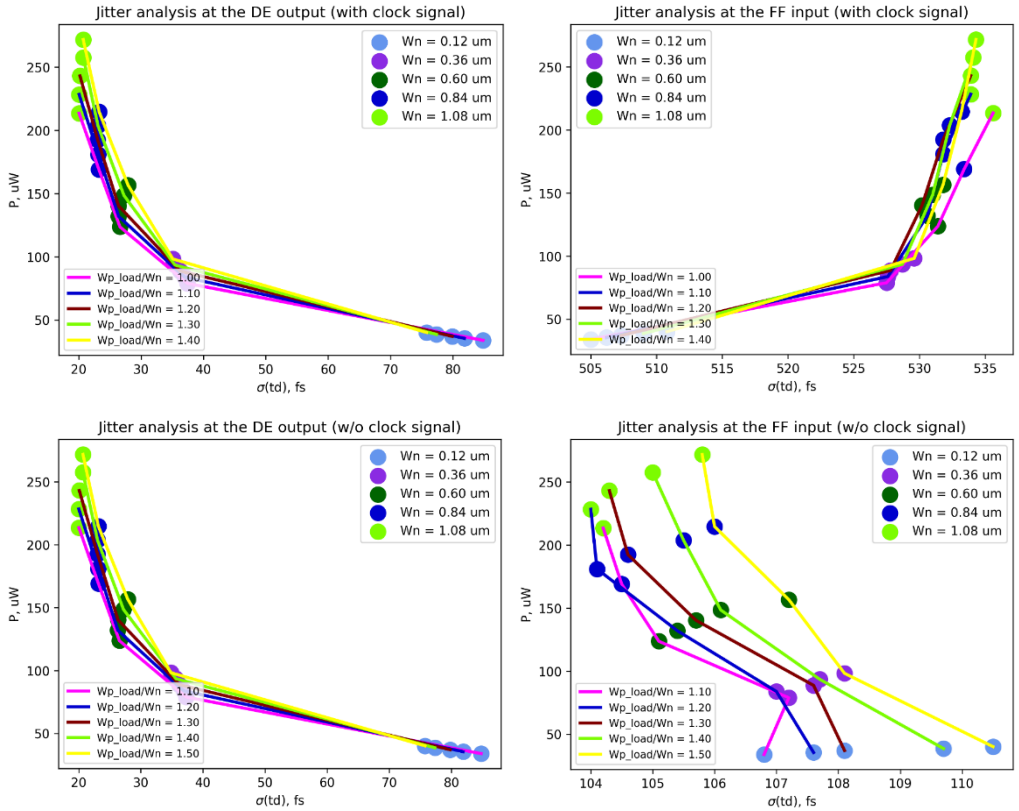


Figure 3.15 Jitter analysis of Lee Kim cell (65 nm). Delay deviation vs power consumption at the DE output and FF input: a) with an event arriving and being sampled at the CLK input of FF, b) no event arrives at FF

To get a tuning range closer to reality, we add capacitors, whose values are equal to the extracted parasitics. Thus, we can estimate the expected degradation due to layout parasitics (Fig. 3.16(a)), also we can translate the delay of a single cell to an expected frequency of a voltage controlled ring oscillator for a PLL stabilized delay line (Fig. 30 (b)), using the formula:

$$f_{VCRO} = \frac{1}{2 \cdot N \cdot t_d}, \tag{14}$$

where N is the number of stages of the oscillator, which typically for application in TDC is the power of two to facilitate counting.

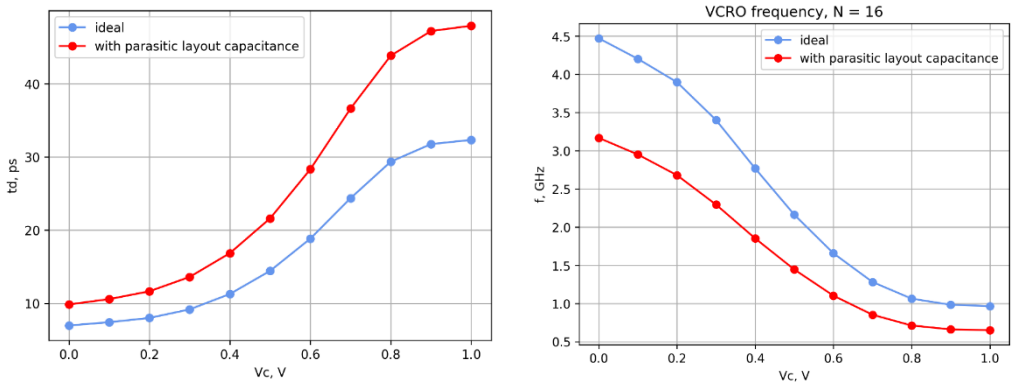


Figure 3.16 a) Tuning range of Lee-Kim cell (65 nm); b) Tuning of 16-stage VCRO based on Lee-Kim cell (65 nm)

Let's simulate the work of the oscillator to find the phase noise (Fig. 3.17) (V_c = 0.4 V), which is very important for the design of the control DAC. At the relative offset frequency of 1 MHz the additive phase noise from a single cell equals -82.3 dBc/Hz.

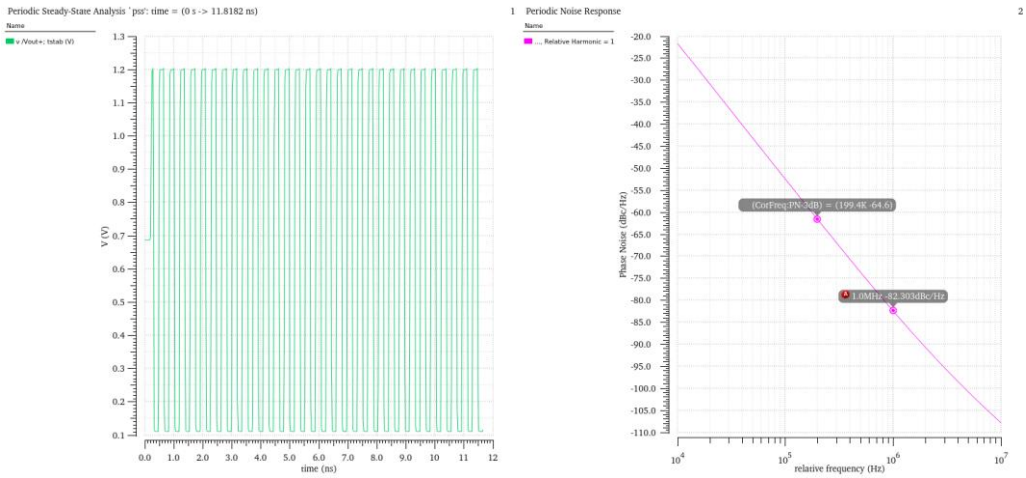


Figure 3.17 Simulation of Lee-Kim (65 nm) based 16-stage VCRO and its phase noise

One of the advantages of a Lee-Kim cell is the near rail-to-rail swing. Nevertheless, at very low control voltages, the lower limit output voltage is higher, since the current starving PMOS are very on.

3.2.2 Maneatis cell

We repeat the same analysis for the Maneatis cell: first, we try to optimize the transistors' sizing for the speed-power trade-off (Fig. 3.18).

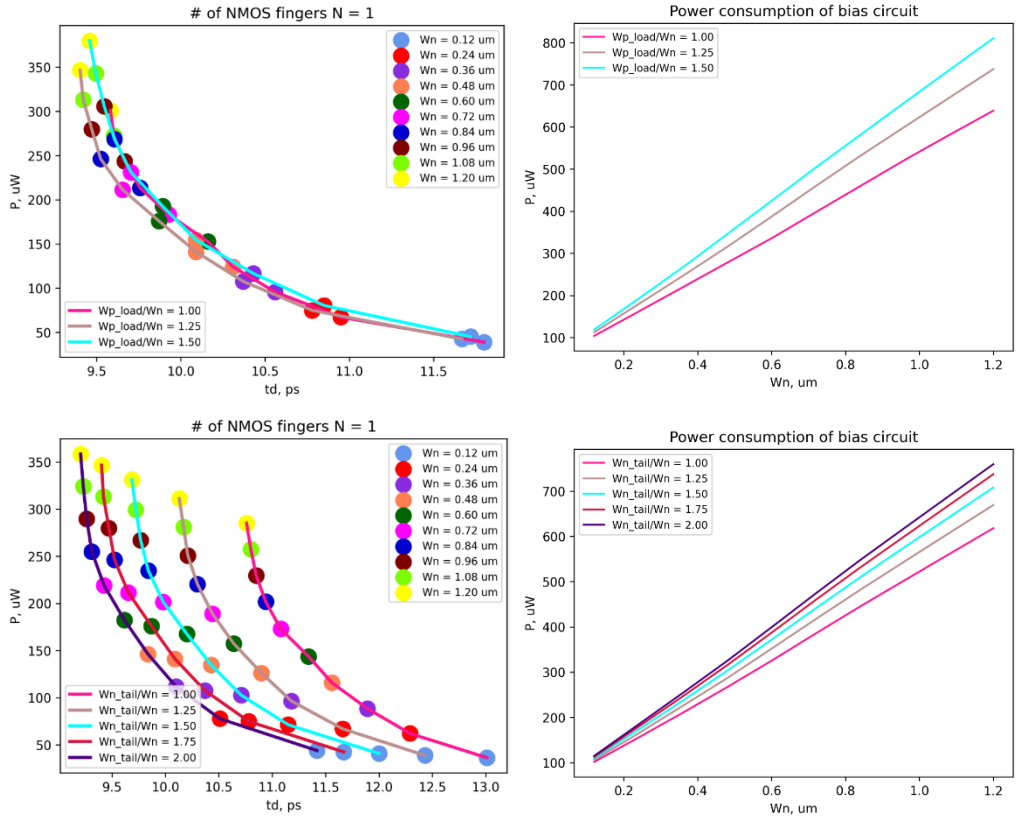


Figure 3.18 Delay vs power consumption of Maneatis cell (65 nm) and power consumption of bias circuit for different NMOS width and a) ratio of widths of load PMOS to NMOS; b) ratio of widths of tail current source to input NMOS

Conclusions

- To minimise the delay we have to increase the width of the input NMOS – W_n (up to 0.84 µm width. Further additional loading of the larger device dominates over increased drive, so we don't have much improvement, but as always the price to pay is increased power consumption, so it's best to settle for a comparatively small NMOS (240…360 nm).
- Even though the width of load PMOS to NMOS ratio doesn't seem to influence either the delay or the power, there's a clear optimum for the former with a W_{p_load}/W_n of 1.25.
- Increasing the width of the tail current source is beneficial for the delay, since the delay of the circuit is reversely proportional to the current, but at the same time, we decrease the output resistance of the current source, making the circuit less immune. A reasonable channel width of tail NMOS is approx. 1.75 times larger than the input transistor.

  Next, we perform simulations to check the circuit's sensitivity to supply variation, here we can investigate the influence of the channel length of the tail current source.

We can see (Fig. 3.19(a)), that delay for the minimal length (60 nm) of the current source (red curve) varies more with the change of supply voltage, than in the cases of longer tail current source (yellow – 120nm, green – 180nm). On the (Fig. 3.19(b)) the relative change of delay due to ±10% supply variation for different length of tail current source is shown.

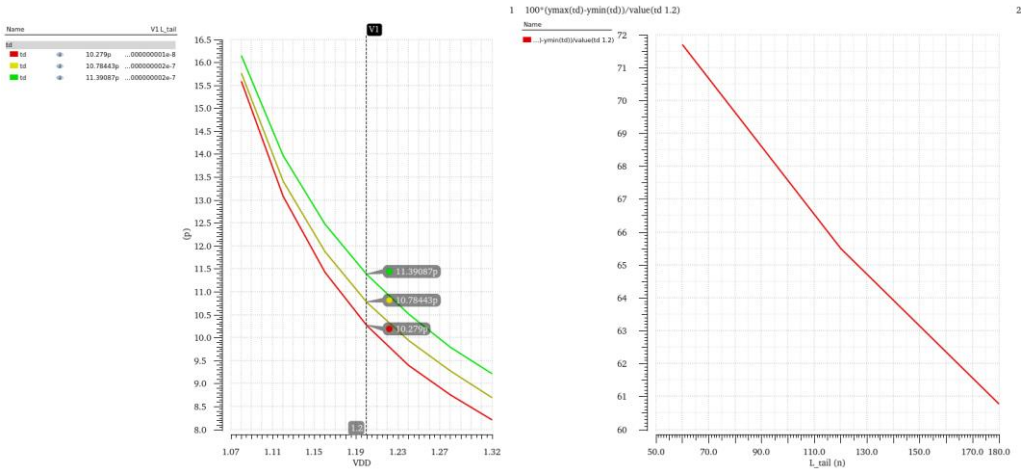


Figure 3.19 a) Delay of a Maneatis cell (65nm) due to V_{DD} change (1.08V...1.32V) with channel length of tail current source as parameter; b) Delay variation (%) of the cell due to V_{DD} change of ±10% (1.08V...1.32V) vs tail current source channel length

We can conclude, that increasing the length of the tail NMOS positively affects the circuit's immunity for supply variations, but at the same time it also increases the delay of the DE, so we have to compromise and a reasonable decision is to make it twice the minimal channel length (120 nm).

To strengthen the circuit against local mismatches of the transistors, a Monte Carlo analysis is performed. Again, we expect a trade-off of robustness versus power, as larger devices are better concerning mismatch (Fig. 3.20).

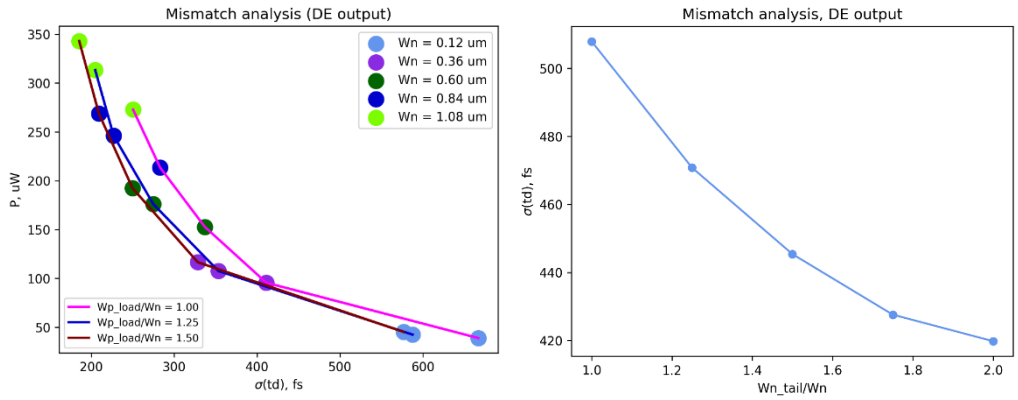


Figure 3.20 Mismatch analysis of Maneatis cell (65 nm). a) Standard deviation of delay due to local mismatch vs power at different input NMOS width (W_n) and widths ratios of load PMOS to input NMOS (W_{p_load}/W_n); b) standard deviation of delay vs ratio of tail source width to input NMOS (W_{n_tail}/W_n)

We can conclude, that a larger input NMOS and PMOS load are indeed better for reducing delay variation of a cell due to local mismatch, but in the case of the latter the effect is rather weak, additionally, a larger tail NMOS is also better for mismatch, even though the impact is quite limited too. Since we aim for low power, we stick with 240-480 nm of input NMOS, symmetrical load PMOS, that are larger with a ratio of about 1.25-1.5, and a tail current source around 1.7 (as the dependency changes slope around that value) times wider, than the input transistors.

To analyse the performance of the circuit with respect to jitter, we run a long transient analysis with added noise and measure the delay in each cycle, thus calculating the standard deviation of the delay (Fig. 3.21).

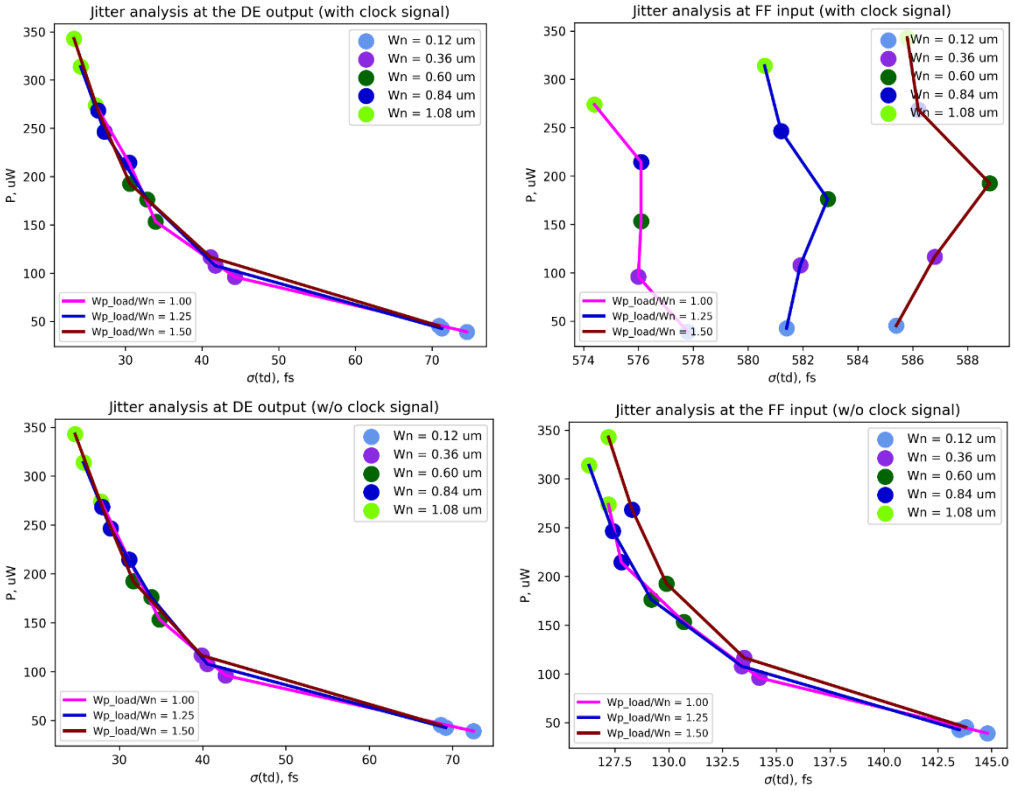


Figure 3.21 Jitter analysis of Maneatis cell (65 nm). Delay deviation vs power consumption at the DE output and FF input: a) with an event arriving and being sampled at the CLK input of FF, b) no event arrives at FF

We can see, that, as before, a clock signal, that arrives at the flip-flop greatly affects the delay, seen at the FF, sometimes helping and sometimes hindering the timing signal. But this can be improved with proper design of distributional buffers, as for now minimally sized Lee-Kim cell is used, which worsens jitter. In the case, when an event is actually being sampled, we can't really affect (introduced improvement of 10 fs can be achieved) the jitter seen at the flip-flop by changing the circuit parameter of the main delay cells. As for the jitter, seen at the output of the DE, enlarged input devices are beneficial (width of 360 nm shows a fine compromise of jitter against power), where PMOS and tail NMOS widths have extremely limited impact.

Formula (14), allows to calculate the expected frequency of the VCRO. Here, this is done for both the ideal case and the case with added parasitics, to estimate the post-layout degradation (Fig. 3.22).

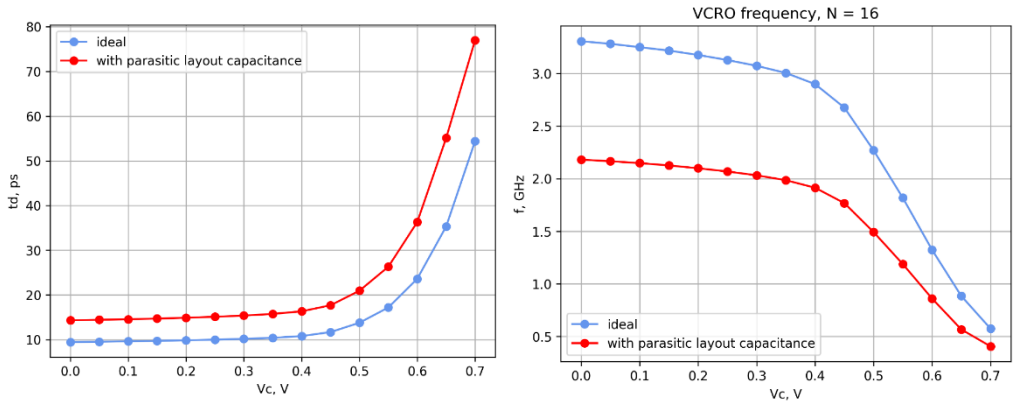


Figure 3.22 a) Tuning range of Maneatis cell (65 nm); b) Tuning of 16-stage VCRO based on Maneatis cell (65 nm)

3.3 Intermediate conclusions

After careful and thorough single-cell analysis, the delay cells of both topologies is compared to choose the best option for the multichannel, low-power TDC chip. Additionally, the performance improvement is estimated for further scaled technologies.

The first thing, that draws attention is the output swing of the cell. Due to the topology of the Maneatis cell, the output voltage cannot go lower than the value of the control voltage, which severely limits the swing (Fig. 3.23 (b)). In this category, the winner is the Lee-Kim DE regardless of technology.

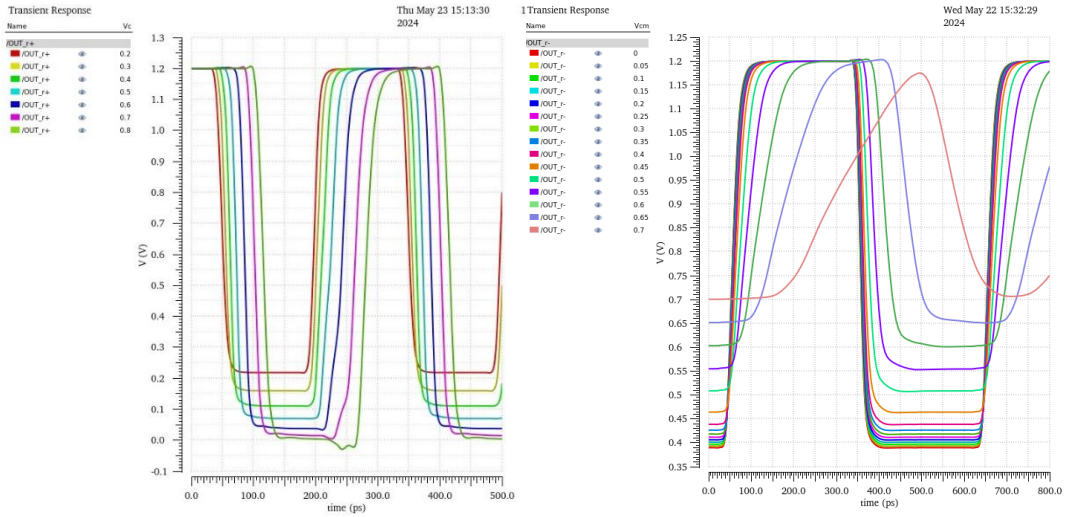


Figure 3.23 Output voltage waveforms at different control voltages: a) Lee-Kim cell; b) Maneatis cell

Next, let's compare the minimal possible delays in a delay line without parasitics, where each cell is additionally loaded with distribution buffers (Table 1).

Table 1 Minimum achievable delays of different cells

	Lee-Kim (UMC180)	Maneatis (UMC180)	Lee-Kim (TSMC65)	Maneatis (TSMC65)
$td_{min,}$ ps	24.2	32	6	9.2
P, mW	2	1.2	0.53	0.35

However, power consumption is crucial for the planned application of the chip, so we have to consider the optimum of the delay and power trade-off. Let us compare different characteristics of the cells for the optimum sizing of the cell (Table 2) as it was mentioned in the respective sections, so it would be possible to decide the final topology for the delay line.

Table 2 Delay cells' characteristic, parameters except tuning range are given for V_c=0.3V for Lee-Kim and V_C=0.5V for Maneatis cell

	UMC180		TSMC65	
	Lee-Kim	Maneatis	Lee-Kim	Maneatis
td, ps	28.1	36.3	8.1	10.6
P, uW	624	466	138	114
$\frac{\Delta td}{\Delta V_{DD}}$, %/%	2.4	3.26	4.6	6.55
σ(td) due to mismatch, fs	156	294	153	342
jitter (DE output), fs	24	29	38	43
jitter (FF input, with event arriving), fs	117	151	527	582
jitter (FF input, no event), fs	52.5	76	108.1	133
control range, V	0…0.9+	0.5…0.9	0…1	0.35…0.7
tuning range, ps	28…65+	34…64	7…32	10…55
$\frac{dt_d/dV_c}{dt_d/dV_{DD}}$	6.09	6.34	6.71	18.51
16-stage VCRO tuning range, GHz	1.1…0.5	0.9…0.5	4.5…1	3.1…0.6

Based on the generally better performance of the Lee-Kim in comparison to the Maneatis cell, it was decided to proceed to the improvement of the former and further incorporation of it into the final multichannel TDC.

4 Lee-Kim improvement

4.1 Fine-tuning

As the initial chosen architecture for the TDC was based on the ADPLL, with timing generation by a delay line in a 16-stage VCRO setup, precise tuning in order to achieve the lock is essential. With the current configuration of the cell (in case, when we add parasitic capacitances to mimic post-layout degradation) gain of the VCRO at the linear part of the characteristic is approximately K_{VCRO} = 4 GHz/V, which is rather high, and would require a very fine DAC. The goal for the gain is in the order of hundreds of MHz/V, so it would make possible control of the delay cells by two (for coarse and fine tuning) DACs, that needn't have a very high resolution.

We have considered two options for incorporating fine-tuning:

- adjusting the current, flowing through the positive feedback latch (Fig. 4.1(a));
- adding a second controllable pair of PMOS (Fig. 4.1(b)).

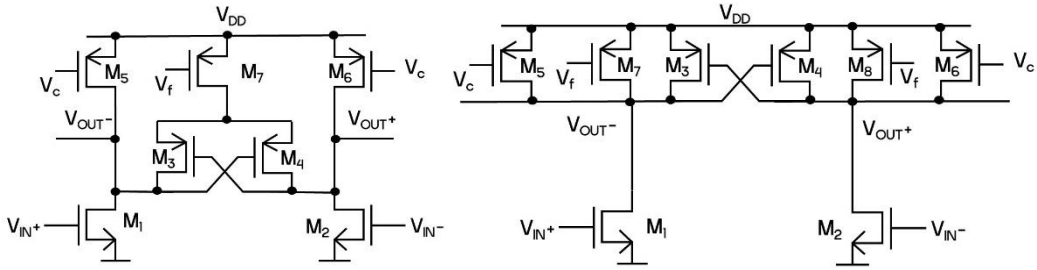
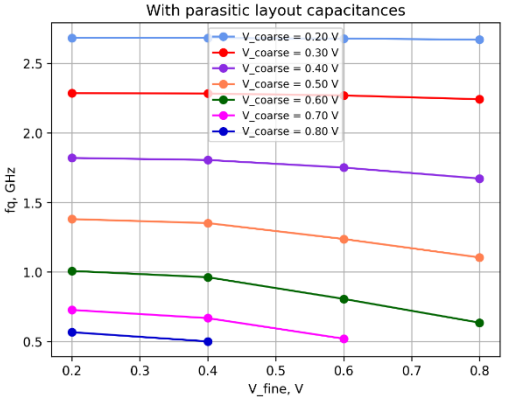


Figure 4.1 Fine-tuning via a) adjusting the current, flowing through the positive feedback latch; b) adding a second controllable pair of PMOS

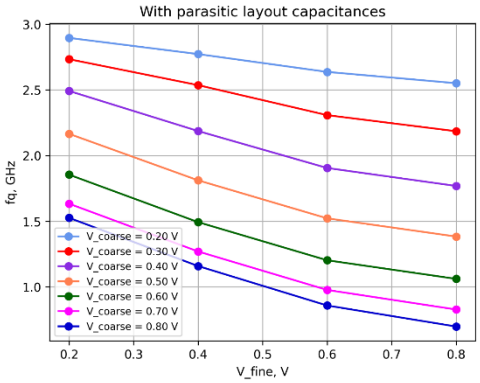
Let's analyse the first case directly translating the delay of the cell into the 16-stage VCO frequency (Fig. 4.2 (a)), here the width of the fine-tuning PMOS is 240 nm. We can see, that fine-tuning in this case is way too fine, additionally, the fine gain of the oscillator is highly non-uniform (Fig. 4.2(b)), this way we would require a rather high resolution of approximately 8-bit for course tuning for the effective control in the region of low coarse control voltage.



V_{coarse}, V	Δf, MHz	Δtd, ps	K_{fine}, MHz/V
0,2	10,65	0,05	17,75
0,3	44,76	0,27	74,60
0,4	148	1,52	246,67
0,5	275	5,65	459,67
0,6	372	18,15	620,17
0,7	206,8	17,07	517

Figure 4.2 a) Fine-tuning (adjusting the current through the latch) characteristic of the oscillator; b) fine gain of the VCRO

The next option is to add a second control pair, here the fine control devices are LVT (as the rest of the schematics), the width and the length are 120 nm to reduce the sensitivity of the device as well as the additional power consumption. This time the sensitivity of the fine control devices is slightly too high (Fig. 4.3) as opposed to the previous option. To reduce this excessive sensitivity, it was decided to switch the fine-control devices to standard (SVT) and high (HVT) threshold voltage device. Both width and length are minimally sized (120 nm and 65 nm respectively). The tuning characteristics for both cases are compared in Fig. 4.4. Both configurations can be controlled with 4-bit control voltage.



V_{coarse}, V	Δf, MHz	Δtd, ps	K_{fine}, MHz/V
0,2	343,3	1,45	572,17
0,3	548,8	2,87	914,67
0,4	723,6	5,13	1206
0,5	782,2	8,16	1303,67
0,6	792,9	12,6	1321,5
0,7	805,7	18,6	1342,83
0,8	827,9	24,3	1379,83

Figure 4.3 a) Fine-tuning (additional control pair, LVT) characteristic of the oscillator; b) fine gain of the VCRO

To decide the best option, the influence of process and temperature variation on the fine gain of the oscillator is checked (Fig. 4.5). The configuration with HVT control PMOS is much more robust to temperature variations and slightly more robust to process variations.

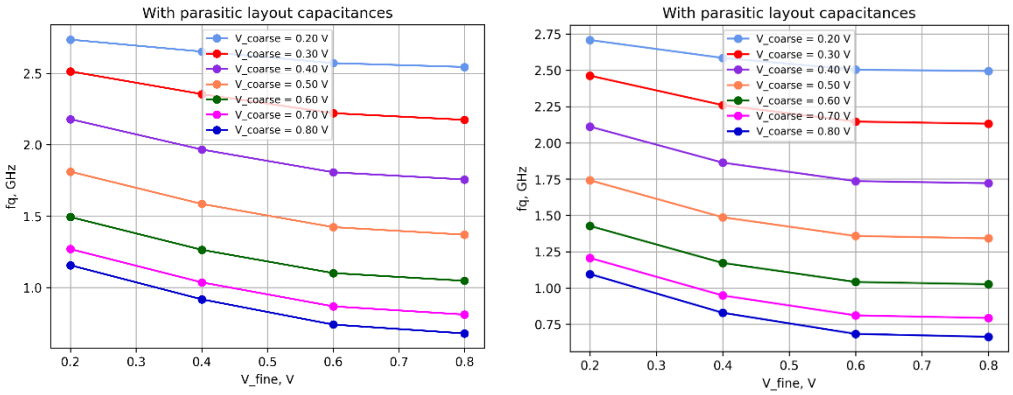


Figure 4.4 Fine-tuning (additional control pair) characteristic of the oscillator: a) SVT control devices; b) HVT control devices

However, the downside of introducing SVT and HVT devices into the design is the possible increase in the delay in the post-layout simulation, because devices with different threshold voltages have different doping levels and cannot be placed very close due to design rules restrictions, thus degrading the delay.

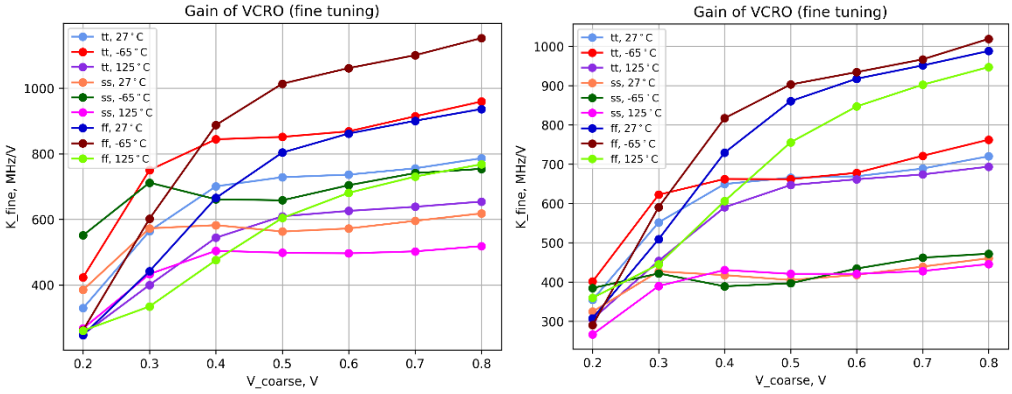


Figure 4.5 Fine gain of the VCO with additional control pair: a) VT devices; b) HVT devices

4.2 Local passive interpolation

Local passive interpolation is an approach to achieve a sub-gate delay resolution [8]. The principle is simple enough: a series of resistors are connected between the input of the differential DE and the respective output, thus forming a voltage divider (Fig. 4.6). The interpolation factor (IF) (the number of times the resolution is improved) is determined by the number of resistors in the divider.

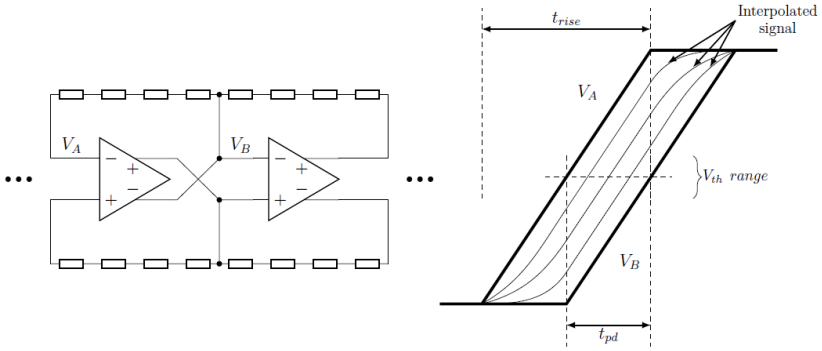


Figure 4.6 Delay cells with local passive interpolation, IF=4 [25]

Theoretically, the divider ratio should depend only on resistors' ratios and not on their absolute value. However, since additional buffers are connected to the interpolation nodes, their capacitive loading together with interpolation resistors form reactive circuits, thus, deviating the circuit's response from the ideal interpolation factor, causing differential non-linearity – DNL. It should be kept small, the typical goal is for DNL to be less, than half an LSB. The main trade-off here is power and non-linearity (Fig. 4.7): large interpolation resistors decrease the transient current, thus reducing

power consumption, but it also worsens the non-linearity of the delay in the interpolation nodes.

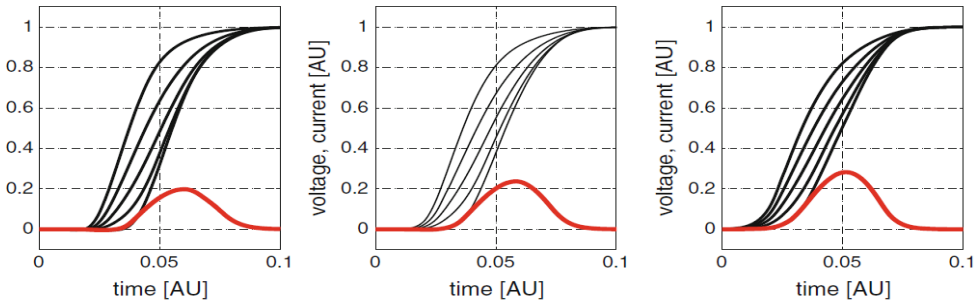


Figure 4.7 Trade-off between ideal interpolation and power consumption: resistors' values decrease from left to right [8]

Additionally, for a given power consumption of the cell, increasing IF degrades the DNL, thus, it has been decided that, as a compromise, an interpolation factor of 4 was chosen.

After careful analysis of the resistors available in the technology, the decision was made to choose polysilicon resistors without silicide. They have shown the best PVT behaviour; the mismatch, which translates into approximately 3% of delay variation; and less parasitic capacitance (as it is manufactured above the oxide layer whose thickness increases the distance between the parasitic capacitor's plates, thus, decreasing its value).

It is important to analyse the speed degradation through post-layout simulation of the delay cells. The designed Lee-Kim cells have W_n = 360 nm, W_{p_cs} = 540 nm and W_{p_fb} = 120 nm as main delay cells and W_n = 240 nm, W_{p_cs} = 360 nm and W_{p_fb} = 120 nm as distributional buffers. The test bench for open-loop simulation is constructed as follows: 5 buffers before and after the delay line, which consists of 16 cells for now. Every DE is loaded with distributional buffers. The interpolation resistors' value was chosen to be 400 Ohm, as it has shown a balance between uniformity of delays along the line (Fig.4.8(a)) and power consumption.

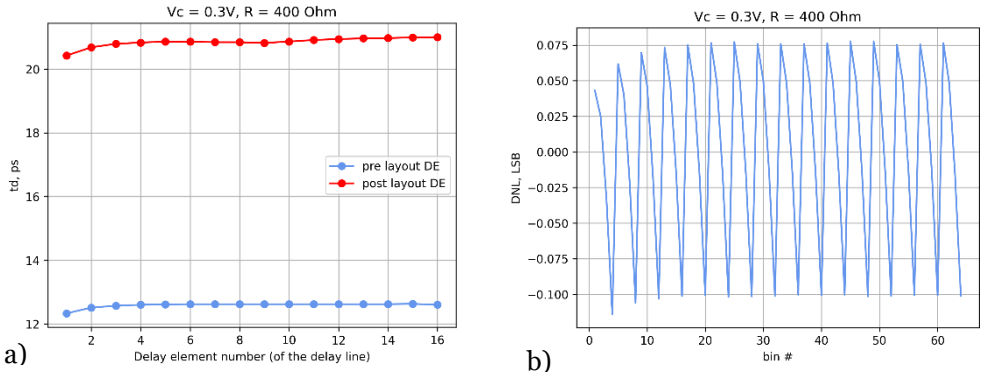


Figure 4.8 a) Cell-to-cell delays along the line; b) DNL in case of all the interpolation resistors being the same (LSB = 5.3 ps)

A repetitive pattern is seen on the DNL. Every 4 bins we have a drop, which can be minimized by tuning the resistors – we have to increase resistance along the interpolation nodes, thus decreasing the delay at the first and increasing at the last. It is best to keep the same length of the resistors (Fig. 4.9 (a)) to facilitate layout design. In this case, we have an improved DNL (Fig. 4.9(c)).

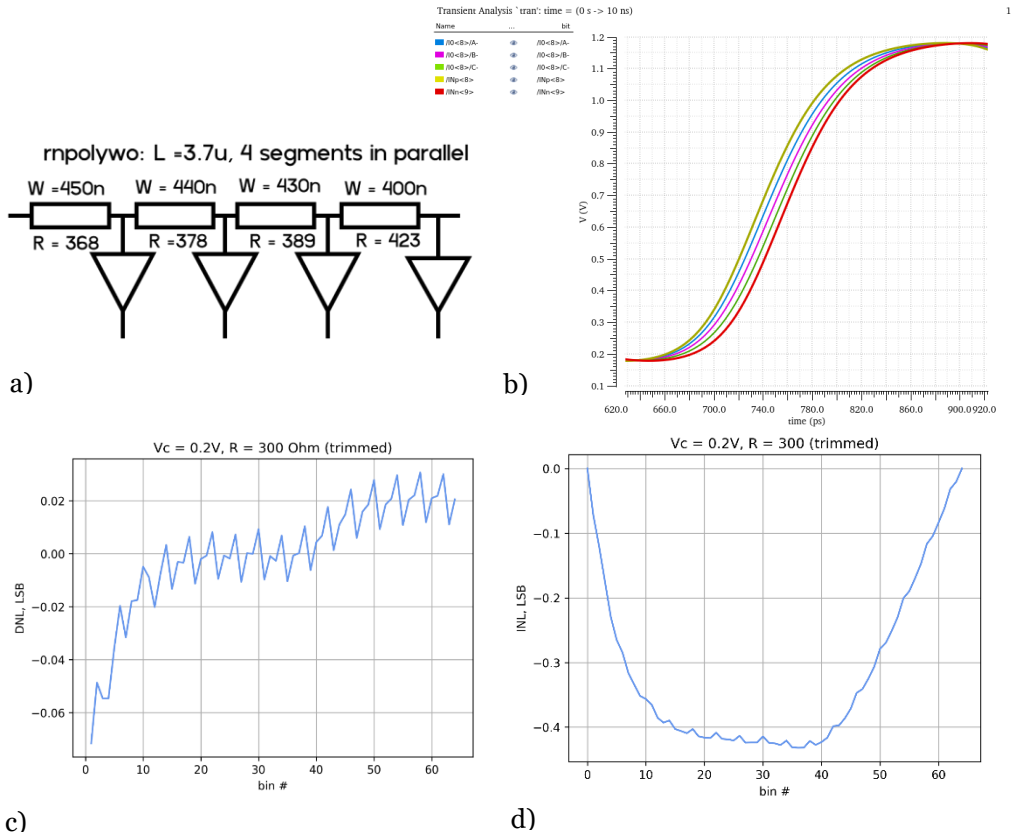


Figure 4.9 a) Resistors' sizing for improved DNL; b) voltage waveforms; c) differential non-linearity (LSB = 4.5 ps), d) integral non-linearity

4.3 Sub-gate delay resolution and fine-tuning

To have a better control of the cell in the PLL we have introduced fine-tuning and the best solution was found to be an additional control pair (with HVT devices), which nevertheless had the disadvantage of potentially increasing the delay. However, when LPI is brought into the design, the coarse gain of the oscillator is reduced from 4 GHz to around 1.7 GHz and the fine gain is reduced respectively. That's why to improve the sensitivity of fine control and with the same stone to kill increased delay – the best option is the use of LVT fine-tuning PMOS. The optimal sizing of this additional pair

was found to be W_{p_fine} = 180 nm, this allows using the coarse control voltage of only 3 bit (Fig. 4.10).

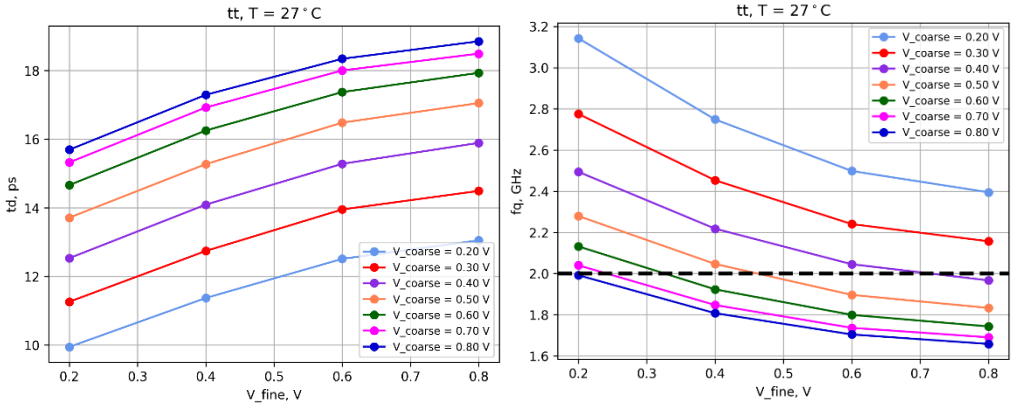


Figure 4.10 a) Tuning range of the delay cell with fine tuning and LPI; b) corresponding tuning range of a 16-stage VCRO

5 Final design of the delay line

At this stage the open-loop architecture with digital calibration, which was discussed in the first chapter, was fully developed. So the final architecture was decided: the open-loop delay line would receive high-speed clock from the ADPLL, the digital calibration of the line would be performed using 4-bit DAC.

5.1 Frequency impact on control range

The central frequency of the previously designed (and characterized) ADPLL is 2.56GHz. Therefore, the delay line needs to handle working at this frequency (which is quite high for this technology), because even though a single cell surrounded by a few buffers can easily work at higher frequencies, degradation of the signal along the line may be critical.

As a result of post-layout simulation, we found that the control range in tt corner at 27°C at this frequency is very limited: the delay line works at a control voltage 0...0.3V (Fig.5.1). However, in the worst corner (ss, 125°C), the delay line is no longer functional.

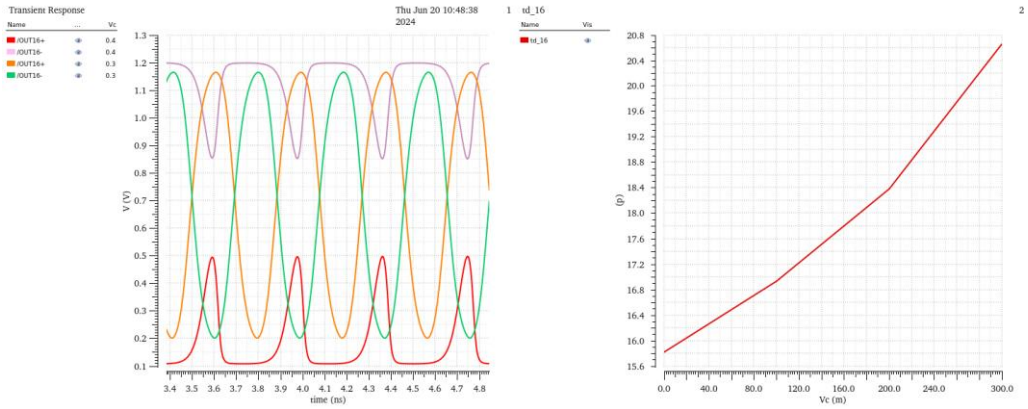


Figure 5.1 a) The output voltage waveforms of the last DE of the delay line at different control voltages (tt, 27°C); b) tuning range of the delay line

The possible options to ensure the correct operation of the line at system level are:

- try to speed-up the cells of the DL (e.g., adjust circuit parameters, add PMOS for inverter-like input to help the rising edge at higher V_c levels, add PMOS feed-forward), which would increase power consumption per cell;
- go for the lowest possible frequency of the PLL (2.32 GHz) to get the delay line working reasonably well with some tunability even in the worst corner, which will lead to a slightly higher number of cells and consequently higher power consumption;
- use the highest possible frequency of the PLL (2.86 GHz) and frequency divider by two, resulting in much more margin for control, but much more delay cells are needed to cover the period of the clock;
- redesign the PLL to work at 2 GHz, which involves additional time spent for redesigning and, as previously noted, a larger number of delay cells will result in higher power consumption.

Firstly, let's try and simulate the control and tuning ranges of the delay cells of the line at different suggested frequencies (Table 3). It is unlikely for modern technology manufacturing to end up in the slow corner, the worst case could be closer to the typical corner at a higher temperature.

It was noticed, that the power consumption doesn't scale up with frequency linearly: when the frequency is increased from 2 GHz to 2.6 GHz (by 30%) the total power consumption increases by 5.8% (from 155.6uW to 162.5uW) for post-layout and by 2.8% for pre-layout (from 138.8uW to 142.7uW). That means, that switching power is only around 19% and 9% of total power for post and pre-layout respectively, the rest being short-circuit power, this was confirmed by estimation of the total capacitance seen at the output node of a delay cell and that way calculating the dynamic power.

Table 3 Frequency and control range of the delay line

f [GHz]	ss, 125°C		tt, 125°C		tt, 27°C	
	V_c [V] (range)	$t_{d,mean}$ [ps] (range)	V_c [V] (range)	$t_{d,mean}$ [ps] (range)	V_c [V] (range)	$t_{d,mean}$ [ps] (range)
2.6	0	17.2	0…0.25	14.9…20.7	0…0.3	14.9…20.4
2.44	0.1…0.15	20.1…21.5	0…0.3	15.2…21.6	0…0.4	15.0…23.1
2.32	0…0.25	17.9…24.95	0…0.35	15.44…23.47	0…0.4	15.07…24.18
2.0	0…0.35	18.5…29.53	0…0.45	15.99…27.5	0…0.45	15.28…27.03

Thus, since most of the power consumption of the cell is static, it will be even more beneficial, than thought initially, to target higher frequency. Even though dynamic power will scale up with frequency, the decrease in the number of delay cells due to the period reduction will result in a lower total power consumption. So, for low-power applications, at least, going for 1.43 GHz (divided by two maximum frequency of PLL) is highly undesirable.

The risk assessment showed, that redesigning the PLL is better avoided, unless no better alternative exists. Therefore, we have either to make sure that the current system works with the available control margin or speed up the buffers to increase this margin.

To allow some margin for the PLL, it is advisable not to target the lowest possible frequency (2.32 GHz), but rather set 2.44 GHz as a goal. This way, if the chip would be in the slow corner (which is not very likely) at T = 125°C there is 0.3 V of control range. Another 'emergency' tool to increase this margin and to reduce the delay of the buffers is to tune the supply voltage, by increasing V_{DD} by an allowable 10% (to 1.32V). This way the control range is 0…0.4V and the corresponding cell delay tuning range 15.5…24.5ps.

5.2 Delay cell improvement

As the frequency reduction inevitably entails quite a significant increase in power consumption, improving the design of the delay cells for higher frequency is very well worth trying.

Possible options to decrease the delay of the buffers are given below.

- Since we don't care about gain (in contrary to the VCRO architecture) it is possible to increase the ratio of current starving PMOS to NMOS, but pay for that in terms of power.
- It is possible to increase the width of the input NMOS, pay in power and additional loading (but parasitics of interconnects won't be that significant in comparison).
- It is possible to make an inverter input (Fig. 5.2(a)) which would help with the rising edge, but also increase loading and power.
- It is possible to add a PMOS feed-forward (Fig. 5.2(b)), the diagram of 1-stage feed-forward is given on Fig. 5.3. This would help with the rising edge, especially at higher levels of control voltage, but also increase loading and power.

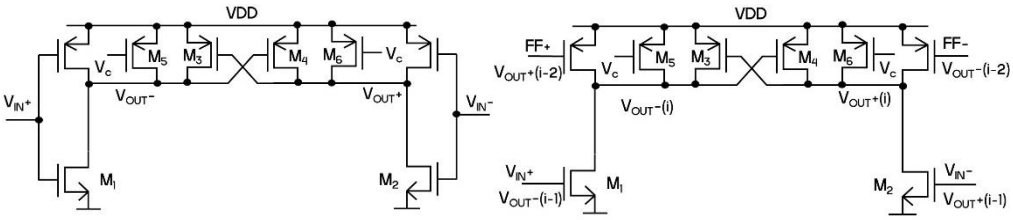


Figure 5.2 a) Lee-Kim cell with inverter-input; b) Lee-Kim cell with PMOS feed-forward

The first two options proved to be ineffective for enhancing the control range. Even though they indeed reduce the delay at low control voltages, the tuning characteristic of the cell becomes steeper and therefore the critical point for the DL delay is reached sooner, ending up with even more limited control range.

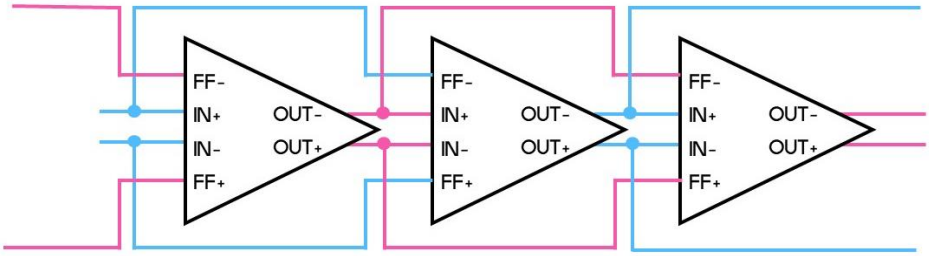


Figure 5.3 A diagram of 1-stage feed-forward

Adding an inverter input allowed to widen the control range to 1 V in tt (27°C), however in the slow corner it showed no improvement compared to the classic Lee-Kim cell. Adding a feed-forward PMOS improved the control range quite significantly, while almost not degrading minimal possible delay of the cell (Fig. 5.4). For the normal Lee-Kim cell the pre-layout control range at 2.6 GHz is V_c = 0…0.4 V and the corresponding tuning range for the delay, t_d, is 10…18 ps, while for the new pre-layout cell it is imporved to V_c = 0…1 V and t_d, is 10…19.

However, due to the additional PMOS and interconnects, associated with the feed-forward, the post-layout degradation was worse than in the case of normal Lee-Kim cell (which has a post-layout 2 times increase in delay), leading to inferior performance:

even with 2-stage feed-forwarding the delay line was not functional in the worst corner (ss, 125°C), though in the typical corner, the control range was improved.

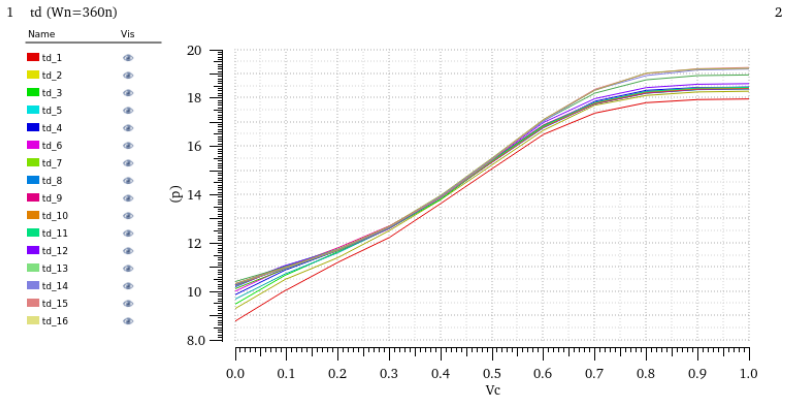


Figure 5.4 Tuning characteristic of Lee-Kim cell with added 1-stage feed-forward PMOS, no parasitics (f=2.6GHz; tt, 125°C)

Another possibility to upgrade the circuit is to try NMOS feed-forward (Fig. 5.5 (a)). While incorporating PMOS feed-forward aimed at addressing the rising edge and decreasing the delay at higher levels of the control voltage, using NMOS feed-forward will help speeding-up the buffers at lower control voltage.

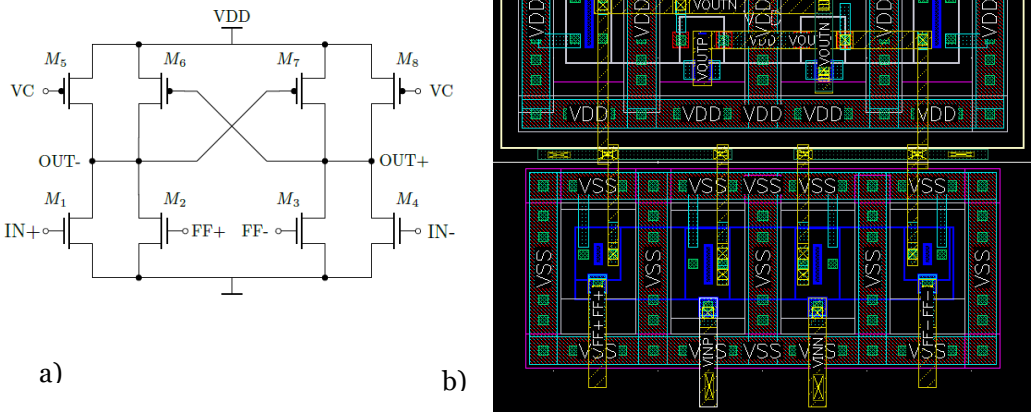


Figure 5.5 Lee-Kim cell with NMOS feed-forward: a) schematic, b) layout

Using a 180 nm wide feed-forwarding device with a 2-stage feed-forward helped to reduce the minimal achievable delay by a factor of two. The post-layout simulations also show significantly reduced delay and much better performance in the worst corner (Fig.5.6). To improve the robustness of the cell to radiation effects it was decided to add guard rings around NMOS and PMOS devices to avoid latch-ups (Fig. 5.5(b)). The possibility of using enclosed layout transistors against TID effects has been considered, however, dismissed due to significantly increased power consumption because of much larger device sizes in this case.

Let's compare the performance of the new cell with NMOS 2-stage feed-forward and normal Lee-Kim cell (Table 4).

Table 4 Performance of the delay line, f=2.44GHz

	2-stage NMOS feed-forward	Classic Lee-Kim
tt, 27°C : td_{min}, ps	10	15
tt, 27°C : control range, V	0…0.5	0…0.4
tt, 27°C : P_{av}, uW (per cell, Vc=0.3V)	149.5	161
tt, 125°C : td_{min}, ps	10.8	15.59
tt, 125°C : control range, V	0…0.5	0…0.3
ss, 125°C : td_{min}, ps	12.8	20
ss, 125°C : control range, V	0…0.4	0.1…0.15
ss, 125°C, VDD=1.32: td_{min}, ps	x	15.5
ss, 125°C, VDD=1.32: control range, V	x	0…0.4

The new cell exhibits superior performance regarding all characteristics, including power consumption, which strikes as a bit counterintuitive, since the added feed-forward should add to the leakage of the cell, due to earlier activation. However, since this frequency is quite challenging for these buffers, the cells end up working mostly on edges, never having time to settle. That's why almost all the time there is a direct path for the short-circuit current, because the transistors don't turn off completely, as the stable voltage level (high or low) can't be maintained even for a short time. And in the case of utilizing an NMOS feed-forward the cell works much faster and has some time to settle, so it doesn't spend as much time on edges, as before, allowing the current, drawn from the V_{DD} pin, to go down.

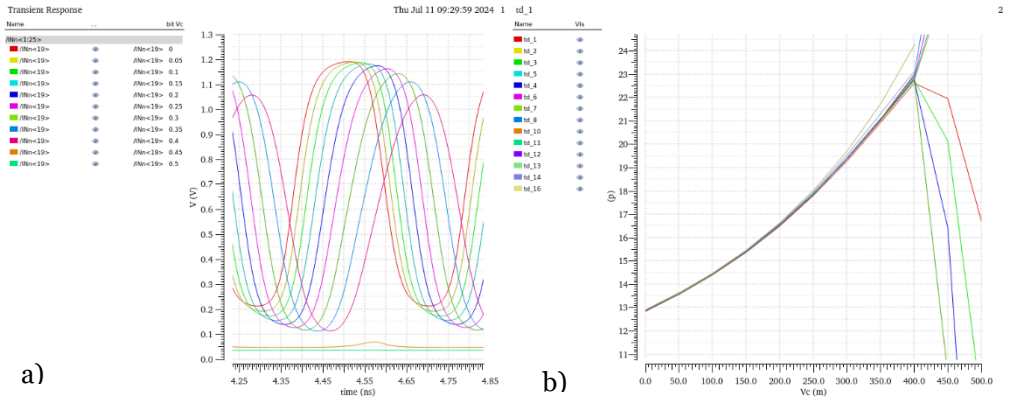


Figure 5.6 a) Output voltages of the delay line (DE: NMOS 2-stage feed-forward) at different control voltages, b) tuning characteristic of the delay line (ss, 125°C)

The new topology of the cell allows even to improve the goal for the resolution after resistive interpolation (5 ps), in the middle of the tuning range (V_c = 0.25V for tt corner at 27°C). The minimum cell-to-cell delay is 13.4ps (achievable in all the corners), which yields a fine resolution of 3.35 ps. However, that also means, that more delay cells are

needed to cover the period of the reference clock with a given fine resolution (N = T_{CLK_REF}/T_{LSB} = 410ps/3.5ps/4 = 30 cells).

We perform a Monte-Carlo simulation on the new cell to estimate the possible effect of local mismatch on the characteristic of the delay line. Using the information obtained in the mismatch analysis, we can plot the DNL/INL and transfer characteristics of the delay line (Fig. 5.7).

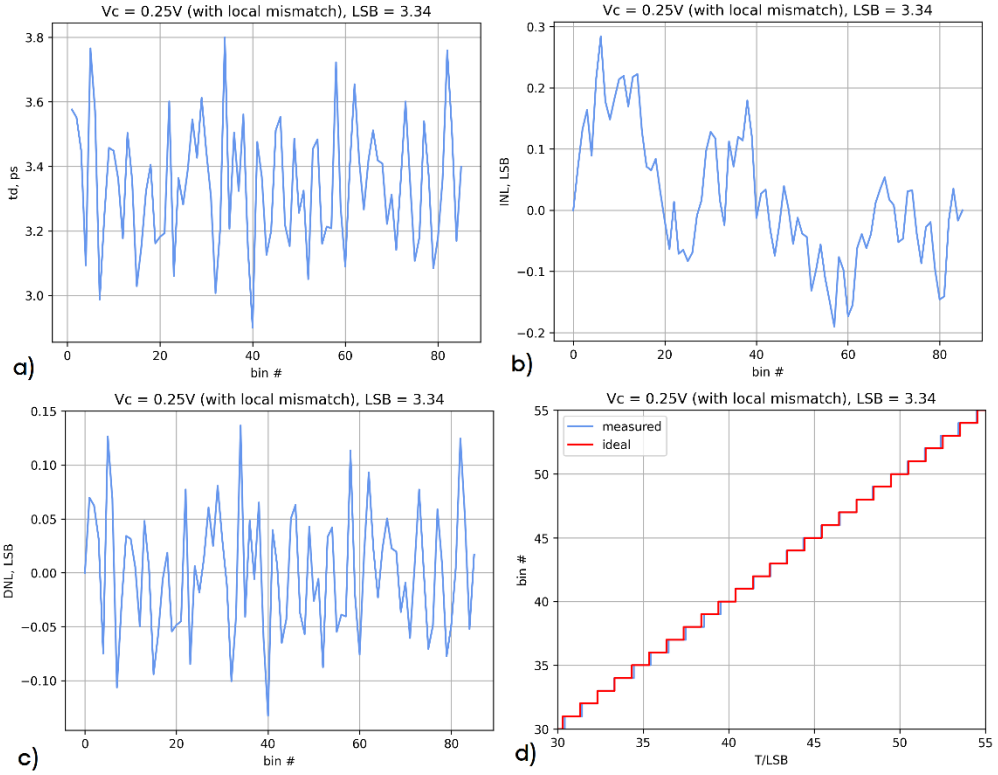


Figure 5.7 a) Delays seen at the interpolation nodes of the delay line (DE: 2-stage NMOS FF); (b) INL and (c) DNL characteristics; d) zoomed-in transfer characteristic of the delay line

5.3 Jitter of the cell

It is interesting to analyse the jitter of the improved cell from a theoretical point. To do that, we need to perform a noise analysis first. The noise contributions of a MOSFET can be modelled as an ideal, noiseless transistor and parallel to its channel – a noise

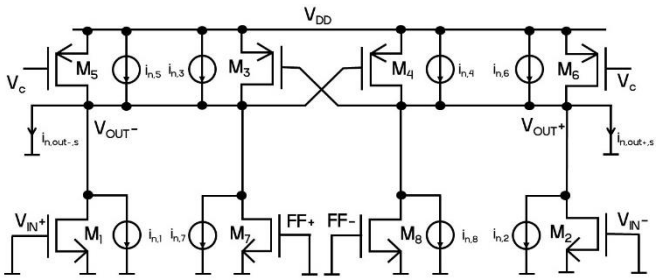


Figure 5.8 Lee Kim cell with added feed-forward NMOS, noise sources depicted

current source [30], thus the noise contributions of the cell can be represented as shown on Figure 5.8.

The easiest way to find the output noise voltage Power-Spectral Density (PSD) for the circuit is via output noise current, which in our case is the sum of all the noise current PSD contributions of the transistors, that consist of thermal and flicker noise. This way, we will look at the noise current as a Norton current source with a capacitive load. This current is integrated during the time from the start of the signal rising till the crossing point to a noise charge, which in turn causes the output noise voltage, that is translated to jitter through the slope of the signal [29]:

$$\sigma_{\text{jitter}} = \frac{V_{n,diff}}{\frac{dV_{out}}{dt}}, \tag{15}$$

here (dV_{out}/dt) is the slope of the differential output voltage of the cell at the zero-crossing point.

To simplify our calculation of jitter, we will only consider the thermal noise of MOSFETs and assume no positive feedback for calculating the output resistance. This way the output noise variance can be found as:

$$\overline{V_{n,out,tot}^2} = \frac{\overline{i_{n,out}^2} \cdot R_{out}^2}{4R_{out}C} = \frac{kT}{C}\gamma\left(\sum_i g_{m,i}\right)R_{out} = \frac{kT}{C}\gamma\frac{\sum_i g_{m,i}}{G_{out}} = \frac{kT}{C}\gamma\frac{\sum_i g_{m,i}}{\sum_i g_{ds,i}}, \tag{16}$$

here $k = 1.38\times10^{-23}$ [J/K] is the Boltzmann constant, T [K] is the absolute temperature, γ is the coefficient, which is equal to approximately 2/3 for long channel device and has to be replaced by a larger value for submicron devices.

Thus, to find the timing jitter of the differential output of the cell, we need to double the value of the noise voltage PSD found for a single output and divide by the slope of the differential signal, using formula (15). To calculate the jitter, we find the operating points of the transistors, total capacitance seen at the output node and the slope of the differential output voltage of the cell from the simulation, and obtain 82.4 fs of jitter.

In order to validate the results of our calculations, we run a full jitter analysis, as we've done for previous versions of the delay cells. Post-layout simulation of the cell shows that jitter seen between input and output of the delay cell is 62.7 fs (at 2.44 GHz and coarse delay of 15 ps). This result is relatively close to our calculated value, with the discrepancy attributed to simplifications in the calculation. For instance, the effect of the positive feedback would increase the output noise voltage but also increase the slew rate which could account for the difference. Additionally, even when considering only thermal noise, the calculation overestimates jitter due to the assumption that the noise voltage results from an infinite integration of the noise current. In reality, however, many noise sources only become active during signal transitions, and their impact is still slight at the beginning of the slope.

If we compare the new improved feed-forward Lee-Kim cell and its jitter performance with the classic one, we can say, that the additional feed-forward speeds-up the cell, increasing the slew rate and thus decreasing jitter, but the feed-forward device also contributes to the total noise seen at the output. Therefore, these two effects counteract and partially cancel out.

If we compare the pre-layout simulation results with the normal Lee-Kim cell of the same sizing, we can see, that the increased slew rate does indeed almost completely cancel out additional noise from the feed-forward device: 35 fs of jitter in case of normal Lee-Kim and 37 fs in case of the new improved cell.

We can estimate the total jitter of the delay line (seen between the input of the first DE to the output of the last one in the line), using the formula [29]:

$$\sigma_{\text{jitter,tot}} = \sqrt{N}\sigma_{\text{jitter,single}}, \tag{19}$$

where N is the number of stages. Thus, for our 28-stage delay line, the estimated post-layout jitter is approximately 330 fs.

5.4 Supply sensitivity improvement

An important parameter of a delay line is its supply sensitivity. In the current architecture, the control voltage for the delay cells is generated by the DAC, which is implemented as a 4-bit R-2R ladder (Fig. 5.9(a)).

With the increase of supply voltage – the delay of the cells is reduced, but if the same supply is used for the DAC, then the control voltage will also increase with V_{DD} (however, not that significantly), thus increasing the delay. Therefore, these two effects counteract each other to some extent. With this kind of DAC control, the supply sensitivity of a single cell is 20 ps/V, which corresponds to 560 ps/V variation of total delay along the line, consisting of 28 stages. This way, to keep the total delay less than 1 ps, a supply variation less than 1.8 mV can be tolerated.

The idea to decrease the cell's sensitivity is to amplify supply fluctuations, thus creating a "virtual supply" used by the DAC. For this an op-amp in a differential amplifier setup and a stable reference voltage V_{ref} = 0.6V is required (Fig. 5.10), since we only need half of supply voltage to effectively control the delay cells. This way by finding the correct

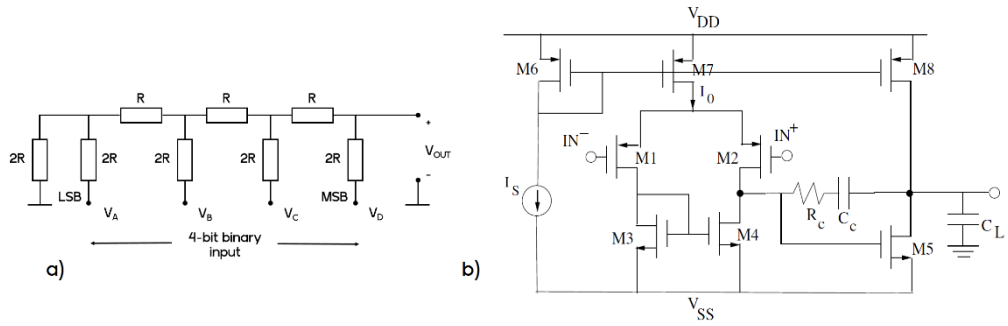


Figure 5.9 a) Diagram of R-2R 4-bit DAC, b) diagram of two-stage Miller op-amp [31]

value of amplification, the variation of the delay caused by supply variation and control voltage change cancel out and, make the cell immune to (low-frequency) supply fluctuations. Local supply decoupling (for every individual cell) should limit the high-frequency supply noise.

This way, the designed op-amp doesn't have to be exceptionally fast as we don't aim to compensate for instantaneous peaks in the supply. The chosen architecture is a two-stage Miller op-amp (Fig. 5.9(b)) with PMOS input pair for better 1/f noise performance, designed for an open loop gain of 60 dB and a bandwidth of 343 MHz.

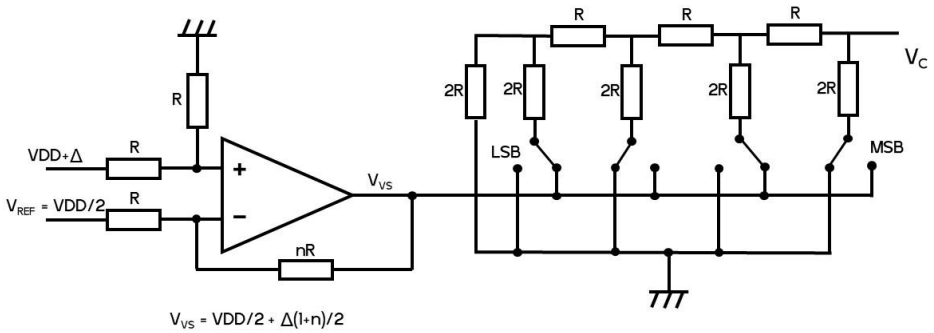


Figure 5.10 Supply fluctuation amplification circuit: V_{VS} here is virtual supply, fed to the DAC; V_C is the control voltage for the delay cells, DAC output

Implementing this fluctuation gain for the active DAC control allows to significantly reduce the cells' sensitivity to supply variation (Fig. 5.11). This way, with a gain of 2.65, it is possible to achieve 78 ps of delay variation (V_{DD}=1.14V...1.26V), thus the sensitivity of a single cell is 0.65 ps/V, which translates to 18.2 ps/V for a total delay change for a 28 stage delay line. In order to keep the total delay variation below 1 ps, a supply

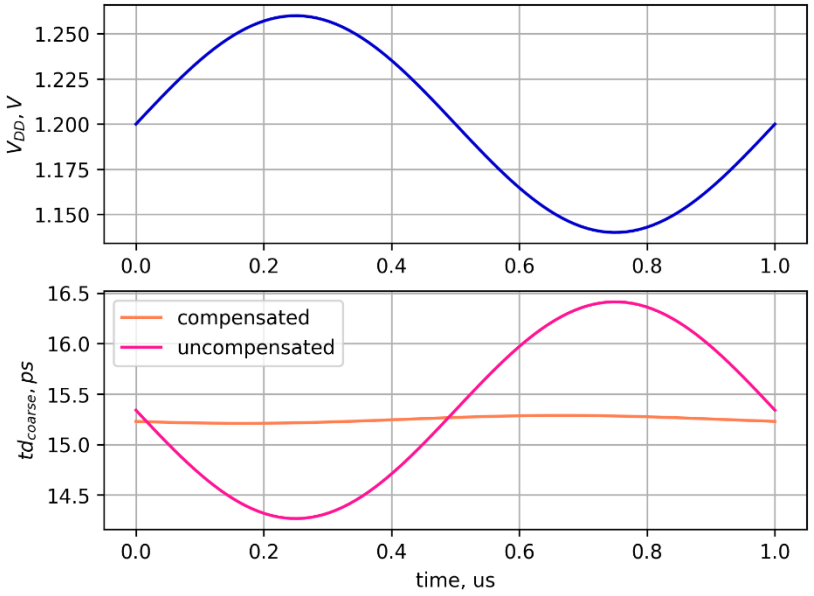


Figure 5.11 Delay variation with VDD fluctuations, for compensated case amplification factor of 2.65 is used

variation of less than 55 mV can be tolerated, which shows great improvement in comparison to the system without active DAC control.

5.4 Design of distributional buffers

For the initial simulations of the delay line, similar Lee-Kim delay cells were used but with smaller size. However, their usage as distributional buffers have a number of shortcomings such as comparatively high power consumption (>100 μW at 2.44GHz) due to the inherently high short-circuit power, lack of rail-to-rail swing and low possible capacitive load (Fig.5.12). The two last facts are crucial for the digital part of the multi-channel TDC design, which is connected to the output of the distributional buffers.

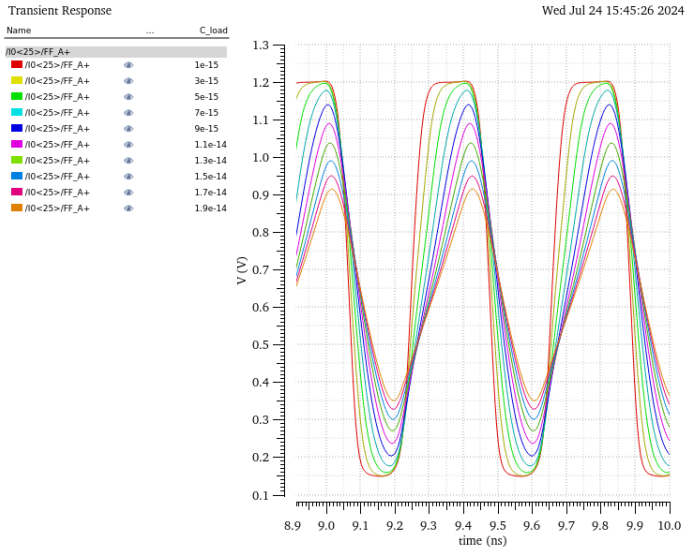


Figure 5.12 Effect of the value of capacitive load on the distributional buffer (Lee-Kim cell) output

Several options were considered as alternative for the Lee-Kim cells, such as using single inverter per interpolation node (Fig.5.13(a)), two inverters in cascade (Fig.5.13(b)) and additional latched inverters connected to the differential outputs of the delay cells(Fig.5.13(c)), all of these solutions aim in overcoming the disadvantages of the Lee-Kim cell as buffer.

As a result of simulation of these options, the first and last options were dismissed. Single inverters, though very power efficient (27 μW at 2.44 GHz with 3fF load), do not allow large loads to be connected to their outputs, if they are small. Otherwise, delay degradation due to additional loading becomes inacceptable. Latched inverters consume quite significant power (121 μW) for the same frequency and load, but show only limited improvement in comparison to the distributional buffers in the configuration of two inverters in cascade.

Therefore, the latter was chosen for the final design of the delay line: with the smallest inverter of the foundry library connected to the interpolation nodes, followed by a 4-times bigger one, since a fan-out 4 shows minimal delay in driving a large load. The

power consumption of this configuration is 66 μW at 2.44 GHz with a copy of the larger inverter as a load. The impact of the connected load on the output voltage waveforms is shown in Fig.5.14(a). However, as the further digital parts of design will only use one of the two differential phases, the larger inverter on one phase can be removed to save some power: resulting power consumption of such configuration is 35.85 μW at the same frequency and with the same load.

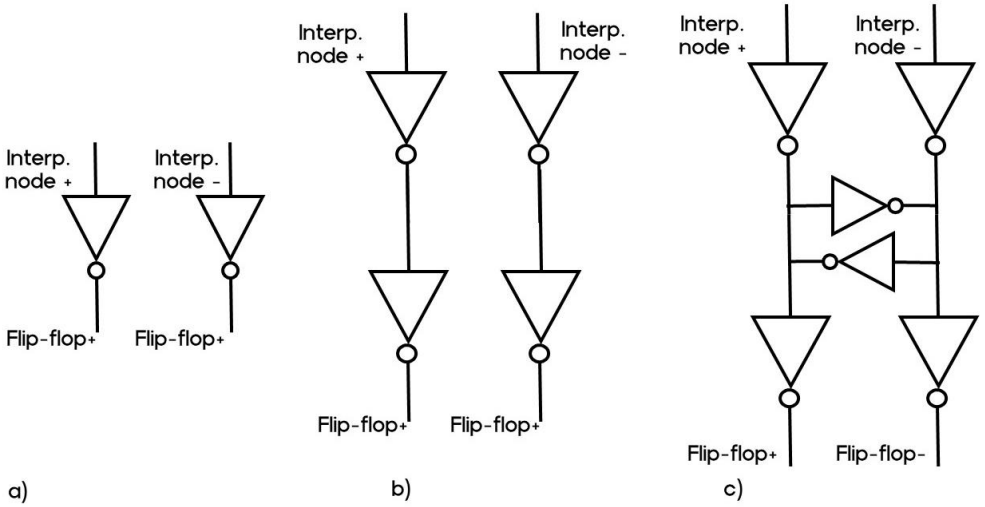


Figure 5.13 Possible option for distributional buffers: a) single inverters, b) series of inverters, c) inverters followed by latched inverters

Due to a slightly increased loading on the main delay cells, the minimum achievable delay is increased, but 15 ps of coarse resolution is still achievable in all PVT corners (Fig.5.14(b)), the main impact here being from the process and temperature, as supply voltage impacts are almost eliminated by the active DAC control.

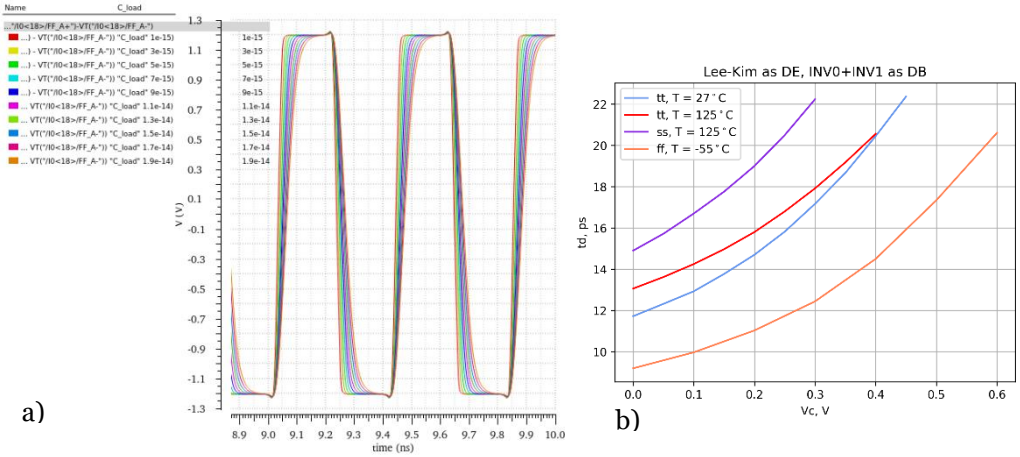


Figure 5.14 a) Distributional buffers' output voltage waveforms with different values of connected load, b) tuning range of the coarse delay of the cells in different process corners

A concern regarding using inverters as distributional buffer was the fact, that they are specifically designed to have a threshold voltage of $V_{DD}/2$, while Lee-Kim is not, which would result in a duty cycle offset. The threshold voltage of the inverters can easily be

changed by a slight redesign. However, the threshold voltage of the Lee-Kim delay cell is highly dependent on the control voltage and process corner (it varies from 770 mV to 450 mV). That's why tuning the inverter to match the threshold voltage of the Lee-Kim in the specific corner at a certain control voltage will bring even further mismatch, if the chip batch ends up in a different corner. Additionally, since the different channels of the TDC will always trigger on the same edge, duty cycle variations should not degrade the performance.

Jitter, seen at the consecutive distributional buffer outputs, is 78 fs. Thus, it has indeed been improved by a proper design of distributional buffers, as it was mentioned earlier, for the jitter seen at the output of a small-sized Lee-Kim cell used as distributional buffer was approximately 110fs.

6 Conclusions and future work

In this work, a comprehensive overview of various TDC architectures, including fundamental and more advanced, is given. A brief summary of ionising radiation effects on MOSFET and possible ways for mitigation is presented.

The analytical and simulation-based analysis of Lee-Kim and Maneatis delay cells provided valuable insights into their performance metrics, including power consumption, delay, mismatch, jitter, and supply sensitivity. The former has demonstrated a superior performance and was chosen to be used in the design of the delay line for the TDC. The analysis has been conducted for two technologies: UMC 180 nm and TSMC 65 nm, which allowed to compare and evaluate the improvement due to technology downscaling.

Further improvements for the Lee-Kim delay cell have been suggested aimed at achieving sub-gate delay resolution using local passive interpolation and feed-forwarding techniques, which resulted in 3.75 ps resolution with a power consumption of 150 μW per cell. This resolution has been verified to be achievable in all process corners. Additionally, a design solution for coarse-fine tuning has been suggested, though not incorporated in the final design due to the system level changes, that eliminated the need for fine-tuning. An innovative active DAC control method has been presented which allows to effectively increase the delay cell's immunity to supply variations, ensuring robust operation.

For future work, the next research is lined-up:

- Experimental validation: after finishing the design of the whole TDC system, it's tape-out and testing is planned to validate the simulation results
- Radiation testing: to ensure correct operation in harsh environments radiation testing is needed to validate that measures taken for radiation hardening of the TDC have been sufficient
- Advanced technology nodes: to achieve higher operating speeds (and thus improved resolution) and lower power consumption in line with higher TID robustness, explore the design in more advanced technology nodes, such as 28 nm FDSOI or 12 nm FinFETs

This future research can further upgrade the performance of TDC: its resolution, power consumption, robustness, etc., thus allowing to broaden the field of application.

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