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# AFM-sMIM Characterization of the Recombination-Enhancing Buffer Layer for Bipolar Degradation Free SiC MOSFETs

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Due to the expansion of defects like single Shockley-type Stacking Faults inside the SiC epitaxial drift layer, during high current stress, classical SiC MOSFETs can be victims of the degradation of their electrical characteristics. The introduction of an epitaxial SiC buffer layer between the substrate and the n- drift epilayer, called recombination-enhancing buffer layer, was shown to avoid this degradation. In this paper, TCAD simulations of the electrical behavior of such a commercial SiC MOSFET device with varying buffer layer thickness are studied, indicating only small modifications of the electrical characteristics. These simulations are combined with the characterization of the local electrical properties using an AFM-sMIM technique, allowing to determine the real thickness of the different layers of the device. These measurements highlight an inhomogeneous conductivity in the SiC substrate, being probably compensated by the introduction of the SiC buffer layer.

## Introduction

While SiC devices are in full development and subject to significant process advances, the performance stability and reliability of these devices remain a crucial point. In fact, the electrical characteristics of the SiC MOSFET can degrade during polarization and under high current stress, with impacting forward voltage drop. Called bipolar-degradation, this mechanism leads to an increase of the forward voltage and the degradation of the drift conductivity. This phenomenon is due to the expansion of defects in the epitaxial drift layer, originated in the SiC-substrate [1,2]. First for SiC PIN diodes and afterwards for SiC-MOSFETs, studies demonstrated that this bipolar degradation is related to single Shockley-type Stacking Faults (SSF), expanding in the SiC epitaxial drift layer directly located on top of the substrate [3-5]. Under bipolar polarization, the electron-hole recombination energy leads to the expansion of the SSFs from Base Plane Dislocations (BPD) and can also create Threading Edge Dislocations (TED) in the drift layer [6]. SSFs involve the introduction of new charge traps and affect the local electrical conductivity by shortening the carrier lifetime. In order to control and suppress the SSF expansion from propagated BPD, different strategies are proposed: the use of SiC substrates with low BPD density, the improvement of device process [7], "proton implantation" prior to the device fabrication [8] and the introduction of a buffer layer between the substrate and the n- drift epilayer [9,11]. All the mentioned methods involve supplementary costs during the fabrication and have their individual advantages and disadvantages.

The impact of the introduction of a buffer layer is demonstrated and studied for SiC PIN diodes, and for SiC MOSFETs. This buffer layer is a highly nitrogen-doped 4H-SiC epilayer, limiting the high-density minority carrier injection into BPDs in the substrate and therefore acting as an Auger recombination enhancing layer. It was shown that the thickness and the doping level of this buffer

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layer impacts the transformation of BPD to SSF after forward bias stress. In order to gain some insight on the role of the buffer layer on the electrical characteristics of SiC MOSFETs, in this paper, the model and characterization at the die level of the buffer layer are performed and analyzed. TCAD simulations are used to investigate the macroscopic electrical behavior of the device, while scanning Microwave Impedance Microscopy (sMIM) [12-13] based on Atomic Force Microscopy (AFM) is used to map the local electrical properties of the different layers in the device, and especially the buffer layer. Indeed, the sMIM mode is based on the combination of the AFM capabilities, in terms of high spatial resolution imaging and versatility, and microwave physics. The advantage of this AFM mode, compared to other electrical modes, is that no applied voltage to the tip-sample nano-contact is necessary. Local electrical properties of the semiconductor layers can be obtained from the RF near-field interaction of an incident microwave with the studied material.

## Device and Methods

### Devices under test

The devices under test (DUTs) are classical 4H-SiC planar n-channel 1.2 kV commercial SiC power VD-MOSFET (TO-247 package). Dedicated for renewable energy applications and high voltage DC/DC converters, the device has an on-resistance of 350 mΩ. The permanent nominal current between drain-source is 7.6 A and 20 A for a pulsed drain current. For AFM investigations and to analyze the SiC MOSFET at the die level, a cross-sectional sample preparation was used. The sample preparation has been based on a backside opening, followed by the mechanical grinding of the copper heat spread. The sample cutting axis is located perpendicular of the gate grids, and the preparation ends with a surface polishing of mirror quality.

### TCAD device simulation of the bipolar-degradation-free SiC MOSFET

For the simulations, a Technology Computer-Aided Design (TCAD) tool for device modeling, called ECORCE [14] is used. ECORCE uses a drift-diffusion model coupled with the heat equation for DC or transient analysis. ECORCE Software also allows to take into account both trapping and the kinetics of radiation induced charges. A dynamic mesh generator is used that frees the user of the difficult stage of meshing. The mesh is automatically adjusted to follow the gradient of the different degrees of freedom (potential and carrier density) at each step of modeling.

### scanning Microwave Impedance Microscope (sMIM) measurements

Based on an AFM, the sMIM mode is a microwave mode is an electrical mode where an incident microwave signal travels through an electromagnetically shielded and electrically conductive tip (Fig.1a). The gigahertz microwave signal travels through the tip and interacts with a local volume of the sample material under the tip. By using a tip optimized for an incident frequency around 3 GHz, the sub-surface is probed. For a material with a conductivity $\sigma$ and a permittivity $\varepsilon$, the AFM sMIM tip–sample impedance is a complex impedance, equivalent to a capacitor in parallel with a resistance (Fig. 1b). After a calibration step and amplification and demodulation of the reflected signal, the complex admittance of the tip-sample impedance is recorded by the real (sMIM-R) and imaginary part (sMIM-C) signals. With this technique, electrical surface and buried properties can be probed [12-13].

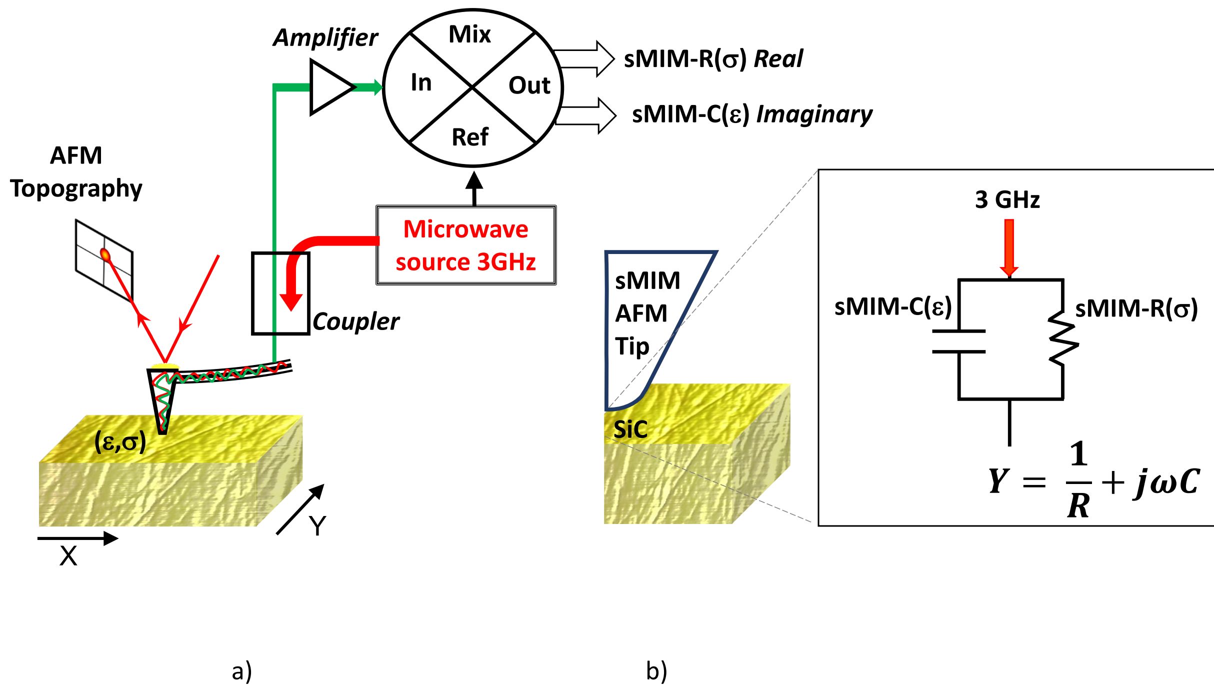


**Fig. 1.** sMIM measurements a) setup based on an AFM, b) equivalent circuit description of the admittance of the tip-sample nano-contact

sMIM measurements are performed using a Bruker Dimension Icon AFM, equipped with a Primenano Scanwave Pro module. The originality of this AFM mode is the use of an electromagnetically shielded and electrically conductive tip. The used conductive and shielded special sMIM probe allows to suppress any parasitic capacitance and enhance microwave sensitivity. The used tip has a radius of 50 nm. A scan rate of 0.3 Hz is employed for a spatial resolution of 512 pixels per line. For these experiments no bias voltage is applied to the sample.

## Results and Analysis

### Simulation of the bipolar-degradation-free SiC MOSFET

The structure of the simulated VD-MOSFET is represented in Fig.2. The doping distributions (p and n type) along the SiC MOSFET are respectively shown in Fig.2a and Fig.2b. The specific additional nitrogen-doped 4H-SiC buffer epilayer is doped at $10^{18}$ n/cm$^3$ whereas the n- drift layer at $10^{16}$ n/cm$^3$. A 50 nm $SiO_2$ layer is localized between the gate and SiC. Three thicknesses of the buffer are considered in comparison of without any buffer: 1,2 and 3 µm.

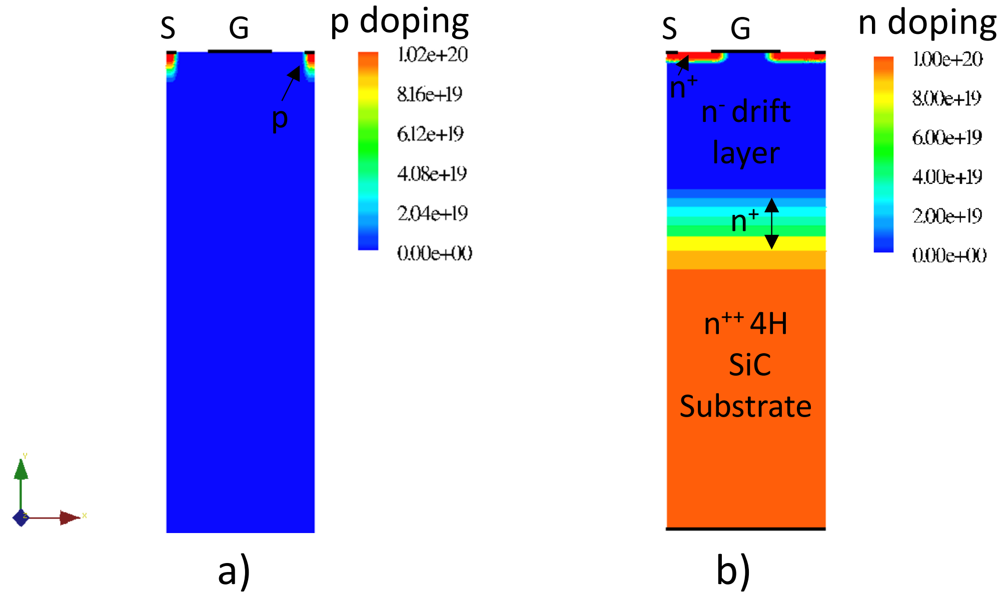


**Fig. 2.** Structure of the SiC MOSFET drawn for the simulation: distribution of the a) p doped and b) n doped regions

From the simulated SiC MOSFET structure, the $I_{DS}$-$V_{DS}$ curves are extracted for the four configurations: without the buffer layer, with a buffer layer with a thickness of 1 µm, 2 µm and 3 µm. Results are drawn in Fig.3. It was observed that the introduction of the buffer layer induces no variation on the forward voltage $V_{th}$ estimated around 6.8V for all curves, but the leakage current is slightly lower ($10^{-12}$ A/µm) with such a buffer layer. For the conduction inside the PIN structure of the MOSFET, a slight modification is observed in the $I_{DS}$-$V_{DS}$ characteristics for low $V_{GS}$. Nevertheless, the thickness of the additional buffer layer does not modify drastically the SiC-MOSFET electrical characteristics.

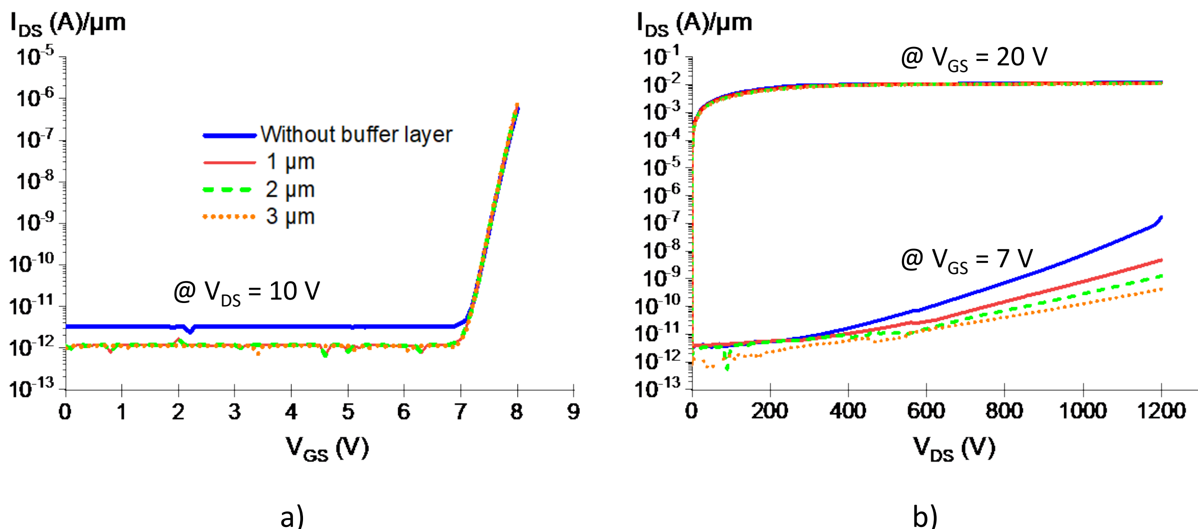


**Fig. 3.** I-V curves from the ECORCE simulation: a) $I_{DS}$-$V_{GS}$ for three thicknesses of the n+ epilayer compared of a structure without buffer layer for $V_{DS}$=10V and c) $I_{DS}$-$V_{DS}$ for three thicknesses of the n+ epilayer compared of a structure without for $V_{GS}$=20V and $V_{GS}$=7V.

**sMIM characterization and analysis of the SiC MOSFET structure**

sMIM results are shown on Fig.4. Four maps are represented: the topography in 2D (a) and 3D view (b), and cartography of the sMIM-R signal (c) and the sMIM-C signal (d). The topography (Fig.4a) allows to distinguish the gate region from the SiC semiconductor layers. At the top of the scanning area the roughness of the sample is due to the mechanical polishing used for the sample preparation, and some nano-scratches are also distinguishable in the SiC semiconductor region. Local electrical properties are acquired simultaneously with the topography by the sMIM signals. sMIM-R and sMIM-C maps reveal details on the internal structure of the device. With both signals, the differently doped layers can be distinguished. Very interestingly, beyond the doped semiconductor layers, the metallic and dielectric materials in the gate regions are also distinguished. Therefore, the sMIM mode allows to analyze the local electrical properties of a large range of materials, independently on their electronic character. Another observation on the sMIM cartographies allows also to underline the accuracy of this AFM mode: the large transversal valley observed in the topography acquisition, probably related to the preparation of the cross section or an inert defect in the device, is barely noticeable on the sMIM-R cartography, and only slightly visible on the sMIM-C one. Therefore, the two signals (topography and electrical) are only sparsely correlated, allowing to interpret the contrast in the electronic cartographies to be only related to variations of the electronic properties, and not induced by topographical differences.

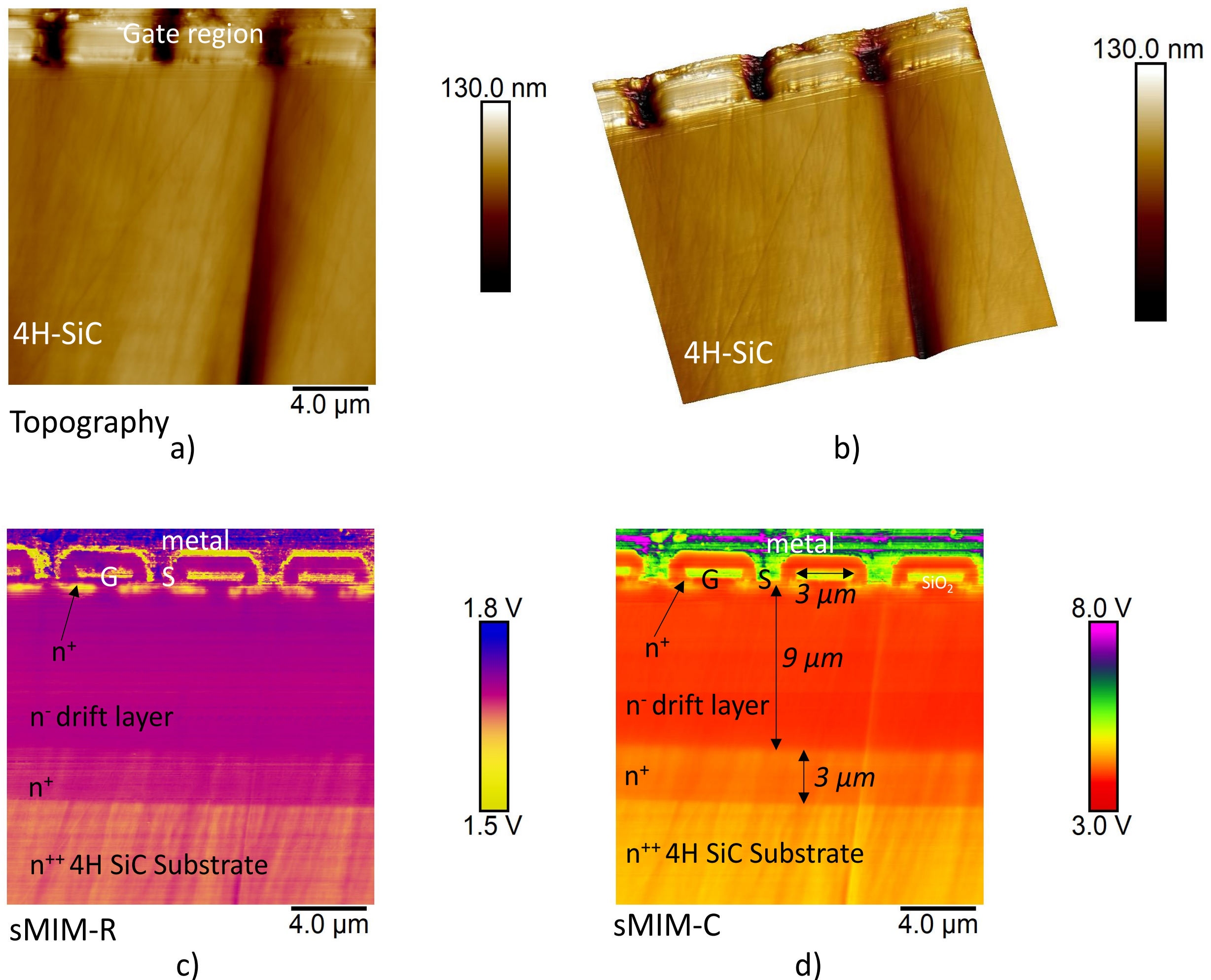


**Fig. 4.** sMIM results a) 2D view of the surface topography of the cross-sectional sample, b) 3D view, c) sMIM-R, d) sMIM-C with the full data scale for the identification of all layers: metal layers, $SiO_2$ and doped SiC (substrate and epitaxial layers)

From the local characterization of the cross-sectional sample of the SiC MOSFET, the effective electrical thickness of the nitrogen-doped 4H-SiC buffer layer is determined to be 3 µm (Fig.4 d)). For further information on the buffer layer, Fig.5 is drawn with a scale bar focused on the properties of the doped SiC layers (the signal of the metals corresponding to sMIM-C > 6 V are saturated in this representation). This representation highlights the doped layers with different carrier concentrations, but even more, inhomogeneities in the n++ substrate can be observed. This contrast is also visible in the sMIM-R cartography, and is therefore, as discussed before, not totally related to a topographical signal. Thus, this inhomogeneity is probably related to defects like SSFs present in the substrate. Finally, the n- drift layer shows much more homogeneous properties, seems to indicate the beneficial effect of the buffer layer on the electronic properties of SiC MOSFETs.

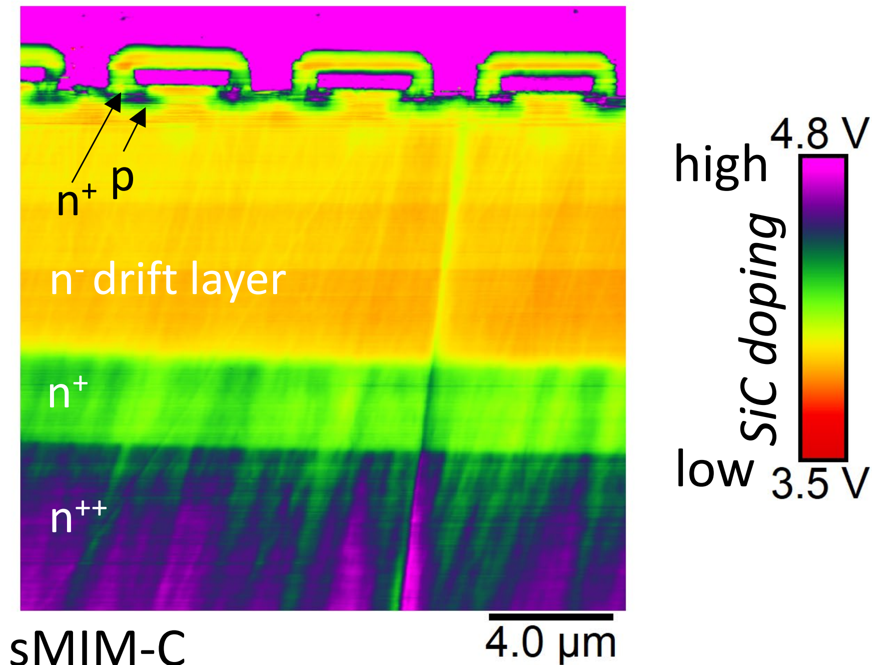


**Fig.5.** sMIM-C with a data scale focused on the doped SiC layers for details inside the $n^{++}$ SiC substrate.

## Conclusion

A modeling and experimental studies of the buffer layer in a SiC MOSFET structure are conducted by using TCAD simulations and AFM-sMIM microscopy. The simulations show the negligible influence of the introduction of the high doped buffer layer on the macroscopic electronic properties, for different buffer layer thicknesses. The local electrical properties obtained by the AFM-sMIM mode of a commercial device with a 3 µm buffer layer have allowed to distinguish the differently doped layers SiC layers of the device, but also to highlight an inhomogeneities in the conductivity of the SiC substrate, which seems to be effectively reduced by the introduction of the buffer layer.

## References

[1] N.A. Mahadik et al., Applied Physics Letters, 100(4) 2012

[2] K. Konishi et al., Journal of Applied Physics, vol. 114, no 1, p. 014504. 2013

[3] J.P. Bergman et al., Mater. Sci. Forum, vol. 353 356, p. 299 302, 2001.

[4] J. D. Caldwell, et al., J. Appl. Phys. 108, 044503, 2010.

[5] A. Agarwal, et al., IEEE Electron Device Lett. 28, 587, 2007.

[6] S. Hayashi et al., Appl. Phys. Express, vol. 10, no 8, p. 081201. 2017.

[7] Y. Bu et al., Journal of Applied Physics, vol. 122, no 24, p. 244504, 2017.

[8] M. Kato et al., Scientific Reports, vol. 12, no 1, p. 18790, 2022.

[9] T. Tawara et al., Journal of Applied Physics, vol. 120, no 11, p. 115101, 2016.

[10] K. Konishi et al., AIP Advances, vol. 12, no 3, p. 035310, 2022.

[11] H. Itoh, H., et al., Materials Science Forum,vol. 1004, pp. 71-77, 2020

[12] S. Friedman, et al., Instrumentation, Metrology, and Standards for Nanomanufacturing, Optics, and Semiconductors VIII, SPIE, 2014.

[13] R. C. Germanicus et al., Beilstein J. Nanotechnol., vol. 11, no 1, p. 1764 1775, 2020.

[14] A. Michez, et al., IEEE Transactions on Nuclear Science, vol. 62, nº 4, p. 1516-1527, 2015.