Master in Radiation and its Effects on MicroElectronics and Photonics Technologies (RADMEP)

In-situ SEE Detection in Integrated Flip-flops

Master Thesis Report

Presented by

Stefan De Raedemaeker

and defended at

University Jean Monnet

11th of September 2023

Academic Supervisor: Prof. dr. Frédéric Saigné
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Jury Committee:

Dr. Arto Javanainen	University of Jyväskylä
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Prof. dr. Sylvain Girard	University of Saint-Etienne

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This thesis was submitted as a partial fulfillment of
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Abstract

Electronic devices are sensitive to single event effects due to one ionizing particle creating a temporary voltage pulse in a transistor of a logic cell. This pulse is called a Single Event Transient. When this pulse is captured in a flip-flop or latch, wrong data can be retained and propagated, which is called a Single Event Upset.
This thesis proposes a circuit level method of detecting the occurrence of a Single Event Effect inside flip-flops, which can be reported to a central processing unit or a dedicated mitigation system.
This work builds further on the principle of a double sampling flip-flop, where one main flip-flop captures the data at the positive clock edge, and a separate shadow flip-flop captures the data on a delayed clock edge. The main and delayed signals are compared by an exclusive or gate, after which this signal is latched to synchronize it with the sequential elements. When both the main output signal and the delayed output signal are the same, no temporary change in the data has occurred around the capturing clock edges of the flip-flops. But when the two signals differ, a transient or upset could have occurred, which needs to be reported.
The thesis presents a double sampling flip-flop design working up to 250MHz in UMC 180 nm technology. The design is synthesized, placed and routed in a layout with a clock tree appropriate for the design. It is shown that the design is functional and can be used as a replacement for a single flip-flop.
The groundwork is laid for a demonstrator chip with a shift register, where every standard cell flip-flop is replaced with the double sample flip-flop design during synthesis. All the Single Event Effects error signals originating from a section of double sampling flip-flops can be compressed through an OR-tree to maintain a single error signal for that section.

Preface

I would like to thank Prof. dr. ing. Jeffrey Prinzie and Prof. dr. Frédéric Saigné for their support and trust during my thesis.

I would like to thank Ing. Karel Appels and the members of the ADVISE research group at KU Leuven, in particular the digital design team, with whom I could have inspiring conversations and grow as an academic and professional.

I would like to thank the RADMEP organization for providing me with the opportunity to participate in this unique educational and cultural experience while meeting and learning from world's greatest experts in the field of radiation effects, microelectronics and photonics.

I'm grateful to the professors, lecturers and staff members of the faculties I visited during my studies, as they made us feel welcome at every new university location and taught us the most fascinating topics in their field of expertise.

Lastly, I would like to thank my family, friends and classmates for their support during these studies, and for the fun moments with lasting memories.

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1. Introduction

1.1. Research Question

The research internship project at KU Leuven presented in this thesis report aims to provide a robust method of detecting and reporting single event effect (SEE) as a consequence of transients in the data signal for standard cell flip-flops in UMC 180 nm technology.

1.2. General Background

The research is performed in the domains of digital chip design and the effects of ionizing radiation on microelectronics.
General principles of ionizing radiation effects on microelectronics are outlined in this section to better understand the context and need for this research.

1.2.1. Radiation Environments

Radiation is a phenomenon of (sub)atomic particles and (electromagnetic) waves propagating through space. Different sources of radiation can be classified in uncharged particles, charged particles and nucleons [1].

The uncharged particle of interest in the domain of effects of ionizing radiation on microelectronics is a photon. This is an electromagnetic particle which can manifest as visible light, but also ultraviolet light, infrared light, x-rays, gamma-rays and radio-waves.
The wavelength of a photon is inversely proportional to its frequency f with wavelength $\lambda = v/f$. The constant v is the propagation speed in the medium of the wave, such as the speed of light in space. A photon with a shorter wavelength, thus a higher frequency contains more energy as illustrated in Figure 1.

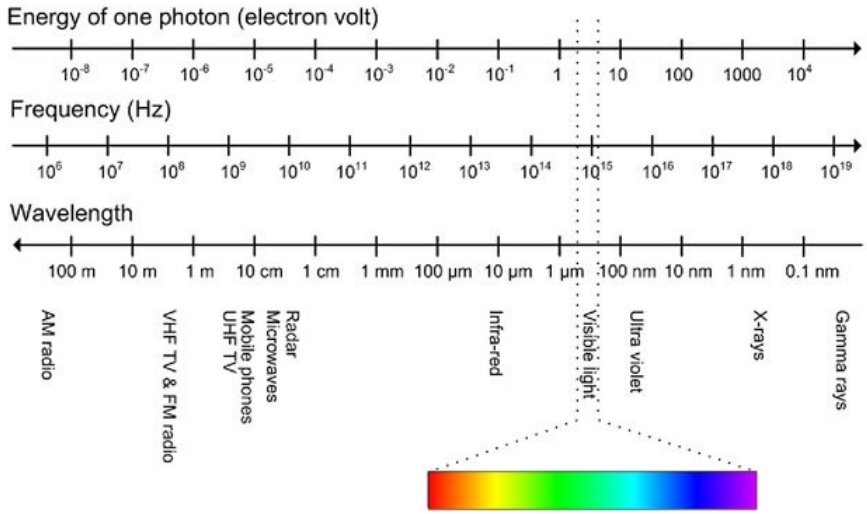

Figure 1: Electromagnetic spectrum showing the energy of one photon, the frequency, and wavelength.

The energy of a photon needs to be high enough to have an ionizing effect in another material. This is discussed in the section Radiation Effects.

Examples of charged particles which can interact with matter through the electromagnetic force are electrons, positrons and (heavy) ions. A well-known ion in the field of radiation effects is He^{+}, which is commonly referred to as an alpha particle or alpha radiation.

The third category of radiation particles interact through the strong force with the nuclei of target material. These particles are protons and neutrons.

The interaction mechanisms of these three categories of radiation particles are described in the section Radiation Effects.

Radiation particles can be found in different environments. The main natural sources of these particles are stars such as the sun in our solar system and big cosmic events such as supernovae.

The sun has a lot of activity in sunspots where magnetic field lines concentrate due to its rotation around its axis. Approximately every 11 years the orientation of this magnetic field reverses, creating cyclic activity of those sunspots, solar flares and coronal mass ejections.
The sun is comprised of plasma of light elements, mainly hydrogen which is fused to small amounts of helium due to the immense pressure and temperature inside. These light particles are catapulted in space every time a bundle of magnetic field lines in a sunspot snaps. Additionally, the sun continuously emits smaller amounts of ionized hydrogen particles which consists of protons and electrons in space, a phenomenon known as the solar wind [2].
Heavier high-energy particles can reach us from outside our solar system and even from outside our galaxy as cosmic rays.

Earth has a magnetic field around it due to Earth's rotation called the magnetosphere, which traps electrons and protons in two shells as illustrated in Figure 2. These shells of trapped particles are called the radiation belts or the Van Allen Belts. The inner belt contains high amounts of electrons and protons, while the outer belt only contains high amounts of electrons. The inner belt of trapped electrons comes very close to Earth's surface above the south of Brazil. This is called the South Atlantic anomaly and can be explained by Earth's tilted magnetic axis and offset of the magnetic center [3].

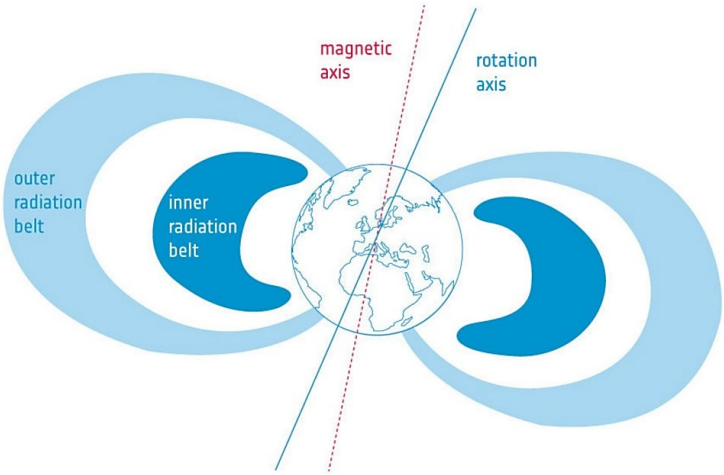

Figure 2: Van Allen Radiation Belts around Earth with the South Atlantic Anomaly. © ESA

The inner radiation belt lies between 1,000 km and 12,000 km above the surface of Earth with its center around 3,000 km. The outer radiation belt lies between 13,000 and 60,000 km, with a maximum density at an altitude of 15,000 km to 20,000 [3] [4].
Because some spacecraft cross these belts during launch or are even placed on an orbit inside the region of a radiation belt, they are an important factor in space missions and deployments.
Low Earth Orbit (LEO) missions stay below 1000 km and usually much lower such as 400 to 420 km for the international space station. Therefore, they have a low impact of the inner radiation belt.
Geostationary Orbit (GEO) missions are placed at an altitude of 35,788 km and therefore need to cross the two radiation belts during launch. Medium Earth Orbit (MEO) missions lie between LEO and GEO altitudes and can therefore be impacted by both radiation belts. Most navigation satellites are positioned in this orbit at an altitude of 20,000 km, right in the center of the outer radiation belt. Geostationary Transfer Orbit (GTO), Polar Orbit and Sun Synchronous Orbit (SSO) missions are even more impacted because the spacecraft crosses the radiation belts multiple times per orbital rotation or hang constantly in the inner radiation belt [5].
To protect spacecrafts against the electrons and protons in these radiation belts, critical electronics systems are shielded with a couple millimeters of aluminum [2].

When we look at the radiation environment in Earth's atmosphere, the main radiation particles of consequence are high energy neutrons. A maximum neutron flux exists at an altitude of around 20 km, which coincides with high altitude aviation. This maximum in neutron flux is called the Pfotzer maximum [6]. On the ground there is still a small influence of those neutrons, but also alpha particles due to spontaneous decay of materials. Under the ground the neutrons from the atmosphere are blocked, but the alpha radiation stays due to the materials in the ground such as uranium ^{238}U.

There are also man-made radiation environments such as nuclear power installations, particle accelerators and nuclear medicine equipment.

1.2.2. Radiation Effects on Matter

Some basic interaction mechanisms between radiation and matter are explained in this section.

The first set of processes involve an uncharged particle which interacts through the electromagnetic force. This is a photon particle, manifesting in for example visible light, x-ray or gamma-ray.
When a photon collides with a bound electron from a target atom, the photon can be deflected from its trajectory into another direction. If the energy of the photon doesn't change, its frequency or "color" doesn't change either. In this case we call it **Rayleigh or coherent scattering**, which has no effect on the target material because the photon doesn't interact with the elements of the target atom.
The energy of an incident photon can also be completely absorbed by a bound electron of the target atom, in which case the bound electron is ejected from the atom. This process is called the **photoelectric (absorption) effect** and only occurs when the photon energy is higher than the binding energy of the electron to the atom. However, the probability of the effect diminishes with higher photon energy as the photons will travel easier through the target material.
If the energy of the photon is higher than the binding energy of an electron to its atom, it is possible for the photon to eject the electron from its atom, and additionally scatter the photon into a new direction with the remaining energy. This is called **Compton or incoherent scattering** because the frequency or "color" of the photon has changed after impact with the electron. A Compton pair consisting of a free electron and a photon whit lower energy than in its initial state are created as a result of this Compton scattering.
The last mechanism for photon-matter interaction mechanisms in the electromagnetic field is **electron-positron pair production**. This happens in two situations, with the first situation being when the photon passes near the nucleus of the target atom and that photon having an energy of more than twice the energy of an electron. The energy of a single electron can easily be calculated with $E_e = m_e \cdot c^2 = 500$ keV with E_e the energy of an electron and m_e the mass of an electron. With this energy of two electrons, the creation of a single electron and a single positron are possible. This first situation is called "pair production in the nucleus field". In a second situation when the photon passes near a bound electron, that electron is ejected from its target atom, in addition to the creation of a single electron and a single positron. This second situation, sometimes called "triple production" or "pair production in the electron field" happens at a photon energy higher of at least four times the energy of an electron. [7] [8].
A graph plotting the cross-section, which is the probability of interaction with the target material in silicon in function of the photon energy, for the different interaction effects is illustrated in Figure 3. We can divide the graph into three different zones, where the photoelectric effect is dominant up to 100 keV, the Compton effect dominates between 100 keV and 10 MeV, and pair production is dominant above 10 MeV.

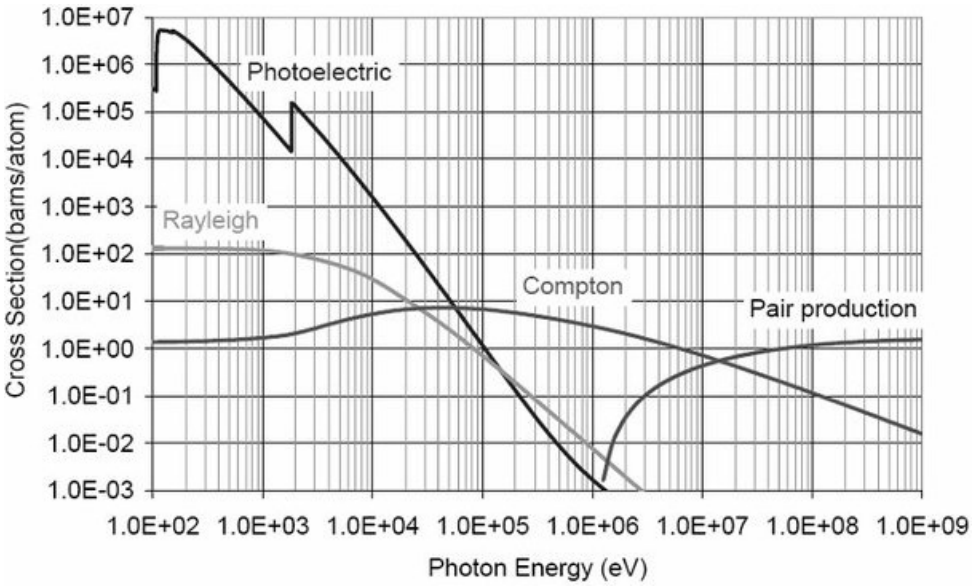

Figure 3: Photon cross-sections in function of energy for different interaction mechanisms.

Two main particle-matter effects can be defined when the incident particle has a charge, such as an electron, positron, proton or ion. These particles also interact through the electromagnetic field.

The first interaction mechanism is **elastic collision**, where the incident charged particle gets deflected into a new direction by the nucleus of the target atom. The target atom can also move slightly in the opposite direction, similar to how throwing the small ball against the bigger metal ball of pétanque would cause little movement to the latter. This process is called scattering, where the total kinetic energy between the incident particle and the atom is preserved.

The second interaction mechanism is **inelastic collision**, where the incident charged particle interacts with the electron shell of the target atom. An electron in the shell can be excited to a higher state by absorbing the needed energy from the incident particle, which will travel further with the remaining energy. It is also possible that the energy transferred from the incident particle is high enough to break the electron away from the atom, ionizing that atom. This mechanism is important for radiation effect is microelectronics.

When the incident charged particle is lightweight, such as an electron or positron, a couple of additional interaction mechanisms are possible.

Bremsstrahlung emission happens when this incident particle gets stopped in the electromagnetic field of the target atom, emitting a photon such as x-ray. The property of reducing the kinetic energy of an incident particle when traversing through a material, thus “stopping” that particle is called the stopping power, often denoted as LET for linear energy transfer [9].

Cerenkov emission happens when the incident particle passes through an insulating material with a speed higher than the propagation velocity of that material. This effect

emits blue light and is comparable to a sonic boom when an airplane travels at hypersonic speed.
When a positron (electron with positive charge) hits a bound electron of the target atom, this electron can absorb the positron's energy and create a photon pair traveling in opposite directions. This process is called **positron annihilation**.

Nucleons, being the particles of the nucleus of an atom such as protons and electrons, have two main interaction mechanisms. They can have **elastic collisions** similar to the elastic collisions of charged particles, but nucleons interact through the strong force instead of the electromagnetic force. In this situation the target atom has also little recoil, and the incident nucleon scatters in a new direction while maintaining the total kinetic energy between the two particles.
Non-elastic collisions are possible when nucleons hit the nucleus of a target atom. The total kinetic energy is not preserved, and new particles are created instead. These new particles can be photons, nucleons, lightweight charged particles or even new ions and atoms.

1.2.3. Radiation Effects in Semiconductor Devices

In this section three main radiation effects in semiconductors are presented.

The first type of radiation effects is due to **total ionizing dose**, abbreviated as **TID**. This is a long-term effect due to an accumulation of charge in the oxide regions of a semiconductor device such as a transistor. This charge is created by high-energy particles hitting the oxide material, creating secondary electron particles by ionizing the material. An incoming photon with an energy greater than the bandgap energy between the valence and conduction bands of the oxide material can raise an electron from its valance band to its conduction band, in essence freeing the electron from its atom as seen in Figure 4. In the case of a high energy neutron or proton hitting the material, non-elastic interactions can occur, which creates secondary ions which scatter away from their original location in the semiconductor material, creating electron-hole pairs along their paths. In the case of a high energy electron or proton hitting the material, an inelastic interaction can occur, which creates an additional electron. It is therefore possible for a single high-energy particle to create thousands of electron-hole pairs as illustrated in Figure 5.

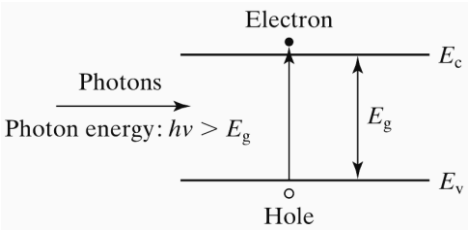

Figure 4: Electron-hole pair creation in semiconductor.

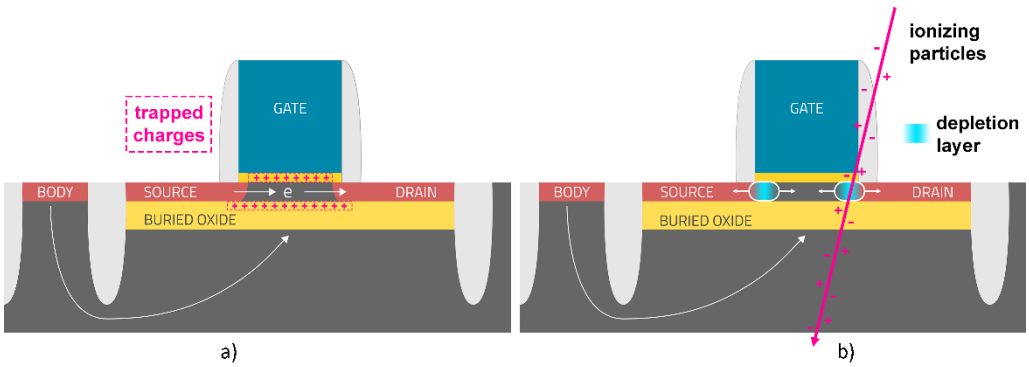

Figure 5: a) Charge accumulation in oxides of FDSOI transistor. b) Ionizing particles creating electron-hole pairs on its path through the device.

Most of the electrons in the oxide material recombine quickly with neighboring holes after their creation. When an electrical potential is applied over the oxide material, the remaining electrons are quickly swept away to the highest (positive) potential terminal, but the holes stay present in the oxide because they have a lower mobility than electrons. Those trapped holes, called oxide traps, move to the lowest electrical potential in the oxide through different localized states, breaking hydrogen bonds on its way. The rate of creation of oxide traps at the interface between the oxide and substrate is much higher than the creation of interface traps due to loose hydrogen bonds at the interface, and it is proportional to the applied gate bias voltage. No interface traps are created when a negative bias voltage is applied at the gate, because the hydrogen protons are attracted by the gate bias, away from the interface. The creation of positively charged oxide traps leads to a negative threshold voltage shift in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). This behavior can be desirable for p-type devices because it reduces its sub-threshold current, but it is undesirable for n-type devices because of an increase in its sub-threshold current. Additionally, the interface traps increase the sub-threshold voltage swing [9] [10] [11] [12].

A second radiation effect is **displacement damage (DD)**, where an incident particle changes the place of atoms in the silicon lattice structure. This effect is very important for optical devices such as light sensitive sensors.

The third category is **Single Event Effects**, often abbreviated to **SEE**, which are the electrostatic effects in semiconductor transistor devices due to a single ionizing particle such as a proton, neutron or heavy ion striking the silicon substrate of the device and (in)directly creating electron-hole pairs in the material. These charges drift quickly to the source/drain implants due to the applied electric field, creating a transient current pulse in the MOSFET. There are still remaining charges after drift, which slowly recombine or move to the surface due to diffusion. This temporal pulse effect due to a single incident ionizing particle is called a **Single Event Transient (SET)**. When the collection of charges at the gate of a transistor in a latch is high enough to create a logical inversion of the state, which remains until a new value is placed in that latch, we call it a **Single Event Upset (SEU)**. The issue of SEUs can be present in any type of digital

circuit type such as flip-flops and memory cells because they are often constructed with latches. A SET can be captured by a sequential cell to become a SEU, holding the wrong data.
A single particle can induce several upsets in different memory cells, which is called a Multiple Cell Upset (MCU). These MCUs can alter values in multiple memory cells in the same logical word, which is called Multiple Bit Upset (MBU).

In this thesis a solution for detecting SEUs in data flip-flops (DFFs) due to a SET being present on its data input is proposed.

Some state-of-the-art techniques for detecting and mitigating SETs and SEUs in sequential elements are discussed in the following section.

1.3. State of the Art

Single Event Transients can propagate trough sequential elements when the transient voltage peak gets captured around the capturing clock edge of such element. It can then become a Single Event Upset, resulting in wrong data and could lead to miscalculation or misconfiguration in a digital system.
The following circuit-level techniques described in this chapter can be used to eliminate the propagation of SETs or the creation of SEUs.

1.3.1. Triple Modular Redundancy (TMR)

One of the most commonly used techniques to prevent a SEE from influencing the state of the digital system is to compare the result of a logic computation against two copies of itself. When a SET or SEU occurs in one of the logic paths, the two other copies of that logic path will still hold the true value. The results of these three paths are compared with each other in a process called voting, where the logic value that is in the majority gets to pass through to the next stage of the digital path. This technique is called Triple Modular Redundancy (TMR), where all logic is triplicated with redundant data paths as illustrated in Figure 6. One could also triplicate the clocks, capturing sequential cells and voters to make the system the most robust against SETs.
This technique works very well to prevent SEEs from influencing the system, but there is a big power consumption and physical area overhead because cells need to be triplicated. The extra voters result in additional timing delays in the data path [13].

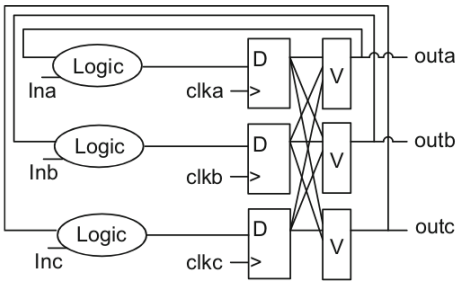

Figure 6: Schematic of full Triple Modular Redundancy.

When a system needs to be SEU tolerant, one could also use the Triple Device Redundancy (TDR) technique, where a whole integrated circuit chip or even electronic system is triplicated. A mitigation device verifies the correct behavior of all three electronic systems and uses voter logic to only use the majority results. There are a couple of advantages with this technique, such as not needing custom radiation hardened integrated circuits, and the ability to use different technologies or devices from different production batches or fabs. It is however not as energy efficient and compact as TMR [14].

1.3.2. Dual Interlock Cell (DICE)

In 1996 T. Callin et. al. [15] proposed a different design technique to make latches insensitive to radiation induced SEUs, called Dual Interlock Cell (DICE). The underlying principle of DICE is to have four interlocked nodes between inverters as illustrated in Figure 7. Nodes x0 and x2 are the inverse of x1 and x3 in this circuit, making sure that any upset in those inverters will be forced back to its correct state by the other nodes.
If for example p-type transistor P1 from node x1 receives charge from a SEE while node x0 and x2 are originally in a "high" state, and x1 and x3 in a "low" state, node x1 can flip into a "high" state. This can in turn activate both N0 from node x0 and P2 from node x2. Because the other side of those two nodes (P0 of x0 and N2 of x2) are still firmly in their original state, node x3 is also unaffected and can force all other nodes back to the correct state, correcting the SEU error.
This technique only works against single node upsets, where only one of the inverter nodes is hit at a time. The error cannot be mitigated when multiple nodes are struck. Additionally, there could be problems with charge sharing between neighboring transistor devices in the inverter nodes of deep-nm technologies when the devices are improperly spaced [16] [17].

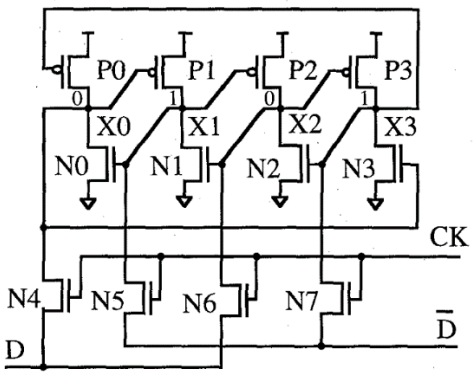

Figure 7: Principle of dual interlocked cell (DICE).

1.3.3. Glitch Filter

Glitch filters are another technique geared towards SET mitigation, based on temporal redundancy. A critical signal such as the result of a combinatorial computation is sent

through a delay chain of buffers or inverters and gets compared against the original signal in a majority voter. This only works for SETs with a transient pulse-width less than the delay time of the delay chain.

1.3.4. Razor Flip-Flop

From the field of high-performant processor design an interesting approach is borrowed for use in radiation-tolerant digital design.
The original goal of the technique was to improve the use of dynamic voltage scaling (DVS) for lowering the power consumption in processors. The authors of this technique wanted to reduce the voltage supply for the transistors as much as possible, right on the edge of creating faulty behavior. The supply voltage would be adapted in function of the detected error rate in the processor, therefore needing an error detection and correction mechanism. The Razor flip-flop uses a double-sample technique on the data path with a fast clocked flip-flop in the data path and a delayed fast clock controlling a shadow latch, as illustrated in Figure 8. The outputs of the main flip-flop and the shadow latch are compared with an exclusive-or (XOR) gate, after which the correct data can be re-applied to the input of the main flip-flop if an error occurs. This system is therefore used to detect timing faults due to failing (late) timing paths when the supply voltage becomes too low [18].

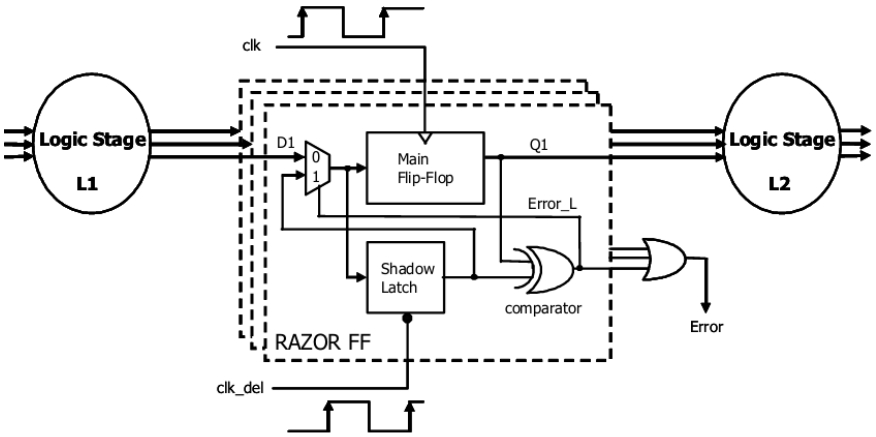

Figure 8: Pipeline augmented with Razor latches and control lines.

1.3.5. Shadow Flip-Flop for SET

The work of K. Appels [19] demonstrates that the use of a shadow flip-flop, similar to Razor, can be used to detect SETs, as the transient pulses behave like timing faults. The additional complexity lies in the unpredictable nature of SETs, as they can occur at any time during a clock cycle. This is solved by monitoring the critical window of setup and hold time around the capturing clock edge of the main flip-flop.
One of the main advantages of performing the error detection outside the main data path is that no additional delays are introduced to it.

2. Methodology

In this chapter the different steps of designing a double sampling error detection flip-flop are outlined.

2.1. Concept

The basic principle of the design for this thesis is the same as the double sampling technique with a shadow flip-flop from K. Appels which was discussed earlier.

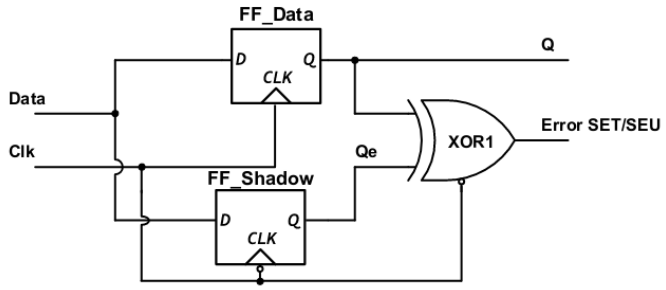

Figure 9 High level layout Double Sampling Error Detection Flip-Flop. (Image from K. Appels).

In the most basic form, a double sampling flip-flop has two flip-flops to capture the data at different times, a comparator in the form of an exclusive OR (XOR) gate, and a latch to retain the result of the comparison until it is stable.
One could use a flip-flop triggered on the positive clock edge, and another one triggered on the negative clock edge to create a data capture delay of half a clock cycle. This principle is shown in Figure 9. The input data signal is therefore expected to remain stable during a hold time of half a clock cycle, and a setup time for the main flip-flop.
One could also use a separate delayed clock for the shadow flip-flop, changing the needed hold time on the data line. This changes the maximum width of a SET that can be detected with this technique.
The latch behind the XOR gate needs to become transparent after the data becomes available at the output Q of the delayed shadow flip-flop and has passed through the XOR gate. Therefore, clock skew needs to be inserted for the XOR latch and data flip-flop to meet setup- and hold constraints.
The signal flow through the double-sampling flip-flop is illustrated in Figure 10. The data (d) arrives at the two flip-flops, and the main flip-flop first captures this data on the positive clock edge (clk), which becomes available at its output (q) after some clock-to-q delay. Half a clock-cycle later, at the negative clock edge (clkd), the data is captured by the shadow flip-flop, which puts the signal on its output (qd) after the clock-to-q delay. This is illustrated with arc “a” in Figure 10. When the data line is not stable around the positive or negative clock edges, due to a temporal voltage spike as a result of for example a SET, the double sampling flip-flop should output a signal to indicate that the flip-flop experienced a SEE, as illustrated on the figure with arc “b”.

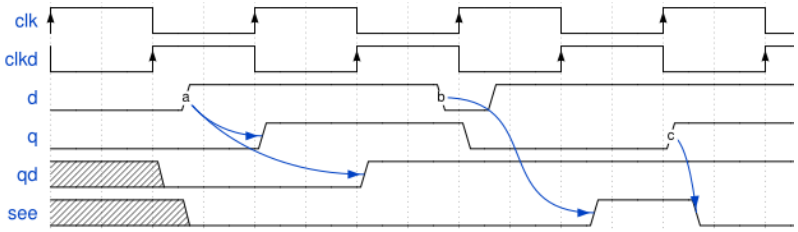

Figure 10 Signal flow of in-situ SEE detection in DFF.

If the latch of the XOR gate would immediately become transparent at the negative clock edge, a small glitch on the SEE error signal would appear, as illustrated in Figure 11 with the red pulses. While the latch is already transparent, the new value on QD still needs to propagate through the XOR gate, resulting in a brief moment where the XOR signal reflects the difference between Q and QD. This is unwanted behavior that leads to additional dynamic power and could lead to unexpected results when the SEE signal is used to take action to mitigate the SEE that occurred.
The LATCH wave in Figure 11 represents the status of the latch, being transparent (TRANS) during the low phase of the cock, and in latch mode (LATCH) during the high phase of the clock. In TRANS mode, the data at the input of the latch can pass immediately through to its output. In LATCH mode, the data at the output stays stable on the original value of the beginning of the LATCH mode phase.
The SEE signal shows the output signal of the latch, after the two flip-flop output signals Q and QD are compared with the XOR gate. This SEE signal is stable for at least half a clock cycle, during the LATCH mode phase.

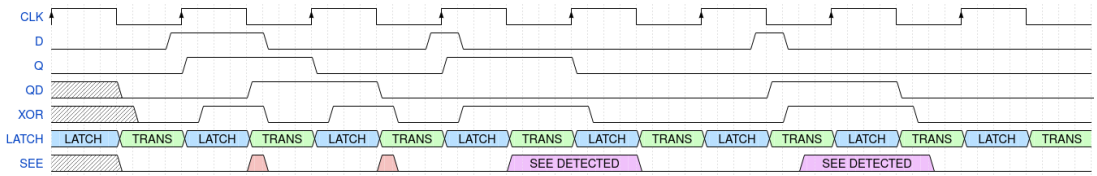

Figure 11: Glitch on SEE signal due to improper latch timing.

When the clock for the XOR gate receives some skew to push it a little further, the problem of the glitch gets solved, as illustrated in Figure 12. The delayed clock CKLD is giving the shadow flip-flop and the XOR gate time to propagate the data signal, before the latch becomes transparent. We only see the SEE signal becoming high when a short spike on the data signal happens around the positive or negative clock flank.

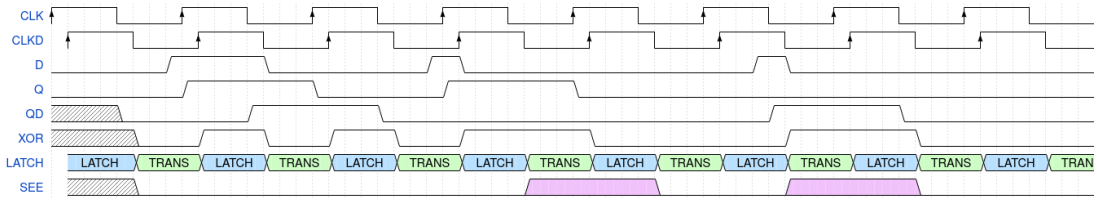

Figure 12: Glitch-free SEE signal due to correct latch timing.

2.2. RTL Design

The RTL design is not very complicated. The following elements were described in the Verilog hardware description language:

- Flip-flop capturing on positive clock edge, with asynchronous active low reset
- Flip-flop capturing on negative clock edge, with asynchronous active low reset
- Latch capturing on negative clock edge
- XOR gate
- Input and output ports
- Wires to connect the different elements in the module.

You can find the Verilog RTL hardware description in Appendix A: Verilog RTL.

The testbench is written in SystemVerilog and makes use of the assert functionality to verify the results of the device under test (DUT).
The testbench contains following items:

- Internal registers to create simulated signals
- Wires to connect to the inputs and outputs of the RTL design
- Local parameters to define the clock
- The DUT module instantiation
- Signal monitoring
- Sequential driving of the data and reset lines
- Clock generation driver
- Functional verification with assert statement

You can find the SytemVerilog testbench in Appendix B: System Verilog Testbench.

2.3. Synthesis

The RTL synthesis was performed with the Cadence Systems Genus tool version 21.10.
A Synopsys Design Constraint (SDC) file was defined to supply with the Genus tool for constraining the timing of the synthesized design. The SDC file can be found in Appendix C: Synopsys Design Constraints.
Tcl scripts were developed to provide the Genus tool with commands to execute the different steps from loading the standard cell library from Faraday for UMC 180 nm, loading the double sampling flip-flop design, elaborating and mapping the design to the cell library, and finally optimizing the design with the SDC, after which the design is exported into a new Verilog RTL file with the mapped standard cells, a new SDC file with updated timing constraints, and a SDF file containing the timing of the different cells in the design.

Setup checks are performed on the optimized design to verify the timing constraints on the design.

2.4. Layout

The layout phase of the design was performed with the Cadence Systems Innovus tool version 21.11.
Tcl scripts were developed to provide the Innovus tool with commands to execute the different steps from loading the standard cell library of Faraday for UMC 180 nm, loading the double sampling flip-flop design synthesized by Genus, including the generated SDC and SDF files, to defining the layout, placing the design, creating the clock tree, routing the design and performing post-route and signoff.
After each major step, a setup and hold time check was performed, and the design was saved to be able to perform functional verification.
Extra care was taken in the clock tree synthesis (CTS) phase, where useful skew and insertion delay needed to be added.
Useful skew allows to introduce variations in the clock arrival time at the flip-flops and latch. This way, the different sequential elements can have an improved timing characteristic in the circuit, allowing for better setup- and hold times between the different elements.

3. Results

3.1. Synthesis

The schematic design generated by the Cadence Systems Genus synthesis tool is illustrated in Figure 13. The two flip-flops, latch and XOR gate are mapped against standard cells from the Faraday library in UMC 180 nm technology.
The input data (d), active low reset (rstn) and clock (clk) are connected to the flip-flop capturing data on the positive clock edge (DFFRBN) and the flip-flop capturing data on the negative clock edge (DBFRBN). The output of those two flip-flops is connected to the XOR gate (XOR2HS), and its output arrives together with the clock at the latch which is transparent at the low clock phase (QDBHS).
A buffer (BUF1S) and inverter (INV1S) are added to the design to ensure proper driving capabilities and meet timing restrictions.
The outputs of the design are main data out (q), delayed data out (qd), inverted main data out (qn), inverted delayed data out (qdn) and single event effect error out (see).

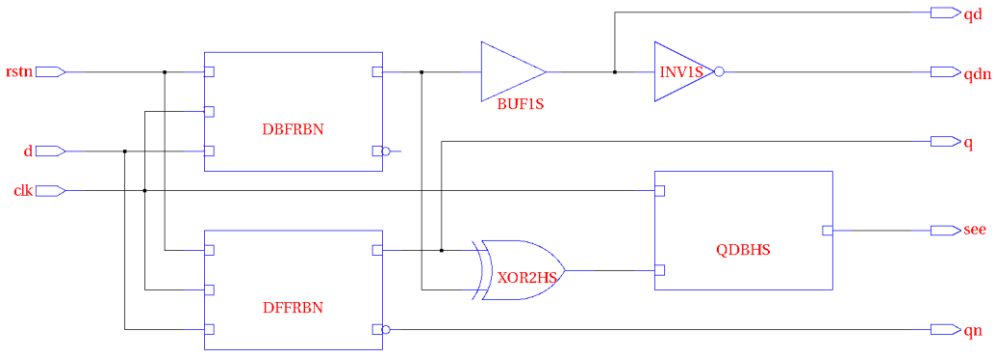

Figure 13: Schematic of fully synthesized and mapped design.

A setup timing report is requested at the end of the optimized synthesis design in Genus. Figure 14 illustrates the timing report of the violated timing path between the shadow flip-flop (qd_reg) and the latch (see_reg). The SDC file defines a clock period of 4000 ps (250 MHz clock), therefore the shadow latch captures the data at 2000 ps, at the falling clock edge. The latch wants to launch its input data during the transparent phase also at 2000ps. This results in a negative slack of -855 ps, which is a timing violation. The latch is not allowed to borrow time and needs to behave very similar to a flip-flop. This is also defined in the SDC file.
We expect this timing violation, because no clock skew or insertion delay is added to the synthesized design. This will be applied in the layout phase.

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.10-p002_1
  Generated on:           Aug 23 2023  12:10:39 pm
  Module:                 see_dsff
  Operating conditions:   _nominal_
  Interconnect mode:      global
  Area mode:              physical library
============================================================


Path 1: VIOLATED (-855 ps)
          Group: clk_i
     Startpoint: (F) qd_reg/CKB
          Clock: (F) clk_i
       Endpoint: (R) see_reg/D
          Clock: (F) clk_i

                    Capture       Launch
        Clock Edge:+    2000         2000
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=    2000         2000

     Time Borrowed:+       0
       Uncertainty:-     100
     Required Time:=    1900
      Launch Clock:-    2000
         Data Path:-     755
             Slack:=    -855

#-------------------------------------------------------------------------------------------------
# Timing Point   Flags    Arc   Edge   Cell     Fanout Load Trans Delay Arrival Instance
#                                                      (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------
  qd_reg/CKB     -        -      F     (arrival)      3    -   300     0    2000    (-,-)
  qd_reg/Q       -       CKB->Q R     DBFRBN         2 21.0   214   602    2602    (-,-)
  g27__2398/O    -       I2->O  R     XOR2HS         1  9.2   343   152    2754    (-,-)
  see_reg/D      <<<     -      R     QDBHS          1    -     -     0    2755    (-,-)
#-------------------------------------------------------------------------------------------------
```

Figure 14: Setup timing report for double sampling flip-flop in Genus

3.2. Layout

The layout phase starts with importing all the necessary libraries to provide the Innovus tool with the data to perform accurate calculations for the physical layout of the design. A floorplan of 100 by 100 micrometers is defined, in which a single double sampling flip-flop design is placed.

During the clock tree synthesis phase, a maximum useful skew of 2 ns and an insertion delay of 200 ps for the main flip-flop are defined in the Tcl script for clock tree synthesis. After clock tree synthesis, the main flip-flop receives the clock signal at 1.196 ns, the shadow flip-flop at 1.241 ns and the latch at 1.154 ns, as illustrated in Figure 15.

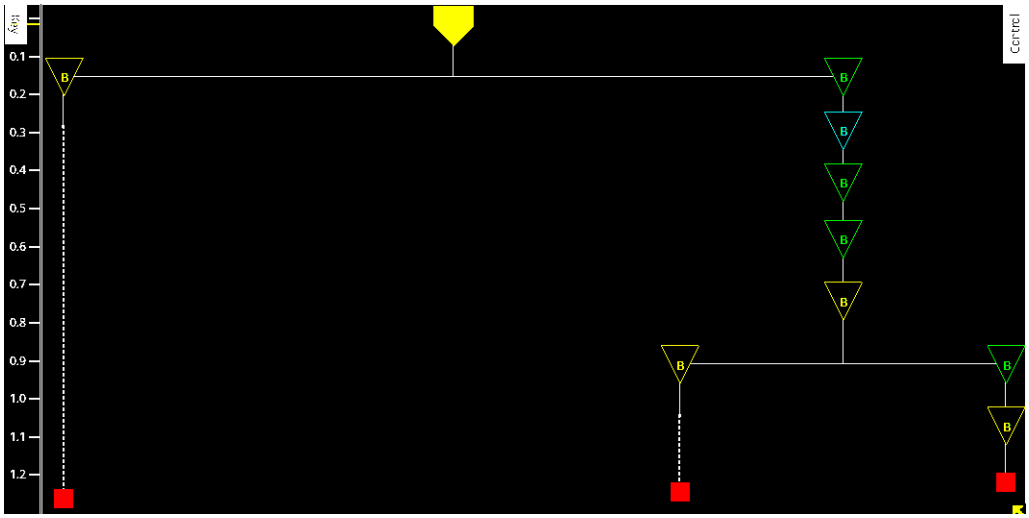

Figure 15: Clock tree of double sampling flip-flop.

The final layout of the double sampling flip-flop is illustrated in Figure 16.

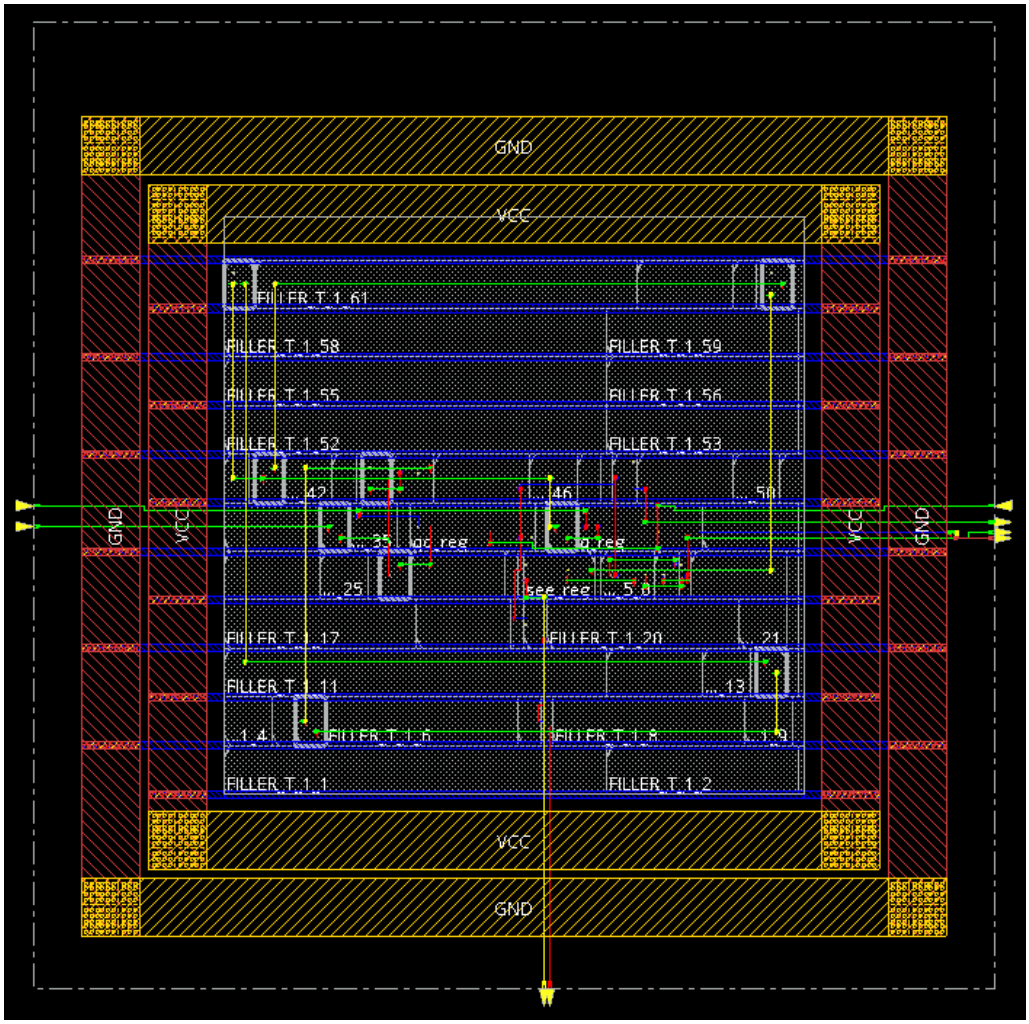

Figure 16: Physical layout of double sampling flip-flop in Innnovus.

Timing checks are reported between every big step in the layout flow to verify correct timing behavior between the different cells in the double sampling flip-flop design.
As illustrated in Figure 17, the setup timing constraints are met after clock tree synthesis and routing. A positive slack of 0.024 ps is reported.

```
#====================================================================
#  Generated by:      Cadence Innovus 21.11-s130_1
#  OS:                Linux x86_64(Host ID stud-r8-15.esat.kuleuven.be)
#  Generated on:      Mon Aug 14 14:13:16 2023
#  Design:            see_dsff
#  Command:           report_timing
#====================================================================
Path 1: MET Latch Borrowed Time Check with Pin see_reg/CKB
Endpoint:   see_reg/D (^) checked with trailing edge of 'clk_i'
Beginpoint: qd_reg/Q  (^) triggered by trailing edge of 'clk_i'
Path Groups: {clk_i}
Analysis View: av_ff
Other End Arrival Time          2.121
+ Time Borrowed                 0.000
+ Phase Shift                   0.000
+ CPPR Adjustment               0.000
- Uncertainty                   0.100
= Required Time                 2.021
- Arrival Time                  1.997
= Slack Time                    0.024
     Clock Fall Edge                 2.000
     + Clock Network Latency (Prop)  -0.268
     = Beginpoint Arrival Time       1.732
     +-------------------------------------------------------------------+
     |  Instance |     Arc      |  Cell  | Delay | Arrival | Required |
     |           |              |        |       |  Time   |   Time   |
     |-----------+--------------+--------+-------+---------+----------|
     | qd_reg    | CKB v        |        |       |   1.732 |    1.757 |
     | qd_reg    | CKB v -> Q ^ | DBFRBN | 0.212 |   1.944 |    1.969 |
     | FE_RC_5_0 | S ^ -> OB ^  | MXL2HS | 0.052 |   1.996 |    2.021 |
     | see_reg   | D ^          | QDBHS  | 0.000 |   1.997 |    2.021 |
     +-------------------------------------------------------------------+
```

Figure 17: Timing report for setup of final layout design of double sampling flip-flop.

The hold timing constraints are also met with a positive slack of 0.092 ps, as illustrated in Figure 18. This means that the double sampling flip-flop design should also be functionally correct, as we will see in the next section.

It took considerable amount of time to find the right approach, commands and values to provide to the Genus and Innovus tools to reach a correctly constrained design, in which the clock tree would be correctly built to reach a functionally working design.
Commands documented by Cadence Systems are not always supported or working as expected, and two parallel sets of commands are in use, making it sometimes difficult to find the counterpart of one command in the other command set.
The use of a latch to synchronize the see error signal adds complexity for the designer to make sure that the timing constraints are properly set for correct behavior. The proposed circuit works within one clock cycle to detect the SEE, making it fast and

efficient for a central processing unit or mitigation system to react and take measures to prevent the propagation or use of wrong data in the system.

```
#====================================================================
#  Generated by:      Cadence Innovus 21.11-s130_1
#  OS:                Linux x86_64(Host ID stud-r8-15.esat.kuleuven.be)
#  Generated on:      Mon Aug 14 13:35:53 2023
#  Design:            see_dsff
#  Command:           report_timing -early
#====================================================================
Path 1: MET Hold Check with Pin see_reg/CKB
Endpoint:   see_reg/D (^) checked with  leading edge of 'clk_i'
Beginpoint: q_reg/Q   (v) triggered by  leading edge of 'clk_i'
Path Groups: {clk_i}
Analysis View: av_ff
Other End Arrival Time          0.129
+ Hold                        -0.034
+ Phase Shift                  0.000
- CPPR Adjustment              0.001
+ Uncertainty                  0.100
= Required Time                0.194
  Arrival Time                 0.286
  Slack Time                   0.092
     Clock Rise Edge                     0.000
     + Clock Network Latency (Prop)      0.052
     = Beginpoint Arrival Time           0.052
     +-------------------------------------------------------------------+
     |  Instance |     Arc     |  Cell  | Delay | Arrival | Required |
     |           |             |        |       |  Time   |   Time   |
     |-----------+-------------+--------+-------+---------+----------|
     | q_reg     | CK ^        |        |       |   0.052 |   -0.040 |
     | q_reg     | CK ^ -> Q v | DFFRBN | 0.177 |   0.230 |    0.138 |
     | FE_RC_5_0 | B v -> OB ^ | MXL2HS | 0.056 |   0.286 |    0.194 |
     | see_reg   | D ^         | QDBHS  | 0.000 |   0.286 |    0.194 |
     +-------------------------------------------------------------------+
```

Figure 18: Timing report for hold of final layout design of double sampling flip-flop.

3.3. Simulation

Functional verification with a System Verilog testbench was performed in Cadence Systems Xcelium tool version 20.09.

First, a simulation of the elaborated design of the double sampling flip-flop is performed, as illustrated in Figure 19. We can notice that no delay between the clock edge and the transition of the signals at the output of the flip-flops and latch are present, because no timing information is present for generic elaborated cells.

Secondly, a simulation of the synthesized and optimized double-sampling flip-flop design is presented in Figure 20, where both a small delay can be perceived, but more importantly three small spikes on the see signal wave are present. This is due to the timing violation between the delayed flip-flop and the latch, resulting in a brief timing mismatch, as explained before.

The last simulation of the design after the place and route flow can be seen in Figure 21, where the spikes on the “see” signal are gone. This is the result we expected and wanted. We can see that every time an instability around the clock edge is present on the data line, an “see” error signal is generated, which stays present for a full clock cycle due to the latch.
Major effort is put in solving the problem of getting a glitch-free behavior in the design during this thesis. The main solutions of solving this problem are to provide the design with enough useful slack in the clock tree, and add some insertion delay to fine-tune the timing margins between the sequential elements in the double sampling flip-flop.

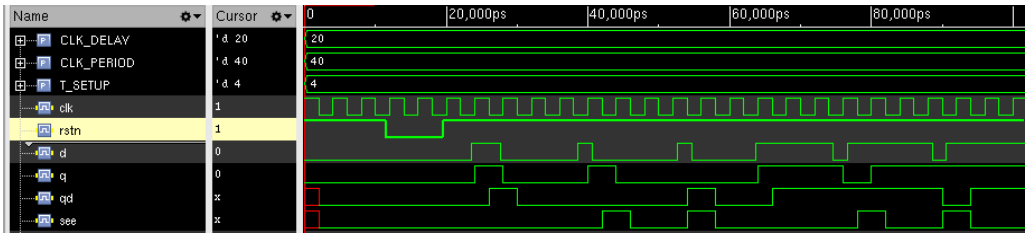

Figure 19 Simulation of elaborated double sampling flip-flop in Xcelium.

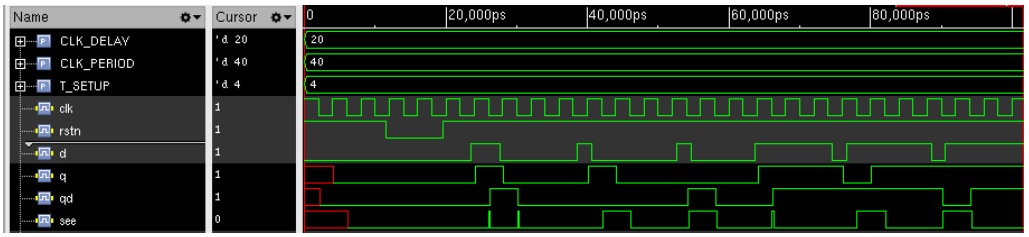

Figure 20 Simulation of synthesized double sampling flip-flop in Xcelium.

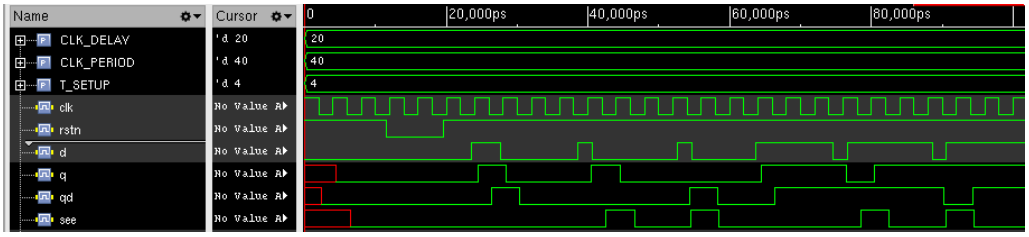

Figure 21: Simulation of placed and routed double sampling flip-flop in Xcelium.

3.4. Shift Register

The finished double sampling flip-flop can be used as a replacement for a standard cell data flip-flop (DFF). To test the feasibility of the proposed design, a test structure consisting of many double sampling flip-flops is useful because it shows that the timing between the flip-flop cells still stays between the design margins and that a large clock tree can be generated for the delayed latches. Therefore, a shift register where all standard cell DFFs are substituted by the proposed double sampling flip-flops is a valid test structure.
The process of substituting the flip-flops can be automated with a Tcl script, where the active design is queried for all DFFs present, which are put into a list. One could change

the parameters to query for only specific DFFs in a subsection of the design or which are marked to be substituted.
Figure 22 illustrates a simple shift register consisting of 8 standard flip-flop cells. Every flip-flop cell needs to be replaced by the proposed double sampling flip-flop cell.

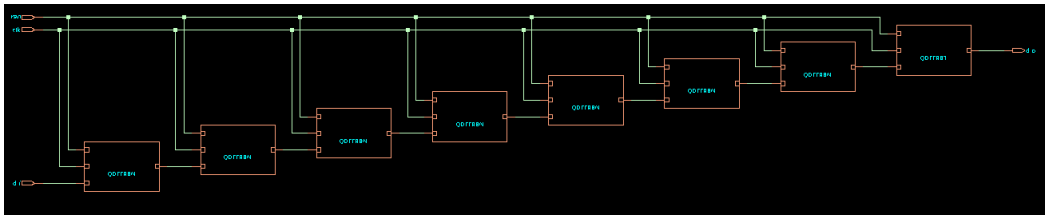

Figure 22: Elaborated 8-bit shift register.

After running the Tcl script during elaboration and synthesis flow, every flip-flop cell is replaced by the proposed double sampling flip-flop cell, as illustrated in Figure 23.
Additionally, the see error signals need to be connected. This is done with an OR-tree, where the error signals are compressed from N separate signals to just one signal, with N the number of flip-flops in the shift register.
A separate Tcl script finds the optimal tree structure of OR gates to compress the design, using only OR2 and OR3 gates, meaning that only OR gates with two or three inputs are used. This guarantees that both odd and even numbers of signals can be compressed in every layer of the OR-tree, as illustrated in Figure 23.

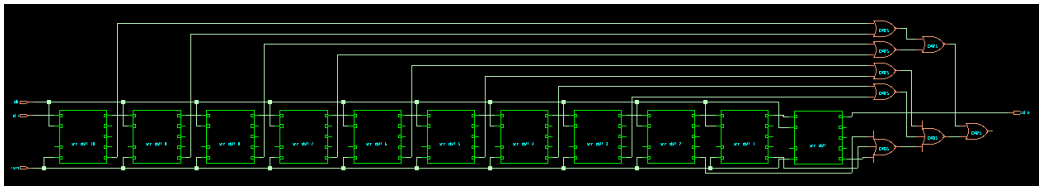

Figure 23 Substituted 11-bit shift register with see error or tree.

A shift register with 128 memory cells in the form of double sampling flip-flops is synthesized, which creates a big structure with a large OR-tree, as illustrated in Figure 24. At the top of the figure, you can find OR2 gates which are connected with its two inputs to separate “see” error signals which are outputs of two double sampling flip-flops. This first layer of OR gates is connected with its outputs to a second layer of OR gates, to aggregate the results, reducing the number of “see” error signals with about a factor of two in each layer of the OR-tree. This process of reducing the number of “see” error signals continues until only one signal remains, which is connected to the “see” output port of the design.

After completing the synthesis of the 128-bit shift register, where every standard cell flip-flop is replaced with the double sampling flip-flop and connected again into the design by a Tcl script, the layout phase of the design can be performed.

A bigger core area for this design is needed than for a single double-sampling flip-flop. I choose a die size of 250 by 250 micrometers, with horizontal and vertical power stripes every 50 micrometers, as illustrated in Figure 25.
The only inputs of the design are the clock, serial data and active low asynchronous reset ports, and the only outputs of the design are the serial data and “see” error ports.

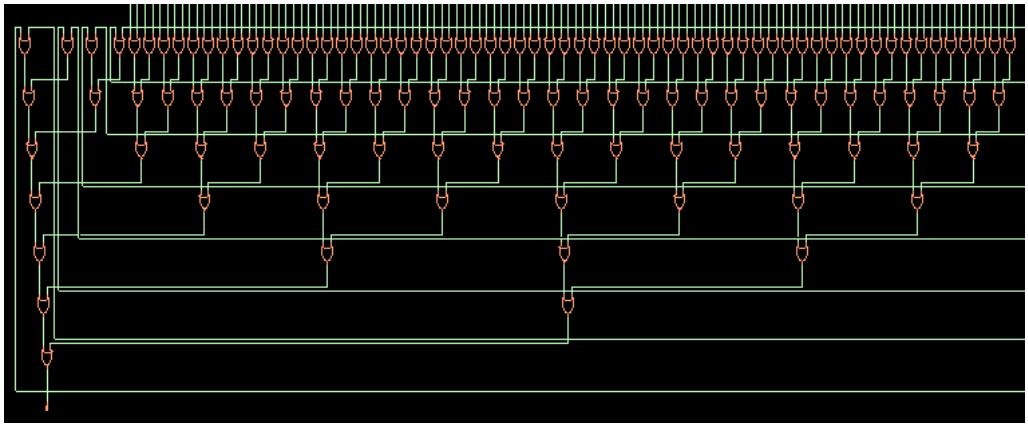

Figure 24: Or-tree for a 128-bit shift register.

There is more than threefold overhead in active power and area by using double sampling flip-flops instead of standard library cell flip-flops.
The sequential elements are put in a tree graph with the start of timing at the top, and the most delayed cells at the bottom of the graph, as illustrated in Figure 26.
We see in this graph that all the main flip-flops are grouped with a similar delay on the left. The shadow flip-flops and XOR latches from the double sampling flip-flops are grouped together on the middle and right branches of the tree. The element on the right bottom is the shadow flip-flop from the last double sampling flip-flop (128th) in the shift register.

Timing reports were extracted at different stages of the design flow of the shift register, to verify correct setup and hold timing behavior.
The finished shift register design meets the setup time conditions as illustrated in Figure 27, where the worst setup timing path is provided. This path is from the shadow flip-flop to the XOR latch in the second-to-last shift register double sampling flip-flop cell. The hold time constraint is also met as illustrated in Figure 28. This timing arc is between the main flip-flop and the XOR latch of the 47th shift register double sampling flip-flop cell. The counting of shift-register elements starts at 0.

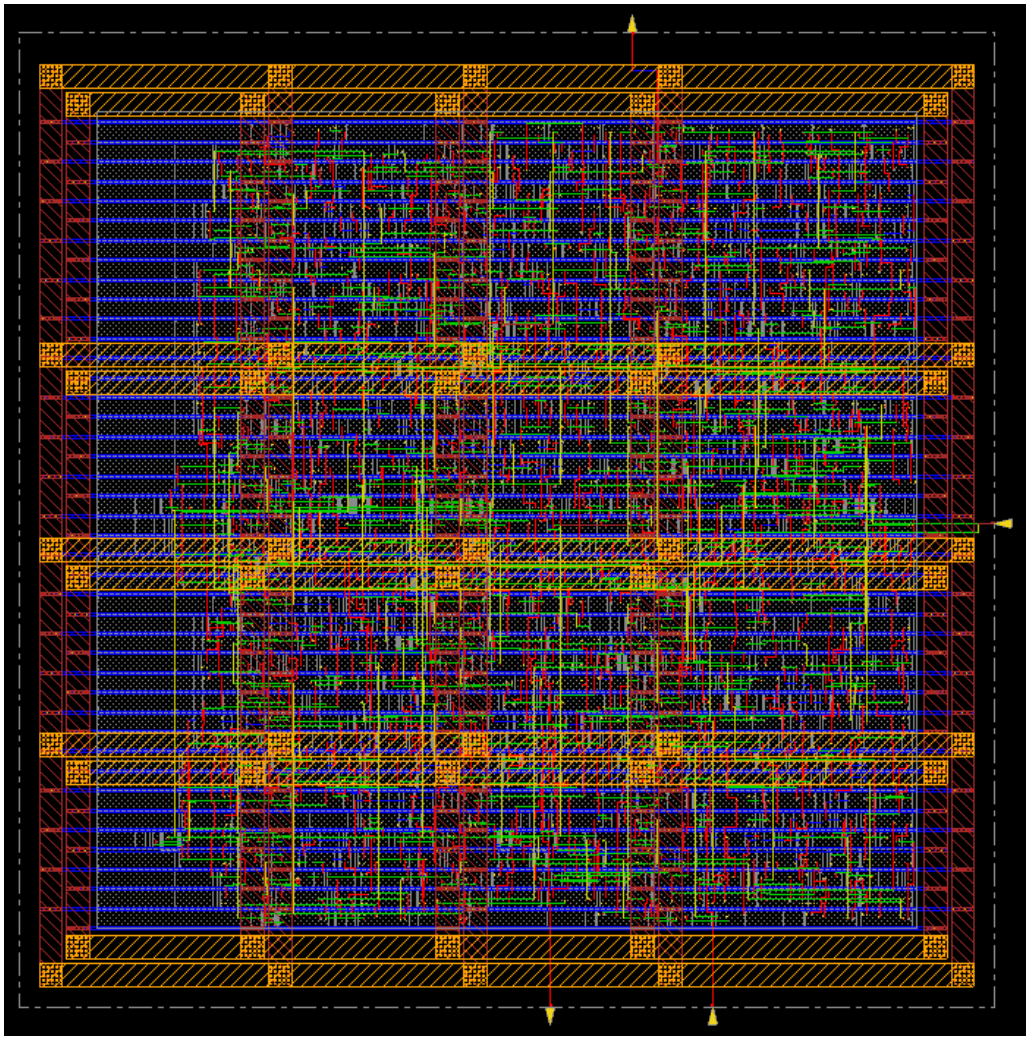

Figure 25: Layout of 128-bit shift register.

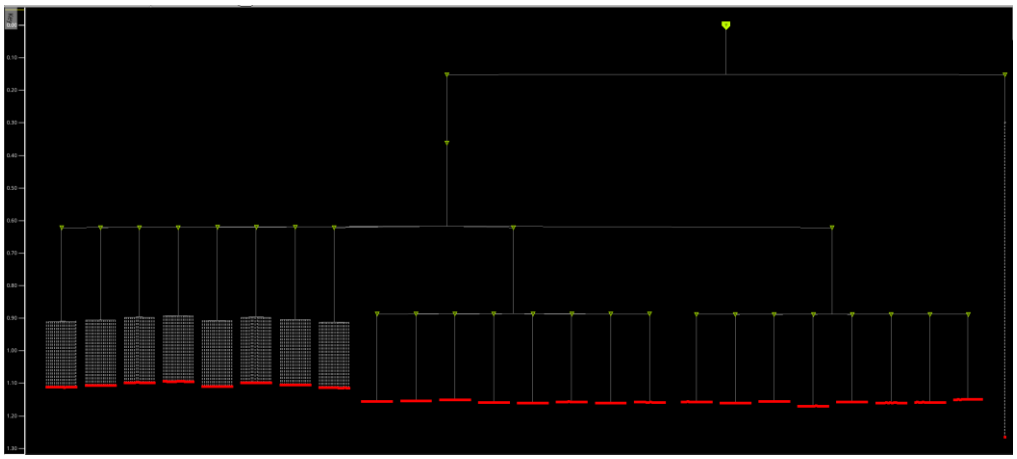

Figure 26: Clock tree of 128-bit shift register.

```
#------------------------------------------------------------
#  Generated by:      Cadence Innovus 21.11-s130_1
#  OS:                Linux x86_64(Host ID stud-r8-20.esat.kuleuven.be)
#  Generated on:      Thu Aug 24 16:22:20 2023
#  Design:            shiftreg_WIDTH128
#  Command:           report_timing
#------------------------------------------------------------
Path 1: MET Latch Borrowed Time Check with Pin shiftregister_reg[126]/see_reg/
CKB
Endpoint:   shiftregister_reg[126]/see_reg/D (^) checked with trailing edge of
'clk_i'
Beginpoint: shiftregister_reg[126]/qd_reg/Q  (^) triggered by trailing edge of
'clk_i'
Path Groups: {clk_i}
Analysis View: av_ss
Other End Arrival Time          2.081
+ Time Borrowed                 0.767
+ Phase Shift                   0.000
+ CPPR Adjustment               0.000
- Uncertainty                   0.100
= Required Time                 2.748
- Arrival Time                  2.748
= Slack Time                    0.000
     Clock Fall Edge                 2.000
     + Clock Network Latency (Prop)  0.081
     = Beginpoint Arrival Time       2.081
     +-----------------------------------------------------------------------------------------+
     |             Instance             |     Arc      |  Cell  | Delay | Arrival | Required |
     |                                  |              |        |       |  Time   |   Time   |
     |----------------------------------+--------------+--------+-------+---------+----------|
     | shiftregister_reg[126]/qd_reg    | CKB v        |        |       |   2.081 |    2.081 |
     | shiftregister_reg[126]/qd_reg    | CKB v -> Q ^ | DBFRBN | 0.541 |   2.623 |    2.623 |
     | shiftregister_reg[126]/g27__2398 | I2 ^ -> O ^  | XOR2HS | 0.125 |   2.748 |    2.748 |
     | shiftregister_reg[126]/see_reg   | D ^          | QDBHS  | 0.000 |   2.748 |    2.748 |
     +-----------------------------------------------------------------------------------------+
```

Figure 27: Setup timing report of 128-bit shift register.

```
innovus 5> report_timing -early
#------------------------------------------------------------
#  Generated by:      Cadence Innovus 21.11-s130_1
#  OS:                Linux x86_64(Host ID stud-r8-20.esat.kuleuven.be)
#  Generated on:      Thu Aug 24 16:22:44 2023
#  Design:            shiftreg_WIDTH128
#  Command:           report_timing -early
#------------------------------------------------------------
Path 1: MET Hold Check with Pin shiftregister_reg[46]/see_reg/CKB
Endpoint:   shiftregister_reg[46]/see_reg/D (v) checked with  leading edge of
'clk_i'
Beginpoint: shiftregister_reg[46]/q_reg/Q   (^) triggered by  leading edge of
'clk_i'
Path Groups: {clk_i}
Analysis View: av_ff
Other End Arrival Time          0.041
+ Hold                         -0.052
+ Phase Shift                   0.000
- CPPR Adjustment               0.000
+ Uncertainty                   0.100
= Required Time                 0.089
  Arrival Time                  0.163
  Slack Time                    0.074
     Clock Rise Edge                 0.000
     + Clock Network Latency (Prop)  -0.081
     = Beginpoint Arrival Time       -0.081
     +-----------------------------------------------------------------------------------------+
     |             Instance             |     Arc      |  Cell  | Delay | Arrival | Required |
     |                                  |              |        |       |  Time   |   Time   |
     |----------------------------------+--------------+--------+-------+---------+----------|
     | shiftregister_reg[46]/q_reg      | CK ^         |        |       |  -0.081 |   -0.155 |
     | shiftregister_reg[46]/q_reg      | CK ^ -> Q ^  | DFFRBN | 0.195 |   0.115 |    0.040 |
     | shiftregister_reg[46]/g27__2398  | I1 ^ -> O v  | XOR2HS | 0.049 |   0.163 |    0.089 |
     | shiftregister_reg[46]/see_reg    | D v          | QDBHS  | 0.000 |   0.163 |    0.089 |
     +-----------------------------------------------------------------------------------------+
```

Figure 28: Hold timing report of 128-bit shift register.

After each major design flow, functional verification is performed with Xilium. The result of the simulation with the finished shift register design to perform functional verification is illustrated in Figure 29.
After performing an active low asynchronous reset to all flip-flops in the shift register, performed by the testbench, a random sequence of 128 bits is supplied to the serial data input of the device under test. When the first of those bits has shifted through the whole shift register, after 128 clock cycles, the data at the output is compared to the original bit sequence.
The simulation shows that the design is functionally correct.

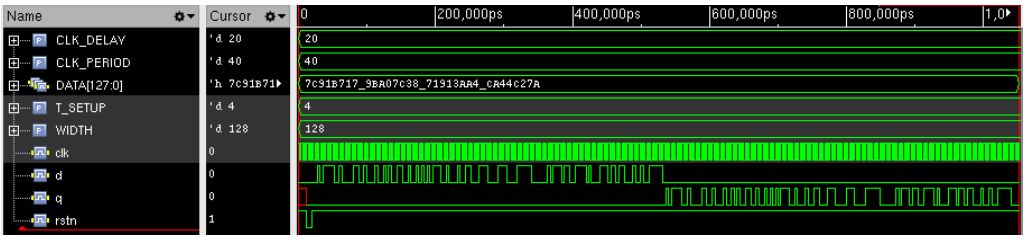

Figure 29: Simulation of routed 128-bit shift register design.

4. Conclusion

This thesis has presented the feasibility of using the double sampling technique for mitigating Single Event Effects in flip-flops in UMC 180 nm at 250 MHz by creating the design and successfully completing the functional verification.
The designer needs to be aware of the timing constraints between the shadow flip-flop and the XOR latch to retain enough setup time, preventing unwanted glitches on the see error signal. This can be achieved by allowing useful skew in the clock tree and providing some additional insertion delay to the main flip-flop to guarantee enough setup time for it.
The proposed double sampling flip-flop can be used as a drop-in replacement for standard cell DFFs to gain a means of detecting Single Event Transients and Single Event Upsets in those parts of the design.
A shift register can be used to test the double sampling flip-flop on a larger scale design, to formally verify the design in a custom chip.

5. Future Work

With the shift register where the standard cell flip-flops are replaced with the custom double sampling flip-flops proposed in this thesis, a tape-out of the design should be done. This design will be placed in a mini@sic multi-project wafer with dimensions 1525 by 1525 micrometer. This chip will be fabricated in the UMC fab on the 180 nm node.

A test platform for this design needs to be developed, consisting of a power source, clock generation and control logic for applying a reset and data stream, and capturing the output of the shift register and the compressed error signal.
This can be implemented on an FPGA, with the custom chip on a daughterboard connected to the FPGA.
This daughterboard should be able to be placed separately under radiation test equipment such as a Single Photon Absorption (SPA) laser system and a Two Photon Absorption (TPA) laser system.

The experimental results from the radiation tests on the custom chip should be compared with the results presented by K. Appels, who has developed a similar double sampling flip-flop system in 22nm FDSOI technology.

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Appendix A: Verilog RTL

```
`timescale 1ns / 1ps
`default_nettype none
//////////////////////////////////////////////////////////////////////////////////
//////
// Company: KU Leuven ESAT - ADVISE
// Engineer: Stefan De Raedemaeker
//
// Create Date: 12/04/2023 11:51:00
// Design Name: see_dsff.v
// Module Name: see_dsff
// Project Name: umc180nm-in-situ-ff-see-detection
// Target Devices:
// Tool Versions:
// Description: Single Event Double Sampling Flip-flop
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
//////

module see_dsff(
  input   wire  d,    // data in
  input   wire  clk,  // clock
  //input   wire  clkd, // delayed clock
  input   wire  rstn, // reset active low
  output  reg   q,    // data out
  output  wire  qn,   // data out inverse
  output  reg   qd,   // data delayed out
  output  wire  qdn,  // data delayed out inverse
  output  reg   see); // single event error out

  wire xor_q;

  assign xor_q = q ^ qd;
  assign qn = ~q;
  assign qdn = ~qd;

  always @(posedge clk, negedge rstn)
  begin : FF_DATA
    if (~rstn)
      q <= 1'b0;
    else
      q <= d;
  end

  always @(negedge clk, negedge rstn)
  begin : FF_SHADOW
    if (~rstn)
      qd <= 1'b0;
    else
      qd <= d;
  end

  always@*
```

```
  begin : LATCH_XOR
    if (~clk)
      see = xor_q;
  end

endmodule
```

Appendix B: System Verilog Testbench

```
`timescale 100ps / 1ps
`default_nettype none
////////////////////////////////////////////////////////////////////////////////
/////
// Company: KU Leuven ESAT - ADVISE
// Engineer: Stefan De Raedemaeker
//
// Create Date: 06/22/2023 11:51:00
// Design Name: see_dsff_tb4.sv
// Module Name: see_dsff
// Project Name: umc180nm-in-situ-ff-see-detection
// Target Devices:
// Tool Versions:
// Description: Testbench for Single Event Double
//              Sampling Flip-flop
// Dependencies: see_dsff.v
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////
/////
module see_dsff_tb;
  reg   clk;  // clock
  reg   rstn; // reset active low
  reg   d;    // data in
  //reg   clkd; // delayed clock
  wire  q;    // data out
  wire  qd;   // data out delayed
  wire  see;  // single event error out
  wire  qn;   // data out inverse
  wire  qdn;  // data out delayed inverse

  localparam CLK_PERIOD = 40;
  localparam CLK_DELAY = CLK_PERIOD/2;
  localparam T_SETUP = 4;

  see_dsff ff1 (
    .d    (d),
    .clk  (clk),
    //.clkd (clkd),
    .rstn (rstn),
    .q    (q),
    .qn   (qn),
    .qd   (qd),
    .qdn  (qdn),
    .see  (see) );

  initial
  begin
    $dumpfile("see_dsff_tb.vcd");
    $dumpvars(0,see_dsff_tb);
    $timeformat(-9, 2, " ns", 10);
    $display("START TEST\t q qd see qn qdn");
    $monitor("T=%0t\t %b  %b  %b   %b  %b",
      $time,q,qd,see,qn,qdn);
  end
```

```
  initial
  begin
    // Initialize values
    d = 0;
    clk = 1;
    //clkd = 1;
    rstn = 1;

    // Active low reset
    #(CLK_PERIOD-T_SETUP);
    #(CLK_PERIOD * 2) rstn = 0;
    #(CLK_PERIOD * 2) rstn = 1;

    // Toggle data line sychronous
    #(CLK_PERIOD)     d = 1;
    #(CLK_PERIOD)     d = 0;

    // SEE injection on posedge clk
    #(2*CLK_PERIOD);
    #(CLK_PERIOD/2);
    #(CLK_PERIOD/4)   d = 1;
    #(CLK_PERIOD/2)   d = 0;
    #(CLK_PERIOD/2);
    #(CLK_PERIOD/4);

    // SEE injection on negedge clk
    #(2*CLK_PERIOD);
    #(CLK_PERIOD/4)   d = 1;
    #(CLK_PERIOD/2)   d = 0;
    #(CLK_PERIOD/4);

    // SEE injection on posedge clk
    #(2*CLK_PERIOD)   d = 1;
    #(2*CLK_PERIOD);
    #(CLK_PERIOD/2);
    #(CLK_PERIOD/4)   d = 0;
    #(CLK_PERIOD/2)   d = 1;
    #(CLK_PERIOD/2);
    #(CLK_PERIOD/4);

    // SEE injection on negedge clk
    #(2*CLK_PERIOD);
    #(CLK_PERIOD/4) d = 0;
    #(CLK_PERIOD/2) d = 1;
    #(CLK_PERIOD/2);
    #(CLK_PERIOD/4);

    #(2*CLK_PERIOD); // end of simulation
    $display("V TEST PASSED");
    $finish;
  end

  // clk_driver
  always #(CLK_PERIOD/2) clk = ~clk;

  // FUNCTIONAL VERIFICATION SECTION
  xor_see:
  assert property (@(posedge clk) (q ^ qd) |-> see)
    else $error("Assertion of signal 'see' did't comply with latched xor
gate.");
endmodule
```

Appendix C: Synopsys Design Constraints (SDC) file

```
### Make SDC compatible with Genus
set_time_unit -picoseconds
set_load_unit -femtofarads

### Set clock 1800ps = 600 MHz
### Set clock 2000ps = 500 MHz
### Set clock 4000ps = 250 MHz
create_clock -name clk_i -period 4000 [get_ports clk]

set_clock_uncertainty 100 -setup -from [all_clocks] -to [all_clocks]
set_clock_uncertainty 100 -hold  -from [all_clocks] -to [all_clocks]

set_clock_latency 0 [all_clocks]
set_clock_transition 300 [all_clocks]

## max_transition = period/5
set_max_transition 800 [current_design]

set_load 5 [all_outputs]
set_max_fanout  8 [current_design]

set_input_delay 0 [all_inputs]
set_input_delay 0 [get_ports d] -clock clk_i -clock_fall

set_output_delay 0  [all_outputs]

## set a false path on the reset pins
set_false_path -from [get_ports rst*]

## remove time borrowing for see latch
set_max_time_borrow 0 [get_cell see_reg]
```

Appendices under NDA: Tcl scripts

Due to confidentiality agreements I'm not allowed to share the Tcl scripts with commands for Cadence Systems Genus and Innovus tools and Faraday UMC180 standard library cells. These scrips are used to run the synthesis and layout flows.