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# Quaternary Reversible Circuit Optimization for Scalable Multiplexer and Demultiplexer

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**ABSTRACT** Information loss is generally related to power consumption. Therefore, reducing information loss is an interesting challenge in designing digital systems. Quaternary reversible circuits have received significant attention due to their low-power design applications and attractive advantages over binary reversible logic. Multiplexer and demultiplexer circuits are crucial parts of computing circuits in ALU, and their efficient design can significantly affect the processors' performance. A new scalable realization of quaternary reversible  $4 \times 1$  multiplexer and  $1 \times 4$  demultiplexer, based on quaternary 1-qudit Shift, 2-qudit Controlled Feynman, and 2-qudit Muthukrishnan-Stroud gates, is presented in this paper. Moreover, the corresponding generalized quaternary reversible  $n \times 1$  multiplexer and  $1 \times n$  demultiplexer circuits are proposed. The comparison, with respect to the current literature, shows that the proposed circuits are more efficient in terms of quantum cost, the number of garbage outputs, and the number of constant inputs.

**INDEX TERMS** Circuit Optimization, Demultiplexer, Multiplexer, Quantum Computing, Quaternary, Reversible Logic, Scalable Realization.

## I. INTRODUCTION

A significant barrier to future circuit design is its high energy consumption. In 1961, Landauer proved that traditional irreversible gate leads to energy dissipation in circuit design [1]. Zhirnov et al. demonstrated that it would be impossible to remove heat from CMOS because of power dissipation [2]. According to Bennett's research, power dissipation can be prevented in circuit design by using reversible gates [3]. Recovering the input vectors from the output vectors in reversible gates is possible because the number of inputs equals the number of outputs.

Moreover, the output vectors are recoverable from the input vectors [4-6]. These circuits are also not permitted to have feedback or fan-out [6]. The inherent reversibility makes quantum technology a promising technology for future computer systems [7, 8].

Quantum computing could reduce the computational complexity of many problems and be much more efficient than classical computing. For instance, exploiting quantum algorithms, only  $\sqrt{N}$  steps are required instead of the  $N$  steps needed in classical algorithms to search an unstructured database [9-11]. Multiple-valued logic has received

considerable attention as future challenges for binary logic are expected to be massive due to severe thermal and reliability problems [12]. With respect to reversible binary logic, reversible multiple-valued logic is more secure in quantum cryptography [13-15] and more potent in quantum information processing [16]. Moreover, it exhibits a lower interconnection complexity [17] and a lower power consumption, and it is more error tolerant for quantum computations [18, 19]. Even though ternary logic is one of the most successful types of multiple-valued logic and many important works in this field [19-30], a limitation is that conventional binary logic functions cannot be easily represented in ternary logic. In quaternary logic, two bits can be grouped into quaternary values to express binary logic functions [31]. The memory unit is a qudit in quantum quaternary logic, and the possible states for a qudit are  $|0\rangle$ ,  $|1\rangle$ ,  $|2\rangle$ , and  $|3\rangle$ . Each of these states is represented by a  $4 \times 1$  vector in (1):

$$|0\rangle = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad |1\rangle = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} \quad |2\rangle = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \end{bmatrix} \quad |3\rangle = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 1 \end{bmatrix} \quad (1)$$

Recently, many essential circuits have been presented based on quaternary reversible logic, such as comparators, parallel adders, full adders, half adders, subtractors, and decoders [32-40].

Demultiplexer and multiplexer circuits are essential components of computers, arithmetic logic units, communication systems, memory systems, and converters [40]. This work proposes a new realization of quaternary reversible multiplexer and demultiplexer circuits. This paper aims to synthesize quantum quaternary circuits that are more efficient than the existing designs in the literature [40-42]. Moreover, we present the characteristics of the proposed circuits in terms of quantum cost, number of garbage outputs, and number of constant inputs, which are described as follows:

**Quantum cost** is the number of quaternary reversible 1-qudit Shift gates and 2-qudit Muthukrishnan-Stroud gates exploited for implementing the circuit. Circuit designers try to decrease the quantum cost as much as possible [40, 45].

**The number of garbage outputs** refers to the unutilized outputs added to the circuit to make it reversible. Increasing the number of these outputs enhances the information loss in reversible circuits [40, 44].

**The number of constant inputs** refers to inputs that must be held constant at a value of either 0, 1, 2, or 3 to synthesize the specified logic function. Increasing the number of these inputs enhances the lines in reversible circuits [40, 43].

In quantum quaternary logic, circuits are synthesized by minimizing these important parameters for better efficiency. The proposed quaternary circuits have better quantum cost, number of garbage outputs, and number of constant inputs compared with the existing designs in the literature [40-42].

This paper is structured as follows. The basic concepts of quaternary Galois field and quaternary reversible gates are explained in Section 2. Our proposed scalable realization of the quaternary reversible multiplexer and demultiplexer is presented in Section 3. In Section 4, the evaluation of the proposed circuits and comparison results are discussed. Finally, the conclusion of this work is provided in Section 5.

## II. BASIC CONCEPTS

This section shows the background on quaternary Galois Field and quaternary reversible gates, exploited in the subsequent sections.

### A. QUATERNARY GALOIS FIELD LOGIC

The algebraic structure of the Galois Field (GF4) in quaternary logic consists of the set of values  $Q = \{0, 1, 2, 3\}$ , the addition ( $\oplus$ ), and multiplication ( $\odot$ ) operations, which are displayed in Table I and Table II. These are associative and commutative operations. Moreover, multiplication is distributive over addition [46].

TABLE I  
THE TRUTH TABLE OF GF 4 ADDITION OPERATION

$\oplus$	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

TABLE II  
THE TRUTH TABLE OF GF 4 MULTIPLICATION OPERATION

$\odot$	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	3	1
3	0	3	1	2

### B. QUATERNARY 1-QUDIT SHIFT GATES

Any transformation of the qudit, in quaternary reversible logic, is represented by a  $4 \times 4$  unitary matrix, as shown in Figure 1. Each unitary matrix in Figure 1 can be realized as a 1-qudit Shift gate [40, 47]. They are 1-input 1-output gates having the mapping (A) to (P= Z transform of A), where the input is A, and the output is P. Figure 2 shows the graphical representation of quaternary 1-qudit Shift gates.

$$\begin{aligned}
 Z(+0) &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} &
 Z(+1) &= \begin{bmatrix} 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} &
 Z(+2) &= \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} &
 Z(+3) &= \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \\
 Z(123) &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} &
 Z(013) &= \begin{bmatrix} 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} &
 Z(021) &= \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} &
 Z(032) &= \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix} \\
 Z(132) &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \end{bmatrix} &
 Z(012) &= \begin{bmatrix} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} &
 Z(023) &= \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} &
 Z(031) &= \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \\
 Z(23) &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{bmatrix} &
 Z(01) &= \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} &
 Z(0213) &= \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} &
 Z(0312) &= \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \\
 Z(12) &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} &
 Z(0132) &= \begin{bmatrix} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \end{bmatrix} &
 Z(0231) &= \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} &
 Z(03) &= \begin{bmatrix} 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \\
 Z(13) &= \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix} &
 Z(0123) &= \begin{bmatrix} 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} &
 Z(02) &= \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} &
 Z(0321) &= \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}
 \end{aligned}$$

FIGURE 1. Quaternary 1-qudit unitary transforms.

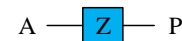


FIGURE 2. The graphical representation of quaternary 1-qudit Shift gates.

The relationship between the input and output of these 1-qudit Shift gates is illustrated in Table III. These are elementary quaternary reversible gates that can be realized utilizing liquid ion trap quantum technology. Therefore, these gates have a quantum cost of 1 [49].

TABLE III  
THE TRUTH TABLE OF QUATERNARY 1-QUDIT SHIFT GATES

A	Z(+0)	Z(+1)	Z(+2)	Z(+3)	Z(123)	Z(013)
0	0	1	2	3	0	1
1	1	0	3	2	2	3
2	2	3	0	1	3	2
3	3	2	1	0	1	0
A	Z(021)	Z(032)	Z(132)	Z(012)	Z(023)	Z(031)
0	2	3	0	1	2	3
1	0	1	3	2	1	0
2	1	0	1	0	3	2
3	3	2	2	3	0	1
A	Z(23)	Z(01)	Z(0213)	Z(0312)	Z(12)	Z(0132)
0	0	1	2	3	0	1
1	1	0	3	2	2	3
2	3	2	1	0	1	0
3	2	3	0	1	3	2
A	Z(0231)	Z(03)	Z(13)	Z(0123)	Z(02)	Z(0321)
0	2	3	0	1	2	3
1	0	1	3	2	1	0
2	3	2	2	3	0	1
3	1	0	1	0	3	2

C. QUATERNARY 2-QUDIT MUTHUKRISHNAN-STROUD GATES

Muthukrishnan and Stroud [47] proposed a family of 2-qudit multiple-valued gates, which are realizable in liquid ion-trap quantum technology. The quaternary Muthukrishnan-Stroud (M-S) gate is basically a controlled 2-qudit gate with two inputs and two outputs that can be defined as:

$$I_V = (A, B)$$

$O_V = (P=A, Q=Z \text{ transform (1-qudit transform) of the controlled input B if the controlling input A is equal to 3; otherwise, the output Q is equal to the controlled input B),$  where  $I_V$  is the input vector, and  $O_V$  is the output vector. Hence the inputs are A and B, and the outputs are P and Q [47].

Figure 3 illustrates the symbolic representation of the quaternary 2-qudit Muthukrishnan-Stroud gate. The quantum cost of this gate is equal to 1.

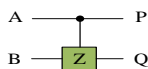


FIGURE 3. Symbolic representation of quaternary 2-qudit Muthukrishnan-Stroud gate.

D. QUATERNARY 2-QUDIT CONTROLLED FEYNMAN GATE

The quaternary Controlled Feynman gate is a 3-input 3-output gate having the mapping (A, B, C) to (P=A, Q=B, R= B ⊕ C) if the input A is equal to 3; otherwise, the output R is equal to the input C), where the inputs are A, B, and C and, the outputs are P, Q, and R [48].

Figure 4a displays the graphical representation of the quaternary Controlled Feynman gate. Figures 4b and 4c demonstrate different realizations of this gate using M-S gates. This gate has a quantum cost of 6. According to the second realization in Figure 4c, it is possible to remove the 2-qudit M-S gate in the red box if the input B is not needed at the output

Q. Thus, the quantum cost can be reduced to 5, and the output Q is equal to B+2 if the input A=3.

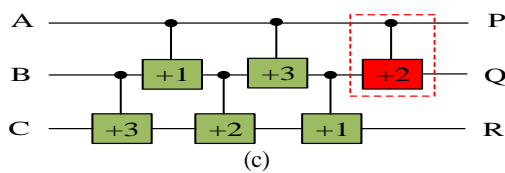
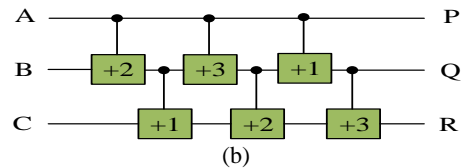
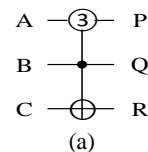


FIGURE 4. Quaternary 2-qudit Controlled Feynman gate. a) Symbol. b) The first realization using M-S gates. c) The second realization using M-S gates.

III. PROPOSED QUATERNARY REVERSIBLE CIRCUITS

In this section, we propose a scalable quaternary reversible 4×1 multiplexer, and we use it to design the quaternary reversible 16×1 and n×1 multiplexers. Moreover, we introduce the new scalable quaternary reversible 1×4 to design 1×16 and 1×n demultiplexers. We use quaternary 1-qudit Shift and 2-qudit controlled Feynman gates. The aim is to reduce the overall quantum cost, the number of constant inputs, and the number of garbage outputs.

A. PROPOSED QUATERNARY REVERSIBLE MULTIPLEXER CIRCUIT

Before discussing our proposed quaternary reversible multiplexer circuit, we provide the basic definitions and properties of the quaternary multiplexer. A quaternary multiplexer with 4<sup>n</sup> inputs, has n select lines to select which input should be sent to the output. Let A be a selector equal to 0, 1, 2, or 3. In a 4×1 multiplexer, when A is equal to 0, 1, 2, or 3, the output equals I<sub>0</sub>, I<sub>1</sub>, I<sub>2</sub>, or I<sub>3</sub>, respectively. Table IV shows the truth table of the quaternary 4×1 multiplexer.

TABLE IV  
THE TRUTH TABLE OF QUATERNARY 4×1 MULTIPLEXER

A	O
0	I <sub>0</sub>
1	I <sub>1</sub>
2	I <sub>2</sub>
3	I <sub>3</sub>

The realization of our proposed quaternary reversible 4×1 multiplexer circuit is illustrated in Figure 5a. As shown in the figure, we used four quaternary 1-qudit Shift gates and four quaternary 2-qudit Controlled Feynman gates. In this

realization, the main inputs are I0 to I3, and one 0 constant input is required. The selector is A, and the main output is O. The circuit produces five garbage outputs that are Q0 to Q3 and P. The output P is equal to the selector A, and the outputs Q0 to Q3 are equal to the inputs I0 to I3, respectively. In this circuit, when the selector A is equal to 0, the controlling value of the first Controlled Feynman gate is 3, and the output O is equal to I0. If A is equal to 1, the second Controlled Feynman gate is 3, and the output O is I1.

Moreover, when the selector is equal to 2 and 3, the output O is equal to I2 and I3, respectively. The realization of this circuit using quaternary Shift and M-S gates is shown in Figure 5b. In this figure, red boxes depict quaternary Controlled Feynman gates. Generally, four quaternary Shift gates and twenty-four quaternary Muthukrishnan-Stroud gates were used. Therefore, the quantum cost of the proposed quaternary reversible 4x1 multiplexer circuit is 28. It is worth mentioning that, in a multiplexer circuit, it is not necessary to restore the input I at the output Q. So, we can remove the red Muthukrishnan and Stroud gates in this realization. The quantum cost can be decreased by 24. In both suggested ways, the number of constant inputs is 1, and the number of garbage outputs is 5.

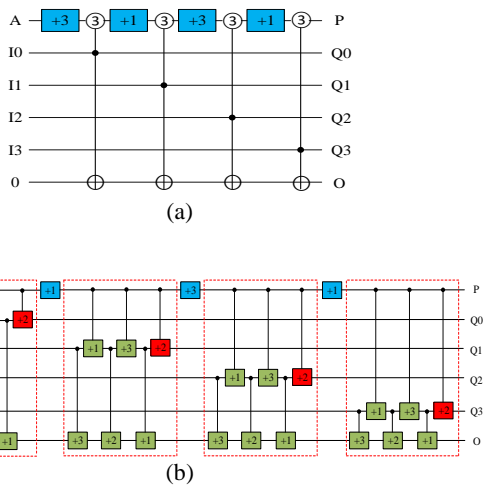


FIGURE 5. The proposed quaternary reversible 4x1 multiplexer circuit. a) Symbol. b) The realization using M-S and Shift gates.

Our proposed quaternary reversible 4x1 multiplexer can be used to construct a 16x1 multiplexer. For designing this multiplexer, 16 inputs, two selectors, and one output are necessary. The truth table of this circuit is shown in Table V. Only the selected input is gated to the output O for a given selector combination of A and B.

Figure 6a shows the logical architecture of the proposed quaternary 16x1 multiplexer using 4x1 multiplexer. As shown, five 4x1 quaternary multiplexers are required. In this design, the first inputs of the first-row multiplexers are activated when input B is equal to 0. Activation of the second inputs of multiplexers occurs when input B is equal to 1. If B

is equal to 2 and 3, the third and fourth inputs of multiplexers are activated, respectively.

TABLE V  
THE TRUTH TABLE OF QUATERNARY 16x1 MULTIPLEXER

Selectors (AB)	Output (O)
00	I0
01	I1
02	I2
03	I3
10	I4
11	I5
12	I6
13	I7
20	I8
21	I9
22	I10
23	I11
30	I12
31	I13
32	I14
33	I15

Moreover, the output of the first multiplexer is gated on the main output O when the selector A is equal to 0. If A is equal to 1, the main input is sent to the main output by the second multiplexer. When A is equal to 2 and 3, the output of the third and the fourth multiplexers are gated on the output O, respectively. Figure 6b illustrates the realization of the proposed quaternary reversible 16x1 multiplexer using a 4x1 multiplexer. The red boxes indicate our proposed quaternary reversible 4x1 multiplexer. In this circuit, there are five constant inputs, which are 0, and sixteen main inputs, which are shown by I0 to I15. The selectors are A and B. The main output is O, and the garbage outputs are P1, P2, O0 to O3, and Q0 to Q15. The outputs P1 and P2 are equal to A and B, respectively. Generally, the first realization of quaternary 2-qudit Controlled Feynman gates is used when inputs need to be restored. In this case, 20 quaternary Shift gates and 120 quaternary Muthukrishnan-Stroud gates are inserted in the circuit. Therefore, the quantum cost is 140. However, in multiplexer circuits, the inputs I0 to I15 are unnecessary as outputs, so it is possible to use the second realization of quaternary-controlled Feynman gates. Therefore, the second realization of quaternary-controlled Feynman gates can be used, and the quantum cost is 120.

We could also combine some gates in designing a quaternary reversible 16x1 multiplexer and present a circuit with a lower quantum cost. As shown in Figure 6c, an optimized multiplexer circuit can be realized. Eight quaternary Shift gates are used along with twenty quaternary Controlled Feynman gates. Due to the use of the second realization of Feynman gates, eight quaternary Shift gates and 100 quaternary Muthukrishnan-Stroud gates were used in total. This results in a quantum cost of 108. This innovative combination provides improvement over the first realization regarding the quantum cost. Moreover, in both realizations,

the number of constant inputs is five, and the number of garbage outputs is 22.

Based on our proposed quaternary reversible  $4 \times 1$  multiplexer, we proposed a generalized quaternary reversible  $n \times 1$  multiplexer circuit, shown in Figure 7. Hence, our design is scalable. A quaternary  $n \times 1$  multiplexer circuit consists of  $n = 4m$  inputs,  $m$  selectors, and only one output. In this circuit,  $m$  rows of  $4 \times 1$  multiplexers are needed. The first row requires  $4m - 1$  multiplexers, the second row requires  $4m -$

2 multiplexers, and the  $m$  row requires one multiplexer. Therefore, we can determine the number of  $4 \times 1$  multiplexers needed to design our proposed  $n \times 1$  multiplexer using geometric series formulas. The number of multiplexers is shown by  $P$  in (2):

$$P = \sum_{i=0}^{m-1} 4^i = \frac{4^m - 1}{3} = \frac{n - 1}{3} \quad (2)$$

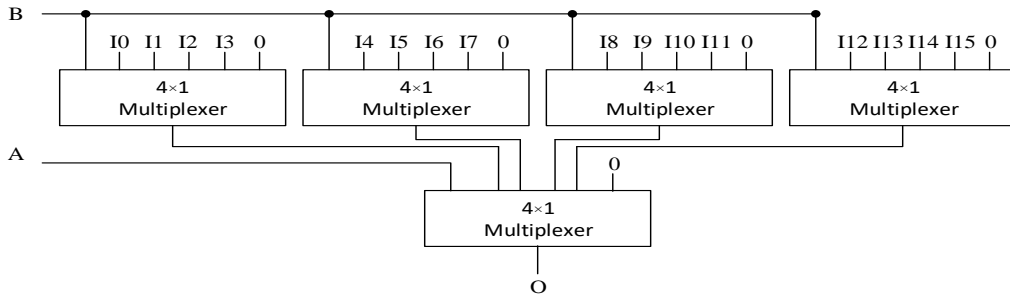


Fig.6-(a)

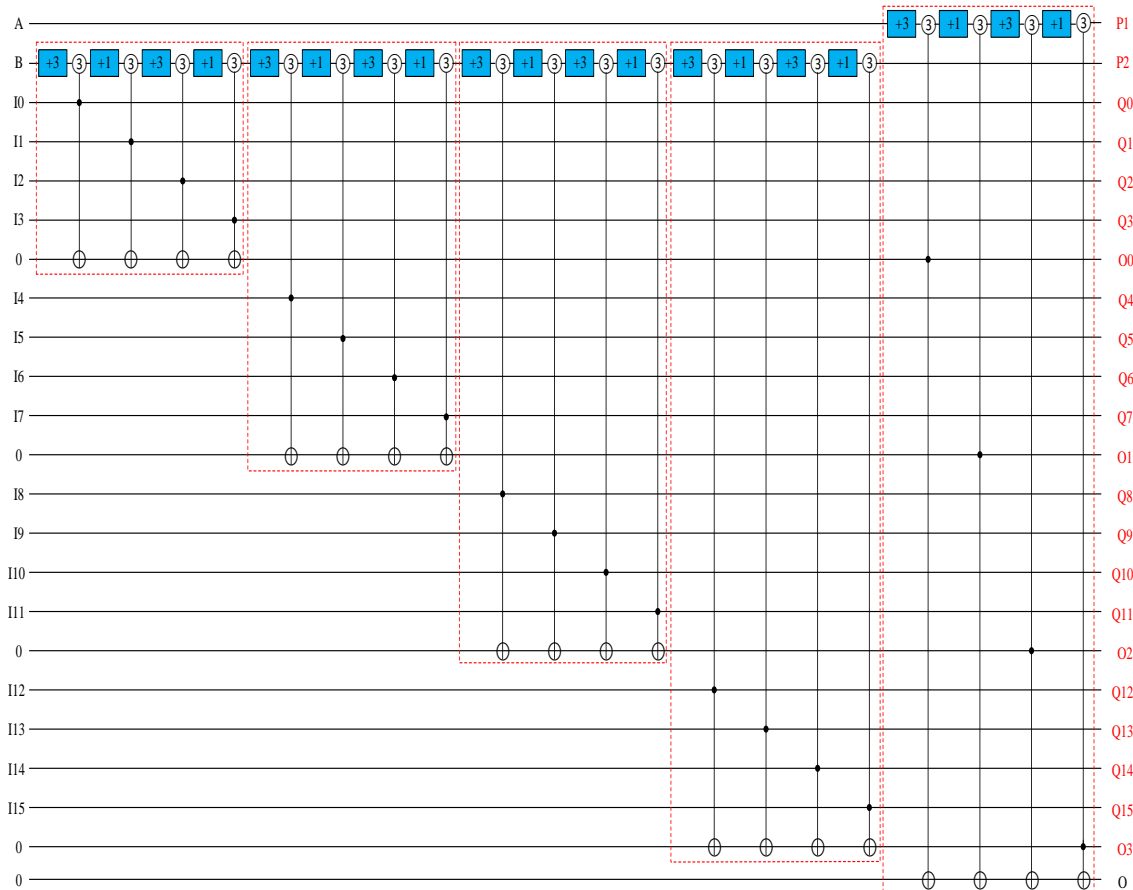


Fig.6-(b)

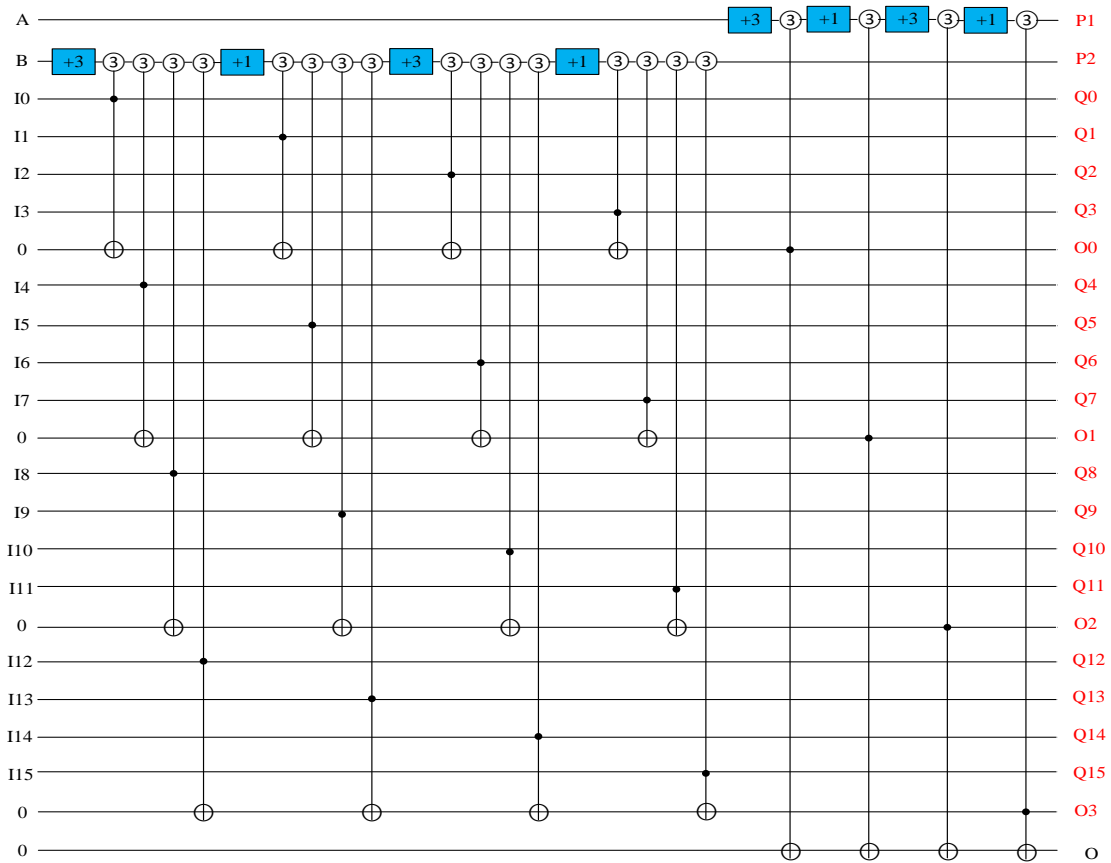
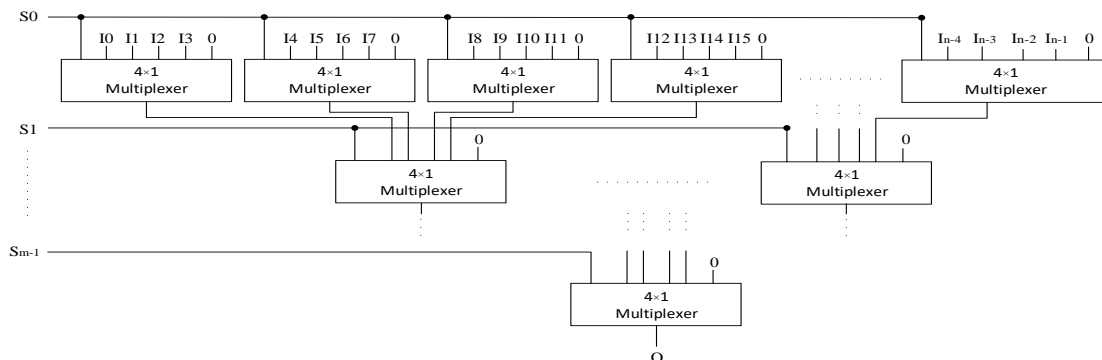


Fig.6-(c)

**FIGURE 6.** The proposed quaternary reversible 16x1 multiplexer circuit. a) The logical architecture b) The primary realization. c) The optimized realization.

The quantum cost of a quaternary reversible  $n \times 1$  multiplexer is  $24((n-1)/3)$ , and it requires  $(n-1)/3$  constant inputs and produces  $(3m+4n-4)/3$  garbage outputs. We can combine the quaternary 1-qudit Shift gates in each row according to the mentioned optimization approach in the last part. In this way, we have four 1-qudit Shift gates in each row. We also have  $4m-1$  and  $4m-2$  Controlled Feynman gates in the first and the second row, respectively. Moreover, in the last row, four Controlled Feynman gates are

needed. Therefore, it can be concluded that in the proposed quaternary reversible  $n \times 1$  multiplexer,  $4((n-1)/3)$  Controlled Feynman gates and  $4m$  1-qudit Shift gates are required, where  $n$  is the number of inputs and  $m$  is the number of selectors. Since we used the second realization of the Controlled Feynman gate, the total quantum cost of this optimized circuit is  $20((n-1)/3) + 4m$ .



**FIGURE 7.** The logical architecture of the proposed quaternary reversible  $n \times 1$  multiplexer circuit.

**B. PROPOSED QUATERNARY REVERSIBLE DEMULTIPLEXER CIRCUIT**

A demultiplexer performs the opposite function of a multiplexer. A quaternary demultiplexer of  $4n$  outputs has  $n$  select lines to send the input to the output. In a  $1 \times 4$  demultiplexer, when the selector A is equal to 0, 1, 2, or 3, the output O0, O1, O2, or O3 is equal to I, respectively. Table VI shows the truth table of the  $1 \times 4$  quaternary demultiplexer.

TABLE VI  
THE TRUTH TABLE OF QUATERNARY  $1 \times 4$  DEMULTIPLEXER

A	O0	O1	O2	O3
0	I	0	0	0
1	0	I	0	0
2	0	0	I	0
3	0	0	0	I

In Figure 8a, we show the realization of our quaternary reversible demultiplexer circuit. Four quaternary 1-qudit Shift gates and four quaternary 2-qudit Controlled Feynman gates are exploited in this design. The main input is I, which requires four constant inputs, all of which are 0. The selector is A. O0 to O3 are the main outputs, and P and Q are the garbage outputs are equal to A and I, respectively. The first Controlled Feynman gate with a controlling value of 1 is applied when the selector is equal to 0, and the input I is sent to O0. This circuit applies the controlling value of the second Controlled Feynman gate when the selector A is equal to 1, and the input I is sent to O1. If the selector is equal to 2 or 3, the outputs O2 and O3 are equal to the input I, respectively. Figure 8b shows how the proposed circuit is realized using quaternary Shift and M-S gates. In this design, quaternary Controlled Feynman gates have shown by red boxes.

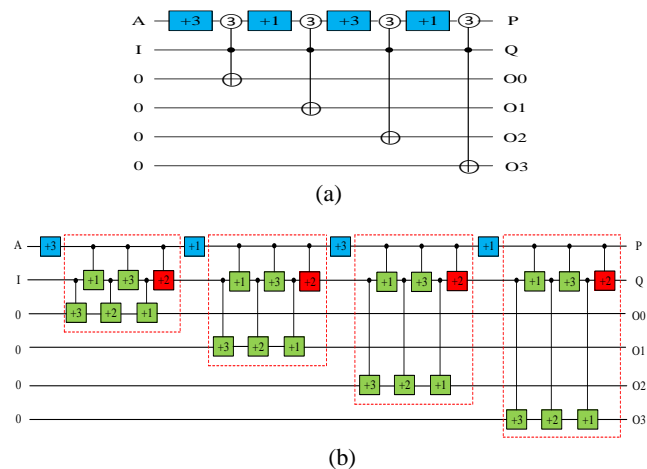


FIGURE 8. The proposed quaternary reversible  $1 \times 4$  demultiplexer circuit. a) Symbol. b) The realization using M-S and Shift gates.

Four quaternary 1-qudit Shift gates and twenty-four quaternary 2-qudit Muthukrishnan–Stroud gates are generally used. As a result, the quantum cost of the proposed quaternary

reversible  $1 \times 4$  demultiplexer circuit is 28. Considering that, in the multiplexer circuit, the input I does not need to be restored at the output Q, the red box can be removed, and the quantum cost is decreased by 24. In both cases, the number of constant inputs is four, and the number of garbage outputs is two.

We can also use our proposed quaternary  $1 \times 4$  demultiplexer to construct  $1 \times 16$  demultiplexer. In this kind of demultiplexer, one input, two selectors, and 16 outputs are needed. The truth table of this circuit is shown in Table VII. The input is gated to the selected output based on a given combination of selectors of A and B.

The logical architecture of the proposed quaternary reversible  $1 \times 16$  demultiplexer, using  $1 \times 4$  demultiplexer, is shown in Figure 9a. As can be seen, it requires five quaternary  $1 \times 4$  demultiplexers. In this design, when the selector A is equal to 0, the main input is gated on one of the outputs in the first demultiplexer. One output of the second multiplexer is gated when selector A is equal to 1. In the third and fourth multiplexers, one output is gated if selector A is equal to 2 and 3, respectively. When the input B is equal to 0, the first input of the second row demultiplexers is activated. If the input B is equal to 1, then the second input of demultiplexers is activated. Moreover, when B is equal to 2 and 3, demultiplexers' third and fourth inputs are activated, respectively.

The realization of the proposed quaternary reversible  $1 \times 16$  demultiplexer using  $1 \times 4$  demultiplexer is shown in Figure 9b. In the figure, red boxes show our proposed quaternary reversible  $1 \times 4$  demultiplexer. The main input is I, and it requires twenty constant inputs, which are 0. The selectors are A and B. The main outputs are O0 to O15, and it produces seven garbage outputs that are P1, P2, I, and from R0 to R3. The outputs P1 and P2 are equal to the selectors A and B, respectively. Generally, since input restoration is not necessary, the second realization of quaternary Controlled Feynman gates can be exploited. In this way, the proposed circuit includes 20 quaternary Shift gates and 100 quaternary Muthukrishnan–Stroud gates, and the quantum cost is 120.

We also could use a lower number of gates for designing the quaternary reversible  $1 \times 16$  demultiplexer and present a lower quantum cost demultiplexer circuit. The realization of the proposed optimized circuit is shown in Figure 9c. As can be seen, twenty quaternary Controlled Feynman gates and eight 1-qudit Shift gates are used. Since inputs restoration is not necessary, the second realization of quaternary Controlled Feynman gates is used, and there are eight quaternary Shift gates and 100 quaternary Muthukrishnan–Stroud gates in the proposed design, so the quantum cost is 108. Compared to our first proposed quaternary  $1 \times 16$  demultiplexer, we improved the quantum cost using this innovative combination. The numbers of constant inputs and garbage outputs for both realizations are 20 and 7, respectively.



TABLE VII  
THE TRUTH TABLE OF QUATERNARY 1×16 DEMULTIPLEXER

Selectors		Outputs														
AB	O0	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12	O13	O14	O15
00	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
01	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
02	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
03	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
30	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
31	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
33	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

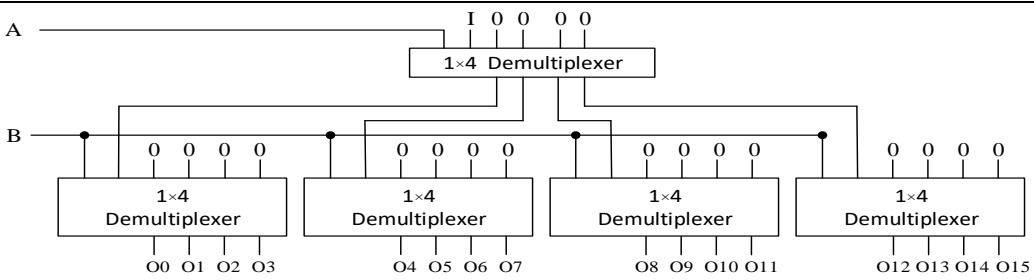


Fig.9-(a)

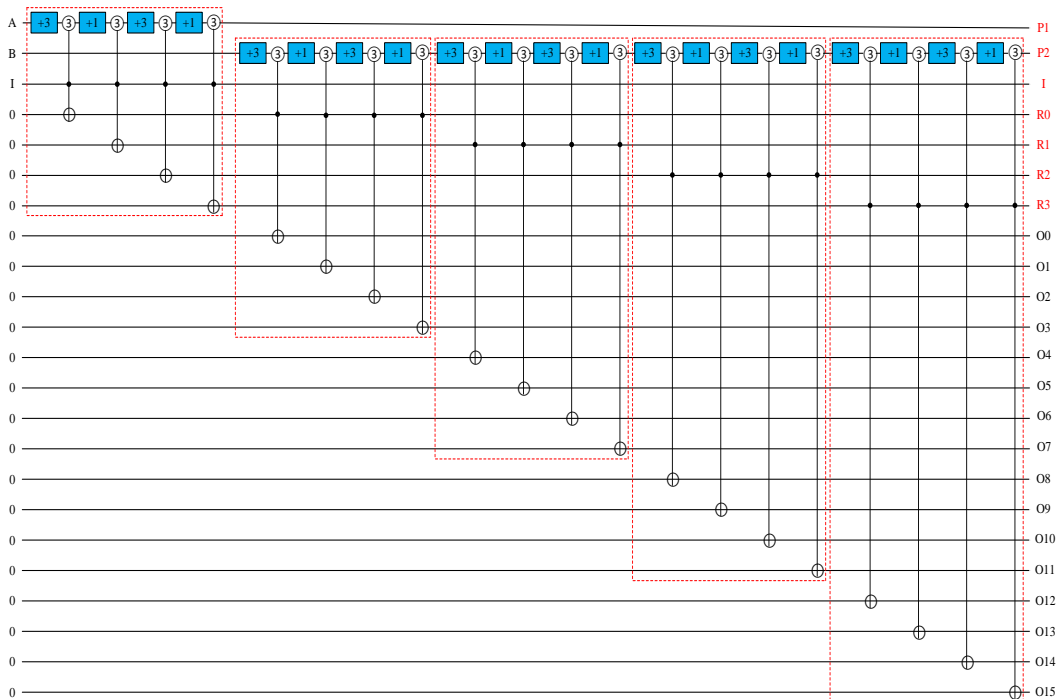


Fig.9-(b)

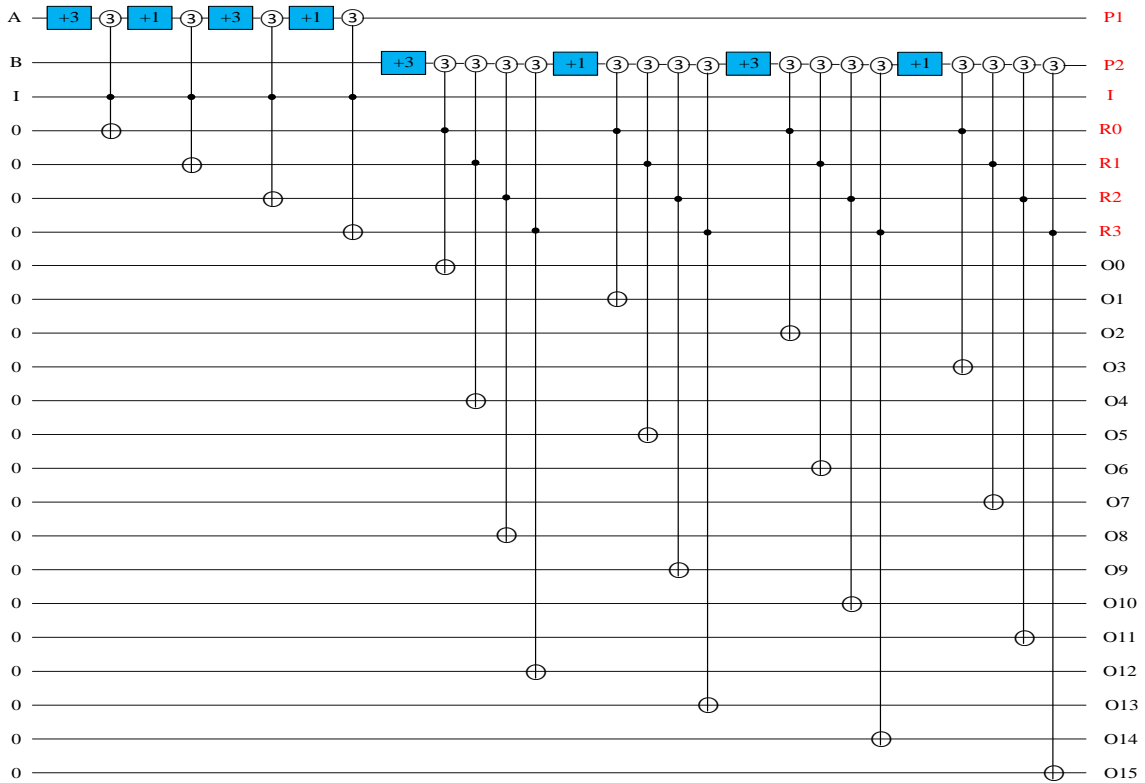


Fig.9-(c)

FIGURE 9. The proposed quaternary reversible 1x16 demultiplexer circuit. a) The logical representation. b) The primary realization. c) The optimized realization.

In addition, our proposed quaternary demultiplexer is scalable. A generalized quaternary reversible  $1 \times n$  demultiplexer circuit, based on quaternary reversible  $1 \times 4$  demultiplexer, is suggested. In a quaternary  $1 \times n$  demultiplexer circuit, there are one input,  $m$  selectors, and  $n = 4m$  outputs. Generally,  $m$  rows of  $1 \times 4$  demultiplexers are needed. It is necessary to use one demultiplexer in the first row, four demultiplexers in the second row, and  $4m - 1$  demultiplexers in the last row. Figure 10 shows the logical structure of the

proposed  $1 \times n$  demultiplexer. We also can use the geometric series formula to determine the number of  $1 \times 4$  demultiplexers that are needed to design our proposed  $1 \times n$  demultiplexer. Using (3), we can determine the number of demultiplexers, represented by  $Q$ .

$$Q = \sum_{i=0}^{m-1} 4^i = \frac{4^m - 1}{3} = \frac{n-1}{3} \quad (3)$$

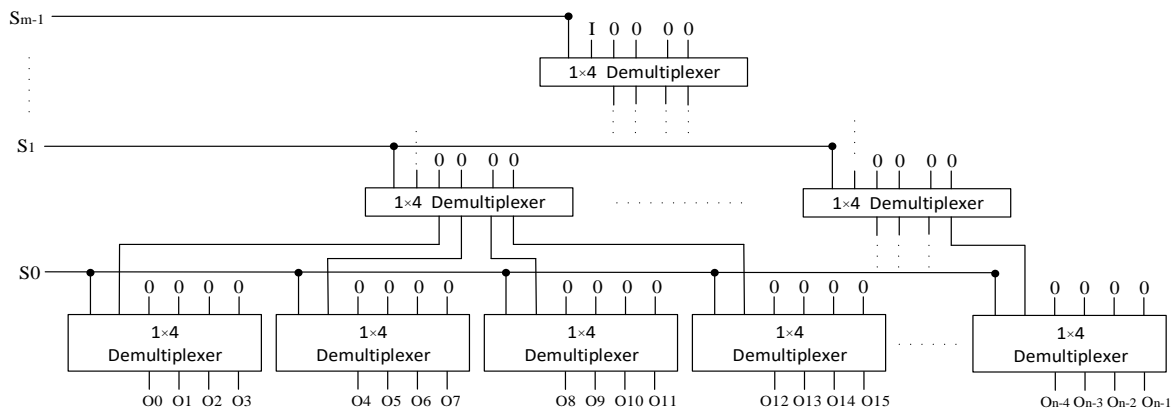


FIGURE 10. The logical architecture of the proposed quaternary reversible  $1 \times n$  demultiplexer circuit.

The proposed quaternary reversible  $1 \times n$  demultiplexer circuit requires  $4((n - 1)/3)$  constant inputs and produces  $(n + 3m - 1)/3$  garbage outputs, with a quantum cost of  $24((n - 1)/3)$ . Based on the optimization approach discussed in the previous section, the quaternary 1-qudit Shift gates in each row can be combined. As a result, each row contains four 1-qudit Shift gates. There are four and sixteen Controlled Feynman gates in the first and the second row, respectively, and  $4m - 1$  Controlled Feynman gates in the last row. Therefore, it can be concluded that there are  $4((n - 1)/3)$  Controlled Feynman gates and  $4m$  1-qudit Shift gates in the proposed quaternary reversible  $1 \times n$  demultiplexer, with  $n$  outputs and  $m$  selectors. Since we use the second realization of the Controlled Feynman gate, this optimized circuit has a total quantum cost of  $20((n - 1)/3) + 4m$ .

#### IV. RESULTS AND EVALUATIONS

In this section, we analyze our proposed realizations of quaternary reversible multiplexer and demultiplexer circuits and calculate the improvement rate with respect to the best results in the literature. We also compare the proposed circuits with the existing designs in [40-42] in terms of quantum cost, number of garbage outputs, and number of constant inputs, which are the most critical parameters in reversible circuit design and are used to evaluate reversible circuits. Lower values of these parameters lead to a more efficient circuit design.

In the following parts, the first comparison is for our proposed quaternary reversible demultiplexer, and the second comparison is for our proposed quaternary reversible demultiplexer. According to Table VIII, whereas both designs of quaternary reversible  $4 \times 1$  multiplexer circuits have the same number of garbage output and constant input, the proposed circuit outperforms the existing design presented in [41] in terms of quantum cost because of its lower values for this parameter. Table VIII also illustrates that our proposed quaternary reversible  $16 \times 1$  multiplexer circuit has great improvement in terms of quantum cost, the number of garbage outputs and the number of constant inputs compared with its counterparts in [40-42]. Therefore, it can be concluded that our proposed design of the  $16 \times 1$  multiplexer in this paper is also much more efficient than the previous designs in [40-42].

TABLE VIII  
EVALUATION OF QUATERNARY REVERSIBLE MULTIPLEXER CIRCUITS

	Quantum Cost	Constant Input	Garbage Output
Proposed $4 \times 1$ multiplexer	24	1	5
$4 \times 1$ multiplexer in [41]	70	1	5
Improvement percentage	65%	--	--
Proposed $16 \times 1$ multiplexer	108	5	22
$16 \times 1$ multiplexer in [42]	580	17	34
$16 \times 1$ multiplexer in [41]	368	8	25
$16 \times 1$ multiplexer in [40]	174	17	33
Improvement percentage	37%	37%	12%

Table IX shows the comparison between our proposed quaternary reversible  $1 \times 4$  demultiplexer and its counterpart in [41]. As can be seen, although both  $1 \times 4$  demultiplexer circuits require four constant inputs and produce two garbage outputs, our proposed design has a quantum cost of 24, and the demultiplexer realization in [41] has a quantum cost of 58. Owing to using lower values of quantum cost, our proposed quaternary reversible  $1 \times 4$  demultiplexer is more efficient than the existing design in [41]. The results given in Table IX show that our proposed quaternary reversible  $1 \times 16$  demultiplexer has 20 constant inputs, even garbage outputs, and a quantum cost of 108. It is obvious, by Table IX, that our proposed design has a less quantum cost, garbage output, and constant input than the previous designs in [40-42]. Since reversible circuits are more efficient when these parameters are minimized, the quaternary reversible  $1 \times 16$  demultiplexer in this study is more efficient than its counterparts in [40-42].

It is to be noted that there is no overhead in the proposed designs. One of the advantages of the proposed designs is that they have no overhead. In addition, the proposed approaches have applications in designing arithmetic circuits (e.g., ALU).

TABLE IX  
EVALUATION OF QUATERNARY REVERSIBLE DEMULTIPLEXER CIRCUITS

	Quantum Cost	Constant Input	Garbage Output
Proposed $1 \times 4$ demultiplexer	24	4	2
Existing $1 \times 4$ demultiplexer in [41]	58	4	2
Improvement percentage	58%	--	--
Proposed $1 \times 16$ demultiplexer	108	20	7
Existing $1 \times 16$ demultiplexer in [42]	580	32	19
Existing $1 \times 16$ demultiplexer in [41]	308	23	10
Existing $1 \times 16$ demultiplexer in [40]	174	33	20
Improvement percentage	37%	13%	30%

#### V. CONCLUSION

A new quaternary reversible  $4 \times 1$  multiplexer circuit, based on quaternary 1-qudit Shift gates, 2-qudit Muthukrishnan-Stroud, and 2-qudit Controlled Feynman gates, has been presented in this paper. The proposed  $4 \times 1$  multiplexer has been exploited to design a quaternary reversible  $16 \times 1$  multiplexer circuit. The proposed design is scalable for  $n \times 1$  multiplexer. Moreover, we have introduced a new scalable realization of  $1 \times 4$  demultiplexer to design our proposed quaternary reversible  $1 \times 16$  and  $1 \times n$  demultiplexers. The proposed quaternary reversible circuits in the present study significantly decrease quantum cost, the number of constant inputs, and the number of garbage outputs. Since designing a reversible circuit with lower values of these parameters leads to increased efficiency, it can be concluded that our proposed multiplexer and demultiplexer circuits are more efficient with respect to their existing counterparts. Our designs have no

overhead compared to the existing designs to be reported. An interesting future work is the study of possible applications of our proposed circuits in designing complex systems.

## CONFLICT OF INTEREST

The authors declare no conflicts of interest.

## REFERENCES

- [1] R. Landauer, "Irreversibility and heat generation in the computing process," *IBM journal of research and development.*, vol. 5, no. 3, pp. 183-191, Jul. 1961.
- [2] V. V. Zhirmov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling-a gedanken model," *Proceedings of the IEEE.*, vol. 91, no. 11, pp. 1934-1939, Nov.2003.
- [3] C. H. Bennett, "Logical reversibility of computation," *IBM journal of Research and Development.*, vol.17, no. 6, pp. 525-532, Nov. 1973.
- [4] M. Perkowski, L. Jozwiak, P. Kerntopf, A. Mishchenko, A. Al-Rabadi, A. Coppola, and M. H. A. Khan, "A general decomposition for reversible logic," Aug. 2001,
- [5] M. Perkowski, and P. Kerntopf, "Reversible logic," Invited tutorial. *Proc. Euro-Micro.*, Sep 2001.
- [6] A. Mishchenko, and M. Perkowski, Logic synthesis of reversible wave cascades. *International Workshop on Logic and Synthesis*, New Orleans, Louisiana, June. 2002.
- [7] M. Sultana, A. Chaudhuri, D. Sengupta, A. Chaudhuri, "Toffoli Netlist and QCA implementations for existing four variable reversible gates: a comparative analysis," *Microsystem Technologies*, vol. 25, no. 5, pp. 1987-2009, May. 2019.
- [8] M. A. Nielson, and I. L. Chuang, "Quantum computation and quantum information," Cambridge University Press, vol.2, no. 8, pp.23, 2000.
- [9] L. K. Grover, "A fast quantum mechanical algorithm for database search," In *Proceedings of the twenty-eighth annual ACM symposium on Theory of computing*, Jul 1996, pp. 212-219.
- [10] M. Boyer, G. Brassard, P. Hoyer, and A. Tapp, "Tight bounds on quantum searching," *Fortschritte der Physik: Progress of Physics*, vol. 46, no. 4-5, pp. 493-505, Jun. 1998.
- [11] C. Zalka, "Grover's quantum searching algorithm is optimal," *Physical Review A.*, vol. 60, no. 4, pp. 2746, Oct. 1999.
- [12] Z. T. Sandhie, J. A. Patel, F. U. Ahmed, and M. H. Chowdhury, "Investigation of multiple-valued logic technologies for beyond-binary era," *ACM Computing Surveys (CSUR).*, vol. 54, no. 1, pp. 1-30, Jan. 2021.
- [13] H. Bechmann-Pasquinucci, and A. Peres, "Quantum cryptography with 3-state systems," *Physical Review Letters.*, vol. 85, no. 15, pp. 3313, Oct. 2000.
- [14] M. Bourennane, A. Karlsson, and G. Björk, "Quantum key distribution using multilevel encoding," *Physical Review A.*, vol. 64, no. 1, pp. 012306, Jun. 2001.
- [15] R. W. Spekkens, and T. Rudolph, "Degrees of concealment and bindingness in quantum bit commitment protocols," *Physical Review A.*, vol. 65, no. 1, pp. 012310, Dec. 2001.
- [16] A. D. Greentree, S. G. Schirmer, F. Green, L. C. Hollenberg, A. R. Hamilton, and R. G. Clark, "Maximizing the Hilbert space for a finite number of distinguishable quantum states," *Physical review letters.*, vol. 92, no. 9, pp. 097901, Mar. 2004.
- [17] D. Bundalo, Z. Bundalo, and B. Đorđević, "Design of quaternary logic systems and circuits," *Facta universitatis-series: Electronics and Energetics.*, vol. 18, no. 1, pp. 45-56. 2005.
- [18] E. Knill, "Fault-tolerant postselected quantum computation: Schemes," Feb 2004, arXiv preprint quant-ph/0402171.
- [19] D. M. Miller, and M. A. Thornton, "Multiple valued logic: Concepts and representations," *Synthesis lectures on digital circuits and systems.*, vol. 2, no. 1, pp. 1-127, Jan. 2007.
- [20] M. A. Asadi, M. Mosleh, and M. Haghparast, "Towards designing quantum reversible ternary multipliers," *Quantum Information Processing.*, vol. 20, no. 7, pp. 1-27, Jul. 2021.
- [21] M. A. Asadi, M. Mosleh, and M. Haghparast, "Toward novel designs of reversible ternary 6: 2 Compressor using efficient reversible ternary full-adders," *The Journal of Supercomputing.*, vol. 77, no. 5, pp. 5176-5197. May. 2021.
- [22] M. A. Asadi, M. Mosleh, and M. Haghparast, "A novel reversible ternary coded decimal adder/subtractor," *Journal of Ambient Intelligence and Humanized Computing.*, vol. 12, no. 7, pp. 7745-7763, Jul. 2021.
- [23] M. M. Panahi, O. Hashemipour, and K. Navi, "A novel design of a multiplier using reversible ternary gates," *IETE Journal of Research.*, vol. 67, no. 6, pp. 744-753, Nov. 2021.
- [24] S. M. Ghadamgahi, R. Sabbaghi-Nadooshan, and K. Navi, "Novel ternary adders and subtractors in quantum cellular automata," *The Journal of Supercomputing.*, pp. 1-43. Jun. 2022.
- [25] M. Haghparast, R. Wille, and A. T. Monfared, "Towards quantum reversible ternary coded decimal adder," *Quantum Information Processing.*, vol. 16, no. 11, pp. 1-25, Nov. 2017.
- [26] M. Ilyas, S. Cui, and M. Perkowski, "Ternary Logic Design in Topological Quantum Computing," Apr 2022, arXiv preprint arXiv:2204.01000.
- [27] P. Mercy Nesa Rani, and P. L. Thangkhiew, "An Overview of Different Approaches for Ternary Reversible Logic Circuits Synthesis Using Ternary Reversible Gates with Special Reference to Virtual Reality," *Advances in Augmented Reality and Virtual Reality.*, pp. 73-90. Jan. 2022.
- [28] A. T. Monfared, and M. Haghparast, "Quantum ternary multiplication gate (QTMG): toward quantum ternary multiplier and a new realization for ternary toffoli gate," *Journal of Circuits, Systems and Computers*, vol. 29, no. 05, pp. 2050071, Apr. 2020.
- [29] S. M. Ghadamgahi, R. Sabbaghi-Nadooshan, and K. Navi, "Novel single-trit comparator circuits in ternary quantum-dot cellular automata," *Analog Integrated Circuits and Signal Processing.*, vol. 111, no. 3, pp. 353-370, Jun. 2022.
- [30] G. Chen, Y. Wang, L. Jian, Y. Zhou, and S. Liu, "Ternary Quantum Key Distribution Protocol Based on Hadamard Gate," *International Journal of Theoretical Physics.*, vol. 61, no. 2, pp. 1-13, Feb. 2022.
- [31] M. M. M. Khan, A. K. Biswas, S. Chowdhury, M. Tanzid, K. M. Mohsin, M. Hasan, and A. I. Khan, "Quantum realization of some quaternary circuits," In *TENCON 2008-2008 IEEE Region 10 Conference*, Nov. 2008, pp. 1-5). IEEE.
- [32] M. H. Khan, "Synthesis of quaternary reversible/quantum comparators," *Journal of Systems Architecture.*, vol. 54, no. 10, pp. 977-982. Oct. 2008.
- [33] A. Taheri Monfared, M. Haghparast, and K. Datta, "Quaternary quantum/reversible half-adder, full-adder, parallel adder and parallel adder/subtractor circuits," *International Journal of Theoretical Physics.*, vol. 58, no. 7, pp. 2184-2199. Jul. 2019.
- [34] M. Haghparast, and A. T. Monfared, "Designing novel quaternary quantum reversible subtractor circuits," *International Journal of Theoretical Physics.*, vol. 57, no. 1, pp. 226-237. Jan. 2018.
- [35] M. H. Khan, "A recursive method for synthesizing quantum/reversible quaternary parallel adder/subtractor with look-ahead carry," *Journal of Systems Architecture.*, vol. 54, no. 12, pp. 1113-1121, Dec. 2008.
- [36] A. Norouzi Doshanlou, M. Haghparast, and M. Hosseinzadeh, "Novel quaternary quantum reversible half adder and full adder circuits," *IETE Journal of Research.*, vol. 68, no. 2, pp. 1525-1531. Mar. 2022.
- [37] A. Norouzi Doshanlou, M. Haghparast, M. Hosseinzadeh, and M. Reshadi, "Efficient binary to quaternary and vice versa converters: embedding in quaternary arithmetic circuits," *The Journal of Supercomputing.*, vol. 77, no. 12, pp. 14600-14616, Dec. 2021.
- [38] A. Raja, K. Mukherjee, J. N. Roy, "Design of dual semiconductor optical amplifier structure based all-optical standard quaternary inverter and quaternary clocked SR flip-flop," *Optical and Quantum Electronics.*, vol. 54, no. 1, pp. 1-23, Jan. 2022.

[39] A. Navidi, R. Sabbaghi-Nadooshan, M. Dousti, "Introducing an Innovative D Flip-Flop for Designing Quaternary QCA Register," *Journal of Intelligent Procedures in Electrical Technology.*, vol. 13, no. 49, pp. 91-101, May. 2022.

[40] M. Haghparast, and A. Taheri Monfared, "Novel quaternary quantum decoder, multiplexer and demultiplexer circuits," *International Journal of Theoretical Physics.*, vol. 56, no. 5, pp. 1694-1707, May. 2017.

[41] M. H. Khan, "Scalable architectures for design of reversible quaternary multiplexer and demultiplexer circuits," In 2009 39th International Symposium on Multiple-Valued Logic, May 2009, pp. 343-348. IEEE

[42] M. H. Khan, "Reversible realization of quaternary decoder, multiplexer, and demultiplexer circuits," In 38th International Symposium on Multiple Valued Logic (ISMVL 2008), May 2008, pp. 208-213. IEEE

[43] M. Mohammadi, and M. Eshghi, "Heuristic methods to use don't cares in automated design of reversible and quantum logic circuits," *Quantum Information Processing.*, vol. 7, no. 4, pp. 175-192, Aug. 2008.

[44] D. Maslov, and G. W. Dueck, "Garbage in reversible design of multiple output functions," In 6th International Symposium on Representations and Methodology of Future Computing Technologies, Mar 2003, pp. 162-170.

[45] S. Lee, S. J. Lee, T. Kim, J. S. Lee, J. Biamonte, and M. Perkowski, "The Cost of Quantum Gate Primitives," *Journal of Multiple-Valued Logic & Soft Computing.*, vol. 12, no. 5-6, pp. 561-574, Aug. 2006.

[46] M. H. Khan, and M. A. Perkowski, (2007, May). "GF (4) based synthesis of quaternary reversible/quantum logic circuits," In 37th International Symposium on Multiple-Valued Logic (ISMVL'07), May 2007, pp. 11-11). IEEE.

[47] A. Muthukrishnan, and C. R. Stroud Jr, "Multivalued logic gates for quantum computation," *Physical review A.*, vol. 62, no. 5, pp. 052309, Oct. 2000.

[48] M. H. Khan, and H. Thapliyal, "Reversible logic-based mapping of quaternary sequential circuits using QGFSOP expression," In 2015 IEEE Computer Society Annual Symposium on VLSI, Jul 2015, pp. 297-302. IEEE.

[49] M. H. Khan, H. Thapliyal, and E. Munoz-Coreas, "Automatic synthesis of quaternary quantum circuits," *The Journal of Supercomputing.*, vol. 73, no. 5, pp. 1733-1759, May. 2017.

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