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Title: Technology Impact on Neutron-Induced Effects in SDRAMs : A Comparative Study

Year: 2021

Version: Accepted version (Final draft)

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Please cite the original version:

Matana Luza, L., Söderström, D., Pio de Mattos, A. M., Bezerra, E. A., Cazzaniga, C., Kastriotou, M., Poivey, C., & Dilillo, L. (2021). Technology Impact on Neutron-Induced Effects in SDRAMs : A Comparative Study. In DTIS 2021 : Proceedings of the 16th IEEE International Conference on Design and Technology of Integrated Systems in Nanoscale Era. IEEE.
<https://doi.org/10.1109/DTIS53253.2021.9505143>

Technology Impact on Neutron-Induced Effects in SDRAMs: A Comparative Study

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Abstract

This study analyses the response of synchronous dynamic random access memories to neutron irradiation. Three different generations of the same device with different node sizes (63, 72, and 110 nm) were characterized under an atmospheric-like neutron spectrum at the Chiplr beamline in the Rutherford Appleton Laboratories, UK. The memories were tested with a reduced refresh rate to expose more single-event upsets and under similar conditions provided by a board specifically developed for this type of study in test facilities. The board has also been designed to be used as a nanosatellite payload in order to perform similar tests. The neutron-induced failures were studied and characterized, presenting the occurrence of single-bit upsets and stuck bits. The cross sections for each type of event and technology node show that the 110 nm model is more sensitive to neutron-induced single-event effects than the other models.

Index Terms

Neutrons, Radiation Effects, SDRAM, SEE, Stuck Bits

I. INTRODUCTION

When designing electronic devices, the consideration of radiation effects is fundamental for applications in harsh environments. For instance, in avionics systems, these effects are extensively studied to ensure high reliability of the system components and provide the required insight for important design decisions.

As the technology nodes get smaller and components more integrated [1], testing components for radiation-induced effects becomes an important issue. Relevant radiation effects might differ when considering different node sizes as, for instance, Single Event Effects (SEE) by direct ionization from protons [2], [3], which is of increasing importance for smaller technology nodes.

This study investigates the radiation effects in three different memory generations of the same Synchronous Dynamic Random Access Memory (SDRAM), each memory model with a different technology node size. The devices were characterized under irradiation with an atmospheric-like neutron spectrum. Other studies have characterized these memory chips under different particle and energy spectra [4], [5], providing knowledge of the behaviour of these devices under harsh radiation conditions.

The approach adopted for this work consists of the comparison of the devices' neutron-induced failures, providing an assessment of the memories' resilience across the different generations. In order to ensure a comparable scenario, the memories were exposed simultaneously under the effective beam area using the same controller board, which assigns similar electrical and behavioural characteristics. During the experiment, static and dynamic test algorithms were run to acquire the location and number of the faults. Also, a round-robin strategy was adopted, which executed static and dynamic tests on the different memories with a rotating schedule to optimize the beam time utilization during each run.

Previous studies have revealed that the memory cells in DRAMs are susceptible to different types of radiation-induced upsets, including Single Event Upsets (SEU), Single Event Latch-up (SEL), Single Event Functional Interrupt (SEFI), and stuck bits [6]. Stuck bits have also been studied in e.g. [7]–[10]. Studies on stuck bits have been made using different types of particle irradiation, including protons and neutrons [11], [12], heavy ions [13], and electrons [5].

This study has been achieved thanks to the financial support of the VAN ALLEN Foundation (Contract No. UM 181387), the Region Occitanie (Contract No. UM 181386), and from the European Union's Horizon 2020 Research and Innovation Programme under the Grant Agreement No 721624 through the RADSAGA ITN.

The stuck bits do often have an intermittent behaviour, where the memory cells have a variable retention time [12], [14].

The main objective of this study is to evaluate the radiation impact on a memory chip across the different generations of fabrication. The paper is organised as follows: Section II presents the Devices Under Test (DUTs), the test facility, the experimental setup and the applied test methodologies; Section III presents and analyzes the results from the irradiation test campaign; Section IV provides the final remarks.

II. EXPERIMENTAL TEST SETUP

A. Devices Under Test

The tested devices in this study are different generations of a memory device produced by ISSI, using different manufacturing node sizes: 110 nm for IS42S16320B [15], 72 nm for IS42S16320D [16], and 63 nm for IS42S16320F [17]. The memories are Single Data Rate (SDR) SDRAMs, with 536,870,912 bits organized on four banks with 8192 rows and 1024 columns of 16 bits. The maximum operating frequency is 143 MHz, with a 3.3 V input supply voltage, and packaged in 54-pin TSOP-II packages. The tested components are summarized in Table I.

TABLE I
SUMMARY OF SPECIMEN USED IN THE EXPERIMENTS.

Memory	Node size (nm)	DUT IDs
IS42S16320B	110	B1, B2
IS42S16320D	72	D1, D2
IS42S16320F	63	F1, F2

These devices were mounted in a tailored platform, designed to be used for experimental evaluation in test facilities and ready for actual space environment missions. This approach was adopted to extend the study of these memories from a ground-based analysis, more intrusive and broad, to a space assessment, the actual targeted environment. For this reason, the development of a tailored platform was required, leading to the board presented in Fig. 1 (known as *Harsh Environment CubeSat Payload* and herein referred to as “HARSH”).

The HARSH board architecture consists of the main controller, a Microsemi system-on-a-chip FPGA (SmartFusion2 M2S025), and the SDRAM chips themselves integrated with a small form factor 6-layers PCB. Also, there are latch-up monitors for each memory and interfaces for integration with a CubeSat platform. The board uses the FloripaSat [18] missions payload standard, targeting the FloripaSat-2 [19] mission scheduled to launch in 2022, and follows a simplified space application design guideline.

The main design considerations and objectives were to produce a reliable platform with commercial off-the-shelf (COTS) components and reasonable development efforts. In order to provide the most accurate results, the memories should have the most similar parameters and test conditions. To accomplish that, the other components on the HARSH board were selected due to their known degree of radiation sensitivity [20] and the board layout followed the applicable space-related criteria proposed by ESA guidelines (ECSS-Q-ST-70-12C). The guideline was not entirely fulfilled due to the proposed application scope of the HARSH board, resulting in a similar approach discussed in [21].

B. Test Facility

The test campaign [22] was carried out at the Rutherford Appleton Laboratories, UK, using the Chiplr beamline at the ISIS Neutron and Muon Source. The beamline is dedicated to the study of single event effects on electronics, and it is designed to provide an atmospheric-like neutron spectrum. The neutron flux is about 5×10^6 n/cm²/s for energies above 10 MeV, with also a thermal neutron component for lower energies (less than 0.5 eV) with a flux of 4×10^5 n/cm²/s. During irradiation a beam window of 20 cm × 7 cm was used (see Fig. 3). More details about the beamline can be found in [23]–[25].

C. Test Procedures and Setup

A schematic diagram of the test setup is shown in Fig. 2. The power supplied to the board was monitored in order to identify SELs. The run-time tests results were logged through a serial port with the logical addresses, error data per address, error flags and operation status. Functional tests of the memory controller were performed between the runs to ensure proper functionality during the experiment sessions.

During each experiment session, the memories were tested with static and dynamic routines using a round-robin strategy to optimize the time utilization. This test procedure is as follows: one memory is under a dynamic routine

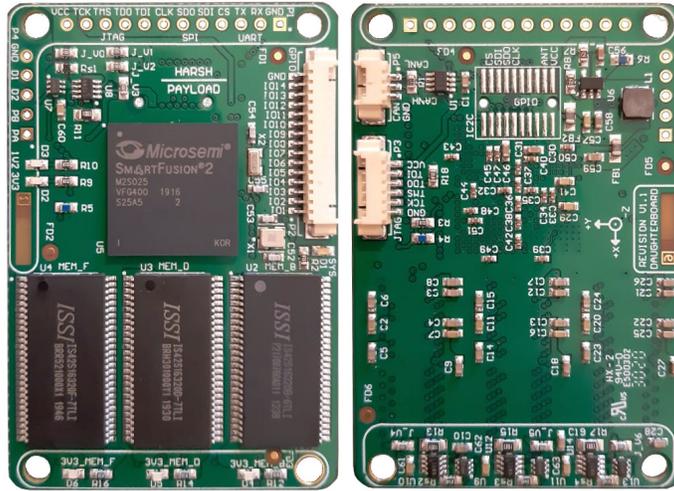


Fig. 1. Top and bottom view of the HARSH board.

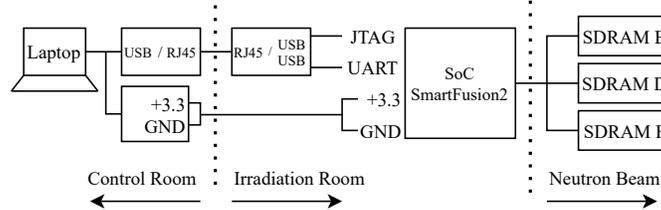


Fig. 2. Schematic diagram of the experimental setup used for exposing the DUT under the beam and acquiring the logs from the board to a remote computer.

per run in a session, while the other two memories are subjected to static routines. After a run of sufficient neutron fluence, the memories shift the routines being executed. This approach distributes dynamic and static tests over the three samples.

The nominal refresh rate of the memories is 8192 refresh operations every 64 ms (which corresponds to sending an auto-refresh command at a frequency of 128 kHz). In these tests, a lower refresh frequency was used to detect a higher number of errors and increase the statistics of the tests. This is discussed, e.g., in [26], so that a lowering of refresh frequency could be used to simulate an increase in temperature, where the memories are more susceptible to radiation-induced errors [27], [28]. In the experiments described in this paper, an auto-refresh command frequency of 6.1 kHz was used throughout all irradiations and characterizations, corresponding to each bit being refreshed at intervals of 1.34 s. No errors were present in the pristine memories at this refresh rate.

Due to the shared utilization of the beamline with other experiments, only one HARSH board was evaluated for a given session, and two identical HARSH boards (using memories of the same manufacturing lots) were used during the test campaign. The memories were positioned in the beam in a way to ensure full coverage by the neutron field while keeping the controlling systems on the board outside the beam. The setup in the beam is presented in Fig. 3. The local environment was at room temperature.

D. Test Modes

The evaluation of the three memories is based on the execution of two different test modes: static and dynamic mode. In static mode, the memories are written with a known data pattern (e.g., solid '0', solid '1', or checkerboard patterns), and the devices are exposed to the radiation during a time interval to reach a defined fluence. Afterwards, the memories' contents are read back, and the corrupted bits are sent to a host computer as error frames. These error frames are logged as described in II-C.

Previous studies on the DUTs have shown that the mechanism of Single-Bit Upsets (SBUs) and stuck bits are suggested to be the same: degradation of the retention time capabilities of the cells [5] at different degree. Then, the procedure described in Fig. 4 was applied to understand if a read performed just after a write operation could

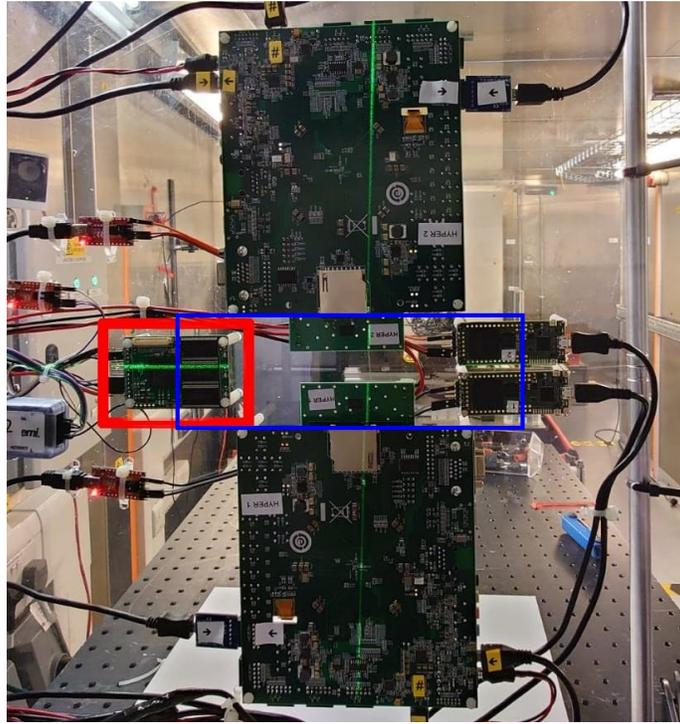


Fig. 3. Test boards fixed in a shared mounting frame ready for the experiment. The HARSH board is in the red rectangle, and the approximate beam window is marked with a blue rectangle.

sensitize a fault. The procedure is composed of a read operation, herein referred to as ‘s1’, which has the objective to identify the expected faults (SBUs and stuck bits). When an error is detected in ‘s1’, a read-write-read operation is performed in the faulty address. The read ‘s2’ is performed to confirm the error in the memory cell, and then write-read accesses are executed to identify the retention capability of the cell since every operation in a DRAM cell refreshes its value. The read ‘s3’ would identify a fault that is not related to degradation on the retention capability of the cell but permanent damage to its structure.

```

1: procedure READ RETENTION(pattern)
2:   for addr = startaddr to endaddr do
3:     data ← sdram_read(addr) ▷ s1
4:     if data ≠ pattern then save_error_frame()
5:       data ← sdram_read(addr) ▷ s2
6:       if data ≠ pattern then save_error_frame()
7:       end if
8:       sdram_write(addr, pattern)
9:       data ← sdram_read(addr) ▷ s3
10:      if data ≠ pattern then save_error_frame()
11:      end if
12:    end if
13:  end for
14: end procedure

```

Fig. 4. Read retention procedure

In dynamic mode, the memory is constantly accessed through read and write operations. This approach enables the detection of functional faults and emulates a more close to a real application [29], [30]. For this purpose, the March C- (1) was applied. In (1), the arrow indicates the addressing order (‘↑’ up or ‘↓’ down), ‘w’ (write), and ‘r’ (read) indicates the operation, and the following Boolean number indicates the data background. Each element enclosed by the parenthesis is applied to the entire address space before proceeding to the following one; the complete dynamic

algorithm is delimited by a bracket pair [31].

$$\{\uparrow(w0); \uparrow(r0, w1); \uparrow(r1, w0); \downarrow(r0, w1); \downarrow(r1, w0); \uparrow(r0); \} \quad (1)$$

III. RESULTS

The DUTs were exposed to the atmospheric-like neutron beam reaching a cumulative fluence of neutrons over 10 MeV of $\approx 1.3 \times 10^{12}$ n/cm² on the DUTs B1, D1 and F1, and $\approx 7.2 \times 10^{11}$ n/cm² on the DUTs B2, D2 and F2. Considering the Chiplr average neutron flux, we had ≈ 113 h of experiments.

Two different types of faults were observed during the irradiation of the memories. The first type was SBU (bit-flip), which manifested as one faulty read of a bit address during the tests, where the bit remained operational after rewriting the memory cell. The other type was stuck bit, which was a bit that returned a faulty value multiple times, even after being rewritten.

The stuck bits were, in general, intermittently stuck, not necessarily having many repetitions of returning a faulty value after rewriting. Therefore, all bits which experienced more than one error were categorized as stuck.

An example of the behaviour of the stuck bits can be seen in Fig. 5, where the detected errors in 7-bit addresses are shown for the tests on the DUT B1.

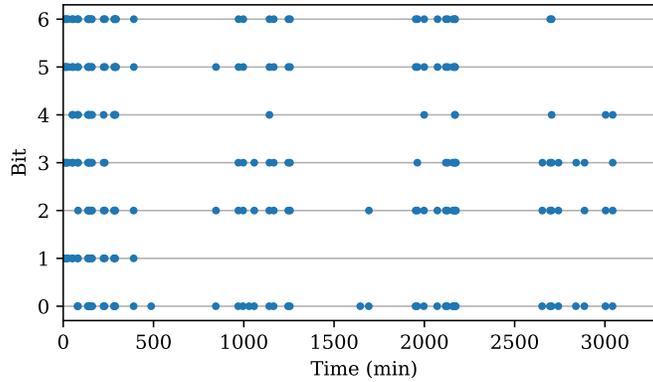


Fig. 5. Timeline plot from a portion of stuck bits in memory B1. The bits are numbered as 0 - 6, and each row shows the behaviour of one bit along with the test campaign.

To evaluate the memory sensitivity to the presented errors, the fault types were divided into SBUs and stuck-at bits. The event cross section (σ) was calculated as

$$\sigma = \frac{N}{F \times M} \quad (2)$$

where N is the number of events, F is the cumulative fluence in particles/cm², and M is the number of bits [32]. The calculated cross section for stuck bits is shown in Fig. 6, and Fig. 7 presents the calculated cross section for SBUs. The error bars in the figures represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

During irradiation, bytes containing two upset bits were also observed. Bytes with two upsets at one occasion are here called 2-BUs (two-bit upsets), and the cross section for this type of event is shown in Fig. 8. This was only observed for two bytes in device B2.

Bytes which repeatedly contained two bits in error were more common and were observed in four of the tested devices. The cross section for this error mode is presented in Fig. 9.

Common among the bytes that have two bits in error is that one or both of the bits also had either one error (registered as SBU) or multiple errors (stuck bit), apart from being registered as having errors simultaneously. These bits have thus not likely been affected by the same incident particle, but rather they are stuck and intermittently stuck bits that accumulate and happen to be in the same byte of the memory.

An example of the pattern of how the two bits in one of the words are intermittently stuck is shown in Fig. 10. In the figure, a bit is shown as stuck if the individual bit has an error during a test (static or dynamic) and unstuck if it has no upsets for the test duration. It can be seen that often only one of the bits has upsets, and occasionally both have upsets at the same time. The shown example is from sample B1.

Since a certain Error Detection and Correction (EDAC) algorithms can handle one error, but not two, per byte, so the bytes containing two stuck or upset bits represent a more critical error than the singly stuck or upset. The

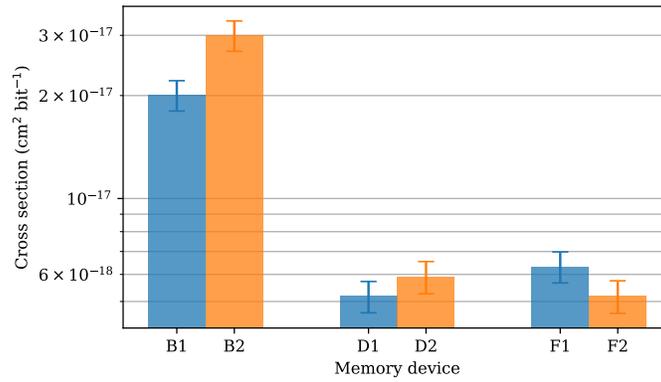


Fig. 6. Stuck bit cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

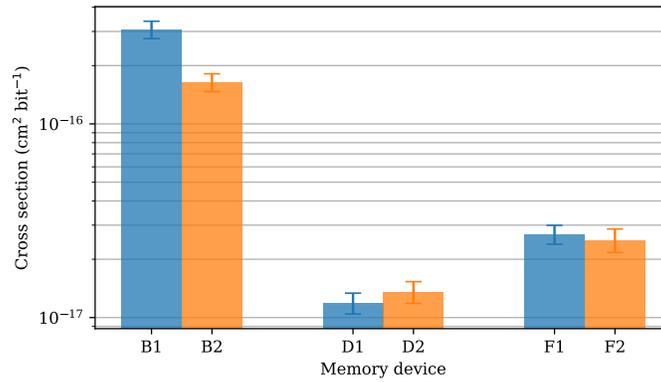


Fig. 7. SBU cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

error cross section for this and the other fault modes are, of course, higher in these figures due to the low refresh frequency used during the tests than if the nominal refresh frequency would have been used.

Analysis from the *Read Retention* procedure (described in Fig. 4) show that SBUs and stuck bits were spotted only in the states 's1' and 's2'. The state 's3' did not return an error in the memory cells. It happens as the write-read operations are performed one after the other, without a time interval (besides the one imposed by the controller part of the system), and also, each operation in the memory cell (i.e., write, read or refresh) restores the cells capacitor charge. The fact that no errors were observed in state 's3' is in line with the SBUs and stuck bit fault mechanism. It suggests that there is a degradation of the retention time of the cells and shows that the cell, even with a degraded retention capability, can retain the charge for a minimum time.

A further evaluation was performed after irradiation in the memories B2, D2 and F2. A write-read operation was performed with both solid data patterns. It is a procedure that enables the identification of stuck bits after the test. Also, using a nominal refresh rate, the same operation was performed, showing a significant decrease in the number of stuck bits, which is directly related to the fault mechanism. The results are presented in Table II.

TABLE II
NUMBER OF STUCK BITS AFTER IRRADIATION ACCORDING THE REFRESH RATE.

DUT ID	Node Size	Refresh Rate			
		6.1 kHz		128 kHz	
		Solid '0'	Solid '1'	Solid '0'	Solid '1'
B2	110 nm	7611	7954	32	48
D2	72 nm	786	876	1	2
F2	63 nm	589	631	0	0

Furthermore, during the tests, the current was monitored by the latch-up monitors, which did not spot any occurrence of SELs.

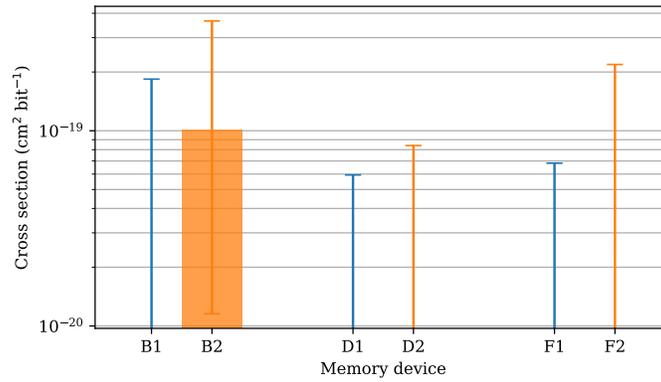


Fig. 8. 2-BU cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

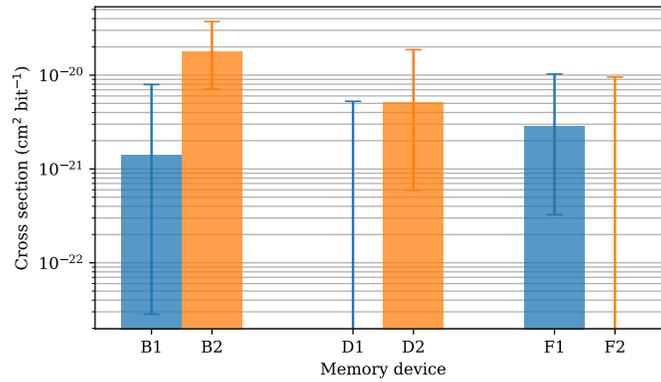


Fig. 9. 2-Stuck bits cross section for each DUT. The error bars represent a 95 % confidence interval with a 10 % beam fluence uncertainty.

A. Comparison among the different technology nodes

Comparing the results obtained for the different device types B, D and F, what can be seen is that type B is more sensitive than the others regarding SBUs and stuck bits. However, the other two device types D and F, with node sizes 72 nm and 63 nm respectively, have very little difference in their sensitivity, with type F even showing a slightly increased SBU cross section over type D in Fig. 7.

The differences between the sensitivity of the memory devices are likely affected by other design changes in the devices than just the change of node size since the sensitivity evolution is not following a visible trend with the technology node scaling. This is shown on Fig. 11, which presents the combined SBU and stuck bit cross sections for each tested device model. In between two consecutive generations of technology nodes, there are effects coming from architectural and material improvements that tend to reduce the neutron-induced effects and other parasitic phenomena. On the other hand, the technology shrinking might lead to a higher radiation sensitivity for the individual cells. On this basis, we can consider that the transition from model B to D, the architecture and material improvement had a larger effect than the shrinking. Also, since model B has the largest node size at 110 nm, the higher sensitivity and error cross section could be related to this memory having a larger cross sectional area of the sensitive volume due to the larger node size. For the transition from D to F, the shrinking seems to be slightly stronger than the architectural and material improvements (if any). The exact changes in the structure and design of the memories between models are, however, not known to the authors.

IV. CONCLUSION

In this paper, a comparative study on the neutron-induced effects on three different technology node SDRAMs is presented. From the realised tests, the induced effects were analysed, leading to the identification of SBUs, and intermittently stuck bits. Also, on very specific occasions, we identified the occurrence of two bit-flips or two stuck bits in a single byte.

The cross sections for the different kinds of faults were estimated for each DUT, showing that the difference in radiation sensitivity between the three different memory types seems to come not only from the technology node sizes but also from other changes in the design between the different memory generations.

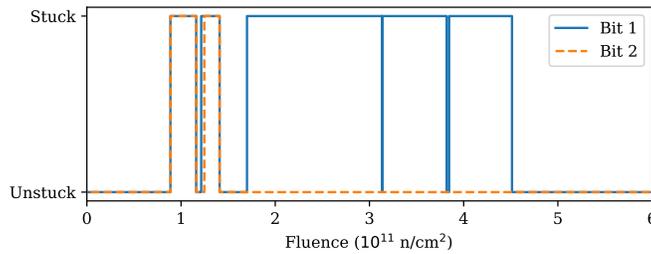


Fig. 10. Intermittent stuckness pattern of two bits within the same memory byte

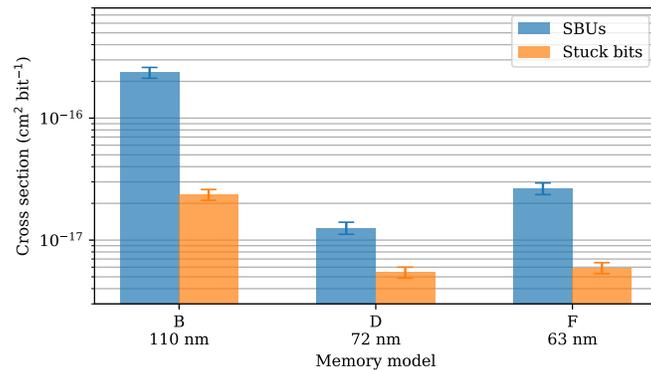


Fig. 11. The SBU and stuck bit cross sections for the tested devices as a function of the technology node size. The cross section at each point is the combined for the two tested samples of each model.

Future studies of these memories using the HARSH board setup is planned and will include tests at different radiation sources, refresh frequencies, and studies of annealing of the radiation-induced stuck bits.

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