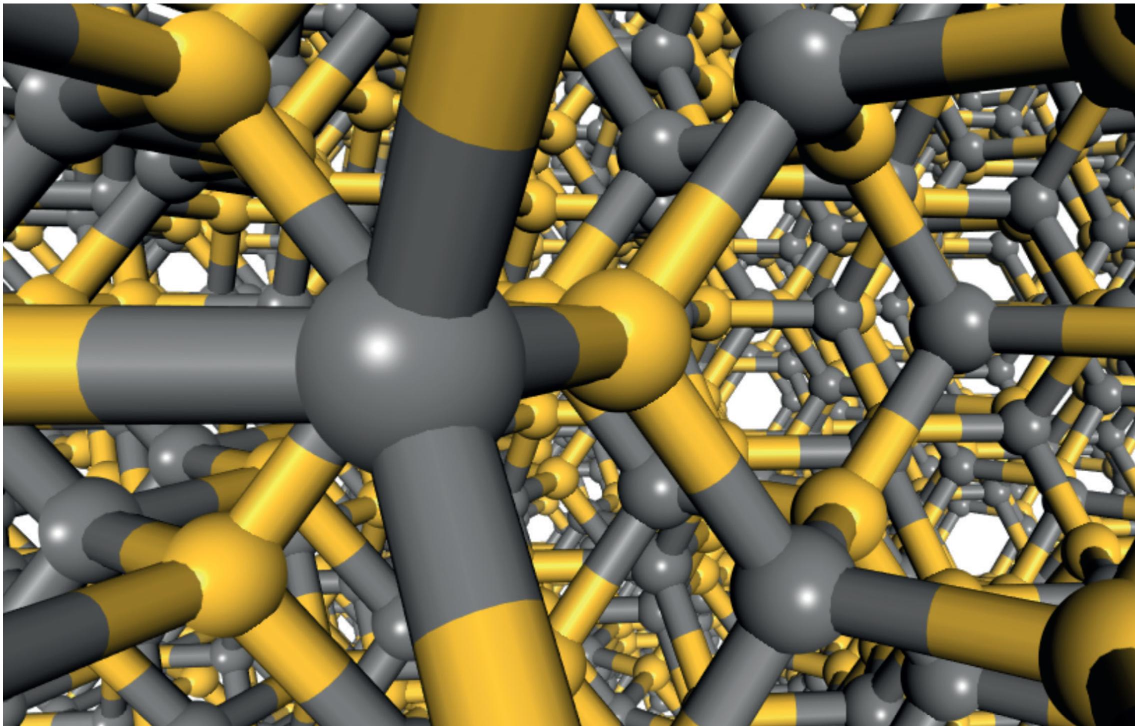
JYU DISSERTATIONS 401

Corinna Martinella

Single-Event Radiation Effects in Silicon Carbide Power MOSFETs



UNIVERSITY OF JYVÄSKYLÄ
FACULTY OF MATHEMATICS AND SCIENCE

JYU DISSERTATIONS 401

Corinna Martinella

Single-Event Radiation Effects in Silicon Carbide Power MOSFETs

Esitetään Jyväskylän yliopiston matemaattis-luonnontieteellisen tiedekunnan suostumuksella julkisesti tarkastettavaksi kesäkuun 18. päivänä 2021 kello 12.

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ABSTRACT

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In this research, the radiation induced single event effects (SEE) observed in silicon carbide (SiC) power MOSFETs have been studied. Heavy ions, terrestrial neutrons and protons were selected as radiation environments to be investigated, as representative of space, avionics and high-energy accelerator applications. SEE tests and electrical analysis were performed in order to identify the modes and mechanisms of failure, and to assess the reliability of commercial SiC MOSFET technologies. The research initially focused on the non-catastrophic SEEs induced by heavy-ion irradiation, which represent a significant risk for the part reliability in space applications. The broad-beam and microbeam results pave the way to the understanding of the degradation mechanism, named single event leakage current (SELC). Two types of degradation are described in this work, involving different parts of the SiC MOSFET structure depending on the applied voltage during the operation. At low bias the SELC is observed in the region under the gate oxide, whereas for voltages over a certain threshold a second mechanism involving the p-n junction is newly added. Heavy-ion latent damage effects were also studied through radiation tests and scanning electron microscopy (SEM) analysis of the damaged site. Two mechanisms were observed, involving the gate oxide and the SiC crystal lattice. Finally, the heavy-ion SEEs are summarised as function of the operational bias and linear energy transfer (LET). The second part of this work focused on SiC MOSFET reliability when exposed to proton and terrestrial-neutron environments. Accelerated single event burnout tests were performed using devices with different architectures. Electrical analysis of the damaged devices was carried out to investigate the failure mechanism. The results provide useful information about the reliability of the commercial SiC MOSFET technologies for avionic and high-energy accelerator applications.

This project was carried out in the framework of a collaboration between the Physics Department at the University of Jyväskylä, the radiation to electronics (R2E) project at the European Council for Nuclear Research (CERN), and the Advanced Power Semiconductor (APS) Laboratory at ETH Zürich.

Keywords: silicon carbide, power MOSFETs, radiation effects, Single Event Effects, SELC, SEB, SEGR, latent damage

TIIVISTELMÄ (FINNISH ABSTRACT)

Martinella, Corinna Yksittäisten hiukkasten aiheuttamat säteilyilmiöt piikarbidipohjaisissa MOSFET-tehotransistoreissa

Jyväskylä: Jyväskylän yliopisto 2021

(JYU Dissertations
ISSN 2489-9003; 401)
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Tässä työssä on tutkittu yksittäisten hiukkasten aiheuttamia säteilyilmiöitä piikarbidista (SiC) valmistetuissa MOSFET-tehotransistoreissa. Tutkimukseen valitut säteilytyypit sisälsivät raskaita hiukkasia, neutroneja sekä protoneja. Näitä hiukkasia tavataan tyypillisesti avaruus-, ilmailu- sekä kiihdytinsovelluksien toimintaympäristöissä. Säteilytestaukset ja sähköiset karakterisoinnit suoritettiin, jotta vauriomekanismien eri moodit saatiin selville, sekä kaupallisten SiC MOSFET-teknologioiden luotettavuus arvioitua. Ensisijaisesti tutkimus keskittyi raskaiden hiukkasten ei-katastrofaalisiin säteilyilmiöihin, jotka luovat merkittävän riskin komponenttien luotettavuudelle ja sen arvioimiselle avaruussovelluksissa. Fokusoituja (ns. mikrosuihkuja) sekä laaja-alaisia suihkuja käyttämällä on mahdollista paremmin ymmärtää SELC-vauriomekanismia (engl. Single Event Leakage Current). Tässä työssä kuvataan kahdenlaista SELC-vauriotyyppiä, mitkä kohdistuvat fyysisesti transistorin eri osiin riippuen käytetystä biasjännitteestä. Matalammilla jännitteillä SELC havaitaan hilaoksidin alueella, kun taas korkeammilla jännitteillä vaurio havaitaan transistorin runkodiodin alueella. Työssä tutkittiin myös raskaiden hiukkasten aiheuttamia piileviä (latentteja) vaurioita kuvantamalla vauriokohtia elektronimikroskoopin avulla. Latentteja vauriotyyppejäkin havaitaan kahdenlaisia, joihin liittyvät alueet komponentin sisällä ovat hilaoksidi sekä SiC substraatti. Yllä mainituista tuloksista on mahdollista määrittää raskaiden hiukkasten SEE-ilmiöiden eri alueet käyttöjännitteen sekä hiukkasen energiajätön funktiona. Työn toisessa osassa keskityttiin SiC MOSFETien luotettavuuteen protoni- ja neutronisäteily-ympäristöissä. Kiihdytettyjä SEB-testejä (engl. Single Event Burnout) käyttäen eri komponenttiarkkitehtuureja tutkittiin. Saadut tulokset antavat hyödyllistä tietoa kaupallisten SiC MOSFET teknologioiden luotettavuudesta ilmailu- sekä kiihdytinsovelluksissa.

Tämä projekti tehtiin yhteistyössä Jyväskylän yliopiston fysiikan laitoksen, CERN:n R2E-projektin (Radiation to Electronics), sekä ETH Zürichin APS (Advanced Power Semiconductor) laboratorion kanssa.

Avainsanat: piikarbidi, teho-MOSFET, säteilynvaikutukset, SEE, SELC, SEB, SEGR, latentit vauriot

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PREFACE

I come to the end of my PhD feeling enriched by all the experiences I had during this four years journey. I had the chance to work in many stimulating environments and to learn a lot, growing both as a scientist and as a person. Before turning page to the next chapter of my life, I would like to thank all the people who contributed to this success.

First of all, I would like to express my deepest gratitude to my supervisor Dr. Arto Javanainen, whose guidance during these years has been essential to complete this thesis. Thanks for driving me through this project and for patiently teaching me how to rationally plan the scientific research, resizing concerns whenever they seemed too big in my eyes. Your supervision and your expertise helped me sharpening my thinking, making me growing as a scientist and becoming more confident about my work. Thanks for your moral support and for putting me back on track every time I needed it.

I would also like to extend my sincere gratitude to Prof. Ulrike Grossner for introducing me in the APS group and always welcoming me at the Laboratory. Your support during these years was fundamental to integrate a different perspective in the work, which shaped my research approach and so the thesis. Thanks for pushing me to explore my own ideas and for your regular encouragement in every step of this journey, it was invaluable for me.

I also want to recognize my gratitude to my supervisors at CERN. I am grateful to Dr. Yacine Kadi for believing in my abilities and giving me the possibility to work on this PhD project. Thanks for your guidance during my time at CERN and for always providing me the tools and the opportunities I needed to further my research. I also wish to thank Dr. Rubén García Alía for all the insightful discussions, for his technical supervision and numerous scientific advices. Thanks for providing me the opportunities to take part in numerous test campaigns.

I would like to express my sincere gratitude to my reviewers, Dr. Jean-Marie Lauenstein and Prof. Arthur Witulski and to my Opponent, Dr. Veronique Ferlet-Cavrois, for accepting to revise my thesis and for providing useful comments on my research.

I would like to acknowledge all the colleagues and staff at CERN who made my access to the research facilities and laboratories simpler. I wish to thank Heikki, Mikko and Jukka for their assistance during the experiments at RADEF. I am also grateful to Roger, Thomas and Alexander from the APS Laboratory, for their help in preparing and performing the experiments, and for the numerous discussions concerning the interpretation of results. Special thanks goes also to my colleague Kimmo, for the help we gave each other and for the friendship we developed during these years.

Working on my PhD has been an incredible experience that gave me the opportunity to travel around the world and live in different countries. Despite the excitement and the unique opportunities these years gave me, completing a PhD can also be a lonely process. Everything would have been much more difficult without the help of many friends who

always welcomed me whether I was in Geneva, Zurich or Jyväskylä. To all of them goes my deepest gratitude.

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I would like to thank my parents, and my brothers Ludovico and Niccoló, for always being proud of me and pushing me to follow my dreams, even though this means accepting to have me far from home. Your presence and support has been essential to accomplish this result which I dedicate to you.

Finally, I wish to thank Andrea for putting the extra into those ordinary days spent writing this manuscript. Your positive thinking and your encouragement gave me the stamina and the confidence to cross the finishing line.

Ultreia! Et suseia!

LIST OF INCLUDED PUBLICATIONS

This thesis is mainly based on the following articles, which are appended at the end of the document. The author planned and conducted the experiments, performed the data analysis and the interpretation of the results. The articles are written by the first author.

I C. Martinella, R. Stark, T. Ziemann, R. G. Alia, Y. Kadi, U. Grossner, A. Javanainen, "Current Transport Mechanism for Heavy-Ion Degraded SiC MOSFETs", *IEEE Trans Nucl. Sci.*, vol 66, no. 7, pp. 1702-1709, Mar. 2019.

II C. Martinella, T. Ziemann, R. Stark, A. Tsibizov, R. G. Alia, Y. Kadi, U. Grossner, A. Javanainen, "Heavy-Ion Microbeam Studies of Single Event Leakage Current Mechanism in SiC VD-MOSFETs", *IEEE Trans Nucl. Sci.*, vol 66, no. 7, pp. 1381-1389, Jun. 2020.

III C. Martinella, R. G. Alia, R. Stark, A. Coronetti, C. Cazzaniga, M. Kastriotou, Y. Kadi, U. Grossner, A. Javanainen, "Impact of Terrestrial Neutrons on the Reliability of SiC VD-MOSFET Technologies", *IEEE Trans Nucl. Sci.* vol 68, no. 5, pp. 634-641, May 2021.

IV C. Martinella, P. Natzke, R. G. Alia, Y. Kadi, M. Rossi, J. Jaatinen, H. Kettunen, U. Grossner, A. Javanainen, "Heavy-ion Induced Single Event Effects and Latent Damages in SiC Power MOSFETs", submitted for publication to *Microelectron. Reliab.*, Jun. 2021

LIST OF OTHER PUBLICATIONS

In the context of the Radiation to Electronics (R2E) project at CERN, Switzerland, the author provided information and analysis to identify the areas in the high-energy accelerators with critical radiation levels for the installation of electronic systems.

I C. Martinella *et al.*, “Radiation levels at the LHC: 2012, 2015 and 2016 proton physics operations in view of HL-LHC requirements,” in Proc. *Int. Particle Accel. Conf. (IPAC)*, Copenhagen, Denmark, May 2017, pp. 2075−2077, paper TUPVA015.

II C. Martinella *et al.*, “Radiation Levels at the LHC during 2015, 2016 and 2017 Proton Physics Operations: Measurements from RadMons”, *CERN-ACC-NOTE 2018-0088*, pp. 1-47, Dec. 2018.

III C. Martinella *et al.*, “Radiation levels at the LHC during the 2015 Pb-Pb and 2016 p-Pb run and mitigation strategy for the electronic systems during HL-LHC operation”, *CERN-ACC-NOTE 2018-0073*, pp. 1-13, Dec. 2018.

IV R. Garcia Alia *et al.*, “LHC and HL-LHC: Present and Future Radiation Environment in the High-Luminosity Collision Points and RHA Implications,” *IEEE Trans. Nucl. Sci.*, vol. 65, no. 1, pp. 448−456, Jan. 2018.

V O. Stein *et al.*, “A Systematic Analysis of the Prompt Dose Distribution at the Large Hadron Collider,” in Proc. *Int. Particle Accel. Conf. (IPAC)*, Vancouver, Canada, Jun. 2018, pp. 2036−2038.

VI O. Stein *et al.*, “Identification and analysis of prompt dose maxima in the insertion regions IR1 and IR5 of the Large Hadron Collider,” in Proc. *Int. Particle Accel. Conf. (IPAC)*, Copenhagen, Denmark, May 2017, pp. 2078−2080.

ACRONYMS

SiC	silicon carbide
Si	silicon
WBG	wide bandgap
MOSFET	metal-oxide-semiconductor field-effect transistor
IGBT	insulated gate bipolar transistor
BJT	bipolar junction transistor
JFET	junction field-effect transistor
JBS	junction barrier Schottky
SEE	single event effect
SEB	single event burnout
SELC	single event leakage current
SEGR	single event gate rupture
DD	displacement damage
TID	total ionizing dose
LET	linear energy transfer
FIT	failure in time
DUT	device under test
I_D	drain leakage current
I_G	gate leakage current
I_S	source leakage current
I_{DG}	drain-gate leakage current
I_{DS}	drain-source leakage current
V_{DS}	drain-source voltage
V_{GS}	gate-source voltage
BV_{DSS}	breakdown voltage
PCB	printed circuit board
SMU	source measure unit
SEM	scanning electron microscope
FIB	focused ion beam
PIGS	post irradiation gate stress

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1 Introduction

The increasing global energy demand requires drastic improvements in energy efficiency to meet the requirements for a sustainable development scenario. During the late 1980s, it was demonstrated that power devices based on Silicon (Si) technology are rapidly approaching their theoretical limits, and new alternatives for materials should be considered in the future to reach higher efficiency. In this context, the wide-bandgap silicon carbide (SiC) semiconductor has emerged as one of the most viable alternative to silicon (Si) for the next-generation material for power devices. In fact, thanks to their physical, electrical and thermal properties, SiC power devices can work at higher switching frequencies, higher voltages and temperatures, achieving lower conduction losses with respect to the Si counterparts [1].

Although research on SiC material has been performed for several decades, the suggestion of using it to manufacture power device served as additional motivation. Since then, Laboratories all over the world have made considerable effort in advancing crystal growth and device processing techniques required for vertical power devices.

The first SiC Schottky diode was commercially released in 2001, followed by the first junction field-effect transistor (JFET) in 2008. Additional years of research were required for the SiC metal-oxide-semiconductor field-effect transistor (MOSFET), due to the challenges related to the high densities of oxide/SiC interface states and oxide traps, that inhibit carrier mobility and lead to instabilities in threshold voltage [2]. Finally, in 2011 the first SiC MOSFET appeared on the market.

It has taken time for the technology to mature, to address the reliability concerns and for the price to drop sufficiently, but eventually these milestones have been achieved by multiple manufacturers, and in the past few years SiC MOSFETs have seen tremendous commercial progress [3]. Nowadays SiC power MOSFETs are found in a variety of applications in the automotive, photovoltaic and power supply segments [4].

Due to the higher energy required for ionization and defects formation in respect to Si, SiC technology has been considered highly suitable to harsh working conditions, including radiation exposure [5]. These advantages make SiC technology desirable also for space, avionics and high-energy accelerator applications [4, 6, 7]. Despite the beneficial characteristics of SiC, its adoption in these fields is still hindered by the unexpected susceptibility to the radiation encountered in these applications, which increases the risk of single event effects (SEEs). These effects are a perturbation of the normal operation of the device, which can cause permanent degradation or complete failure of the component, preventing the implementation of the current commercial technologies in these fields. During recent years, extensive work has been done by the community to understand the SEE mechanisms in SiC power technology, with the objective to ultimately develop more SEE-tolerant devices [8].

1.1 Objectives of the thesis

This project was carried out in the framework of a collaboration between the Physics Department at the University of Jyväskylä, the radiation to electronics (R2E) project at the European Council for Nuclear Research (CERN), and the Advanced Power Semiconductor (APS) Laboratory at ETH Zürich.

The research focuses on the physical SEE mechanisms observed in commercial SiC power MOSFETs exposed to heavy-ion, terrestrial-neutron and proton radiation environments. In order to assess the reliability of commercial SiC MOSFETs technologies, experimental SEE tests were performed in different European facilities. After the irradiation, the electrical characteristics of the devices were analysed to investigate modes and mechanisms of failure.

The first part of this work focused on the degradation and latent damage mechanisms observed when exposing the devices to heavy-ions, which is critical for space applications. Successively, terrestrial-neutron and proton SEE tests were performed in order to study the reliability of different commercial SiC MOSFETs for avionic and high-energy accelerator environments.

1.2 Outline of the thesis

This thesis is structured in five chapters, summarized below.

Chapter 2 is an introduction on SiC material properties, SiC power components, and SiC MOSFETs applications. The physical, electrical and thermal properties of SiC are described, highlighting the interesting features for power applications. SiC power devices are introduced, focusing especially on SiC MOSFETs, describing the planar and trench architectures and the market projection. The second part of the chapter discusses the potential applications of SiC MOSFETs as semiconductor switches for the injection kicker system in high-energy accelerators at CERN.

Chapter 3 provides the underlying concepts regarding radiation interaction with matter and radiation effects in electronics. The critical radiation environments for SiC power applications in space, avionics and high-energy accelerators are described, followed by a list of useful concepts for radiation testing. The final part of the chapter reviews the literature on SEE in Si and SiC power components. An overview of the mechanisms of degradation and failure in MOSFETs and diodes is provided, highlighting the context where this research is inserted.

Chapter 4 focuses on the heavy-ion experiments, relevant especially for space applications. The heavy-ion facilities and the experimental setup and methods are described before presenting the results and discussion for leakage current degradation and latent damage. The chapter concludes with a summary of the SEEs induced by heavy-ion in SiC power MOSFETs.

Chapter 5 describes the experiments and the results obtained with lighter particles, such as atmospheric-like neutrons and protons. This chapter is relevant for avionics and high-energy applications. After the description of the facilities and the experimental setup and methods, the results for terrestrial-neutron and proton irradiations are discussed.

Chapter 6 provides a list of suggestions collected along the years, followed by a summary of the main findings of this research and some possible follow-up studies that might expand the work presented in this thesis.

2 Background on SiC properties and SiC power devices

SiC crystallizes in wide variety of structures, each of which exhibits unique electrical, optical, thermal and mechanical properties. Due to these characteristics, SiC has emerged as the most viable alternative to silicon for next-generation semiconductor for high-efficiency and high-power density applications.

This chapter briefly describes the properties of the main SiC polytypes and the advantages of SiC as a wide bandgap semiconductor for power applications, giving an overview on SiC power devices, their properties, applications and market projection. The design and working principle of SiC power MOSFETs are described for commercial planar and trench technologies.

SiC power devices are considered an interesting technology for space, avionics and high-energy accelerator industries. An overview of the potential SiC power MOSFETs applications in the CERN accelerator complex is given. After introducing the Large Hadron Collider (LHC), its upgrade the High-Luminosity LHC (HL-LHC) and the Future Circular Collider (FCC), three case studies are reported for SiC MOSFETs applications in the kicker systems used to inject and extract the beam along the acceleration chain.

2.1 Properties of SiC

2.1.1 Crystal structure

SiC is a wide bandgap (WBG) semiconductor, with a rigid stoichiometry of 50 % Si and 50 % carbon (C). Both Si and C atoms are tetravalent elements, with 4 valence electrons in the outermost shells. In the ground states, Si and C have the following electronic structures:

$$\begin{aligned} Si, 14e^- &: 1s^2s^22p^63s^23p^2 \\ C, 6e^- &: 1s^22s^22p^2 \end{aligned} \tag{2.1}$$

In SiC crystal, Si and C share electron pairs in sp^3-hybrid orbitals with covalent bonds. The basic structural unit is a tetrahedron of four carbon atoms with a silicon atom in the middle. The high energy of the Si-C bond (4.6 eV), gives SiC a varieties of outstanding properties [9], as described below.

SiC exists in about 250 different crystalline forms and it is the best known example of polytypism. This phenomenon, which is a variant of polymorphism, is characterized by a variation of the periodicity only along the growth axis, leading to different crystal structures between polytypes, without changes in the chemical composition [10, 11]. A certain polytype is defined by the Si-C bilayer stacking sequence along the stacking direction (c-axis) of the hexagonal close-packed system. The SiC bilayer is known as the basal plane and can be viewed as a planar sheet of Si atoms coupled with a planar sheet of C atoms, while the c-axis is defined normal to the Si-C bilayer plane. On each Si-C bilayer (A), there are two possible stacking sites (B, C) as illustrated in Figure 2.1. The Ramsdell's notation is commonly used to identify the SiC polytypes. In this notation, the number of Si-C layers in the unit cell are combined with the letter representing the Bravais lattice type i.e., C for cubic, H for hexagonal, and R for rhombohedral. The structures of popular SiC polytypes, 2H-SiC, 3C-SiC, 4H-SiC and 6H-SiC, are schematized in Figure 2.2 in a ball-stick model, after [12, 13]. Yellow and black circles represent Si and C atoms in a three-dimensional perspective. The chain structure which defines the stacking sequence are in black, while Si-C bonds are in red.

SiC is used mostly in its synthetic form because it is extremely rare in nature. The mechanical and thermal properties are very similar among different polytypes, while the optical and electrical properties vary a lot. For this reason, for device applications, the polytype control is a crucial aspect of SiC crystal growth. The technological process for crystal growth is not discussed in this work, but an overview can be found in [9, 14−16].

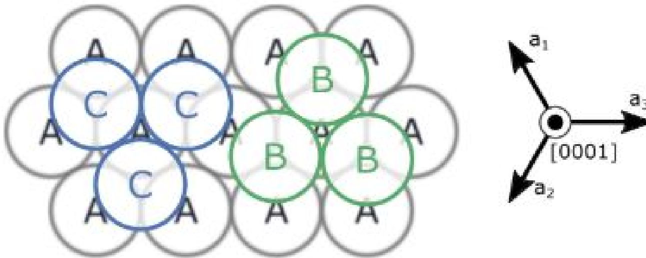


Figure 2.1: The SiC bilayer (A) is a planar sheet of Si atoms with two possible stacking sites (B, C). The c-axis is defined normal to the Si-C bilayer plane. Image from the public domain.

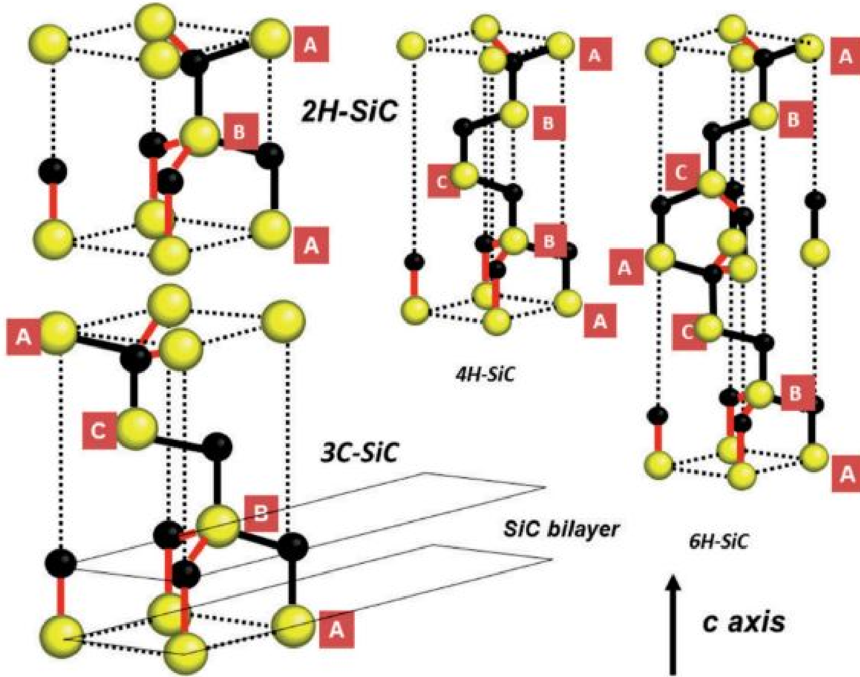


Figure 2.2: Representation of the most popular SiC polytypes, 2H-SiC, 3C-SiC, 4H-SiC and 6H-SiC, in a ball-stick model. Yellow and black circles represent Si and C atoms in a three-dimensional perspective. Si-C bonds are in red, while the chain structure, which defines the stacking sequence, are in black. Reprinted with permission from [13]. © 1994, APS.

2.1.2 Band structure

The bandgap is defined as the difference in potential energy between the valence and the conduction band. It is the minimum energy required for an electron to be excited from valence to conduction band, where it is considered as "free". Depending on the bandgap, materials can be divided into metals, semiconductors and insulators. SiC belongs into the semiconductor category, but it has a wider band with respect to Si, therefore it is defined as a WBG material. The bandgap values at room temperature of the most common SiC polytypes are respectively 2.36 eV for 3C-SiC, 3.26 eV for 4H-SiC and 3.02 eV for 6H-SiC, whereas it is 1.12 eV for Si.

2.1.3 Impurity doping and carrier density

The intrinsic carrier density at room temperature (i.e. the electrons and holes generated by thermal excitation), indicated as n_i, is extremely low in SiC due to the wide bandgap. Specifically it is about 0.13 cm^{-3} for 3C-SiC, 5 x 10^{-9} cm^{-3} for 4H-SiC and 1 x 10^{-6} cm^{-3} for 6H-SiC. The Fermi level, which is the probability of electron occupancy at different energy levels, does not approach the midgap (intrinsic level) even at high temperature of 700-800 K, as expected from such low n_i. This gives the great advantage for SiC electronic devices to operate at high temperatures with still low leakage current. Figure 2.3 shows the intrinsic carrier density for major SiC polytypes and Si [9]. For the same temperature, n_i is orders of magnitude lower than Si for all the main SiC polytypes.

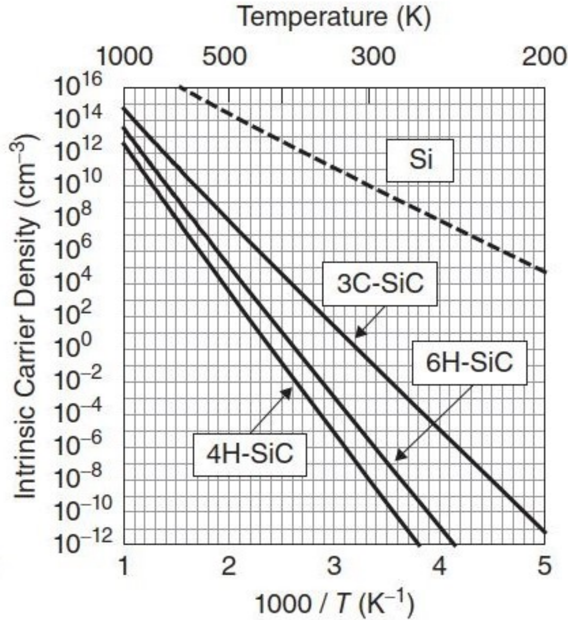


Figure 2.3: Temperature dependence of the intrinsic carrier density for 3C-SiC, 4H-SiC, 6H-SiC and Si. Reprinted with permission from [9]. © 2014, John Wiley and Sons.

2.1.4 Mobility

The effective electron mass and its anisotropy has a strong dependence on the SiC polytypes, while for holes the polytype dependence is weaker. As the mobility, indicated as μ, is inversely proportional to the effective mass, there is a large variation of electron mobility among SiC polytypes. Moreover, the anisotropy of the electron mass causes different mobility and therefore different electron transport among the crystal planes of the same polytype [17].

In this context, 4H-SiC is the most attractive polytype for vertical power devices fabricated on 0001 wafers. Indeed, at a given dopant density, the electron mobility of 4H-SiC is almost double of 6H-SiC, also the hole mobility is slightly higher. This is visible in Figure 2.4, where the electron and hole mobilities for these two polytypes are reported as function of the donor and acceptor densities at room temperature and along the c-axis. Furthermore, usually hexagonal SiC polytypes exhibits strong anisotropy in electron mobility. However, in 4H-SiC the mobility anisotropy is relatively small (i.e., the electron mobility along the c-axis is only 20% than the one perpendicular to the c-axis).

2.1.5 Drift velocity

The saturated drift velocity is a key parameter for semiconductor materials. It determines frequency limitation of semiconductor devices and consequently the range of the most effective application. For 4H-SiC, the saturated drift velocity for electrons is estimated $\sim 2.2 \cdot 10^7$ cm/s at room temperature (vs $\sim 1 \cdot 10^7$ cm/s for Si and GaAs), making SiC suitable for higher frequencies applications (RF and high power microwave devices).

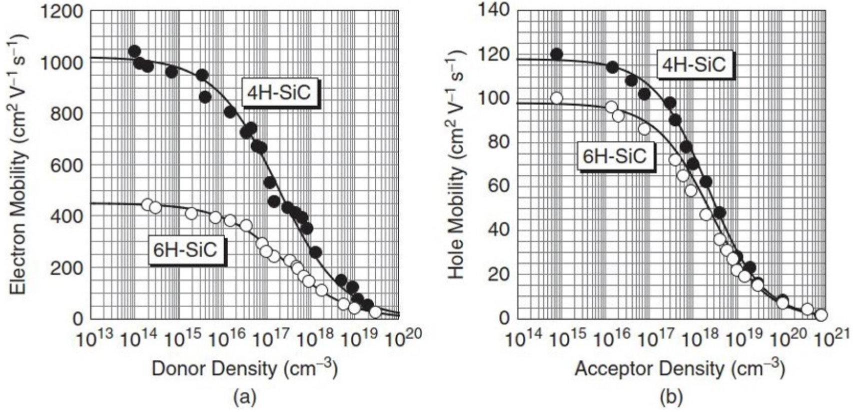


Figure 2.4: Comparison between 4H-SiC and 6H-SiC low-field electron (a) and holes (b) mobility along the c-axis versus donor and acceptor densities at room temperature. The electron mobility of 4H-SiC is almost double of 6H-SiC, also the hole mobility is higher, making 4H-SiC the most attractive polytype for vertical power MOSFETs. Reprinted with permission from [9]. © 2014, John Wiley and Sons.

2.1.6 Breakdown electric field strength

High reverse voltage applied across a p-n junction or a Schottky barrier, can induce the electric field to exceed certain limits, causing the breakdown of the junction. SiC can withstand electric fields over eight times greater than Si or GaAs without undergoing avalanche breakdown. This makes SiC an interesting material for high-voltage, high-power devices, such as power transistors and diodes and power thyristors and surge suppressors. Two mechanisms can cause breakdown namely the avalanche breakdown and the Zener tunneling breakdown. For junctions with a region lightly doped, the avalanche breakdown is dominant, as in most power devices. The carriers can gain very high kinetic energy while travelling through high electric field regions and undergo scattering events with the electrons in the valence band. The excessive energy is transferred to these electrons, which are excited to the conduction band, generating a new electron-hole pair. If these newly-generated electrons have sufficiently high energy, they can cause a secondary branch of impact ionization. Consecutive collisions can cause the multiplication of carriers and a rapid increase in their density, triggering an avalanche effect and leading to the breakdown.

2.1.7 Thermal conductivity

The thermal conductivity of SiC is much higher than Si (i.e., 4.9 W $cm^{-1}K{-}1$ at room temperature for high-purity SiC, while it is 1.4-1.5 $cm^{-1}K{-}1$ for Si). It is not sensitive to the SiC polytype, but it is influenced by the crystal direction and the doping density [18]. Having higher thermal conductivity, SiC devices can operates at higher power levels with respect to Si and still dissipate the large amounts of excess heat generated.

2.1.8 Mechanical properties and hardness

SiC is one of the hardest known material. The Young's modulus, which is a measure of the stiffness of a material and it is defined as the ratio between stress and strain, is much higher for SiC (380-700 GPa [19]) with respect to Si. SiC maintains the high hardness and elasticity also at high temperatures.

2.2 SiC power devices

2.2.1 SiC advantages for power applications

Thanks to its physical, electrical and thermal features described before, SiC outperforms Si in several material properties, as shown in Figure 2.5.

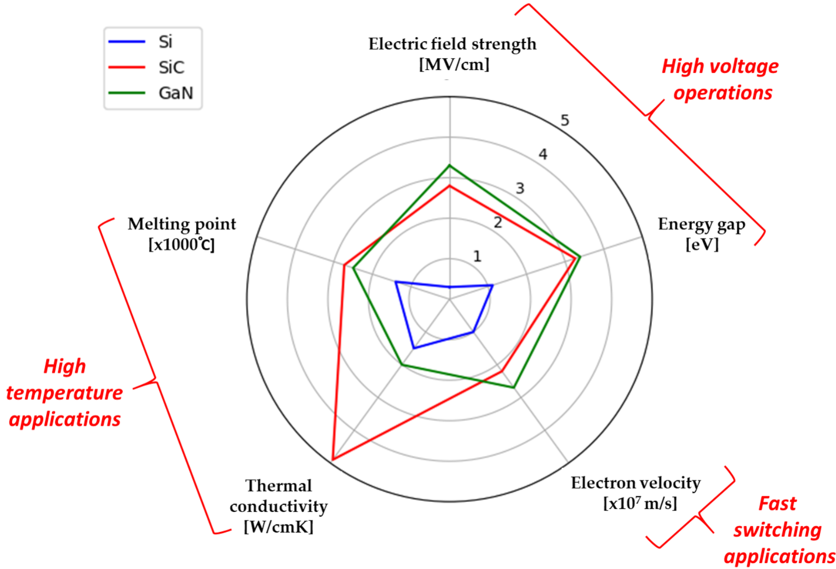


Figure 2.5: Radar chart of Si, SiC and GaN relevant material properties, remade after [20].

SiC has about 10 times higher electric field strength compared to Si, which allows to manufacture SiC power devices with much thinner drift layers in respect to Si ones. Since the resistance of high-voltage devices is mostly determined by the thickness of the drift region, SiC can reduce the resistance per unit area for the same blocking voltage capability, and therefore reduce the conduction losses. This makes SiC devices particularly suitable for high-voltage operations.

SiC has 3 times higher thermal conductivity in respect to Si, meaning 3 times more efficient cooling capability, permitting higher power density. Due to the wide bandgap, the intrinsic carrier density at room temperature is extremely low, giving the great advantage for SiC electronic devices to operate at high temperatures with low leakage current. For the current SiC device, the guaranteed operating temperature is between 150°C and 175°C, mainly due to the thermal reliability of the package. When properly packaged, they can reach 200°C [21]. Finally, the saturated electron drift velocity in SiC is about twice to that of Si (i.e. 4H SiC at room temperature), making SiC devices suitable for higher frequencies applications.

These properties make SiC an attractive material for manufacturing power devices that can far exceed the performance of their Si counterparts. However, even though the benefits of SiC for power applications have been widely demonstrated, it has taken time for SiC technology to mature, to address the reliability concerns and for the price to drop sufficiently. For these reasons, the growth of SiC adoption has been relatively slow until 2017, especially for the replacement of Si MOSFET and Si insulated gate bipolar transistor (IGBT) devices.

2.2.2 Applications and market overview

SiC devices have penetrated into different sectors of ground applications, and nowadays they are found in a variety of applications in automotive, photovoltaic and power supply segments. During the next years, the SiC industry is expected to accelerate even further, as industrial players have increasing confidence in the SiC power market. An overview of the power electronics market per device type and the projection for the following years, is visible in Figures 2.6, after [22]. The SiC MOSFET and SiC MOSFETs module shares are expected to increase and take part of the Si MOSFET market share, reaching 10 % of the Si market by 2025 [21].

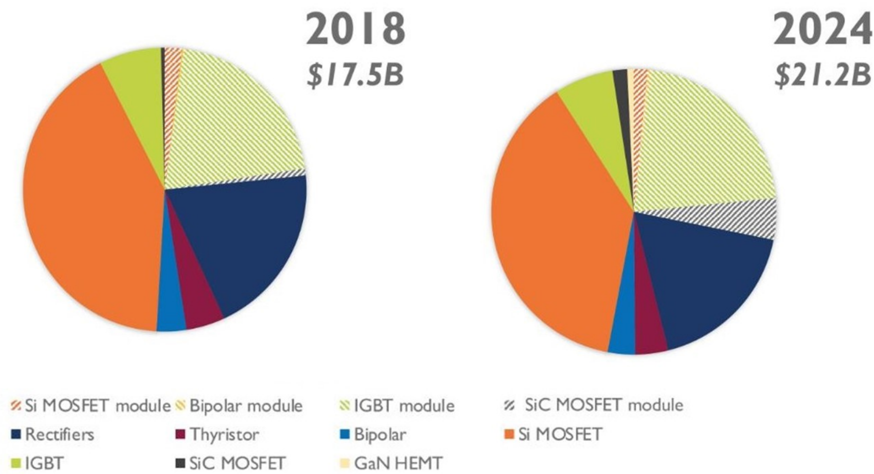


Figure 2.6: Power electronic market share split by device in 2018 and 2024, after [22].

The SiC power device market is expected to reach 1.4 billion dollars by 2023. Figure 2.7 after [23], shows the SiC power device market revenue split by application between 2017 and 2023. Today the automotive segment is dominant, especially for electric vehicles (EV) and hybrid electric vehicles (HEVs), and it drives both the technological development and market demand [24]. For example, Tesla integrated SiC MOSFET based power modules in its Model 3 inverter in 2017 [25], and many automotive manufacturers had implemented SiC devices in on-board and off-board charging systems. The power factor correction (PFC)/power supply segment is also a leading application. While in the future, electric vehicle (xEV)-related applications, rail, photovoltaic (PV) and others are also expected to contribute to the market evolution. Traditional applications will eventually open up to SiC as prices fall. Finally, over a long time frame, the 3300 V - 10 kV class products will be used in applications such as railway traction, high voltage DC power conversion, MW motor drivers for wind, ship and industrial use, solid-state breakers, etc. [21].

In addition to the aforementioned ground applications, the advantages of SiC MOSFETs make these devices attractive also for space and avionics, where higher efficiency results in a more compact design, lower wait and cost reduction. SiC MOSFETs have been considered also for applications in high-energy accelerators at CERN. An overview of three possible use cases in the CERN accelerator chain are described in Section 2.3.

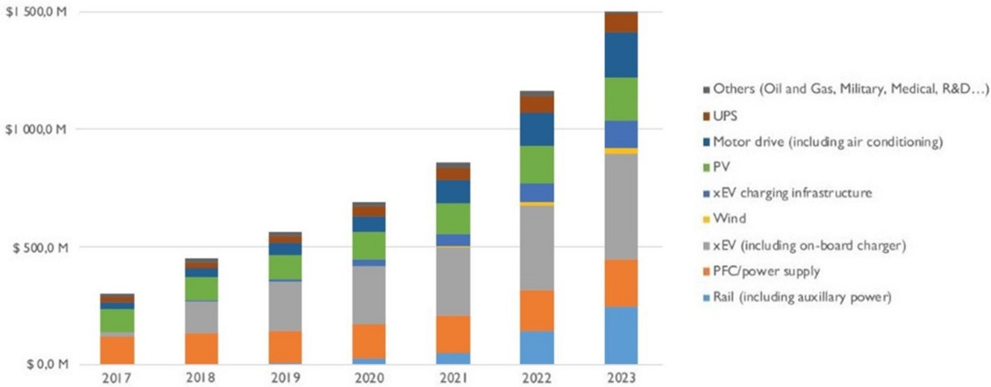


Figure 2.7: SiC power device market revenue split by application from 2017 to 2023, after [23].

2.2.3 SiC power MOSFET basics

The metal−oxide−semiconductor field-effect transistor or MOSFET is a field-effect transistor (FET) with a metal gate electrode, which is insulated with an oxide layer from the semiconductor channel. SiC power MOSFETs and SiC modules are used in a wide range of applications, such as power supplies, DC-to-DC converters, low-voltage motor controllers, and many others.

Figure 2.8 (a) shows a commercial SiC power MOSFET in a conventional 3-pin packages (TO-247). The presented device is a 80 mΩ N-channel MOSFET from the 2nd generation manufactured by Cree/Wolfspeed. The MOSFET is rated for 1.2 kV, and has the reference number of C2M0080120. This device type has been used as the baseline for this work. From the package cross-section in Figure 2.8 (b), it is visible how the chip (or die) is soldered on the heat sink. Source and gate are connected to the pins through the bond-wires, whereas the drain is directly connected to the heat sink at the back of the package. Figure 2.8 (c) shows a front-side picture of a bare die. The gate and the source pads are highlighted, while the drain is on the bottom of the die. The gate stripes are also visible. A short summary on the power MOSFET working principles and designs are discussed below. This is not intended to be an exhaustive overview on power MOSFETs, and more complete discussions can be found in [26−28].

For high blocking voltage applications, power MOSFETs are designed in a vertical structure. The source and the drain are at the opposite sides, in order to accommodate a wide depletion region across which the high drain-source voltage is applied, while minimizing the die area. The current flows through a lightly-doped epitaxial layer (or epi-layer) and a substrate. The latter is located in the bottom side, closer to the drain, and it is usually degenerately doped to minimize the impact on the on-state resistance.

There are currently two designs of SiC MOSFETs commercially available: planar-gate and trench-gate devices [29−31]. Among the trench devices, single and double-trench design can be distinguished, where the first have only a trench gate, whereas the second has a trench source and a trench gate [29]. The schematics of a single cell for the three architectures are shown in Figure 2.9. In particular, a general design for a planar device (as the devices from Cree/Wolfspeed), a double trench MOSFET from Rohm and the $CoolSiC^{TM}$ trench MOSFET from Infineon are presented. The epi-layer and the

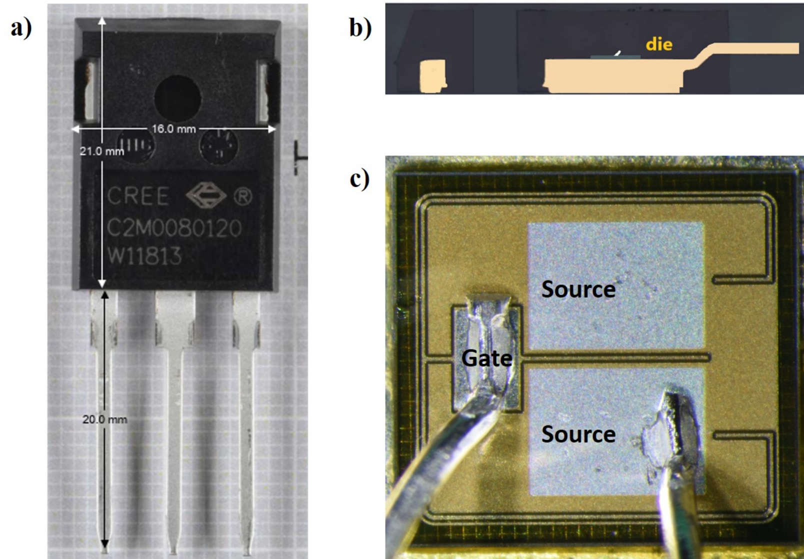


Figure 2.8: a) Commercial SiC power MOSFETs from Cree (C2M0080120D) in a TO-247 package; b) cross-section of the device; c) frontal picture of the bare die.

substrate are represented in green and in blu, respectively. The gate, source and drain contacts are labelled accordingly, as the p- and n-well.

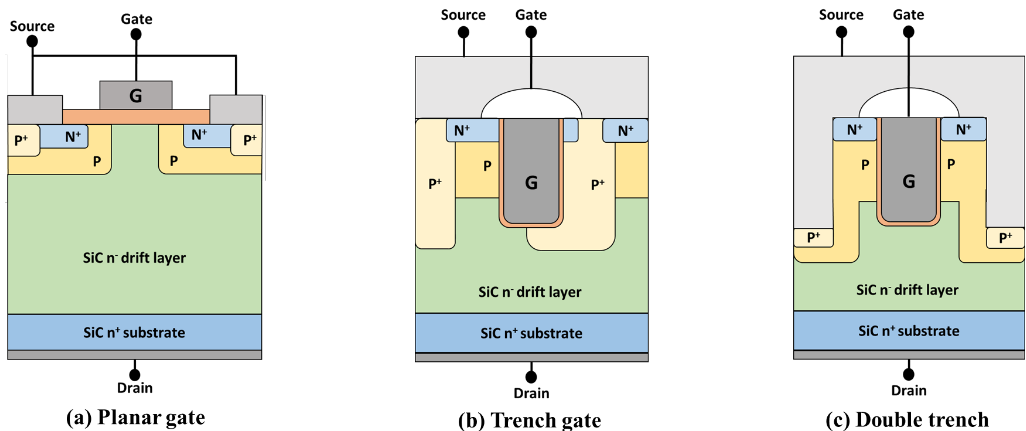


Figure 2.9: Cell schematic of the three architectures of SiC power MOSFETs: (a) general design for planar gate, (b) trench gate design of *CoolSiC*^{TM} MOSFET from Infineon and (c) double trench (trench source and trench gate) design from Rohm. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

The gate-source voltage (V_{GS}) determines the conductivity of the device, independently from the architecture, meaning that the current flowing through the main channel between the drain and source is dependent on the gate (control) voltage. The characteristic of changing the conductivity with the gate voltage is used for switching or amplifying signals. In normal operation, no current flows in the gate, as the gate oxide isolates the gate

electrode from the rest of the device structure.

Most power MOSFETs are manufactured on a single chip structured with a large number of closely packed identical cells. One of the reason is to minimize the MOSFET resistance between the drain and the source when the device is in the on-state, therefore to reduce the voltage drop and increase the power-switching performance. This parameter is called $R_{DS(on)}$ and it is the sum of many contributions, as visible in Figure 2.10 (a) for a planar device:

$$R_{DS(on)} = R_S + R_D + R_{Ch} + R_{Sub} + R_{JFET} + R_A + R_{wcml} \tag{2.2}$$

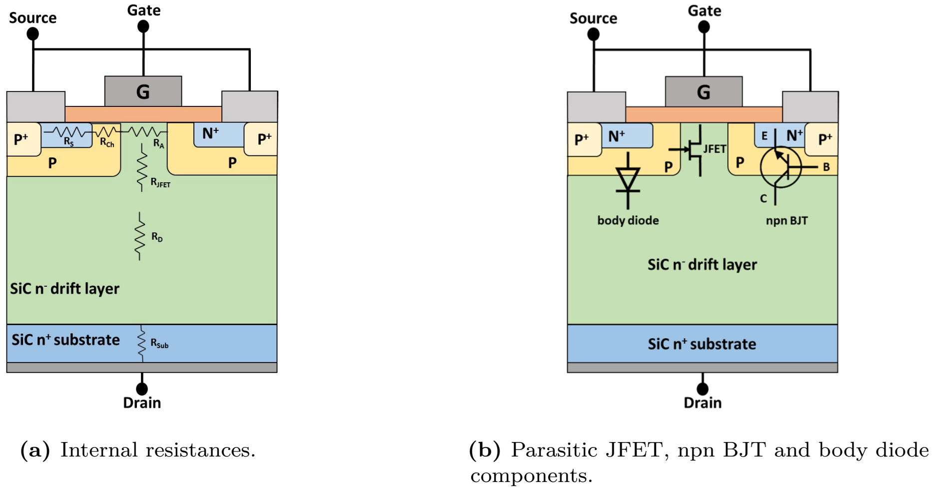
where:

- R_S is the source diffusion resistance;
- R_D is the drift region resistance;
- R_{Ch} is the channel resistance;
- R_{Sub} is the substrate resistance
- R_{JFET} is the resistance of the parasitic JFET component between the two body regions;
- R_A is the accumulation resistance;
- R_{wcml} is the sum of the bond wires, the contact resistance between the source and the drain, the metallization an the lead frame contributions.

For devices with increasing breakdown voltage, the epi-layer must become less doped and thicker, penalising the on-state resistance. Therefore, in high voltage device the $R_{DS(on)}$ is dominated by the epi-layer resistance (R_D) and the JFET resistance (R_{JFET}). Conversely, for low-voltage applications the $R_{DS(on)}$ is dominated by the channel resistance, and the competitiveness of SiC MOSFETs is limited by the much higher values.

As a consequence of the vertical power MOSFET structure, some parasitic components are formed, such as the parasitic JFET, the parasitic npn bipolar junction transistor (BJT) and the body diode. They are represented in Figure 2.10 (b) for a N-type planar MOSFET and are further described below:

- The parasitic JFET is created between the two body, in a region also called "neck region". At increasing drain-source voltage (V_{DS}), the depletion widths of the two adjacent body diodes extend into the drift region and it restricts the current flow.
- The parasitic npn BJT of the MOSFET has its collector at the n- layer in the drain, the base at the source p-well, and the emitter in the source n+ well. This parasitic structure can make the device susceptible to unwanted device turn-on and premature breakdown. The activation of the parasitic BJT is the cause of SEB in Si-power MOSFETs, as further described in Section 3.5.1.2.
- The body diode is formed between the n- layer of the drain (cathode) and the p+ well of the source (anode). When the MOSFET is in the OFF state with $V_{GS} = 0$ V, the leakage current is flowing entirely through the body diode.



(a) Internal resistances.

(b) Parasitic JFET, npn BJT and body diode components.

Figure 2.10: (a) The $R_{DS(on)}$ is the sum of different contributions. (b) Parasitic components formed in the vertical structure of the power MOSFET.

In respect to the planar MOSFET, the trench structure features higher cell densities, which allow having lower $R_{DS(on)}$ specifications per unit die size. However, trench MOSFETs are more difficult to manufacture compared to the planar design. The gate oxide and the metallization are deposited in a trench cut into the wafer surface. The gate field in a trench device exerts influence over a much greater region of the active semiconductor. As a result, the cells can be physically smaller yet yield the same $R_{DS(on)}$ as planar devices. The channel is formed vertically, which allows the vertical flow of the current. The basic MOSFET operation and details discussed above apply also for the trench and the double-trench design presented in figure 2.9.

Nowadays, trench MOSFETs from manufactures like Rohm and Infineon [30, 31] compete with advanced planar technologies from Cree/Wolfspeed, ST-Microelectronics, Microsemi, etc. Most of the results discussed in this work refers to the N-channel planar MOSFETs from Cree/Wolfspeed [33]. However, additional commercial devices from different manufacturers were used for the neutron study discussed in Chapter 5, which included both planar and trench technologies.

2.3 SiC applications in high-energy accelerators at CERN

2.3.1 The European Center for Nuclear Research (CERN)

The European Center for Nuclear Research (CERN) or Organisation Européenne pour la Recherche Nucléaire is a research center based in Geneva. It was founded in 1954 with the scope of using science for peace, investigating the fundamental structure of the universe. To perform this task, the most powerful accelerator complex was built across the franco-swiss border by CERN and its member states.

2.3.2 CERN accelerator chain

The accelerator chain at CERN is a succession of machines that accelerate particles (i.e., protons and ions) to increasingly higher energies. The last stage of the chain is the Large Hadron Collider (LHC), the largest accelerator in the world, which straddles the French-Swiss border going from the lac Léman to the Jura mountain. It is about 27 km long, buried from 50 to 175 m. The particles reach energy of 6.5 TeV per beam and of 7 TeV for the future operation called High-Luminosity LHC (HL-LHC) planned for 2025.

The CERN's accelerator chain is illustrated in 2.11. Each accelerator boosts the energy of the protons before injecting the beam into the next machine in the sequence. The first machine in the chain is the Linear accelerator 2 (LINAC 2). At the exit, the protons have an energy of 50 MeV and gained 5% in mass. Then the particles enter the Proton Synchrotron Booster (PSB), the next step in CERN's accelerator chain, and accelerate them to 1.4 GeV for injection into the Proton Synchrotron (PS), which operates up to 25 GeV. The Super Proton Synchrotron (SPS) is next. It operates at up to 450 GeV and provides the beam to the LHC and experimental areas. Beams are injected in LHC through two transfer lines and they travel along the 27 km ring in opposite directions close to the speed of light, colliding in four experiment: ATLAS, CMS, ALICE and LHCb. The total energy at the collision is 13 TeV (increasing to 14 TeV with HL-LHC). There, the large detectors placed in the experimental caverns collect information about the particles shower coming from the collisions, so that physicists can pin down the particles identity. Lead ions are also accelerated during few weeks at the end of the year: those starts from a source of vaporized lead and are injected in the Linac3 and in the Low Energy Ion Ring (LEIR). They then follow the same chain to LHC (PS, SPS, LHC), where ALICE is the experiment dedicated to this run.

Along the accelerator the beam is also extracted for many different experiments. An example is the CERN High energy AcceleRator Mixed field facility (CHARM) built in the PS east area and fashioned to test electronic systems meant to be installed in the underground areas of the accelerator chain [34]. For a complete description of the LHC accelerator chain and experiments refer to [35].

During the acceleration beam losses occur along the chain and create a mixed radiation environment, unique in terms of energies and particles involved [36−38], as further described in Section 3.3.3. This harsh environment creates a significant risk for the electronic systems installed in the underground areas if they are not designed for such radiation levels. The results for protons and ions operations analysed during Run 2 (2015-2018) are presented in [39−43], whereas an overview for HL-LHC can be found in [36, 44]. The Radiation to Electronic (R2E) Project started in 2007 with the main objective to reduce the number of failures due to radiation in the LHC and its injector chain, minimizing the downtime of the machine.

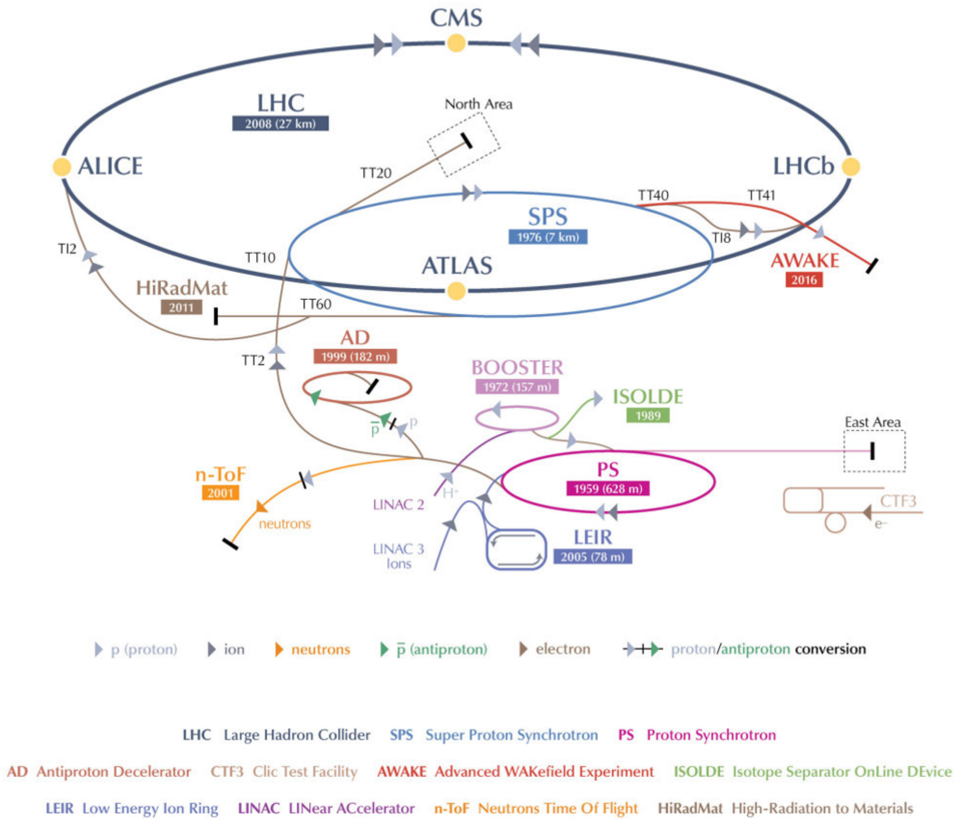


Figure 2.11: CERN's Accelerator Complex. Image from the public domain.

2.3.3 The Future Circular Collider (FCC)

The Future Circular Collider (FCC) study was performed by CERN to develop the design for a higher performance particle collider to extend the research currently being conducted at the LHC, once it reaches the end of its lifespan. The purpose of the FCC is to reach collision energies of 100 TeV, in the search for new physics. To do that, an underground tunnel of 100 km, close to the current LHC site, is needed. A schematic map showing the proposed location for FCC is visible in Figure 2.12. Three different scenarios for particle collisions were examined: hadron (proton-proton and heavy ion) collisions [45], like in the LHC; proton-electron collisions and electron-positron collisions. Physics and detector studies are performed for each option. In-depth analyses of infrastructure and technologies required were also carried out by a team of experts. A conceptual design report for the FCC was submitted in January 2019, as input to the next update of the European Strategy for Particle Physics [46].

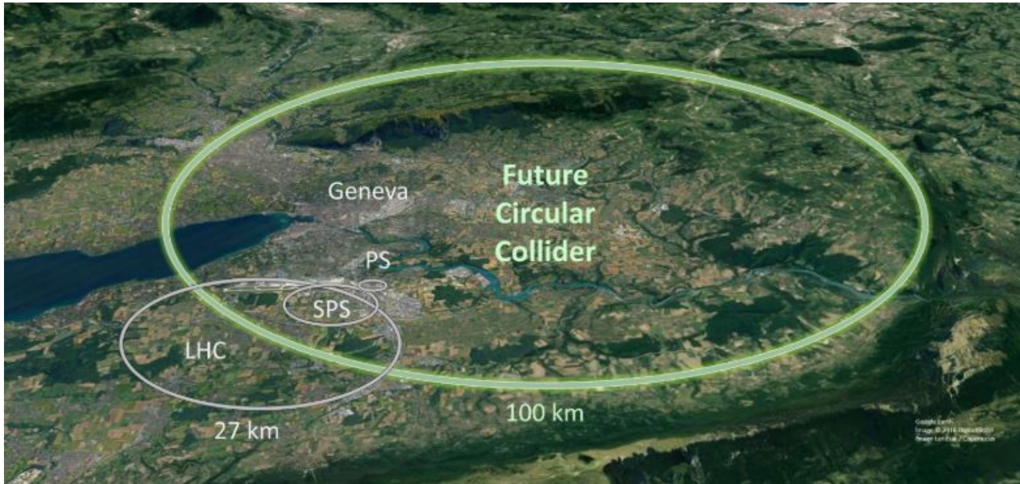


Figure 2.12: Schematic map of the proposed location for the FCC tunnel. Image from the public domain.

2.3.4 SiC applications in high-energy accelerators

Kicker systems are used for the injection and extraction of the beam along the accelerator chain at CERN. Historically, the pulse generators for kicker system use thyratrons. Recently, multiple studies have been carried out to employ semiconductor switches instead of thyratrons and several prototype inductive adders (IAs) are under constructions at CERN. Compared to the traditional systems, IA has several advantages, such as the modularity, the scalability and the possibility to improve the pulse quality reducing the ripple.

A prototype IA based on semiconductor switches was designed for the kicker pulse generator of the FCC injection system, which requires a very fast system to achieve a high filling factor [7, 47]. The IA consists of a stack of toroidal 1:1 transformer cores, as visible in the schematic drawing in Figure 2.13, after [47]. The FCC injection kicker requirements for a beam energy of 3.3 TeV are a pulse length of 2.00 μs a rise and fall times of 430 ns in the magnet and < 75 ns for the current pulse in the generator, a system impedance of 6.25 Ω and a total voltage and current of respectively of 15.70 kV and 2.50 kA. The semiconductor switches have a relatively low ratings for voltage and current compared to the traditional thyratron, hence multiple switches in series and parallel are needed. The rated pulse current of fast switching MOSFETs is typically between 100 and 250 A, hence the need for the primary of each transformer to have multiple parallel branches in order to provide the output current of 2.5 kA, as required. Among the semiconductor switches available on the market, SiC MOSFETs rated for at least 1.2 kV and 190 A, were identified as the most appropriate, thanks to the low on-state resistance (less than 50 mΩ) and the fast switching times. Indeed, even though IGBTs are available up to several kV and several hundreds Amps, the switching times are not sufficiently fast. For Si MOSFETs, instead, the on-state resistance is in the range of several hundreds mΩ, which can induce a relatively high voltage drop for a low impedance system.

The IA is also a very interesting option to upgrade the older existing kicker system. An example is the kicker system of the PS accelerator, which was built is 1970s and, due to the need for maintenance and difficulties to source components, would benefit from the

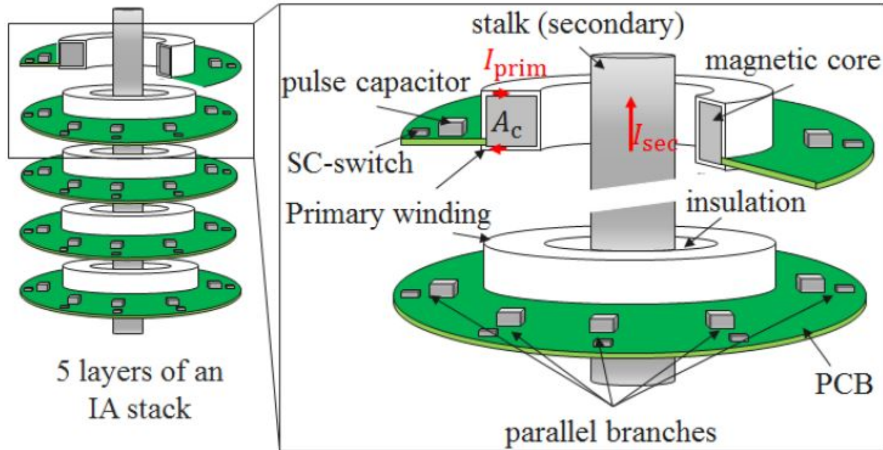


Figure 2.13: Schematic of two inductive adder layers. Reprinted from [47]. © 2016, Kramer *et al.*, licensed under CC-BY-3.0.

substitution with a modern technology. The IA designed for the FCC can be used as a basis and modified to obtain the required output for the PS injection and extraction kicker systems [48]. However, the requirements for rise time of the output pulse of the PS system (i.e., 42 ns - 49 ns) are significantly more challenging than the ones for the FCC system.

Finally, the IA technology is not suitable for kicker systems which require longer pulses, such as SPS and LHC. Nevertheless, a new Marx generator based on SiC MOSFETs is under study for use in SPS and potentially LHC [49]. The specifications of the output pulse are: 3 μs flat top duration, 40 kV, 3.2 kA, 1 Hz repetition rate and 30 ns rise and fall time. The first results with a four-stage Marx generator, operating at 800 V per stage and 2700 A, exhibited promising rise and fall times, indicating that parallel SiC MOSFET technology can be used for replacing thyratrons in kicker applications. However, additional tests need to be performed to validate this technology.

In order to evaluate the reliability of commercial SiC MOSFETs technology for applications in high-energy-accelerator radiation environments, several commercial SiC MOSFETs were tested with high-energy protons and neutrons, which are the most dominant particle species in this environment. The devices under tests were selected considering the requirements for the inductive adder. Among the tested devices, the one from Rohm with reference number SCT3030KL was identified as the most interesting solution for this application. The experiments and the results are discussed in Chapter 5.

3 Background on radiation effects

This chapter focuses on radiation effects on SiC power MOSFETs. In order to comprehend them, firstly the physical mechanisms of radiation interaction with matter are introduced, describing the electronic stopping, the nuclear stopping and the nuclear reaction physics.

Secondly, the radiation effects on electronic devices are discussed, focusing in particular on the SEE mechanisms and relevant radiation environments which can induce SEEs on SiC power MOSFETs (i.e. space, terrestrial atmosphere and high-energy accelerator environments). Some background concepts for radiation testing are also given, in order to understand the experimental results in Chapter 4 and 5.

The last section of this chapter reviews the scientific literature about SEEs on power diodes and MOSFETs; from the first studies with Si components, toward the most recent results obtained from experimental campaign and simulations on SiC devices.

3.1 Particle interactions with matter

Understanding of the physical SEE mechanisms in SiC MOSFETs must be based on a familiarity with the fundamental processes by which particles interact with matter. First of all, two broad categories for particles can be defined, as in Table 3.1 [50]: charged radiation and non-charged radiation. Depending on the type of particle and its energy, the interaction occurs via different mechanisms. The most relevant for this work are the interactions of heavy-ions, atmospheric neutrons and high-energy protons (energy of 200 MeV) as summarised in Table 3.2. An overview is briefly given below, whereas the mechanisms for electrons and electromagnetic radiation interactions are not discussed, but a complete description can be found in [50].

Table 3.1: Classification of charged and uncharged radiation.

Charged particulate radiation	Uncharged radiation
Heavy-ions Protons Electrons	Neutrons EM radiation (X-rays, γ-rays)

Table 3.2: Interaction mechanisms.

Electronic stopping	Nuclear stopping	Nuclear reactions
Heavy-ions High-energy protons	Heavy-ions High-energy protons	Heavy-ions High-energy protons Atmospheric neutrons

3.1.1 Stopping power

For charged particles the stopping power S is defined as the average energy loss of a particle per unit path length, measured for example in [keV/um] [50]:

$$S = -\frac{dE}{dx} \tag{3.1}$$

sometimes it is divided by the density of the target and referred as a mass stopping power. By definition S is a force and not a power, and it is also sometimes referred to as stopping force [51].

The stopping power is the sum of three main processes: (i) electronic stopping, (ii) nuclear stopping and (iii) radiative emission of energy. The first describes the slowing down due to the inelastic collisions between the orbital electrons of the absorber and the particle moving through it. The second refers to the elastic collisions between the particle and the nuclei of the absorber. The third can be neglected for ion energies well below the speed of light, as in the cases discussed in this work. Therefore the stopping power can be written as the sum of two independent components [52]:

$$S = S_{electronic} + S_{nuclear} \tag{3.2}$$

Generally, for low energy ions, the nuclear stopping is dominant, whereas for high energy ions the energy is mostly lost through electronic stopping [53]. At intermediate energies both mechanisms are important. A schematic representation is shown in Figure 3.1, while the two mechanisms are further described in the next sections.

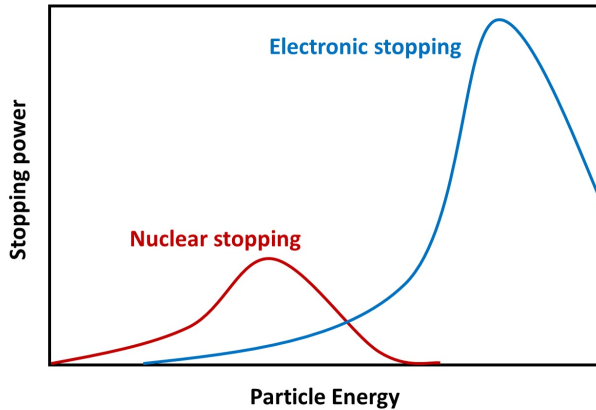


Figure 3.1: Schematic representation of the nuclear stopping and electronic stopping contributions to the stopping power, as function of the particle energy.

3.1.2 Electronic stopping

Charged particles interact with matter primarily via Coulomb forces between their positive charge and the negative charge of the orbital electrons within the medium they cross [50]. Any time the particle passes in the vicinity of an orbital electron, the latter feels an impulse of attraction due to the Coulomb force. Depending on the proximity of the encounter, this impulse can excite the valence electron to a higher shell within the absorber atom or remove it completely, ionizing the atom. The second process is called direct ionization.

The energy transferred to the electrons is coming from the incoming charged particle, which progressively loses energy through multiple interactions, decreasing velocity along its trajectory, until it stops. At the beginning, the particle track is not greatly deflected by any of the encounters which occur isotropically, and it tends to be quite straight. As the energetic particle slows down, it may deviate more easily from this linear path, particularly near the end of the range (i.e., the maximum length of penetration).

The products of these interactions are either excited atoms or ion pairs formed by a positive ion of the medium and a free electron. The positive ion usually recombines to form a neutral atom, whereas the free electron in some cases has enough kinetic energy to create additional ions. These energetic electrons, often called delta rays, are emitted in the surrounding volume and interact with other atoms, releasing their energy and producing additional tracks. Usually, they have a smaller range respect to the primary charged particle, so the additional tracks are created as clusters closed to the primary one. These delta rays represent an indirect process by which the primary particle releases its energy in the medium (i.e. indirect ionization). For charged particles, the specific energy loss can be described with the Bethe formula as [50]:

$$-\frac{dE}{dx} = \frac{4\pi e^4 z^2}{m_0 v^2} NB \tag{3.3}$$

where

$$B = Z\left[ln\left(\frac{2m_0v^2}{I}\right) - ln\left(1 - \frac{v^2}{c^2}\right) - \frac{v^2}{c^2}\right] \tag{3.4}$$

here, v represents the velocity and z the charge of the primary particle, N is the density number and Z the atomic number of the absorber atoms, m_0 is the electron rest mass, e is the electronic charge and I represents the average excitation and ionization potential of the absorber.

The Bethe equation is valid for charged particles at larger velocities in respect to the velocity of the orbital electrons of the absorbing atoms. For lower particle energies, where the charge exchange with the absorber becomes important, the Bethe formula begins to fail. The positive particle will tend to pick up electrons from the absorber, until it becomes a neutral atom. Near the end of the track, the charge and therefore the electronic energy loss are reduced, and the curve falls off. A plot of the specific energy loss along the track is known as a Bragg curve; an example for an alpha particle at energy of 5.49 MeV traveling in air is shown in Figure 3.2.

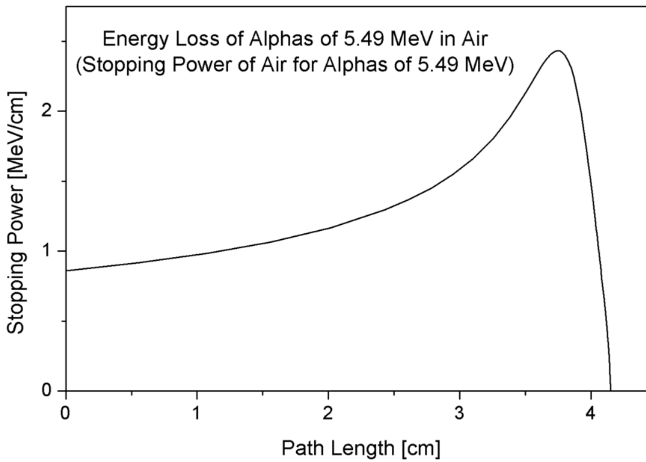


Figure 3.2: Bragg curve for an alpha particle in air. Image from the public domain.

3.1.3 Nuclear stopping

The incoming charged particle can also interact with the nuclei of the target which is surrounded by an electrostatic barrier, called the Coulomb barrier [54, 55]. If the energy of the incident particle is below the energy necessary to overcome the Coulomb barrier, then the particle is scattered by elastic collisions with the nuclei of the target atom. The theoretical framework behind the nuclear stopping describes the classical collision between two charged particles and it will not be discussed in this context. However, a simplified representation is given in Figure 3.3. Due to the interaction, the incoming particle is deflected by and angle θ and part of its kinetic energy is transferred to the target atom. If this energy is higher than the bonding energy of the lattice, then the atom is released (called primary recoil or knock-on atom) and can produce additional subcascades if it has high enough energy.

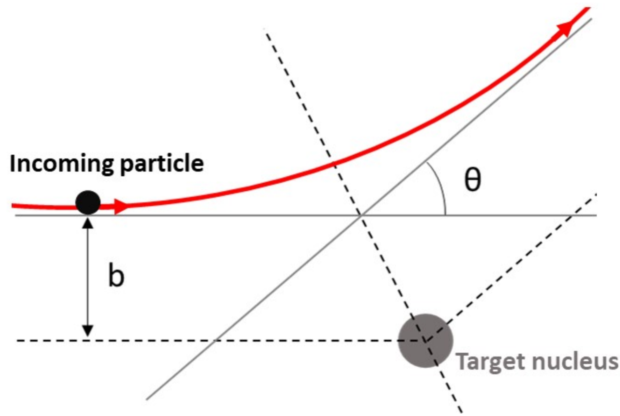


Figure 3.3: The incoming particle is deflected of an angle Θ, which depends on the impact parameter b, the electric charges of the incoming particle and target nucleus, and their relative velocity.

3.1.4 Nuclear reactions

Finally, if the energy of the incident particle is sufficient to overcome the Coulomb barrier of the target atoms, or if the particle has no charge as in the case of a neutron, nuclear interactions can occur including fission and spallation reactions, which causes the fracture of the nucleus of the lattice atom [50, 56]. The recoiling products of the fission and spallation reactions can also produce ionization tracks and are part of the class of indirect ionization processes.

An ion may exchange energy, momentum, even nucleons with the target nucleus; however, for charged ions, these processes are more likely to happen at high energy levels, due to the electrostatic forces which separate the nuclei.

Conversely, neutrons release their energy only through indirect ionization. In fact, neutron particles must first undergo interactions which alters their properties, transferring full or partial energy to the electrons, the nuclei of the medium atoms or the recoils produced by the nuclear reactions. Consequently, these products will ionize the atoms of the absorber. The interactions between neutrons and the target nuclei include elastic and inelastic scattering, neutron captured and fission reaction [50, 57]. The resulting nuclei after the inelastic scattering (i.e., spallation reaction) or neutron capture might be at an excited state, which eventually de-excitate via different modes, including alpha and beta decay and gamma-ray emission. The neutron cross-section for nuclear reactions depends on the particle energy and on the target isotope [58].

3.2 Consequences of irradiation

The incident radiations can lose energy interacting with the target atoms through different physical processes. Eventually, the transferred energy can ionize the atoms of the medium either through direct ionization via electronic stopping of the incident particle, or through indirect ionization from electronic stopping of recoiling products.

In semiconductors and dielectrics, the electron which is ionized and removed from its bound state, leaves a hole behind which appears to have a positive charge, due to the fact that the ripped electron is not screening anymore the nucleus charge of the original atom. Therefore holes can be studied as virtual particles with a positive charge, which can move among nearby atoms being filled by bound electrons, leaving in turn hole behind. Depending on the target material, the ionization process can have a wide range of consequences, with effects more or less severe. For electronic components, three different categories of effects are identified: single event effect (SEE), total ionizing dose (TID) and displacement damage (DD). While SEEs are caused by the interaction of a single energetic particle, TID and DD are instead cumulative effects related to the ionizing dose and the particle fluence respectively. The present work focuses on SEEs, hence the effects related to the TID and DD are not discussed in detail the present study.

3.2.1 Single Event Effects

SEEs are radiation effects produced by the passage of a single energetic particle through microelectronic and optoelectronic devices/components, causing tracks of charge carriers (i.e., an electron-hole (e-h) plasma) and consequently the disturbance of the normal operation [59, 60]. For old technologies, SEEs were usually dominated by direct ionization processes involving heavy-ions, since the threshold LET for SEE was below the LET of protons and electrons [61]. However, to push for higher performance devices and integrated circuits (ICs), transistors and other elements of devices have scaled to progressively smaller sizes [62]. This scaling phenomena have reduced the critical charge necessary to produce SEEs, therefore the threshold LET necessary to initiate an SEE. Nowadays, some devices have reached dimensions such that direct ionization from energetic protons [63, 64], energetic muons [65] and even energetic electrons [66] can produce SEEs.

A particle striking into the depletion region of a reversed-biased diode or of a transistor in off-state generates e-h pairs which are separated by the intense electric field applied in that region. The drift of the electrons toward the positive electrode and of the holes toward the negative one generates a current pulse, which can induce a transient or a permanent effect. This ranges from recoverable corruption of data to complete and irreversible loss of the system, depending on the target device. The impact of the SEE can expand to the IC level and affect subsystems and systems. A list of common SEEs is shown in Table 3.3 for completeness. However, only single event burnout (SEB), single event leakage current (SELC) and single event gate rupture (SEGR) are relevant for this work, and are further discussed later in this chapter, in Section 3.5.

3.2.2 Total Ionizing Dose

The Total Ionizing Dose (TID) is a cumulative effect caused by ionizing radiation which induces the creation of excess charge in the dielectric layers used for insulation in electronic devices, as for example the silica insulator (SiO_2) of MOS technology. When a MOS device is irradiated, e−h pairs are created in the dielectric. For an oxide under bias, the

Table 3.3: List of Single Event Effects

SEE	Acronym	Effect
Single Event Burnout	SEB	Destructive failure. It occurs in power devices.
Single Event Gate Rupture	SEGR	Conductive path through a damaged gate dielectric. It occurs in power devices.
Single Event Leakage Current	SELC	Permanent increase of the gate and drain leakage currents. It occurs in SiC power devices.
Single Event Hard Error	SEHE	An irreversible change in operation typically associated with permanent damage to one or more elements of a device (e.g., gate oxide rupture)
Single Event Upset	SEU	A bit flip in a logic memory.
Multiple Cell Upset	MCU	Bits in multiple cells flips.
Multiple Bit Upset	MBU	Multiple-cell upset in which two or more error bits occur in the same word.
Single Event Transient	SET	Current or voltage transient.
Single Event Multiple Transient	SEMT	Multiple current or voltage transients.
Single Event Latchup	SEL	An anomalous current path is formed which can cause an abnormal high-current state in a very short time scale. Recovery requires power cycling the device. Permanent damage may also occur.
Single Event Functional Interrupt	SEFI	A soft error that causes the component to reset, lock-up, or otherwise malfunction.

electrons which do not recombine are typically drifted and eventually collected in the order of picoseconds. The holes, instead, have much lower mobility in respect to electrons in SiO_2 and, in case of positive bias during the exposure, transport dispersively towards the Si/SiO_2 interface, where a fraction is trapped at defects sites. Over time, this cause a positive charge built-up in the insulator which alters the electric field. The macroscopic consequence of the trapped charge is the shift of the threshold voltage, which can have a drastic impact on the proper operation of the electronic system in which the MOS is integrated. With increasing temperature, the trapped holes can escape the defects sites and drift out of the insulator, reducing the TID effects; this process is known as annealing. The TID effects in MOS and bipolar devices have been extensively reviewed by Fleetwood in [67] and [68], providing an overview of the progress among the last fifty years.

3.2.3 Displacement Damage

The bombardment of a target with heavy-ions, neutrons and protons but also high-energy electrons and gamma-rays can induce DD effects [69]. This is a cumulative long-term non-ionizing effect, characterised by the displacement through nuclear scattering, fission and nuclear reactions of some of the target atoms from their original position. This effect can modify the electrical and optical properties of the target material. In semiconductors, an atom displaced from its original lattice position, creates a vacancy (the absence of an atom from its lattice position) and an interstitial (an atom in a non-lattice position). The combination of a vacancy and an adjacent interstitial is known as a Frenkel pair. These defects in the crystal lattice lead to the generation of new energy levels in the bandgap of the semiconductor, which act as traps and can be occupied and left by the carriers, degrading the electrical and optical properties of the irradiated device [70]. In insulators, the DD may induce the creation of low-resistivity paths of defects, which, under high bias condition, can lead to the increase of leakage current and eventually cause dielectric breakdown [71]. A review of DD in devices and materials was done by Srour *et al.* in [72].

3.3 Variety of radiation environments causing SEEs

The variety of radiation environments that can cause SEEs increases as technology advances. In this section, an overview of the radiation environment encountered for space, ground, avionic and high-energy accelerator applications of SiC power devices are presented. Radiation tests and simulations are needed in order to study the reliability of the commercial technologies in these environments.

3.3.1 Space radiation environment

In space, SEEs can be caused by ionizing radiation produced by three different sources [73, 74]: galactic cosmic rays (GCRs), solar energetic particles (SEPs), and radiation belt particles (Van Allen Belts) trapped in space around the Earth. The three sources are illustrated in Figure 3.4.

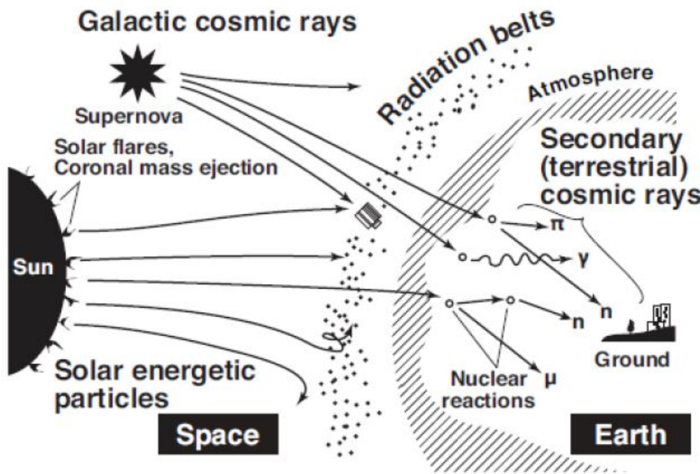


Figure 3.4: SEE in space are caused by three different sources: galactic cosmic rays, solar energetic particles and Van Allen radiation belts, after [75]

SEPs are products of dynamic solar activities and they are connected with the eleven-year cycle of the Sun, which culminates with a dramatic increase of the solar flare intensity, especially during periods when there are numerous sunspots. A solar eruption is shown in Figure 3.5 (image from NASA/SDO/Steele Hill). In turn GCRs are produced by events outside the solar system but primarily within the Milky Way galaxy, such as supernova explosions, pulsars, stellar flares and the explosions of galactic nuclei. GCRs are composed by high-energetic-heavy ions of elements that have had all their electrons stripped away and that are traveling through the galaxy at nearly the speed of light. The distribution of particle species in GCRs is approximately 90 % of protons, 9% of alpha-particles and the residual 1% are heavier atomic nuclei with a wide range of LETs [73]. They can pass practically unimpeded through a typical spacecraft, inducing SEEs.

Because of the interaction with the Earth atmosphere, some particles (most GCRs) can be trapped, forming the Van Allen radiation belts. They have a double-ring structure, with an inner and an outer belt, composed of trapped protons and electrons. The proton distribution, which exhibits a single ring structure and correspond to the inner belt, extends to 4 R_E, where R_E represents the radius of Earth. The energy of the trapped

Figure 3.5: Solar eruption in April 2018. The Earth is superimposed on this image to give readers a sense of the scale. The eruption was about 20 times the diameter of our planet, after NASA/SDO/Steele Hill.

protons is up to GeV and it is sufficient to cause SEE through the indirect ionization mechanism. The trapped electrons also have a double-ring structure [73, 75], with energies up to 100 MeV. Recently, the electrons at Jupiter's belts, which have energy up to GeV, are also attracting attention [76]. These electrons can cause SEEs through the indirect ionization process similar to protons [77].

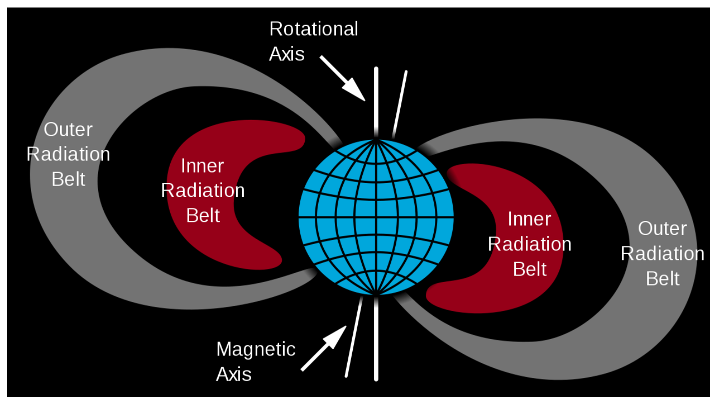


Figure 3.6: Van Allen radiation belts. Image from the public domain.

3.3.2 Atmospheric radiation

The SEP and GRC particles which are not repelled by the terrestrial magnetic field can enter the Earth's atmosphere and react with Oxygen (O) and Nitrogen (N) atoms, creating a shower of secondary cosmic rays. These showers of secondaries can reach the ground, causing SEEs in avionics and ground level applications. The cosmic ray cascades are illustrated in Figure 3.7. The physics of the cosmic ray interaction in the atmosphere has been previously reviewed in many works [78–81] and it is briefly explained below.

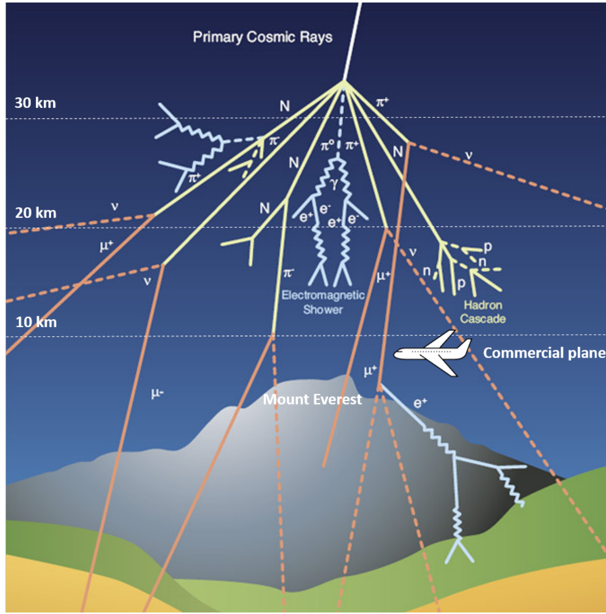


Figure 3.7: Cosmic rays cascade in the atmosphere. Image from the public domain.

The Earth's atmosphere is mostly composed of O and N gases, with variable densities depending on the altitude [74]. The particles with strong interactions, called hadrons, such as nucleons and pions, undergo several collisions and none of the original primaries reach the surface. Instead, they create a cascade of secondaries which consist mainly of pions, muons, neutrons, electrons, and photons. These particles differ in their type of interaction with other particles, their mass and lifetime. The heavier particles are least deflected, causing narrow dense cascades, while light particles form a more diffuse halo. Fever than one in a hundred primary particles create a cascade which reaches the sea level. Indeed, as the particles penetrate the atmosphere, there are also many absorption processes. Most of the particles are lost from the cascade because either they decay spontaneously (i.e., the mean lifetime for pions is in the order of ns, while for muons it is about a μs), or they lose energy in collisions and reach thermal energies before arriving at the surface. The peak of the cosmic ray intensity, and therefore of the atmospheric neutrons, occurs at about 10-25 km, which is critical for avionic applications, being the altitude of many commercial airplane flights [74]. Below, there is a net loss of total particles in the cascades, having, for example, a neutron flux at sea level of 13 n/(cm^2h) for energies higher than 1 MeV (reference conditions at sea level in NYC from JEDEC JESD89A standard [82]). Additional details about the atmospheric neutron spectra are discussed in Section 5.1.2.

3.3.3 The high-energy-accelerator environment

A detailed knowledge of the LHC radiation field is important in order to reduce the risk of SEEs for the electronic systems installed in the underground areas, with a possible direct impact on beam operation and a consequent downtime of the machine. In-depth studies of the radiation field and beam loss productions are required to allow predictions for the future levels for the HL-LHC operations [36] and the FCC project. For this reason,

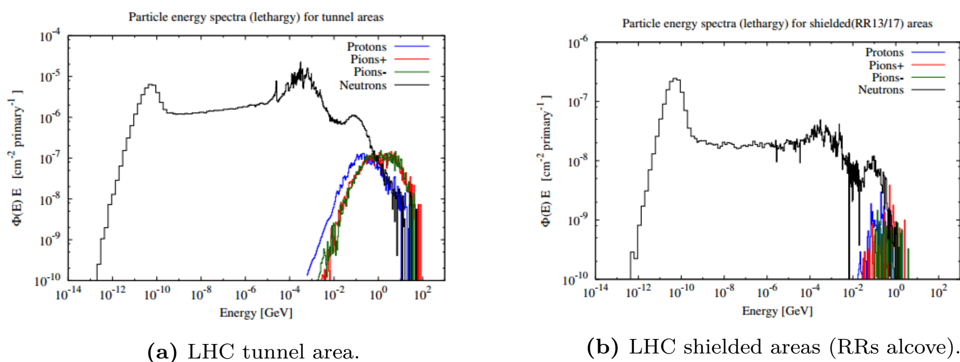
measurements are performed every year and are used as a baseline for the predictive scaling. For the purpose of this study, the present LHC radiation environment was considered as reference for the high-energy accelerator applications.

The sources of losses in the LHC tunnel and in the close shielded areas, can be grouped in three main categories [39]:

- Particles debris generated during the collisions in the experimental caverns;
- Particle showers in the collimation areas, in the absorbers and in the injection/extraction regions;
- Beam-gas interaction inside the beam pipe all around the ring.

The variety of sources create a mixed radiation field composed of charged and neutral hadrons (protons, pions, kaons and neutrons), photons, electrons and muons [37].

For the purpose of radiation tests in a LHC-like environment, hadrons with energy above 20 MeV, defined High Energy Hadrons (HEH), are considered to be equally effective in inducing SEEs due to their similar interaction cross-section that has a rapid decrease below 20 MeV. Moreover, at lower energies, the HEH are no longer able to reach the sensitive area of the devices. Below 20 MeV the contribution from HEH is therefore considered insignificant for the damage on the electronics. Neutrons are not included in this definition since they can contribute also at lower energies. However, the extensive use of concrete in the tunnel walls and in the shielding of the alcoves, induce a significant contribution of thermal neutrons (i.e., energy $\sim$ 0.025 eV). Figure 3.8 (a) and 3.8 (b) show respectively the particle energy spectra for the tunnel and the shielded areas of LHC, where the latter are the zones adjacent to the tunnel with a certain amount of concrete shielding. In the tunnel the HEH fluence is orders of magnitude higher than in the shielded areas, in the order of $10^{10} cm^{-2} y^{-1}$ with energies up to 100 GeV. In the shielded areas, instead, the fluence is dominated by neutrons, with a fraction of charged hadrons ranging from 2-10 % [37].



(a) LHC tunnel area.

(b) LHC shielded areas (RRs alcove).

Figure 3.8: FLUKA Monte-Carlo simulation of the particle energy spectra (lethargy) for RRs (shielded areas) in LHC for a nominal operation at 7 TeV. The spectra are normalized for one proton-proton collision. Reprinted with permission from [38]. © 2011, IEEE.

3.4 Useful concepts for radiation testing

It is known that use of commercial electronic components (COTS) provides several advantages. However, the parts need to satisfy the quality and reliability requirements in order to be qualified for the specific applications. Here quality means the assessment of the manufacturing and test process, evaluating the matching of the qualifications and the presence of faulty parts. With reliability, instead, it is considered the probability of parts to meet the relevant specification over the time, under the worst operational conditions.

In order to study the physical SEE mechanisms and the reliability of SiC power MOSFETs exposed to heavy-ion, neutron and proton environments, radiation tests were performed in different European facilities. This section provides several concepts about radiation testing useful for the comprehension of the results discussed in Chapter 4 and Chapter 5.

3.4.1 Linear Energy Transfer (LET)

An important quantity, closely connected to the stopping power described before, is the linear energy transfer (LET), defined as the amount of energy locally deposited ($\mathrm{d}E_L$) per unit of distance travelled by the ionizing radiation (dl) [50]:

$$LET = \frac{dE_L}{dl} \tag{3.5}$$

The LET is usually expressed in [keV/μm]. The difference between the LET and the stopping power S is the fact that the latter is defined as the average energy loss per unit path length, therefore it also includes the electrons with higher kinetic energy which travel further from the main track (the delta rays). This means that for small target volumes the LET is less than S. Differently, for large target volumes LET and stopping power are considered as equals. This is the case of normal radiation testing procedure, where for most of the devices the target volume size is unknown.

3.4.2 Particle range

The particle range is defined as the total path length travelled by the ion inside the target until it comes to rest. The projected range perpendicular to the surface can also be used to indicate how deep the particle has penetrated in the target.

3.4.3 Cross-sections, failure in time (FIT) and degradation rate

Two standard figure of merits are used to evaluate the probability of destructive failure for SiC power components exposed to radiation environments: the failure cross-section (σ) and the failure in time (FIT) rates, where the second is used only for ground applications. The failure cross-section is defined as the number of failures detected per unit beam fluence:

$$\sigma = \frac{failures}{fluence} \tag{3.6}$$

The FIT rate is defined as the number of failures considering 10^9 hours of operation at a sea level, with a cosmic-rays-induced neutron flux of 13 n/(cm^2h) for energies above 10 MeV (reference conditions at sea level in NYC from JEDEC JESD89A standard [82]).

An additional parameter called degradation rate was also used in this work to evaluate the susceptibility of the devices to leakage current degradation. In this case, the degradation

rate is defined as the difference between the leakage current after and before the exposure, normalized by the fluence and the active area of the device under test (DUT).

3.4.4 Test standards

There is currently no test standard dedicated to radiation tests of WBG power devices. However, during the recent years, several efforts have been done in order to collect information and produce guidelines for the radiation effects community. While waiting for a dedicated document, the standards for radiation tests of silicon power components are commonly used as reference:

- United States military standard MIL-STD-750E M1080.1 [83];
- JEDEC JESD89A standard [82];
- JEDEC JESD57A standard [84].

3.5 SEEs in Si power devices - State of the art

When SiC power devices appeared on the market in 2001, many studies about SEE mechanisms were already available for their Si counterparts. This knowledge was used as a baseline to investigate whether the same radiation effects were observed also in SiC devices or not. During the last 20 years, a lot has been done around this topic, differences among effects observed in Si and SiC devices have been reported and some new SEE mechanisms have been identified for SiC components. As the basic understanding of SEE mechanisms in Si power devices is required in order to comprehend the susceptibilities of SiC power devices, firstly an overview on SEEs in Si in given below, followed by the description of the current knowledge available for SiC power MOSFETs in Section 3.6. A review of SEEs in Si and SiC power devices was published by Lauenstein in [8].

3.5.1 Overview of SEEs in Si power MOSFETs and diodes

Si power MOSFETs are susceptible to two different catastrophic failure modes: SEB and SEGR. The first observations on SEB in Si power MOSFET were reported by Waskiewicz *et al.* in 1986 [85], while exposing different commercial power MOSFETs to a Californium-252 ion source. Later, a non-destructive test setup has been developed in order to allow measurement of the SEB cross-sections [86]. Since SEB were observed also with low LET ions (< 10 MeVcm^2/mg), it was hypothesised that also recoil atoms induced by high-energy neutrons and protons were able to cause SEB, as Oberg *et al.* reported later in 1996 [87]. The first review papers on SEB and SEGR in Si vertical planar MOSFETs were published in 1996 by Titus and Wheatley [88] and by Johnson *et al.* [89]. Since then, SEB and SEGR have been extensively studied, more recent and updated bibliography on this subject was provided by Titus in [90]. Furthermore, a review of heavy-ion induced SEEs in Si trench MOSFETs was published by Galloway in [91].

Finally, SEB can occur also in BJTs [92, 93], power p-n diodes [94−96] and Schottky diodes [97−100], whereas IGBT are susceptible to SEGR and SEL [101−103]. The SEE mechanisms for Si MOSFETs and diodes are summarized in the next sections.

3.5.1.1 SEGR mechanism in Si power MOSFETs

This section describes three different SEGR mechanisms proposed for Si power MOSFETs: the dielectric breakdown, the micro-break and the thermal runaway.

Dielectric breakdown. The first and most well-known mechanism for SEGR in Si power MOSFETs exposed to heavy-ions is the oxide breakdown. As firstly proposed by *Fischer* [104], it involves both the interaction of the primary ion with the gate oxide and the charge ionization in the epitaxial layer of the device. The critical electric field required for dielectric breakdown, is temporarily reduced by the passage of the impinging particle, through a mechanism which is still unclear, but different hypothesis were formulated and three of them are presented below.

The first hypothesis, states that the oxide electric field is enhanced by the ion strike [105, 106]. For a n-type VD-MOSFET in off-state with a positive drain-source bias, the vertical drift field in the epi-layer causes the electrons and holes to be transported from the oxide/silicon (Si/SiO_2) interface toward the drain contact and the body region, respectively. However, electrons are transported faster than holes, therefore a higher concentration of positive charges is created at the Si/SiO_2 interface. This accumulation

of holes induces negative mirror charges in the oxide, creating a transient increase of the electric field in the gate oxide, in addition to the applied one, causing the dielectric breakdown if a sufficiently high electric-field strength is reached. The coupling of the drain voltage with the Si/SiO_2 interface is a function of the ion penetration range, the strike location [89], the angle of incidence and the drain-source bias during the exposure [8, 107]. The worst condition for SEGR occurs when the ion strikes the neck or JFET region (the area between the p-well), with an angle parallel to the vertical electric field, penetrating completely through the epitaxial layer. In addition, considering a given ion species, the energy which results having the Bragg peak at the interface between the epitaxial layer and the substrate, represents the worst-case condition, due to the increasing LET along the epitaxial layer [108, 109]. Conversely, the e-h pairs generated in the highly-doped substrate do not contribute to the SEGR mechanism.

The second hypothesis for the oxide electric field to approach breakdown strength, was formulated by Boruta *et al.* [110]. They proposed that among the carriers generated by ionization in the oxide, the electrons are swept away faster than the holes, creating net oxide charges which induce non-uniform electric field in the oxide, which could induce a breakdown at a lower voltage respect to the situation with a uniform electric-field.

A third hypothesis, formulated by Carlotti *et al.* [111], proposed structural modifications at the Si/SiO_2 interface which result in a Si bump into the oxide, creating a high-curvature region, inducing intense local electric field.

Micro-break. Scheick *et al.* [112] proposed two additional SEGR modes for Si power MOSFETs; the micro-break and the thermal runaway. The micro-break mechanism was observed in devices which exhibited a multitude of small-magnitude SEGR events accumulated during a single exposure. This mode is characterised by a slow increase of the drain leakage due to small steps in the order of few nA or tens of nA (for those specific testing conditions), which are quantified as micro-breaks and do not recover once the irradiation is stopped. The proposed model for enhanced current associated with a micro-break, is the tunneling of electrons from trapping sites in the oxide into the conduction band or from the metalization into the oxide conduction band (or both). The defects created by the displacement damage induce by the ion strike in the oxide, represent damage sites with a reduced potential barrier, which increase the probability of electron tunneling. The micro-break SEGR mode requires lower electric-field strength in respect to massive SEGR, and therefore can occur at lower bias voltage.

Thermal runaway. Micro-breaks may alter the device operation only slightly, but they represent a significant risk to the part reliability. Scheick *et al.* [112] showed how the micro-break evolved into a thermal meltdown when additional stress was applied during the post-irradiation analysis. Even though the device is barely affected by the initial micro-break, the defects which contribute to the enhancement of current through the tunneling mechanism (which is dominant at lower temperatures), can also increase the current due to thermally induced mechanism (which becomes dominant at higher temperatures). Initially the current flowing through the oxide is increased by the tunneling mechanism, by Joule heating the temperature rises and it increases the thermal conductivity of the oxide by enhanced thermal generation of carriers, which in turn causes a further increase of the leakage current through the oxide. This regenerative process can induce an unstable condition called thermal runaway and eventually lead to the oxide meltdown. Therefore, the ion interaction can reduce the electric field needed to cause such effect, having a post-IV induced thermal runaway.

3.5.1.2 SEB mechanism in Si power MOSFETs

Multiple works discuss the SEB mechanism for Si power MOSFETs [113−117]. In this case, the SEB mechanism involves the parasitic BJT, which is an inherent structure formed in the vertical design of a power MOSFET between the n+ source (emitter), the p-body (base), and the epitaxial layer (collector) (for a N-type MOSFET, as described in 2.2.3). Figure 3.9 shows a quasi-stationary simulation of a Si MOSFET I-V characteristic at different stages of breakdown (image from [90] after [118]).

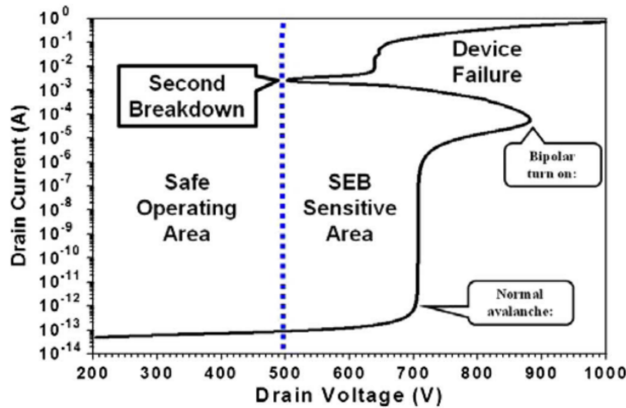


Figure 3.9: Quasi-stationary simulation of a Si MOSFET I-V characteristic at different stages of breakdown. Reprinted with permission from [90], after [118]. © 2013, IEEE.

Considering firstly this characteristic, independently from the ion strike, it is observed that when the drain-source bias reaches a certain level, the MOSFET is driven into avalanche breakdown mode (at 708 V in this example), having a rapid increase of the drain current, with a small increase of the drain voltage. As the drain current increases, the passage through the p-body region causes a voltage drop which, if higher than the built-in potential ($\sim$ 0.7 V), induce the activation of the parasitic BJT. The process becomes self-sustaining and substantially higher current flows along this path, and through the source [90]. Rapidly the device reaches a condition which induces a second breakdown, characterised by a sudden decrease in the blocking voltage capability and an uncontrolled current increase, which ultimately causes the catastrophic failure of the device.

When a heavy-ion with sufficient LET crosses the sensitive regions of a MOSFET biased in its off-state condition, a certain amount of charge is created. If the induced current is sufficiently high, this event induces a transition of the device from its normal off-state blocking voltage into its bipolar turn-on state or into its second breakdown state, inducing a destructive SEB. However, the transition process and the positive feedback loop can be interrupted using circumvention techniques, which quenches the drain current before the second breakdown occurs, as firstly demonstrated by Oberg and Wert [86]. This effect is achieved using an external resistor in series at the drain, which causes a voltage drop and a momentarily reduction of the drain bias, sufficient to stop the second breakdown [119]. Based on these considerations, a non-destructive circuit for SEB test with Si power MOSFETs was developed and its commonly used, as also reported in the test standards [83]. Differently, as discussed later in section 3.6.3.2, it is not possible to design a non-destructive circuit for SEB test of SiC MOSFETs, due to the higher energy stored in the parasitic capacitance of the device.

3.5.1.3 SEB mechanisms in Si-based PiN and Schottky diodes

SEB induced by cosmic-rays in Si-PiN diodes was firstly reported in 1994 by Kabza *et al.* [120] and Zeller [121]. The failure was attributed to a localized breakdown in the bulk of the device, but the exact mechanism was not identified. As no parasitic BJT structure is present in diodes, the mechanism has to be different from the one described for Si MOSFETs. Furthermore, the failure could not be prevented using external resistors in series, suggesting that the capacitive energy stored in the p-n junction could provide sufficient current density for the destructive event, with no possibility to limit it. Simulations performed later by Walker *et al.*, suggested a possible mechanism for SEB, involving a thermal feedback in which the heat generated from the impact-ionized charge current results in temperature rising to the level at which the intrinsic carrier concentration begins to dominate. This increased current sets off the feedback loop by continuing to raise the temperature and thus the intrinsic carrier current until burnout occurs [8, 122]. Albadri *et al.* published a review of the research on SEB mechanisms in PiN diodes in [95]. Destructive failures have been reported also for Si-Schottky diodes in [98−100]. The pin, Schottky and JBS diode structures are shown in Figure 3.10, after [8].

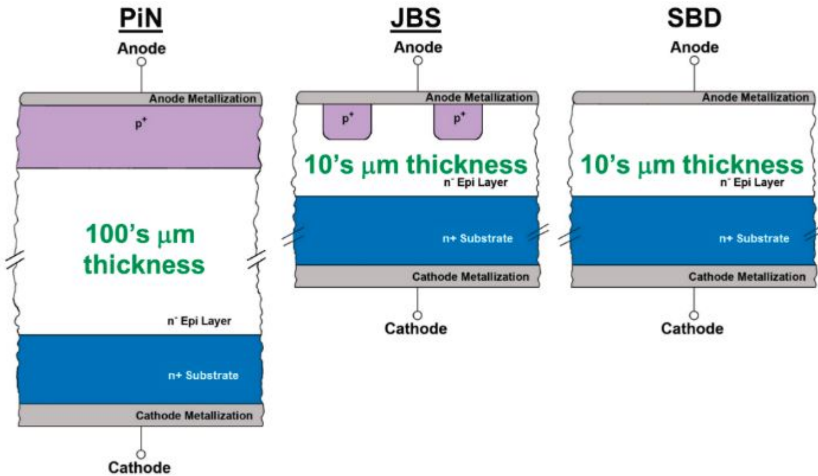


Figure 3.10: Pin, Schottky and JBS diode structures, after [8].

3.5.1.4 Leakage current degradation in Si devices

For Si components, the single particle induced degradation (SELC) is less common in respect to SiC, and it is generally not considered as an issue. However, in the following two works degradation was observed also in Si components.

Casey *et al.* [100] reported leakage current degradation in Si-Schottky diodes. Casey performed a test campaign with 45 different Si-Schottky diodes from 10 manufacturers tested using xenon ions at energy of 10 MeV/amu (LET of 59 MeVcm^2/mg). Non-catastrophic effect, characterised by an increase of the leakage current degradation was observed in approximately one quarter of the diodes. Among those, only few were seriously damaged, with leakage level out of specifications after a Xe fluence of 10^6 ions/cm^2.

During terrestrial neutron experiments, Asai *et al.* observed that the currents in Si IGBT and Si MOSFET increased step by step in a staircase pattern [123]. Asai called this effect “micro-burn”, which however has not been observed in SiC MOSFETs and diodes.

3.6 SEEs in SiC power devices - State of the art

3.6.1 Overview of SEEs in SiC power MOSFETs and diodes

The susceptibility of SiC devices to SEEs was firstly discovered in SiC power diodes, as they became commercially available about ten years before SiC MOSFETs. The very first SEB in SiC devices was observed in Schottky diodes during displacement-damage experiments performed with protons by Scheick *et al.*, and also was confirmed with heavy-ions in the same study [124]. Additional experiments with heavy-ions revealed a non-catastrophic damage observed at lower bias voltage in respect to the SEB threshold, characterised by a permanent leakage current increase in the device [125, 126]. Once SiC power MOSFETs became available on the market, their susceptibility to both the SEB and the leakage current degradation was observed with heavy-ions [99, 127−129]. This effect was recently named Single Event Leakage Current (SELC) [130]. Furthermore, atmospheric neutrons were also reported to cause destructive failure through recoiling atoms produced by the elastic and inelastic reactions with the SiC-lattice [131−135], and by protons through fragments of spallation reaction. However, at the time of writing this work, degradation has not been reported for proton and neutron irradiations.

In the next sections, first the heavy-ion induced SEEs are discussed for SiC diodes, then for SiC MOSFETs. In the case of SiC MOSFETs, SEEs induced by atmospheric neutrons and protons are also presented. A review of SEEs in WBG (i.e., SiC and GaN) power devices have been compiled by Lauenstein in [8].

3.6.2 SEEs in SiC power diodes

Depending on the beam parameters and the reverse bias (V_R), three different responses can be observed in the reverse leakage current (I_R) of SiC Schottky diodes exposed to heavy-ions, as shown in Figure 3.11 [125, 126]. At low reverse bias, enhanced charge collection is observed. In this case, I_R is higher in respect to the effect attributable to the ionization, however no permanent damage is observed. At higher reverse bias during irradiation, a permanent increase in I_R is measured. This effect is usually referred to as leakage current degradation or SELC. At even higher bias there is the region of the destructive SEB. The same has been observed also for PiN and JBS diodes [6, 129].

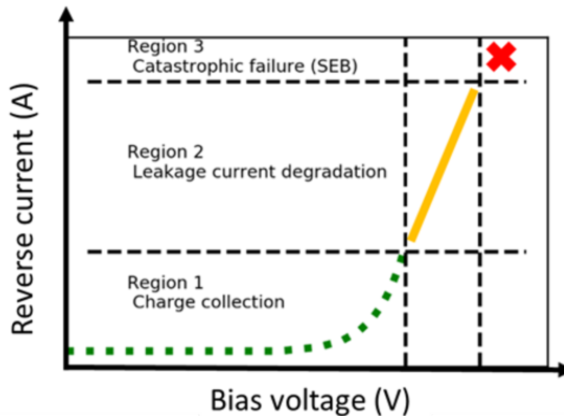


Figure 3.11: Different regions of response observed for SiC Schottky diodes under heavy-ion exposure, remade after [126].

Even though the degradation effect is non-destructive, the device operation is altered, and it complicates the assessment of radiation reliability for the tested parts. The threshold for SEB becomes difficult to identify, due to the increasing leakage induced by degradation. The device eventually fails due to the cumulative damage, before a minimum fluence required to identify the SEB threshold is reached. However, despite the difficulties to identify the minimum threshold for SEB, the maximum SEB cross-sections (when the destructive failure is instantaneously observed as soon as the DUT is exposed to the beam), can still be experimentally measured [8].

Witulski *et al.* irradiated 1.2 kV junction barrier Schottky (JBS) diodes with different ions, and mapped the dependency of the SEE mode thresholds on bias and LET, as shown in Figure 3.12 [136]. Leakage current degradation was observed for LET as low as 3 MeVcm^2/mg at V_R below device specifications. LET values above 10 MeVcm^2/mg, immediate SEB were observed at V_R lower than 50% of device specifications.

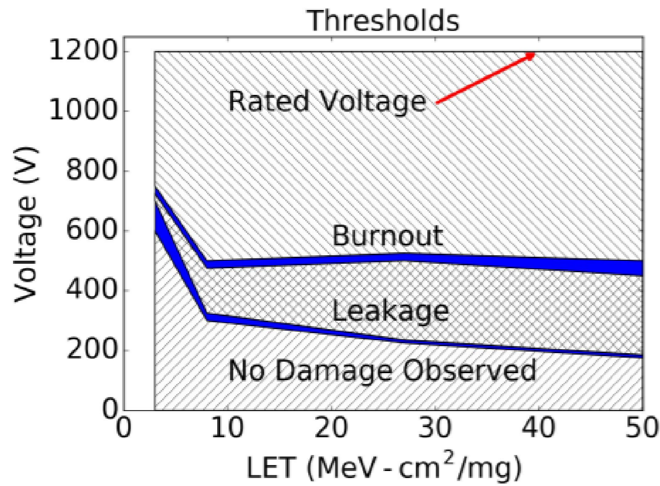


Figure 3.12: Measured thresholds for SEEs in SiC JBS diodes as a function of the ion LET and the reverse bias (V_R). The width of the line indicates minimum and maximum voltage at which the effect was observed. Reprinted with permission from [136]. © 2018, IEEE.

3.6.2.1 SELC SiC power diodes

The degradation effect or SELC is dependent on the V_R, the fluence and the ion LET. Differently with respect to the case of Si power components discussed in section 3.5.1.3, the degradation is always observed in SiC devices exposed to heavy-ions with a minimum LET of 10 MeVcm^2/mg. Depending on V_R, even a single ion strike can induce a degradation step in the I_R that exceeds the specification level. However, a minimum V_R threshold is required in order to observe degradation, which varies depending on the ion species and energy. Kuboyama [126] and Kamezawa [125] demonstrated that the peak power (P_P) resulting from the ion strike can be used to normalize the threshold voltage for damage, where the peak power is proportional to the square of the V_R and the LET as [126]:

$$P_P[W] \propto V_R^2 \cdot LET \tag{3.7}$$

concluding that the leakage current path is introduced by a thermal effect (local heating).

Working with these concepts, Johnson *et al.* performed numerical simulations of SiC Schottky diodes rated for 600−1700 V, concluding that the diode active layer does not influence the total instantaneous power [137]. In fact, due to the redistribution of the electric field during the ion strike at a given bias, the total instantaneous power becomes a constant value. Therefore, the degradation threshold is found to be independent of device parameters, including the breakdown voltage and the epitaxial depth and doping density, and to be only a function of the ion LET, voltage bias and material properties [137, 138]. This means that de-rating devices with higher breakdown voltage (lower epitaxial doping density or greater epitaxial depth) gives no advantage in preventing degradation in respect to using devices specified for lower breakdown voltages, as the threshold is representative of the characteristics of 4H-SiC itself. To mitigate the problem, Abbate *et al.* suggested the reduction of the substrate doping by a factor of two, to limit the diode current and therefore the maximum temperature [139].

Supporting the hypothesis of the thermal effect, Javanainen *et al.*, performed molecular dynamic (MD) simulations showing that amorphous regions appear along the ion track starting from a certain value of applied bias, below the one required for destructive failure [140]. However, the material modifications induced by the heavy-ion strike in biased SiC power devices, are still a matter of discussion. Laser irradiation were used to study the phase separation of SiC, providing also insight into the possible effects that the localised heat generation caused by the heavy-ions could have on 4H-SiC crystal [141].

Finally, Lauenstein reported that the degradation onset was observed at a lower reverse bias in Schottky diodes compared to PiN ones [6]. However, among the Schottky devices, the same threshold was observed for devices rated for different voltages (i.e. from 650 V to 1700 V), confirming that the degradation might be related to material properties rather than electric field strength.

3.6.2.2 SEB in SiC power diodes

Schottky and PiN diodes with different voltage ratings and produced by different manufacturers, were observed to experience SEB at a similar fraction of their rated voltages, suggesting a strong dependence on the electric field [6].

The underlying SEB mechanism in SiC Schottky diodes was suggested by Kuboyama *et al.* in [142] based on the previous research performed by [126, 136, 143, 144], and summarized by Lauenstein in [8]. Kuboyama identified the roles of impact ionization and electron tunneling, and the mechanism of the electric field clamping at the Schottky contact, in triggering thermal runaway and SEB. Figure 3.13 shows the carrier densities, temperature, and electric field near the Schottky contact, obtained by ECORCE TCAD simulations [145], and their step-by-step interactions, in order to understand the mechanism of thermal runaway [142].

1. In Step 1, the recombination of electrons and holes generated by the heavy-ion track is higher at the contact in comparison with the area below it ($\sim$ 29 nm). The reduced carrier density increases the electric field at the contact, which initiates the impact ionization process.

2. In Step 2, the electric field is clamped at the Schottky contact. As a result of the impact ionization, the density of holes at the contact surface exceeds the one below it, clamping the electric field at a value of $\sim$ 4 MV/cm (in agreement with Witulski [136]), and sustained for at least 200 ps. This event occurs as a result of

impact-ionized charge due to the high field. This process sets up an opposing field by increasing the hole concentration at the contact, inducing a Joule power density which increases the temperature.

3. In Step 3 the thermal runaway is activated. The temperature is rapidly increased, which induce the injection of more electrons from the Schottky contact and the recombination, reducing the high concentration of holes. At this point, the thermal runaway process is establish due to the positive feedback of the Joule heating and increased electron injection, inducing the destructive SEB.

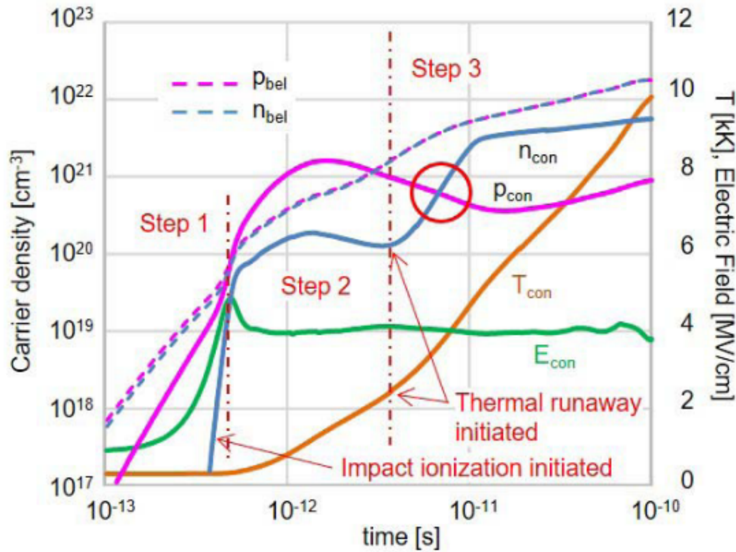


Figure 3.13: Simulations of the SEB mechanism in SiC Schottky diode, divided in three steps. The picture shows the time evolution of the following variables at the Schottky contact: temperature ("T_{con}", orange), vertical electric field ("E_{con}", green), electron and hole carrier density ("n_{con}", blue and "p_{con}", magenta). In addition, the carrier density below the contact (29 nm) are indicated as n_{bel} and p_{bel} (blue and magenta broken line). Reprinted with permission from [142]. © 2019, IEEE.

Furthermore, Shoji explained that the peak electric field strength in SiC power devices ($\sim$ 4 MV/cm) is ten times higher than in Si devices ($\sim$ 0.4 MV/cm), resulting in a heat generation density in SiC devices about 100 times higher than in Si ones [143] (as the Joule power density is proportional to the square of the electric field). This leads to a much more rapid increase in lattice temperature during an ion strike, supporting the conclusion that the higher sensitivity of SiC devices to SEB is caused by the significantly higher heat-generation density compared to Si devices.

3.6.3 SEEs in SiC power MOSFETs

3.6.3.1 Single Event Leakage Current - SELC

As SiC diodes, also SiC power MOSFETs are susceptible to leakage current degradation when exposed to heavy-ions. This mechanism was studied in Paper I and Paper II, where the degradation is named SELC [130, 146]. These works analysed the effect of broad-beam and microbeam irradiations for SiC MOSFETs of the 2nd and 3rd generation; as discussed in more details in Chapter 4. The degradation in SiC MOSFETs was previously reported by Mizuta *et al.* [127], Lauenstein *et al.* [129] and Abbate *et al.*[147−149].

As described in Paper I [146], differently from the case of the SiC diodes, two mechanisms of degradation were identified for SiC MOSFETs. Initially, at a sufficiently high V_{DS}, an increase in drain-gate leakage current (I_{DG}) is observed during the exposure, with a current path between the gate and drain terminal and a linear proportionality to the fluence. This effect is non-catastrophic, but it can hamper the device operation. However, also at very low V_{DS}, where the leakage current degradation is limited to tens of nA for a fluence as high as 10^6 ion/cm^2 and it alters the overall function very little, this effect can represent a significant risk to part reliability. In fact, devices with increased leakage experience accelerated damage, resulting in a much earlier device failure. A destructive failure characterised by a complete gate rupture is always observed during post irradiation gate stress (PIGS) test of devices which exhibit this type of degradation [150]. However, a minimum LET is required to observe this degradation. Furthermore, not all the MOSFETs exhibit pronounced I_{DG} degradation, suggesting that this mechanism can be mitigated by design [8]. In Paper II, microbeam studies indicated the JFET region and the adjacent channels within the MOSFET structure as the sensitive regions are involved in this type of damage [130]. Abbate's work confirmed that the I_{DG} degradation does not involve damage in the body-drain p-n junction [148].

The second mechanism of degradation, was also discussed in Paper I [146]. For V_{DS} higher than a certain threshold, the I_{DG} keeps increasing linearly with respect to the fluence, whereas the drain-source leakage current (I_{DS}) starts increasing with a much larger magnitude with respect to I_{DG}. From the microbeam studies presented in Paper II, the p-n junction was identified as the sensitive region for this effect [130]. Furthermore, it was suggested that this second mechanism of degradation observed in SiC MOSFETs, is the same as the one observed in SiC diodes. As already discussed for SiC diodes in section 3.6.2.1, the Joule heating is responsible of this type of degradation, which results in increasing temperature and phase change, confirmed also by molecular dynamics simulations [140], as further described in 4.4.1. Finally, a similar mechanism for degradation and SEB in SiC MOSFETs and SiC JBS diodes was suggested by Ball *et al.* [151], proposing highly-localised pulses induced by the ion strike as responsible for the damage. Lower magnitude energy pulses were identified as responsible for degradation, assuming the SEB being a more catastrophic form of SELC, as described at the end of the next section.

3.6.3.2 SEB

Figure 3.14 from Witulski *et al.* [136] reports a summary of 1.2 kV SiC MOSFETs SEB susceptibility with heavy-ions. The data are collected from different experiments performed during the recent years by Witulski, Mizuta *et al.* [127] and Lauenstein *et al.* [152]. The image reports also 3D-TCAD SEB simulations. The SEB thresholds are presented as a function of the LET, and it follows a hockey-stick trend, saturating at ~ 500 V (less than 50 % of the rated voltage) for LET > 10 MeVcm^2/mg. The vulnerability

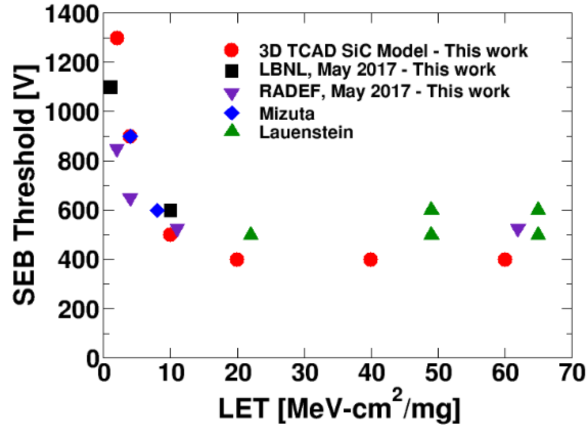


Figure 3.14: SEB threshold voltage for 1.2 kV SiC MOSFETs collected from several heavy-ion experiments presented by Mizuta in [127] and Lauenstein in [152], comparing with 3-D TCAD SEB simulations. In the legend, the label "This work" refers to the original work from Witulski. Reprinted with permission from [136]. © 2018, IEEE.

to immediate SEB was observed with LET as low as 1 MeVcm^2/mg, due to primary knock-on atoms during 70 MeV proton irradiations [127].

The SEB mechanism has been subject of debate during the last years, in particular concerning the role of the parasitic BJT. On one side, the hypothesis that the parasitic BJT turn-on was necessary to achieve the SEB, as in Si MOSFETs, was supported by numerical simulations performed by Witulski et al. [136]. Avalanche breakdown, coupled with a parasitic BJT in a positive feedback loop, was suggested as the reason for the simulated runaway drain current. Laser studies performed by Johnson *et al.* on MOSFET and JBS diode sharing the same fundamental epi-layer properties, identified enhancement of current in the source region closer to the gate, demonstrating parasitic BJT charge amplification [153]. In addition, studies of short-circuit ruggedness suggested that the BJT can be turned on and trigger thermal runaway [154], supporting the active role of the BJT in SEB mechanism. On the other hand, experimental data collected during both heavy-ion and neutron irradiations, showed that there exists no consistent difference in SEB tolerance between SiC diodes and SiC MOSFETs, leading to the conclusion that the parasitic BJT is not involved in the SEB failure mechanism [123, 129, 134, 155]. This hypothesis is also supported by the fact that, compared to a Si MOSFET, the parasitic BJT in SiC MOSFET requires higher voltage to switch on (i.e. the higher forward voltage drop is higher in SiC), having also a significantly lower gain due to the high doping levels in the p-body. Supporting this hypothesis, Shoji *et al.*, studied the neutron-induced SEB in SiC diodes [143] and SiC MOSFETs [155]. In the latter work, Shoji performed numerical simulations of an ion strike in a SiC MOSFET and in a SiC diode structure that eliminated the n+ source diffusion region from the MOSFET. The ion trajectory extended over the n+ source region near the gate, which was identified as the most susceptible region for BJT current amplification by the laser study of Johnson [153]. The results from the numerical simulation are visible in Figure 3.15, and demonstrated that no significant difference is observed in current and lattice temperature when the n+ region is included (i.e. MOSFET structure, including parasitic BJT) or not (i.e. diode structure, excluding parasitic BJT). In both cases, the simulated temperature eventually

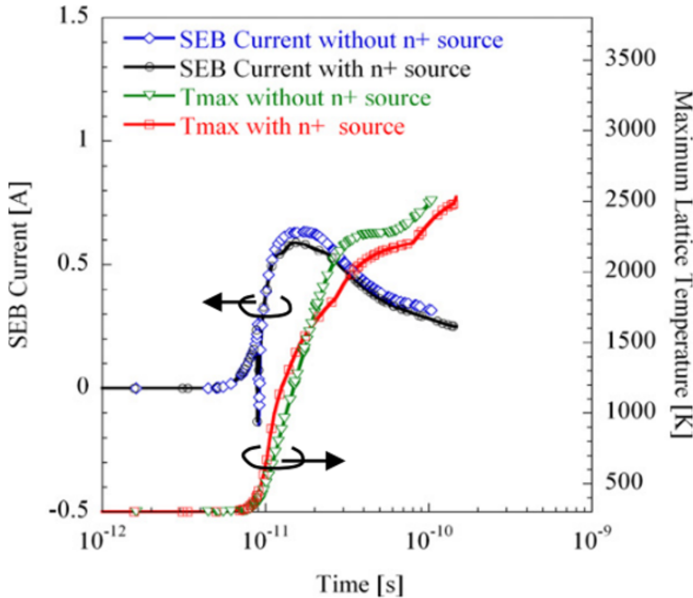


Figure 3.15: SEB currents and maximum lattice temperature simulated with and without the n+ source diffusion region in SiC power MOSFET. In the case without the n+ region, the structure forms a SiC diode. Reprinted with permission from [155]. © 2015, Elsevier Ltd.

reaches the sublimation temperature of SiC. The results led to the conclusion that the SEB mechanism in SiC MOSFETs is not due to the BJT action, but to a shift in the peak electric field and the punch-through at the n+ source diffusion region, similar to the case of SiC power diodes [155].

The discrepancy between the findings of Witulski and Shoji concerning the role of the parasitic BJT, was explained by the experimental work and simulations performed by Ball *et al.* [151, 156]. Ball carried out heavy-ion experiments using a non-destructive technique in attempt to suppress the SEB, inserting a resistor of 100 kΩ between the power supply and the drain node, to limit the current and induce a voltage drop under the critical levels for SEB. A similar approach was previously attempted using a 1MΩ resistor [157]. However, in both cases, the presence of the resistor had no impact, finding similar SEB and degradation thresholds for SiC MOSFETs and JBS diodes. Ball stated that, due to the time constant of the circuit, the presence of the resistor should have provided some protection if the SEB failure resulting from transient was happening on the order of ns to μs. As this was not the case, then the SEB event was happening at lower time scales in the order of ps, before the parasitic BJT can contribute significantly to the MOSFET response. This explained the similarity of SiC MOSFETs and diodes tolerance to SEB and degradation experimentally measured. Furthemore, this time scale corresponds to the SEB mechanism in SiC Schottky diodes as proposed by Kuboyama [142] and explains the difference between Witulski and Shoji conclusions [8].

In the same work, by performing 3-D TCAD simulations of a 1.2 kV SiC MOSFET and a 1.2 kV JBS diode, Ball showed that for approximately 100 ps after the ion-strike occurs, the current transients behave identically in both structures, while after that they begin to deviate, as shown in Figure 3.16 for LET = 10 MeVcm^2/mg and a drain bias of 500 V [151]. The energy dissipation occurs during the first 10 ps after the strike event.

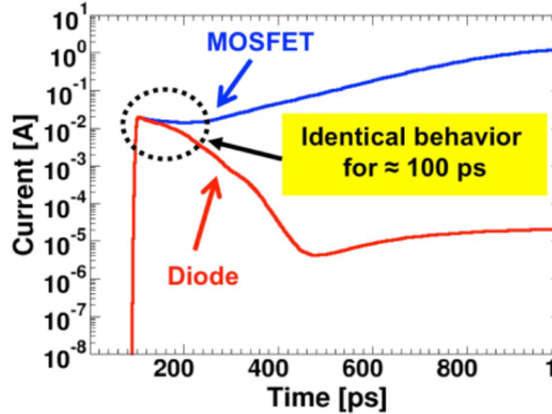


Figure 3.16: Simulated ion-induced current transient for a 1.2 kV SiC MOSFET and 1.2 kV JBS diode, with identical behavior for the first 100 ps. Reprinted with permission from [151]. © 2020, IEEE.

The electric field is redistributed, with peaks at the body/drain junction and at the epi/substrate interface, with the latter resulting in a peak of ∼ 3.2 MV/cm, determined as the critical electric field to induce avalanche breakdown. The authors also showed that ∼ 40 % of the power density is dissipated at the epi/substrate interface region.

For LET and bias conditions which experimentally result in SEB, the energy dissipated during the 10 ps after the ion strike, was calculated integrating the power density across the entire epi-region. The energy resulted in a value ranging between 2-3 nJ [151]. The series of events was described similar for non-destructive degradation, but the energy dissipation resulted lower in magnitude, suggesting that SEB is a more catastrophic form of degradation. Ball *et al.* proposed highly localized energy pulses induced by the ion-strike, as a common mechanism responsible for both SEB and leakage current degradation in SiC MOSFETs and JBS diodes; with lower magnitude energy pulses responsible for degradation.

3.6.3.3 SEGR

Most of the knowledge available for the SEGR mechanism is provided by studies performed on Si power devices, as described in section 3.5.1.1. In addition, Deki *et al.* studied SEGR susceptibility of 4H-SiC MOS capacitors as a function of LET, suggesting that SiC MOS capacitors may be less susceptible to SEGR than silicon MOS capacitors [158, 159]. Casey *et al.*, studied the first generation SiC MOSFETs tolerance to heavy-ion-induced SEGR, observing that the results fit the estimation of the critical voltage required to observed SEGR provided by the Titus-Wheatley equation, which was derived for Si MOSFETs based on ion atomic number (Z) [160, 161]. This result led to the conclusion that any difference in SEGR susceptibility between SiC and Si MOS devices is likely caused by differences in the semiconductor, rather than in the oxide [160]. In addition, Pintacuda *et al.* studied the oxide reliability of MOS capacitors made of SiC and Si, and SiC MOSFETs with different gate oxide thicknesses and epitaxial layers, when exposed to heavy-ions. The results of the failure analyses summarise the tolerance of the different structure to SEGR and PIGS failure, the latter caused by latent damage, confirming the location of the damage in the neck region [150].

3.6.3.4 Latent damage

Some authors have observed experimentally latent gate oxide damage in SiC MOSFETs heavy-ion exposure. Even though no degradation was observed during the irradiations in off-state, PIGS testing revealed increased gate leakage current [8, 150, 162]. In respect to the Si counterparts, the latent damage in SiC MOSFETs is observed at significantly lower fraction of the rated voltage, despite the fact that the gate oxide maximum field strength is comparable between the two technologies. The explanation of this effect is due to the fact that the oxide field is about three times the field in the semiconductor, and that the electric field strength in SiC is 10 times higher than Si [8, 27]. For this reason, it is more likely for the oxide in SiC to exceed its breakdown field strength. Abbate *et al.*, performed numerical simulations of the heavy-ion strike, confirming that the voltage in the gate oxide can reach the oxide breakdown level at V_{DS} values comparable with the experimental ones [148]. However, it was experimentally demonstrated that a minimum LET is required to observe latent damage during the PIGS test [8].

The minimum threshold voltages to observe oxide latent damage were identified in this work for 2nd generation Cree devices exposed to different heavy-ion species. The results are tabulated and discussed in Section 4.3.4.2. In addition, a second latent damage mechanism was observed in the post-irradiation analysis when exposing the devices in the pre-SEB region ($V_{DS} \sim 450$ V for LET > 7.7 MeVcm^2/mg). This effect is discussed in Section 4.3.4.1.

3.6.3.5 Proton and neutron induced SEE

High-energy protons and atmospheric-neutrons, undergo nuclear reactions with the SiC lattice, generating fragments which can induce SEBs in both SiC MOSFETs and diodes.

Atmospheric-neutrons Neutrons are non-ionizing particles which interact through elastic or inelastic scattering with the lattice atoms. This generates recoiling particles which can indirectly give rise to ionization and create a large number of e-h pairs along their trajectories, inducing SEB following the same physics described for heavy-ions. A schematic of the neutron interaction with the 4H-SiC lattice is shown in Figure 3.17.

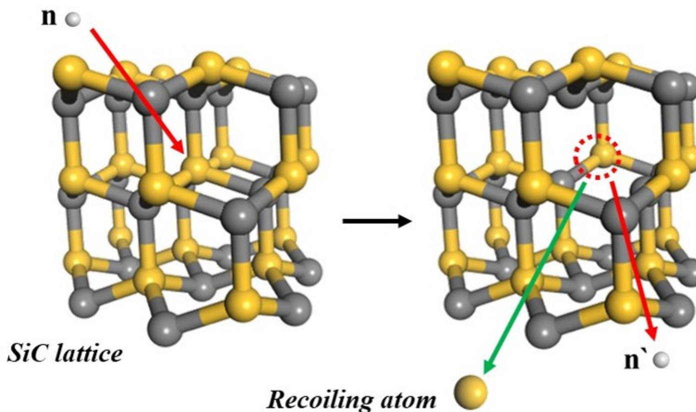
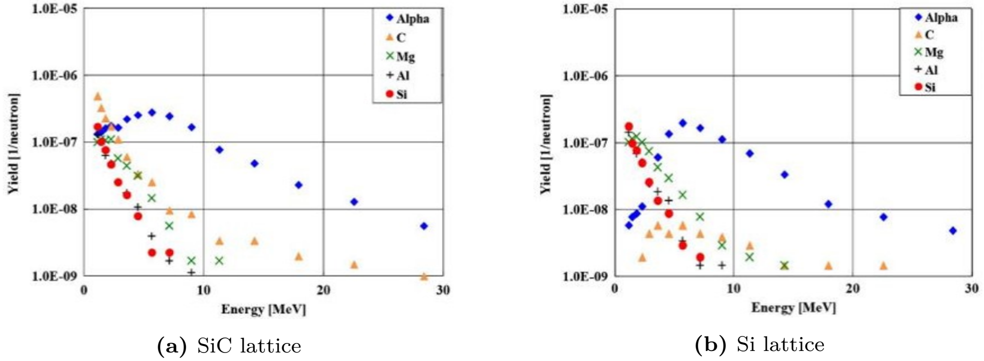


Figure 3.17: Neutrons interact with 4H-SiC lattice through elastic and inelastic scattering, creating recoiling atoms (i.e., α, C, Si, Mg, Al) which generate ionizing tracks inside the power device. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.



(a) SiC lattice **(b)** Si lattice

Figure 3.18: Energy of the secondary particle between 1 and 30 MeV generated by the atmospheric neutron interaction with (a) SiC and (b) Si lattice. The main difference among the two simulations are the yields for carbon and alpha atoms. The results were obtained by PHITS calculation. Reprinted with permission from [123]. © 2014, IEEE.

Asai *et al.* performed PHITS Monte Carlo simulations of the nuclear reactions and the collisions between the atmospheric neutrons and the lattice atoms of SiC and Si devices [123], extracting the different yield, energy and range of the reaction products [123]. The energy spectra of the secondary particles in SiC and Si devices in the range of 1 to 30 MeV are shown in Figure 3.18. The yield of the secondary alpha and carbon atoms is much higher in SiC with respect to Si. Asai *et al.* also calculated the projected range of the secondary particles, demonstrating that in the case of SiC, both the secondary carbon and alpha particles have enough energy to cross the entire drift layer of the SiC device (with average range of 10 μm), increasing the probability of SEB. In the case of Si devices, instead, the drift layer is 10 times larger (average 100 μm), and only the secondary alpha atoms may have this range and therefore trigger the SEB mechanism.

Many works have been performed about SEEs induced by terrestrial neutrons and, although they will not be discussed in details here, the reader can found more information in [123, 131−135, 144, 163−165]. It should be noticed that leakage current degradation is generally not considered an issue during terrestrial-neutrons irradiation, due to the low LET of the secondary particles. However, as described in Paper III and in Chapter 5, from the post-irradiation analysis of different commercial SiC MOSFETs technologies, a partial gate-rupture mechanism was observed in some parts. For the planar devices, this effect was found to be similar to the leakage current degradation caused by heavy-ions. Similarly, a leakage current increase during terrestrial-neutron exposure was previously observed in Si IGBTs and Si MOSFETs by Asai *et al.* [123], as mentioned in 3.5.1.4. Therefore, further investigations are needed in order to understand if the recoiling atoms produced by the neutron interaction, have a sufficiently LET to induce micro-break, and therefore degradation of the leakage current in SiC devices.

Protons Concerning the physics of the proton interaction, according to Mizuta *et al.* [127], the SEBs observed in SiC SBDs exposed to 70 MeV protons with an LET of 0.0079 MeVcm^2/mg, were mainly caused by fragments created by the proton spallation reaction with the SiC lattice. Through Geant4 simulations, Na and Al ions were identified as the most probable ion species responsible to cause the destructive failure [166], following the

same mechanisms described earlier for heavy-ions. Mizuta also concluded that Na and Al ions must be also the responsible spallation fragments for SEBs in SiC power MOSFETs.

As for atmospheric-neutrons, leakage current degradation is generally not considered an issue during high-energy proton irradiations. The preliminary results obtained from proton experiments are discussed in Chapter 5.

4 Heavy-ion induced degradation and latent damage

This chapter discusses the heavy-ion experiments performed with the broad-beam and microbeam. Commercial SiC power MOSFETs from the 2nd and 3rd generation Cree/Wolfspeed were used as DUTs. In particular, the device from the 2nd generation with $R_{DS(on)} = 80$ mΩ is used as a reference device to generally discuss the results.

Firstly, the broad beam and microbeam facilities, the beam features, and the experimental setups and methods are introduced. Then, the results are presented for the heavy-ion-induced degradation and latent damage (Paper I and II). For the latter, not only electrical measurements, but also focused ion beam (FIB) coupled with scanning electron microscope (SEM) analysis of the failure area are discussed (Paper IV). Finally, the degradation rates are summarized for the broad-beam and the microbeam results.

Two different mechanisms are described for the heavy-ion degradation in SiC MOSFETs, involving different regions of the device. An electrical equivalent is proposed to explain the current-transport mechanism in heavy-ion-degraded devices. Finally, at the end of the chapter, all the heavy-ion SEEs observed during the test campaigns are summarized, highlighting the critical areas for each SEE as function of the ion LET and the drain-source bias during the exposure.

4.1 Heavy-ion broad beam experiments

4.1.1 RADEF facility

The heavy-ion broad beam experiments were performed at the RADiation Effects Facility RADEF in the Accelerator Laboratory of the University of Jyväskylä, Finland. RADEF is an European Space Agency (ESA) supported European Component Irradiation Facility (ECIF) since 2005, specialized in radiation effects in electronics and related materials. Additional information on RADEF can be found in [167].

4.1.2 Heavy-ion broad beam line

The heavy-ion beams are provided by the electron cyclotron resonance (ECR) ion sources and accelerated by the K-130 cyclotron. During the experimental campaign, the boards were placed at the end of the main beam line, in a vacuum chamber with an height of 81 cm and an inside diameter of 75 cm, whose layout is reported in Figure 4.1. The irradiations were performed in vacuum. The printed circuit board (PCB) were fixed on an aluminum plate which is mounted on a linear movement apparatus (LMA) remotely operated, which allowed the vertical and the horizontal movements of the board. For all the irradiations discussed in this work, a standard beam size of to 2×2 cm^2 was used. Four photomultiplier tubes with BC-408 plastic scintillator material, installed on the sides of the beam aperture, were employed to measure the beam flux and uniformity, while the purity of the ion species was verified though the energy spectrum. The flux information were provided as +5 V TTL pulses, where the signal frequency corresponds to the average flux over the previous second. Real-time flux information were also available. The main source of uncertainty was considered from the fluence measurement, with an error of +10%. Finally, all the information about the beam such as the ion species, energy, LET, flux, cumulative fluence, range in Si, collimators and LMA setting, were displayed in the control barrack and stored in a log file for each irradiation run.

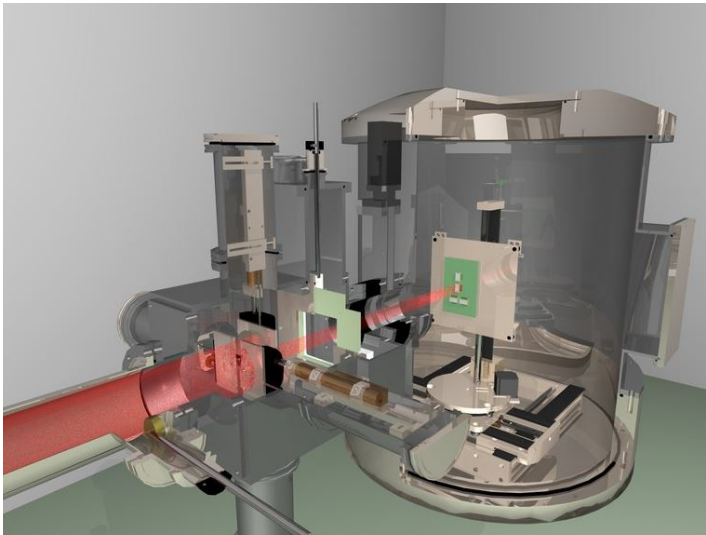


Figure 4.1: Irradiation chamber for heavy-ion and diagnostic equipment, after [167].

4.1.3 Heavy-ion cocktails at RADEF

The heavy-ion cocktails at RADEF are a mixture of ions with almost the same mass to charge ratio, allowing a fast swap between species. The ions are taken to the target one species at the time. Two ion cocktails with the energies of 9.3 MeV/amu and 16.3 MeV/amu are available up to Xe. Table 4.1 and Table 4.2 summarize the parameters for the heavy-ion species used in the broad-beam experiments discussed in this chapter. Figure 4.2 shows the LET profiles as a function of the penetration depth in SiC in vacuum mode, estimated for the two ion cocktails with ECIF [168]. The vertical dash lines highlight the epitaxial layer of a SiC MOSFET which extends between 5 μm and 18 μm from the die surface (i.e., 2nd generation). It confirms that the ions penetrate deep enough and the energy deposition is well defined within the active layer to meet the worst-case energy deposition criterion as discussed in [169].

Table 4.1: Characteristics of the 9.3 MeV/amu cocktail in vacuum.

Ion	Energy [MeV]	Energy/nucleon [MeV/amu]	LET@Surface [MeVcm^2/mg]	Range SiC [μm]
$^{56}Fe^{15+}$	523	9.33	20.05	64.2
$^{83}Kr^{22+}$	768	9.25	33.75	62.5
$^{131}Xe^{35+}$	1217	9.29	62.39	60.1

Table 4.2: Characteristics of the 16.3 MeV/amu cocktail in vacuum.

Ion	Energy [MeV]	Energy/nucleon [MeV/amu]	LET@Surface [MeVcm^2/mg]	Range SiC [μm]
$^{40}Ar^{14+}$	657	16.42	7.71	175.0
$^{57}Fe^{20+}$	941	16.50	14.64	136.4
$^{83}Kr^{29+}$	1358	16.36	25.38	125.7
$^{126}Xe^{44+}$	2059	16.34	49.10	112.2

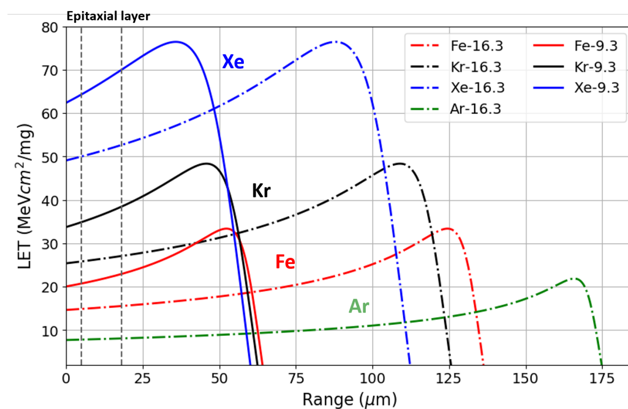


Figure 4.2: LET as a function of the penetration depth in SiC for the 16.3 MeV/n and 9.3 MeV/n cocktails (estimation from ECIF). The vertical dash lines highlight the epitaxial layer.

4.1.4 Setup and method for the broad-beam experiments

4H-SiC MOSFETs from the manufacturer Cree/Wolfspeed, available as bare die, were selected as DUTs for all the experiments [33]. Bare die were used to directly expose the chip surface to the beam, allowing sufficient penetration of the heavy-ions through the sensitive layer of the device (i.e., 5-18 μm), without being stopped in the package materials [169]. Devices for the 2nd and 3rd generation were used. All the devices differ in $R_{DS(on)}$ and are rated for 1.2 kV if from the 2nd generation, and 900 V if from the 3rd. The electrical characteristics of the DUTs are listed in Table 4.3. The 80 mΩ from the 2nd generation was selected as reference device.

Table 4.3: Devices used for the heavy-ions test campaigns with the broad-beam.

DUT	Manufacturer	Gen.	$R_{DS(on)}$ [mΩ]	V_{DS} [kV]	$I_{D@25}$ [A]
CPM2-1200-0080A	Cree/Wolfspeed	II	80	1.2	36
CPM2-1200-0025A	Cree/Wolfspeed	II	25	1.2	81
CPM2-1200-0040A	Cree/Wolfspeed	II	40	1.2	60
CPM2-1200-0160A	Cree/Wolfspeed	II	160	1.2	18
CPM3-0900-0065A	Cree/Wolfspeed	III	65	0.9	32

Figure 4.3 shows the PCB board used during the experiment. The die were mounted on a custom FR-4 carrier boards with gold (ENIG) surface using standard SAC 305 solder paste. Gate and source were connected by aluminum wire bonds with 300 μm diameter, whereas the drain connection was made by the large soldered bottom pad. Only a single source wire was used, to minimize shadowing by the wires. Each board housed 5 die individually biased with BNC connectors for gate and drain.

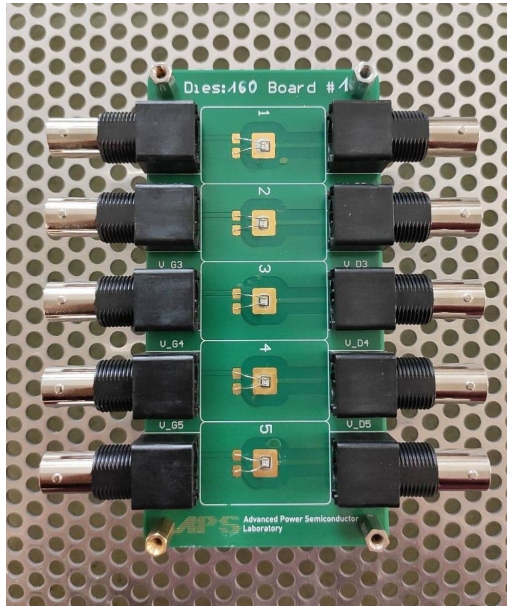


Figure 4.3: PCB used at RADEF for the 160 mΩ DUTs irradiations.

Keithley source measure unit (SMU) models 2636 (two channels, up to 200V) and 2410 (one channel, up to 1100V) were used for biasing gate and drain respectively and measure the drain leakage current (I_D) and the gate leakage current (I_G). The source leakage current (I_S) was not measured during the exposure. A protection module of 1 MΩ was installed between the gate terminal and the SMU 2636, to protect the instrument in case of destructive failure. BNC cables of 1 m were used inside the vacuum chamber, while the electronics was installed right next to it, so that the cable length was as short as possible. A GPIB-cable was installed between the two SMUs to allow a simultaneous control. A GPIB-USB was connected to the Keithley 2410 and then to a laptop placed in the control barrack through an USB cable of approximately 10 m. The operations were controlled by a python script. The cumulative count of heavy-ions hitting the device was recorded during the irradiation using a simple digital counter based on an Arduino Leonardo microcontroller.

During the irradiations, the V_{GS} was set to 0 V to hold the device in off state, while the V_{DS} was set to constant positive value during the irradiation. Each device was irradiated several times and the V_{DS} increased after each run until the device was considered broken due to the degradation. The boards were mounted in a vacuum chamber and the beams were at normal incidence to the DUT surface. I_D-V_{DS} and I_G-V_{GS} characteristics were measured after each run. All the irradiations and the I-V characterizations were performed at room temperature.

A detailed description of the experiments performed at RADEF is reported in Paper I and Paper IV.

4.2 Heavy-Ion microbeam experiments

4.2.1 GSI UNILAC facility

The heavy ion micro-probe or microbeam facility is situated at the end of the UNIversal Linear ACcelerator (UNILAC) at the Helmholtzzentrum für Schwerionenforschung (GSI) in Darmstadt, Germany. The GSI-UNILAC microbeam facility is a unique tool in Europe, to clearly identify sensitive functions and mechanisms of errors and failures in electronic components for space and high-energy physics applications, as reported on the GSI webpage [170] and in the following works [171−173].

4.2.2 Heavy-ion microbeam

The GSI microbeam facility provides ions from carbon to uranium with energies between 1.4 MeV/amu to 11.4 MeV/amu. The beam is focused to a focal spot of about 500 nm in diameter by means of magnetic quadrupole lenses [174]. An optical microscope situated in the chamber allows a precise definition of the micrometric area to be scanned with the ion beam. Deflecting magnets, situated downstream of the focusing lenses, are used to move the beam in the focal spot. To assure a beam free of scattered particles, the ions enter the beam line through object slits. A channel electron multiplier (CEM) discriminates the single hits detecting the secondary electrons emitted by the materials after the ion hit. To ensure the irradiation with a preset number of particles and to avoid double hits at the same position, a fast electrostatic beam switch is controlled by the hit detection system. When a hit is detected, the microbeam is switched off and the probe is moved to the new coordinates. The irradiation is performed under vacuum.

Gold (Au) and calsium (Ca) ions with an energy of 4.8 MeV/amu and LET values of 94 MeVcm^2/mg and 17 MeVcm^2/mg respectively, were used during the experiments, as reported in Table 4.4. In the case of Au, a scanning area with a size of 55×50 μm^2 was selected and exposed to a total of 1600 ions for each scan. For the Ca-beam, 520 ions were used with a scanning area of 30×25 μm^2. For both configurations, the average distance between the steps in each, X and Y, direction, was in the order of $\sim$ 1 μm.

Table 4.4: Characteristics of the heavy-ion microbeams.

Ion	Energy/nucleon [MeV/amu]	LET [MeVcm^2/mg]	Range SiC [μm]	Window size [μm^2]	ΔX [μm]	ΔY [μm]
Au	4.8	94	35.4	55×50	1.1	1.56
Ca	4.8	17	29.7	30×25	0.93	1.56

4.2.3 Setup and method for the microbeam experiments

The same setup designed for the broad-beam experiments at RADEF and described in 4.1.4 was employed at GSI-UNILAC and adjusted to be used with the focused beam. The main difference among the two experiments is the beam focal spot; at GSI-UNILAC the microbeam has a focal spot of 500 nm and the irradiation frame is selected using a microscope, whereas the minimum beam size at RADEF is 2×2 cm^2, and it is not possible to have higher resolution of the ion-track location. Hence, the focused beam irradiation allows micron-accurate localization of the irradiation spot and, consequently, of the radiation-sensitive regions.

The same devices used for the broad-beam experiments were tested also at GSI and are listed in Table 4.3 (a part the DUTs with $R_{DS(on)}$ = 40 mΩ and 160 mΩ). Also in this case, the results are discussed mostly for the 80 mΩ from the 2nd generation. The PCB used at RADEF housed 5 dies, while 3 die were installed on the boards used at GSI and the BNC connectors were soldered on the bottom side. This was done to comply with the micro-probe-irradiation requirement of having the area to be irradiated as the outermost surface on the board, to allow the movement of the scanner probe. A picture of the GSI board is shown in Figure 4.4 (a).

In both the experimental campaign, the same Keithley SMU models 2636 and 2410 were used following the same procedure during the irradiation and the same I-V characterisations between the runs, as described in 4.1.4. The cumulative count of heavy-ions hitting the device and the scanner position within the frame were also recorded for each ion. Each DUT was irradiated several times scanning the beam spot in different pristine regions of the die selected with the microscope, until the I_D reached several 100 μA. Figure 4.4 (b) shows the regions irradiated with Au beam for the 80 mΩ die (not to scale).

A detailed description of the experiments performed at GSI is reported in Paper II.

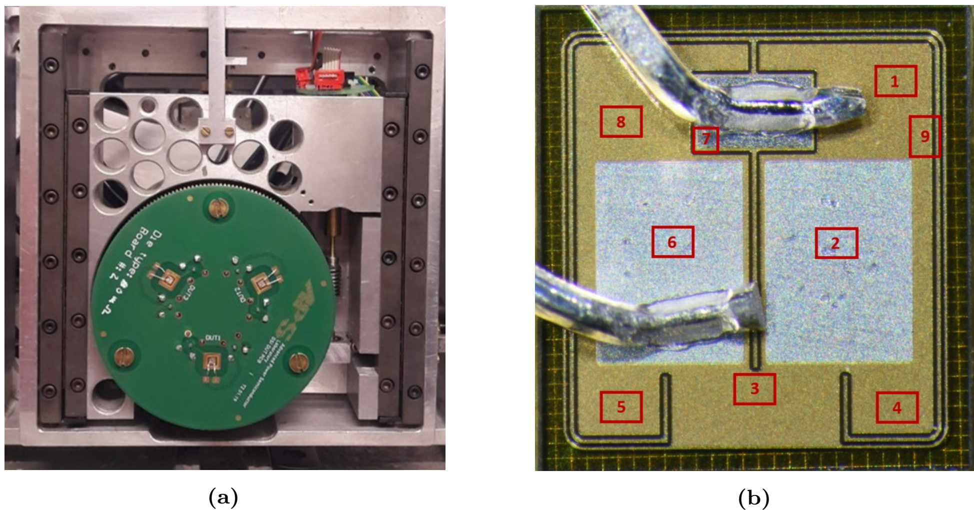


Figure 4.4: (a) PCB used at GSI-UNILAC for the 80 mΩ DUTs irradiations. (b) Regions irradiated with Au beam for the 80 mΩ die (not to scale).

4.3 Experimental results

4.3.1 Broad-beam

The first experiment at RADEF was performed with $^{56}Fe^{+15}$, $^{83}Kr^{+22}$ and $^{131}Xe^{+35}$ ions from the 9.3 MeV/amu cocktail. The characteristics are reported in Table 4.1. Each exposure was run up to a fluence of 10^6 ions/cm^2 with an uncertainty of 10 %. The results discussed for the 80 mΩ DUTs, were also observed with the 25 mΩ and the 160 mΩ devices from the same generation, which have the same vertical cell structure, but different active area. The same considerations can be extended also to the 65 mΩ (3rd gen.).

At sufficiently high V_{DS} during the irradiation, the I_D and I_G increase with increasing fluence, inducing a permanent degradation in the device, also named SELC. The threshold for SELC degradation was observed at V_{DS} = 300 V for $^{56}Fe^{+15}$, V_{DS}= 200 V for $^{83}Kr^{+22}$ and V_{DS}= 120 V for $^{131}Xe^{+35}$. Figure 4.5 presents the absolute values of the gate and drain leakage current measured during the exposure as function of the fluence. The results are shown for a 80 mΩ DUT exposed to $^{56}Fe^{+15}$ and $^{131}Xe^{+35}$ at V_{DS} = 300 V and V_{DS} = 350 V. Independently from the ion, two scenarios were commonly observed:

- I_{DG} degradation at $V_{DS} < 350$ V: the absolute value of the gate and drain leakage currents increase with the same rate and magnitude, and a drain-gate leakage path is observed, as in Figure 4.5 (a) and (b);
- I_{DS} degradation at $V_{DS} \geq 350$ V: the drain leakage increases at higher rate than the gate leakage, as in Figure 4.5 (c) and (d). The leakage current is divided between drain-gate and drain-source paths;

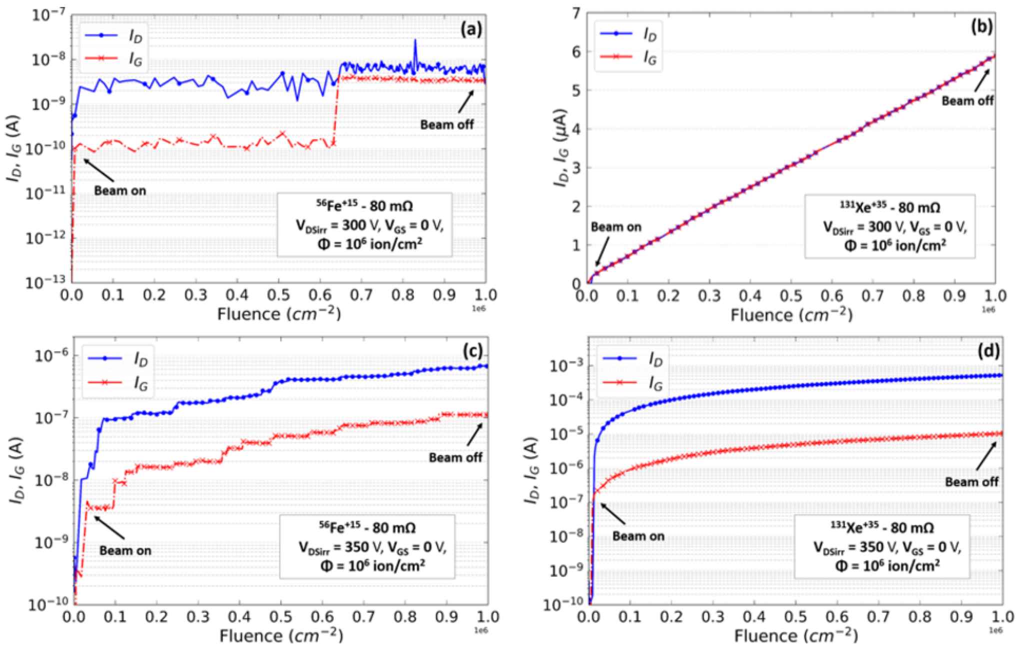
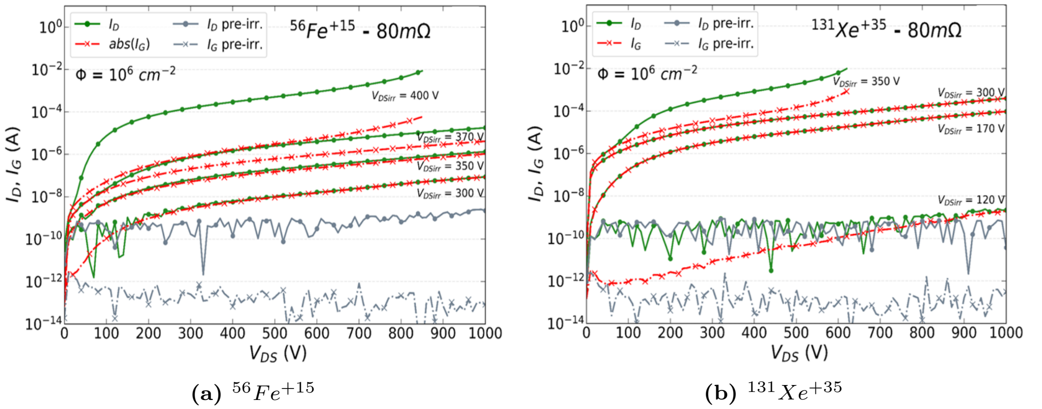


Figure 4.5: Equal rate of increase in I_G and I_D during the irradiation at V_{DS} = 300 V with (a) $^{56}Fe^{+15}$ and (b) $^{131}Xe^{+35}$. Each step in the leakage currents is caused by a single incident heavy ion. The y-axis in (b) is in linear scale and μA. Over V_{DS} = 350 V, the I_D increases with higher rate than the I_G, as visible during (c) $^{56}Fe^{+15}$ and (d) $^{131}Xe^{+35}$ irradiations. Reprinted with permission from [146]. © 2019, IEEE.

$I_D V_{DS}$ and $I_G V_{DS}$ were measured promptly after each run, with V_{DS} = [0 V - 1000 V] and V_{GS} = 0 V. The $I_D V_{GS}$ and the $I_G V_{GS}$ were also measured, with V_{GS} = [0 V - 5 V] and V_{DS} = 1 V. Permanent damage in the gate oxide and in the blocking capability was observed for the devices exhibiting SELC. The results for the 80 mΩ DUTs exposed to $^{56}Fe^{+15}$ and $^{131}Xe^{+35}$ are shown in Figure 4.6 (a) and (b), respectively. The data for $^{83}Kr^{+22}$ are not reported, but they are consistent with the one discussed. The history of the consecutive exposures is indicated on the graph as V_{DSirr}. The I_D and

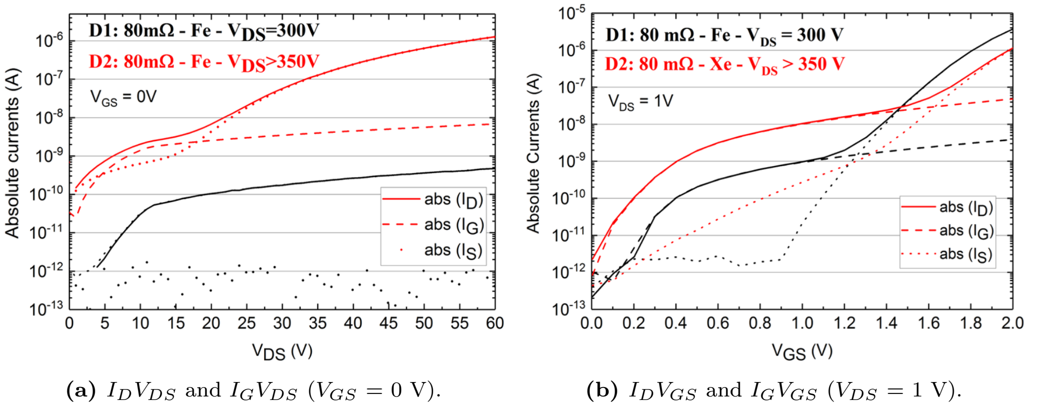
the I_G are represented in green and red, respectively. The pristine values are plotted in gray. The analysis confirms that, for the degraded DUTs exposed at $V_{DS} < 350$ V, the leakage-current path is formed between drain and gate, as visible by the equal leakage currents values ($|I_D| = |I_G|$). Differently, for the DUTs exposed at $V_{DS} \geq 350$ V, the I_G and the I_D are equal at low V_{DS} during the sweep, but at higher V_{DS} the leakage path forms between drain and source through the channel (|ID| > |IG|). The magnitude of this effect varies with V_{DS} during the irradiation and with the ion LET.

Two DUTs exposed to $^{56}Fe^{+15}$ at $V_{DS} = 300$ V and 350 V were compared measuring the I_D, the I_G and the I_S while sweeping the V_{DS} and the V_{GS}. Figure 4.7 (a) confirms different current paths for the two situations. Figure 4.7 (b) shows that the channel is still controllable in both DUTs, even though the I_G is very high. Indeed, at low V_{GS} the I_D flows from drain to gate, whereas at higher V_{GS} it flows from drain to source. Hence, the assumption that I_D flows through the channel and not through the base is confirmed.



(a) $^{56}Fe^{+15}$ (b) $^{131}Xe^{+35}$

Figure 4.6: $I_D V_{DS}$ and $I_G V_{DS}$ performed between irradiations of the same device with a fluence of 10^6 ions/cm^2 per run. The V_{DS} during the exposure is reported in the graph as V_{DSirr}. Reprinted with permission from [146]. © 2019, IEEE.



(a) $I_D V_{DS}$ and $I_G V_{DS}$ ($V_{GS} = 0$ V). (b) $I_D V_{GS}$ and $I_G V_{GS}$ ($V_{DS} = 1$ V).

Figure 4.7: Comparison of two devices irradiated at $V_{DS} = 300$ V and $V_{DS} = 350$ V. Reprinted with permission from [146]. © 2019, IEEE.

4.3.2 Microbeam

The following results are discussed for the Au irradiation of the 80 mΩ device. However, the same considerations are valid also for the 25 mΩ from the same generation an for the 65 mΩ from the 3rd generation and for the Ca exposures. The irradiations were performed consecutively on the same DUT, in pristine areas of region 2 (as shown in Figure 4.4), selected with the optical microscope. The results are shown in Figure 4.8 for irradiations at $V_{DS} = 210$ V and $V_{DS} = 300$ V, and in Figure 4.9 for $V_{DS} = 350$ V and $V_{DS} = 400$ V. These two figures are composed of four panels, further described below.

The exact positions of the irradiated area is is shown in the first panels from the top, where the irradiation frame is visible on top of the microscope image.
The I_D and I_G were monitored during the exposure, and the ion-induced degradation was calculated considering a minimum threshold of 2.5 nA for each step, to discriminate from the background noise. The data are shown in the second panel of the figures. Due to the different magnitude of degradation between I_D and I_G, a second axis is used for the I_G for the runs at 350 V and 400 V. Also, it should be notice that for the run at 350 V, due to a problem with the beam scanner during the exposure, a total of 1200 ions instead of 1600 was used. This explains the flat measurement towards the end of the run.
The I_D and I_G steps were analysed as function of the scanner position within the area exposed during the run. In order to do that, the data for the scanner position originally logged as computer-aided measurement and control (CAMAC) standard were converted into the ASCII format and, then, into x−y coordinates inside the irradiated frame (using micrometer units). Successively, each leakage step was associated with the corresponding scanner position. From this set of data, heat maps for the gate and drain degradation were generated for each run. The results are presented in the third and fourth panels. The gate stripes are indicated with dotted lines on top of the maps, to guide the eyes. The distance between the stripes is 9.1 μm, based on the technological information available for the DUT. For each run, the stripes were aligned with the degradation observed in the gate heat map, assuming the sensitive region for the gate leakage current being in the oxide of the gate-stack. For each of the four column, the periodicity in the lateral response observed in the leakage current degradation analysis reflects the periodicity of the striped structure, which is comparable with the one indicated in the microscope image in the first panel. This result indicates that the entire MOSFET cell is not uniformly sensitive to SELC, but the response strongly depends on the ion strike location. Generally, the sensitive region for degradation enlarges with increasing V_{DS} during the exposure.
The results observed during the broad beam experiment and discussed in 4.3.1, indicate that for irradiations performed at $V_{DS} < 350$ V, the leakage current path is between drain and gate (|ID| = |IG|), whereas for $V_{DS} \geq 350$ V, the leakage paths are divided between the drain-gate and drain-source path, which is also confirmed by the microbeam results. In Figure 4.8 it is observed that for irradiations at $V_{DS} < 350$ V, the sensitive regions are aligned with the gate stripes in the neck area (JFET region) for both gate and drain heat maps. This area probably includes also the channel regions. However, at $V_{DS} \geq 350$ as in Figure 4.9, the sensitive areas for I_G degradation are still aligned with the same regions, but those for I_D degradation are now between the gate stripes, i.e., in the p-implanted body-diode region of the VD-MOSFET.

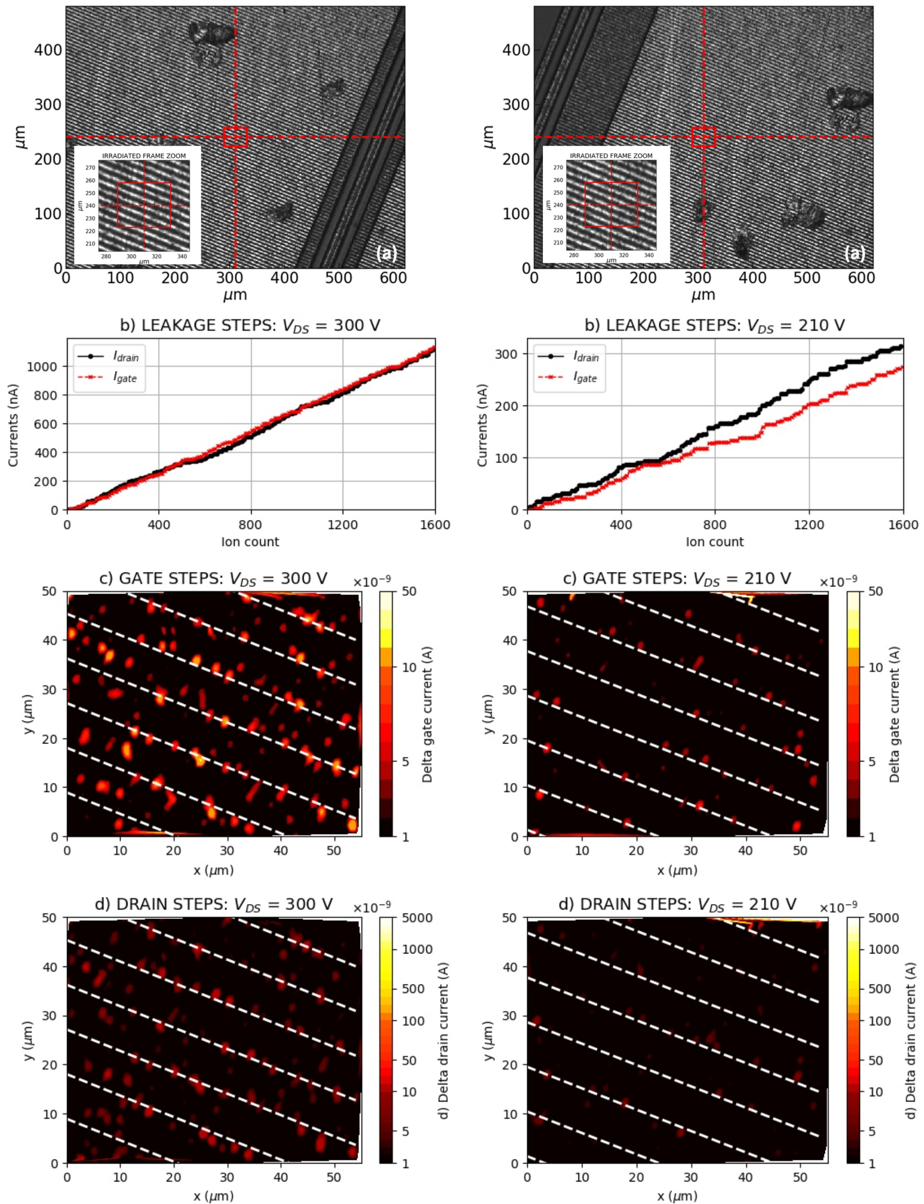


Figure 4.8: The runs refer to an 80-mΩ DUT exposed in region 2. (Left) V_{DS} = 210 V. (Right) V_{DS} = 300 V. From the top: (a) the frame selected for the irradiation is visible on top of the microscope image; (b) drain and gate leakage current steps measured during the irradiation; (c) gate degradation heat map (d) drain degradation heat map. In (c) and (d) the current steps are represented as a function of the scanner position. Also, the gate stripes are plotted within a distance of 9.1 μm (based on the technological information) and they are comparable with the stripes in the zoom visible in (a). Reprinted from [130]. © 2020, Martinella *et al.*, licensed under CC BY 4.0.

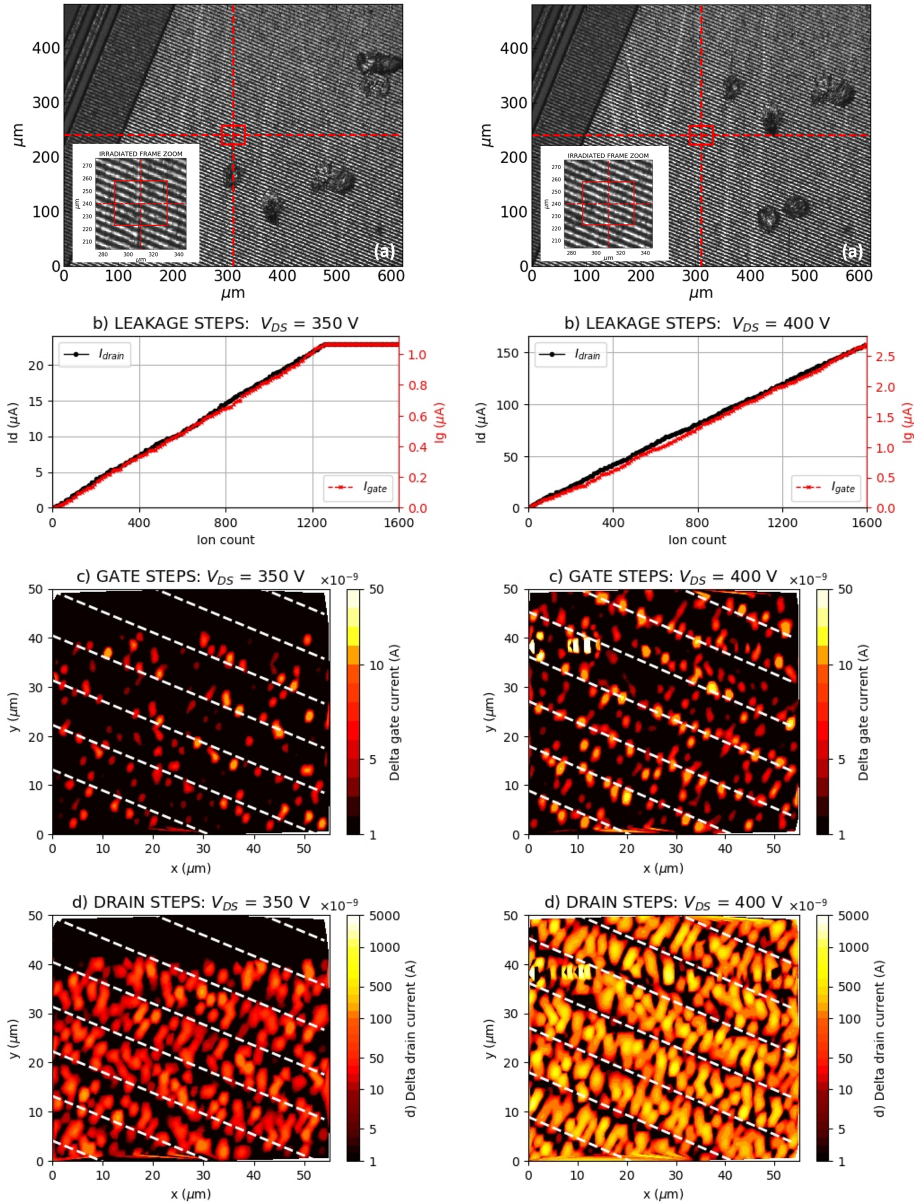


Figure 4.9: The runs refer to an 80-mΩ DUT exposed in region 2. (Left) V_{DS} = 350 V. (Right) V_{DS} = 400 V. From the top: (a) the frame selected for the irradiation is visible on top of the microscope image; (b) drain and gate leakage current steps measured during the irradiation; (c) gate degradation heat map (d) drain degradation heat map. In (c) and (d) the current steps are represented as a function of the scanner position. Also, the gate stripes are plotted within a distance of 9.1 μm (based on the technological information) and they are comparable with the stripes in the zoom visible in (a). Reprinted from [130]. © 2020, Martinella *et al.*, licensed under CC BY 4.0.

4.3.3 Cross-sections

The degradation rates were calculated both for the broad-beam and microbeam experiments and the details are discussed respectively in Paper I and Paper II.

The results from the broad-beam are reported in Figure 4.10 for the three tested devices, i.e., 25 mΩ, 80 mΩ and 160 mΩ. The results are shown for $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ ions from the 9.3 MeV/amu cocktail. The degradation rates for the drain current are normalized with the total fluence accumulated for each exposure (i.e., 10^6 ions/cm^2) and with the active area of each device. Furthermore, the two degradation mechanisms were equally observed in pristine devices and in devices irradiated multiple times, exhibiting degradation rates at the same magnitude, concluding that the prior degradation does not affect the degradation rate.

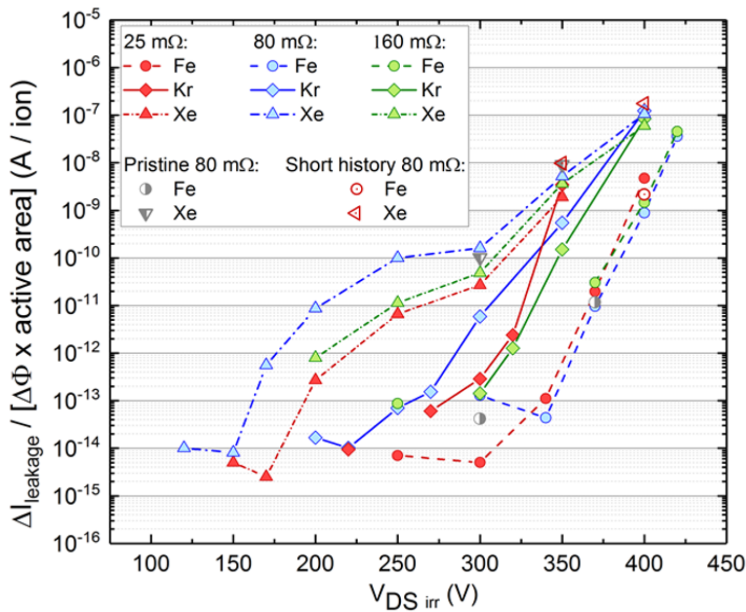


Figure 4.10: Drain degradation rates for the 25 mΩ, 80 mΩ and 160 mΩ devices from the exposed to heavy-ion broad-beam. Reprinted from [130]. © 2020, Martinella *et al.*, licensed under CC BY 4.0.

The microbeam results are compared with the broad beam ones in Figure 4.11, where the degradation rates are shown for both I_D and I_G. For the broad-beam data the approach was the same as discussed before, whereas for the microbeam the results were normalized considering the total amount of ions injected in the scanner frame. The two degradation mechanisms are clearly visible from these results, as the gate degradation rate generally diverges from the drain one and saturates at $V_{DS} \geq 350$ V. Furthermore, independently from the ion, the drain degradation rates converge when approaching the SEB region at $V_{DS} = \sim 500$ V. This is in agreement with the fact that for LET above 10 MeVcm^2/mg the SEB threshold is independent on LET.

Finally, the complementary cumulative distribution function (CCDF) or tail distribution was calculated for the degradation induced in the I_D and I_G by the microbeam irradiations. The results are shown in 4.12, for the four bias conditions discussed earlier in Section

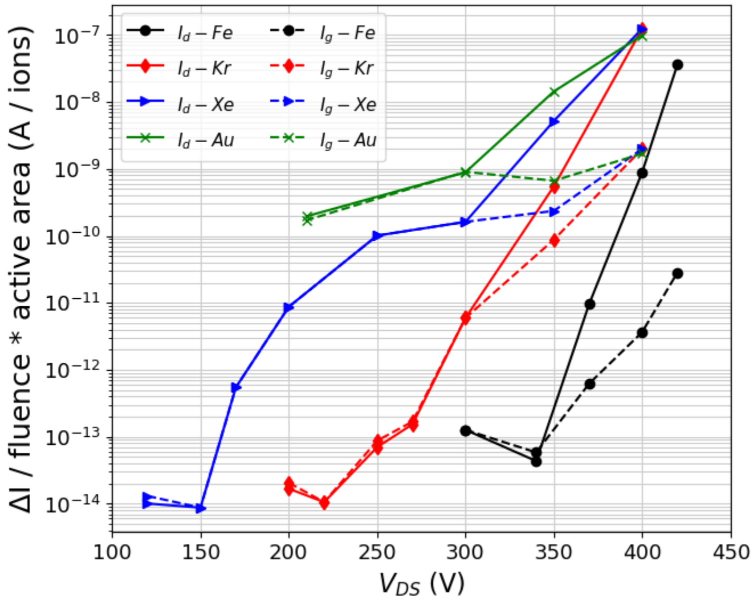


Figure 4.11: Gate and drain degradation rates for the 80 mΩ DUTs exposed to heavy-ion broad-beam and microbeam.

4.3.2. Each bin represents the probability of a degradation step with an amplitude larger than a given x-axis value, normalized by the bin width and the total number of ions. The irradiation window and the estimated neck region are illustrated on the graph. As expected, the probability of higher degradation steps increases with increasing V_{DS}. Furthermore, the probability for I_G saturates to values closer to the neck region, whereas for I_D this is observed only for exposures at $V_{DS} < 350$ V.

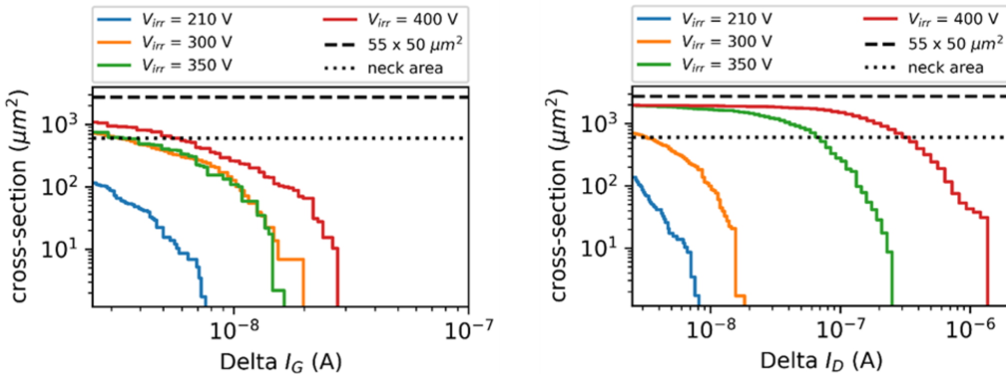


Figure 4.12: Tail distributions of the gate (lefts) and drain (right) degradation at different drain-source bias during the irradiation. For reference, the estimated neck (or JFET) area and the size of the exposure window are illustrated in the graphs. Reprinted from [130]. © 2020, Martinella *et al.*, licensed under CC BY 4.0.

4.3.4 Latent damage

Two additional experiments were performed at RADEF in order to study the latent damage in the SiC crystal lattice and in the gate oxide. These are fully discussed in Paper IV. In both cases, the irradiation were carried out using the 16.3 MeV/amu heavy-ion cocktail and selecting $^{40}Ar^{+14}$, $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ as the ion species for the test. The characteristics of the heavy-ions are reported in Table 4.2 and the setup used was the one described earlier in Section 4.1.4.

4.3.4.1 SiC crystal lattice latent damage

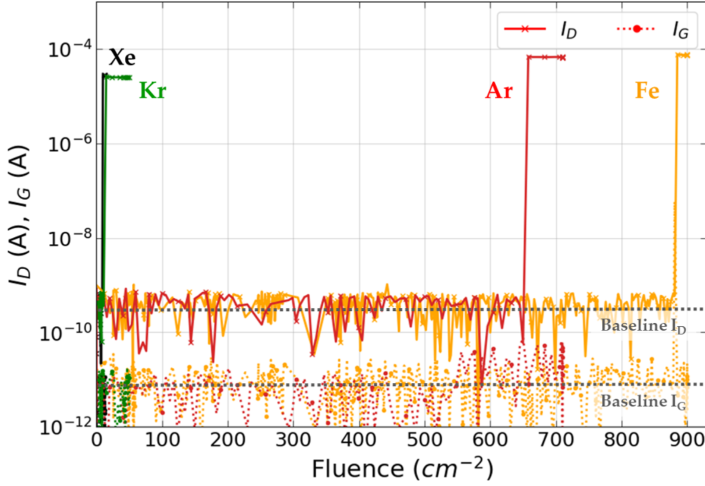
The first experiment was performed with the objective of investigating the failure observed during the post-irradiation V_{DS}-sweep (at V_{GS} = 0V) for devices exposed in the pre-SEB region. Bare die rated for V_{DS} = 1.2 kV with $R_{DS(on)}$ = 40 mΩ (CPM2-1200-0040B) were selected as DUTs (additional details in Table 4.3). During the exposure, V_{DS} = 450 V in order to protect from the SEB (for these parts approximately at V_{DS} = 500 V with LET > 10 MeVcm^2/mg) and investigate the pre-SEB region. The V_{GS} = 0 V, to force the DUTs in off-state. A flux of few tens of ions/cm^2s was used, and each die was exposed until the first radiation-induced step was observed in I_G and/or I_D. At this bias during the exposure, the very first signal of degradation can manifest itself in two different ways depending on the ion strike location, further described below.

In the first case, the first degradation step was observed only in the I_D, whereas no observable change was measured in the I_G . The results are summarized in Table 4.5 (DUTs 1-4). This observation is reported in Figure 4.13 (a), where the I_D and I_G measurements are shown for four pristine DUTs during the irradiations with $^{40}Ar^{+14}$, $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$. After the exposure, the V_{DS} was swept up to 1000 V at V_{GS} = 0 V, measuring the I_DV_{DS} and the I_GV_{DS} characteristics simultaneously. As visible in Figure 4.13 (b), all the four DUTs exposed at V_{DS} = 450 V failed during the post-irradiation V_{DS} sweep at 580 V < V_{DS} < 700 V. The failure was defined as I_D = 20 mA, which is the level of the compliance.

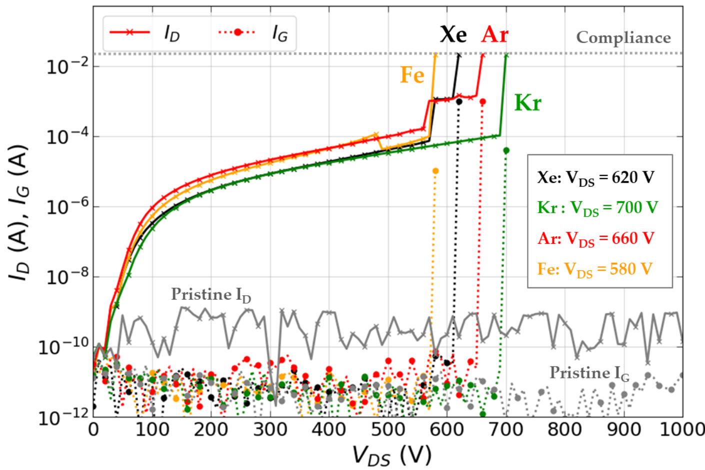
Table 4.5: Summary of degradation steps for each DUT

DUT	Ion	LET [MeVcm^2/mg]	Range SiC [μm]	ΔI_D [μA]	ΔI_G [μA]	$V_{DSfailure}$ [V]
1	$^{131}Xe^{+35}$	49.1	112.2	27.4	0	620
2	$^{82}Kr^{+22}$	25.3	125.7	24.7	0	700
3	$^{40}Ar^{+14}$	7.7	175.0	67.2	0	660
4	$^{56}Fe^{+15}$	14.6	136.4	75.1	0	580
5	$^{40}Ar^{+14}$	7.7	175.0	0.0013	0.0013	550

In the second case, during the exposure the step was observed both in the I_D and I_G ($|I_D| = |I_G|$). At V_{DS} = 450 V, this was observed only with $^{40}Ar^{+14}$, which has the smallest LET among the selected species. In this case, the device did not fail during the post-irradiation I-V measurements, showing the typical behaviour of the heavy-ion degraded device, with the current flowing between drain and gate, as already discussed in 4.3.1. However, after a second irradiation at V_{DS} = 480 V, the same post-irradiation failure was observed at V_{DS} = 550 V.



(a) First degradation step observed during the exposure.



(b) Post-irradiations $I_D V_{DS}$ and $I_G V_{DS}$. All the devices failed at 580 V $< V_{DS} <$ 700 V.

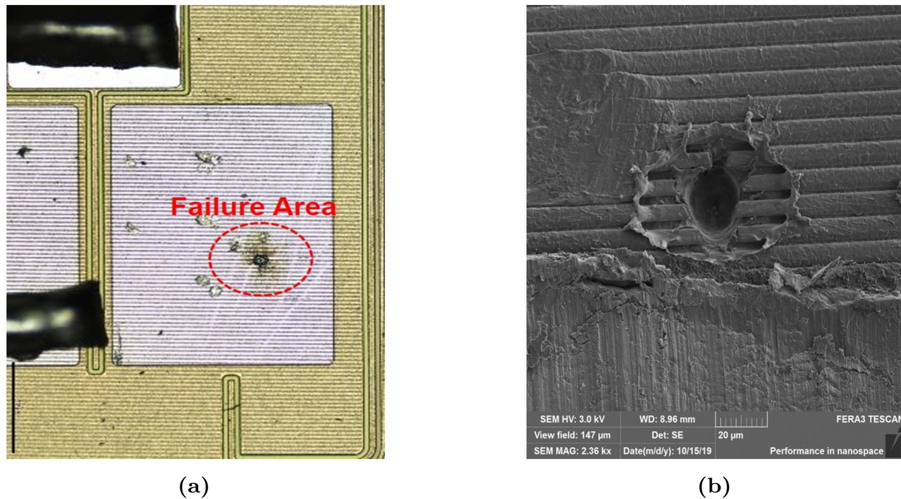
Figure 4.13: Results from irradiations with $^{40}Ar^{+14}$, $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ ions.

In conclusion, although the devices were sufficiently derated to protect from the SEB during the exposure, DUTs irradiations at V_{DS} = 450 V caused the DUTs failure during the post-irradiation operations. During the exposure, the very first degradation step was observed only in the I_D and involved the second mechanism of degradation via I_{DS} described earlier. However, for $^{40}Ar^{+14}$ which was the lightest ion used (i.e., LET = 7.71 MeVcm^2/mg), depending on the ion strike location the degradation was either observed only in I_D, or equally in I_G and I_D. In the first case the ion-induced damage involved the p-n junction region, while in the second the neck region. However, for $^{40}Ar^{+14}$ this result is expected, as V_{DS} = 450 V is the threshold to start observing degradation and the V_{DS} for the two mechanisms are not well defined as with the other ions.

This failure during the post-irradiation analysis was also frequently observed during the other test campaigns with the broad-beam and microbeam. In order to further investigate

this event, a Tescan Xe plasma FIB-SEM model Fera3 was used for inspection of the damage site of some devices that failed during the microbeam irradiation at GSI. The configuration is such that the electron and ion beam focal points coincide, enabling simultaneous SEM imaging during FIB milling tasks with Xe plasma. In the SEM two types of signal can be detected; the secondary electron (SE) and the backscatter electron (BSE). In the first case, due to inelastic interactions between the primary electron beam and the sample, the secondary electrons are emitted from the surface of the sample, providing information on the topography of the surface. In the case of BSE, the backscattered electrons originate from the elastic interaction with the atoms, creating a signal which is proportional to the atomic number, and therefore the BSE detector provides images that conveys information on the sample composition.

The area to be investigated was firstly identified with the microscope, as visible in Figure 4.14 (a). Figure 4.14 (b) shows a SEM image of the damage site on the die surface measured with SE detector. The hole generated by the failure extends over more than three gate stripes, for a length of ∼30 μm and a width of ∼20 μm.



(a) **(b)**

Figure 4.14: (a) Microscope image of the damaged area. (b) SEM image of the damage site on the die surface measured with SE detector.

The top row of Figure 4.15 shows the cross-section of the damaged site after FIB milling. The SEM images are measured with SE detector on the left and BSE detector on the right. Similarly, the SEM images in the bottom row, show a zoom on the damaged area. The hole has a depth of ∼18 μm, and it extends over the entire epitaxial-layer (5-18 μm). The image shows that the SiC crystal has melted, meaning that the localized temperature in the failure region reached the sublimation temperature of SiC (3003 K), and the materials in the layers above, which have a lower melting point, filled the hole. A crack which starts at the bottom of the hole is visible in both images. Finally, the vertical columns which appear in the cross-sections are artefacts due to the preparation of the sample.

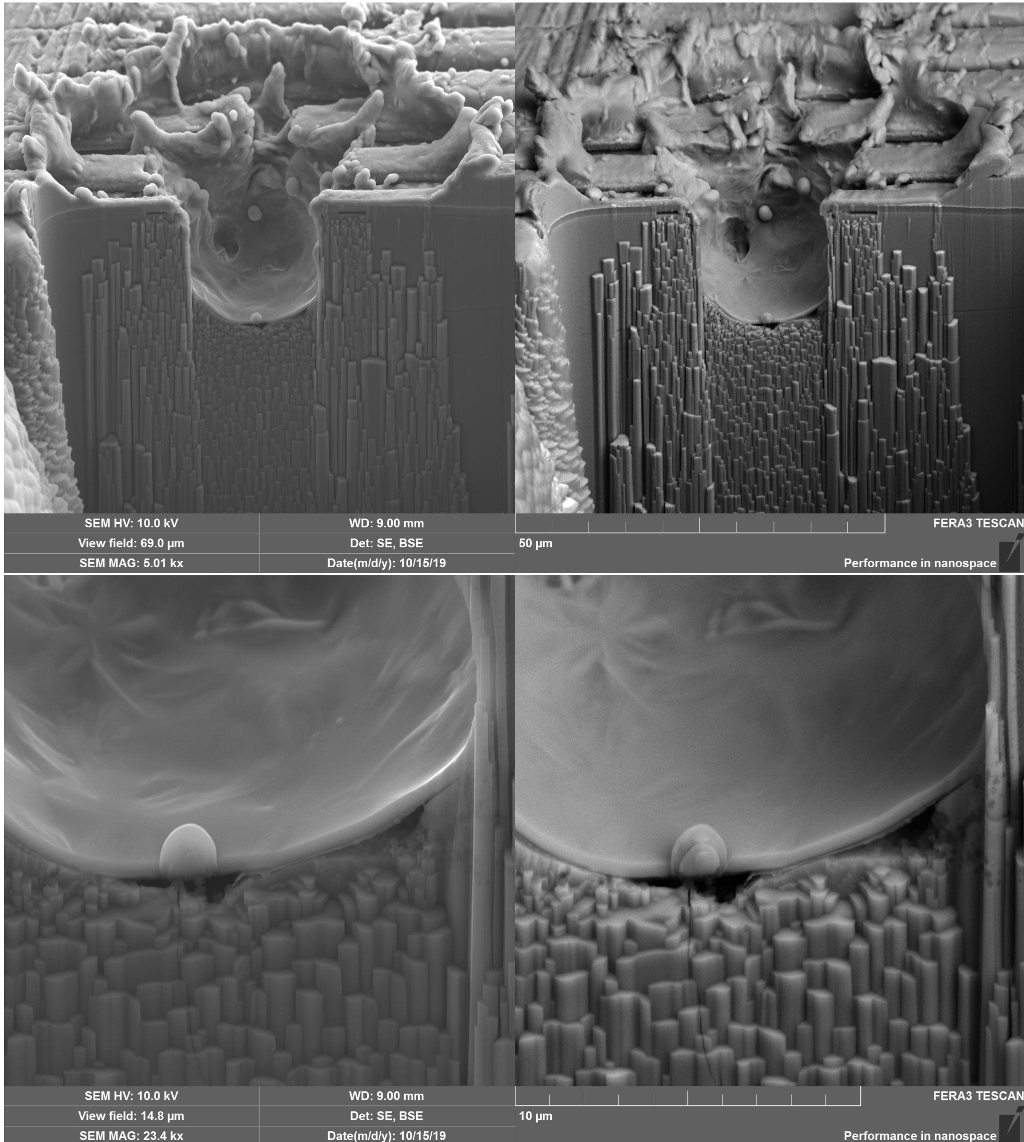


Figure 4.15: Top: cross-section of the damaged site after FIB milling. Bottom: zoom on the hole. The SEM images were measured with SE detector (left column) and BSE detector (right column).

4.3.4.2 Gate latent damage

The second experiment was performed with the objective to investigate the latent gate damage observed during the post-irradiation V_{GS} sweep (at V_{DS} = 0.1 V) for devices exposed in the pre-degradation region. Bare die rated for V_{DS} = 1.2 kV with $R_{DS(on)}$ = 160 mΩ (CPM2-1200-0160B) were selected as DUTs (additional details in Table 4.3). During the exposure, the V_{DS} was set sufficiently low to protect from degradation, whereas the V_{GS} = 0 V, to force the DUTs in off-state. Each run was performed with a flux of 10^4 ions/cm^2s and up to a fluence of 10^6 ions/cm^2. No degradation steps were observed during the exposure. If the degradation was observed, the run was repeated with a pristine device decreasing the V_{DS} during the irradiation. After each run the following post-irradiation measurement were performed:

- $I_D V_{DS}$ and $I_G V_{DS}$ with V_{DS} = [0 V - 1000 V] and V_{GS}= 0 V;
- $I_D V_{GS}$ and $I_G V_{GS}$ with V_{GS} = [0 V - 20 V] and V_{DS}= 0.1 V;
- $I_D V_{GS}$ and $I_G V_{GS}$ with V_{GS} = [0 V - -5 V] and V_{DS}= 0.1 V;

where V_{GS} = -5 V/+20 V are the recommended operational values from the datasheet. From the experiment it was possible to identify a threshold V_{DS} for each ion species where no degradation is observed during the exposure, but the latent damage at the gate is sufficient to cause the oxide rapture during the post-irradiation V_{GS} sweep up to +20 V. The range for the threshold voltages are listed in Table 4.6. For comparison, also the threshold voltages for degradation are reported. The results from the run with $^{131}Xe^{+35}$ at V_{DS} = 60 V are shown as an example in Figure 4.16. No degradation was observed during the exposure, however the gate oxide failed at V_{GS} = 10 V during the post-irradiation sweep, showing a gate latent damage induced by the ion-exposure. From the operational point of view, the device is considered not operable anymore, being the $I_G > 10^{-9}$ A and therefore out of specifications.

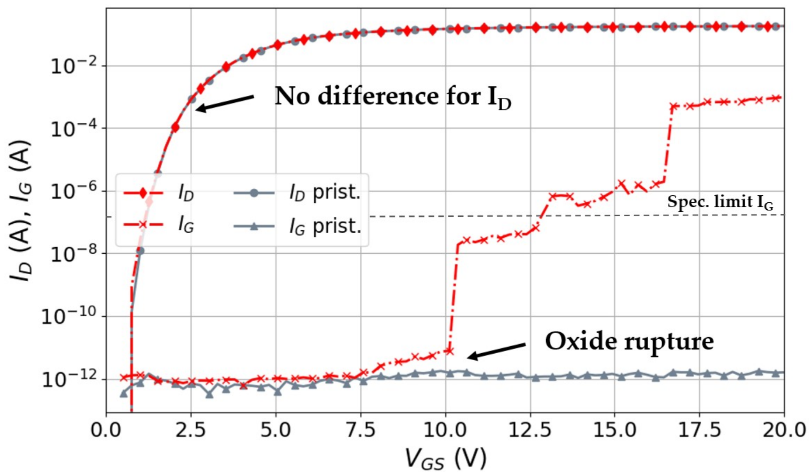


Figure 4.16: $I_D V_{GS}$ and $I_G V_{GS}$ of a DUT exposed to $^{131}Xe^{+35}$ at V_{DS} = 60 V. No degradation was observed during the exposure, but the oxide broke at V_{GS} = 10 V due to the latent damage.

Table 4.6: Threshold voltage for gate latent damage $V_{DS-l.d.}$ and degradation $V_{DS-degr}$.

Ion	LET [MeVcm^2/mg]	Range SiC [μm]	$V_{DS-l.d.}$ [V]	$V_{DS-degr.}$ [V]
$^{131}Xe^{+35}$	49.1	112.2	50-60	120
$^{82}Kr^{+22}$	25.3	125.7	50-80	170
$^{56}Fe^{+15}$	14.6	136.4	80-100	300
$^{40}Ar^{+14}$	7.7	175.0	350-370	450

It should be noticed that the V_{DS} necessary to observe gate latent damage is extremely low compared to the maximum rated voltage (less than one tenth). It is also much lower in respect to Si power MOSFETs, despite the fact that the gate oxide maximum field strength is comparable between the two technologies. In fact, as already discussed in 3.6.3.4, the oxide in SiC can easily exceed its breakdown field strength, if not designed properly [8, 27]. Abbate *et al.* performed numerical simulations to confirmed that the voltage in the gate oxide can reach the oxide breakdown level for V_{DS} thresholds comparable with the experimental ones [148].

Finally, the threshold voltages for gate latent damage presented in this work did not consider LET $<$ 7.7 MeVcm^2/mg. However, it was experimentally demonstrated that a minimum LET is required to observe latent damage during the PIGS test, and no oxide latent damage was reported for LET = 1.0 MeVcm^2/mg [8] .

4.4 Discussion

4.4.1 SELC mechanisms

As anticipated in 3.6.3.1, two different mechanisms were identified for the SELC degradation, involving different areas of the MOSFET structure. The first mechanism was observed for irradiations at $V_{DS} < 350$ V and it is attributed to the oxide damage, which results in a leakage path between drain and gate (I_{DG} degradation). The second mechanism, instead, was observed at $V_{DS} \geq 350$ V and it involves the p-n junction, resulting in a leakage path mostly between drain and source (I_{DS} degradation). The second mechanism is triggered when certain electrical conditions are created within the p-n junction during the exposure. For the 2nd gen. Cree/Wolfspeed this threshold was observed at $V_{DS} \sim 350$ V (~30 % of the maximum voltage), but it can vary depending on the rated voltage and the manufacturer. For the 3rd gen. devices rated for 900 V, the threshold was identified at $V_{DS} \sim 320$ V (~35 % of the maximum voltage). The variability between the two gen. is likely to be related to the differences in the neck width, with the 3rd gen. devices having a smaller cell pitch and thus narrower neck region [6].

The different regions for the drain leakage response of a device exposed to heavy ions are summarised in Figure 4.17 and updated with the new observations. At low bias voltages, is the region of the charge collection, where no permanent damage is observed in the device and the charge induced by ionization is collected with a similar multiplication mechanism as in Si MOSFETs. Increasing the bias, is the region of the degradation, where two sub-regions are identified. First, between V_{th1} and V_{th2}, the area underneath the gate (JFET and channel regions) is the most sensitive for SELC. The second mechanism is newly added at biases higher than V_{th2}, when higher SELC is measured in the p-n junction region, with a remaining smaller leakage through the gate-oxide. In the third region, at sufficiently high bias above V_{th3}, a destructive SEB failure occurs.

The first mechanism of degradation is explained through the hypothesis of a soft oxide breakdown, previously discussed for Si power MOSFETs in [149, 162]. The Quantum Point Contact (QPC) model was employed to explain the enhanced leakage currents, involving the generation of conductive paths in the gate oxide which behave as point contacts between the gate and the substrate [175].

Concerning the second mechanism of degradation, the SELC via p-n junction is hypothesized to originates from the thermal stress induced by the highly located power dissipation, as previously suggested by Ball *et al.* [151], and described in 3.6.3.2. In the same work it was suggested that a common mechanism is responsible for leakage current degradation in SiC power MOSFETs and JBS diodes. However, from the experimental observations, we hypothesized that the common degradation mechanism only involves the SELC through the p-n junction, and therefore observed for voltage bias higher than V_{th2} (i.e., $V_{DS} > 350$ V for the studied DUTs). Moreover, molecular dynamic (MD) simulations showed that amorphous regions appear along the ion track starting from certain values of applied V_{DS} during the exposure [176]. These regions are unlikely to recrystallize back completely, leaving permanent structural modification in SiC lattice [177]. Therefore, it is hypothesized that the thermal transient and excessive lattice temperature cause the formation of permanent extended defects (EDs) which can be different dislocations, amorphous pockets, different SiC solid-phase (polytype) inclusions, stacking faults, clusters, and so on. Further investigation of the irradiated structures with electron microscopy and optical methods [178, 179] could provide additional information on the ED nature.

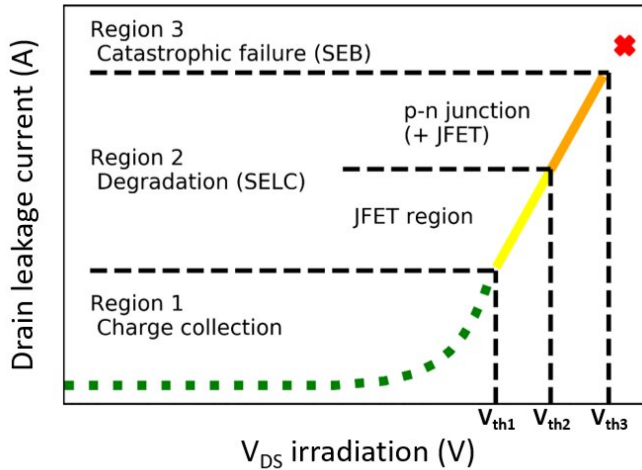


Figure 4.17: Three characteristic regions of damage for a SiC power MOSFETs exposed to heavy-ions. The I_D is represented as a function of the V_{DS}. Two sub-regions are identified for degradation (region 2). Firstly, between V_{th1} and V_{th2}, the area underneath the gate (JFET or neck region + channels) is the most sensitive for SELC. The second mechanism is newly added at biases higher than V_{th2}; higher SELC is measured in the p-n junction area, but a smaller leakage remains also through the gate oxide. Reprinted from [130]. © 2020, Martinella *et al.*, licensed under CC BY 4.0.

4.4.2 RADMOS model

An electrical equivalent for the current leakage path in a degraded SiC vertical MOSFET was discussed in Paper I and it is shown in Figure 4.18. It represents the leakage current path observed for a device which was exposed to heavy-ions at $V_{DS} > 350$ V, and therefore which experienced degradation in the JFET and p-n junction regions. The electrical equivalent models the current transport for $I_D V_{DS}$ and $I_G V_{DS}$ with V_{DS}=[0 V - 100 V].

Initially, at low V_{DS}, the current flows from drain to gate with a linear dependence on the applied bias. Therefore, the current-voltage characteristic can be modeled by a simple resistor which has two components:

- R_{ox} which represents the oxide resistance and it is divided in R_{ox1} and R_{ox2} to simulate the potential gradient inside the oxide;
- R_{epi} which represents the epitaxial layer resistance.

For a pristine device, $R_{ox} \sim \infty$ and I_G is negligible, the leakage flows through the body diode, hence trough the body resistance R_{body}. However, this is not the case for a degraded device, meaning that $R_{ox} \ggg R_{body}$ in a pristine device and $R_{body} \ggg R_{ox}$ in a degraded one. Differently, increasing the V_{DS}, the current path was observed to be mostly between drain and source, with a small contribution between drain and gate.

Following these observations, it was hypothesized that the leakage path through the gate oxide generates a voltage drop sufficient to partially open the channel. This effect sets the MOSFET in a condition of "partial on-state", which allows the current path to the source. A MOSFET named RADMOS was used to model the very small part of the channel

which opens as a consequence of the voltage drop in the gate oxide. The gate terminal of the RADMOS is controlled by the potential created in the gate oxide. If the gate leakage current is sufficiently high, the $V_{GS-RADMOS} \geq V_{th-RADMOS}$, the MOSFET is in a partial on-state condition and the current starts to flow to the source.

In order to confirm this hypothesis, the measurements for I_D, I_S and I_G of the 80 mΩ DUT irradiated with $^{56}Fe^{+15}$, $^{83}Kr^{+22}$ and $^{131}Xe^{+35}$, were compared with fit lines and simulations performed in LTspice software. The details are discussed in Paper I and only the general procedure is reported here. Firstly, fits were performed for the I_G and I_D measurements. It was demonstrated that for $V_{DS} < 100$ V, the I_G follows a linear characteristic (i.e., ohmic), whereas the I_D follows a quadratic trend, typical of the MOSFET in on-state. The following equation was used to fit the drain current:

$$I_S = \frac{1}{2}K\left(\frac{V_{DS}}{B-2.6}\right)^2 * (1+\lambda V_{DS}) \tag{4.1}$$

where K is the transconductance, B = $(R_{ox1}+ R_{ox2})/R_{ox2}$ and λ = ΔL/L where L is the channel length. All the parameters (i.e. B, K, λ and R_{ox}) were extracted for each of the three ions and are tabulated in the paper. Successively, electrical simulations were performed using the electrical equivalent showed in Figure 4.19 to describe the degraded device. R_{ox1} and R_{ox2} were adjusted for each case on the values extracted from the fit, as described above. As first approximation, the RADMOS was considered to have a threshold voltage of 2.6 V, which is the typical value for a pristine device.

The comparison between the current measurements, the simulations results and the fit are shown in Figure 4.20 (a) and (b) for the DUTs exposed to $^{56}Fe^{+15}$, and $^{131}Xe^{+35}$, respectively. The results for $^{83}Kr^{+22}$ are reported in the paper, and the same considerations apply also in this case. A very good agreement is observed between the measurements, the fit and the electrical simulations, which confirms the linear ohmic behavior for the gate current and the MOSFET behavior above the RADMOS threshold voltage for the

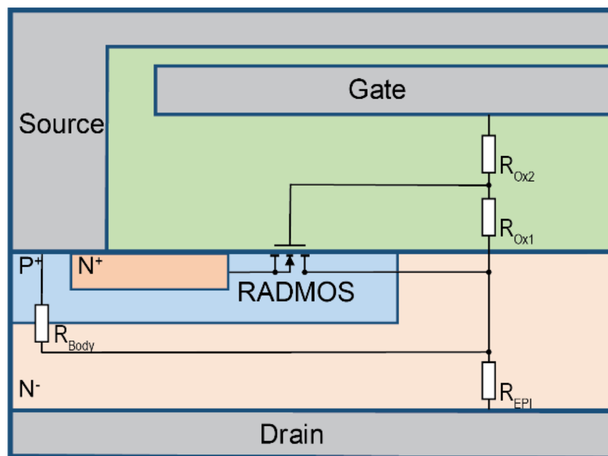


Figure 4.18: Electrical equivalent for the heavy-ion induced current transport model in a degraded SiC power VD-MOSFET, valid at $V_{DS} < 100$ V. Reprinted with permission from [146]. © 2019, IEEE.

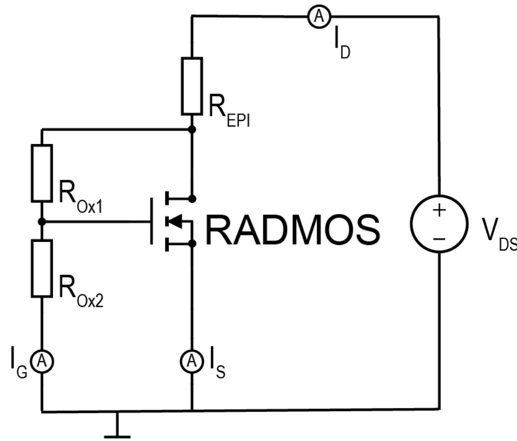
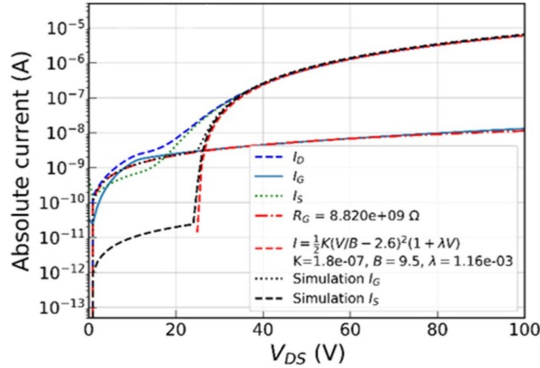


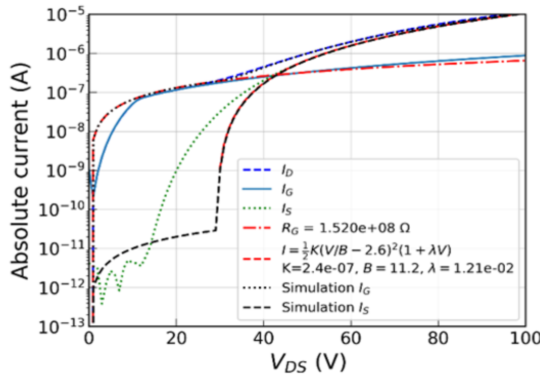
Figure 4.19: Electrical schematic of the model proposed, used to perform simulations at V_{DS} < 100 V. Reprinted with permission from [146]. © 2019, IEEE.

drain and source current. In conclusion, the model proposed describes accurately the current path at V_{DS} < 100 V for a degraded device irradiated with $^{56}Fe^{+15}$, $^{83}Kr^{+22}$ and $^{131}Xe^{+35}$ at V_{DS} > 350 V (i.e. V_{th2} in Figure 4.17).

Differently, at V_{DS} > 100 V another current transport mechanism becomes dominant, which is not fully explained by the model above. The I_G and I_D are observed to follow an exponential trend, with a linear dependency between them, as visible in Figure 4.21. The current amplifications, which are different depending on the heavy-ion used, are reported on the graph and indicated as β.



(a) $^{56}Fe^{+15}$.



(b) $^{131}Xe^{+35}$.

Figure 4.20: Comparison of measurements, fit and simulation results. The electrical model proposed accurately describes the current path for a degraded 80 mΩ device at $V_{DS} < 100$ V. Reprinted with permission from [146]. © 2019, IEEE.

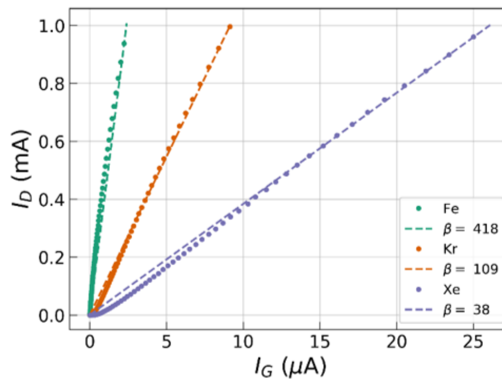


Figure 4.21: At $V_{DS} > 100$ V, the drain and gate current have an exponential trend, with a linear dependency between them. The current amplification β is reported in the plot. Reprinted with permission from [146]. © 2019, IEEE.

4.5 Summary of heavy-ion effects

A large data set was collected during the different tests campaign performed with the heavy-ion-broad beam and microbeam. The heavy-ion-induced SEEs observed for the devices from the 2nd generation Cree/Wolfspeed, are graphically represented in Figure 4.22 as function of the ion LET and the V_{DS} bias during the exposure. The results are also summarized in Table 4.7. However, since in this work all the heavy-ion experiments were performed using planar MOSFETs from Cree/Wolfspeed, and considering that design and carrier concentrations vary between device types and manufacturers, the results cannot be transferred to all SiC power devices without further analysis.

Five different regions of damage with the respective thresholds are identified varying the LET and the V_{DS} selected during the experiments. A "hockey stick" trend is observed for all the effects, with the regions becoming narrower and the threshold voltages less distinguishable with decreasing LET. No data were collected for LET < 7.7 MeVcm^2/mg, but eventually the ion damage is insufficient to induce degradation and latent damage, and the device directly experiences SEB at higher bias.
At low drain-source bias, the first type of effect observed is the gate latent damage. The V_{DS} necessary to observe this effect is extremely low compared to the maximum rated voltage (less than a tenth). At higher bias, the heavy-ion exposure induces the first type of SELC, named "degradation I", where the area underneath the gate oxide is the most sensitive (JFET region + channels). Increasing the voltage, the second type of SELC, labelled "degradation II", is observed. In this case the damage involves mostly the p-n junction region, but a smaller leakage remains also through the gate-oxide. Over a certain V_{DS} threshold, in the pre-SEB region, a second latent damage involves the SiC crystal lattice. After the irradiation, when drain-source bias is applied, the localized power density induces an increase of temperature, which ultimately causes the sublimation of the SiC crystal. Finally, for higher voltages, the device experiences directly a destructive SEB, as reported in [180] for $V_{DS} > 500$ V and LET > 10 $MeVcm^2/mg$.

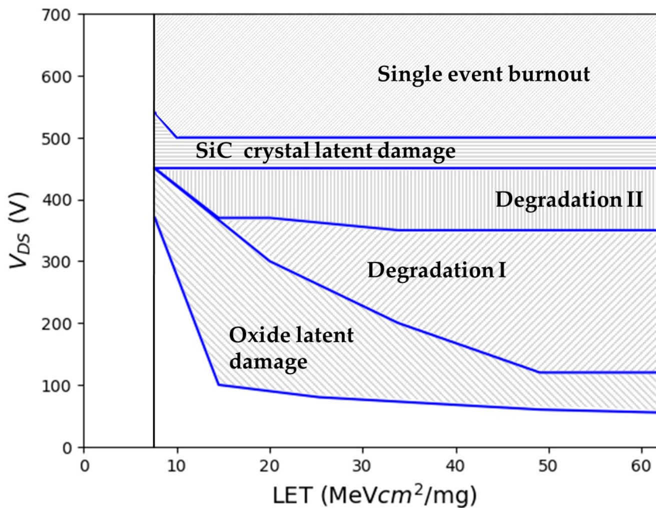


Figure 4.22: Heavy-ion-induced effects observed during broad-beam and microbeam experiments, as a function of the ion LET and drain-source bias during the exposure. The plot follows the representation as proposed for SiC JBS diodes in [136].

Table 4.7: Summary of heavy-ions effects for broad-beam and microbeam irradiations.

Ion	LET	Energy/amu	Facility	Range SiC	$V_{DS-l.d.}$	$V_{DS-degr.I}$	$V_{DS-degr.II}$	$V_{bulkfailure}$	SEB
	[MeVcm^2/mg]	[MeV/amu]		[μm]	[V]	[V]	[V]	[V]	[V]
$^{40}Ar^{+14}$	7.7	16.3	RADEF	175.0	350-370	450	450	450	500
$^{56}Fe^{+15}$	14.6	16.3	RADEF	136.4	80-100	300	370	450	500
Ca	17	4.8	GSI	29.7	-	340	370	-	500
$^{56}Fe^{+15}$	20.0	9.3	RADEF	64.2	80-100	300	-	-	-
$^{82}Kr^{+22}$	25.3	16.3	RADEF	125.7	50-80	170	-	450	500
$^{82}Kr^{+22}$	33.7	9.3	RADEF	62.5	-	200	350	-	500
$^{131}Xe^{+35}$	49.1	16.3	RADEF	112.2	50-60	120	350	-	500
$^{131}Xe^{+35}$	62.3	9.3	RADEF	60.1	50-60	120	350	-	500
Au	94	4.8	GSI	35.4	-	140	350	-	500

5 Atmospheric-neutron and high-energy proton experiments

This chapter discusses the SEB experiments performed with lighter particles, such as atmospheric neutrons and high-energy protons, on different commercial SiC technologies produced by different suppliers. Three different types of architecture were selected: planar gate, trench gate and double-trench, where the last has a trench gate and source. Firstly, the beamline is introduced for each experiment, providing the details of the beam parameters. Then, after presenting the experimental setup and method, the results are discussed.

Concerning the terrestrial-neutron irradiations, failure cross-sections and FIT rates were calculated for the tested references. From the post-irradiation analysis, the failure mode and the impact of gate rupture in planar and trench gate design are discussed, highlighting the differences among the device types. Finally, the results for the post-irradiation gate stress (PIGS) are also presented. A detailed description of the experiment is discussed in Paper III [32].

From the high-energy proton experiments, the maximum drain-source bias at which no SEB occur were identified, for a target fluence of 10^{11} protons/cm^2. Additionally, the effect of the beam angle of incidence was also investigated. However, the proton results have to be considered preliminary, as additional statistics are needed in order to consolidate the outcomes.

5.1 Atmospheric neutrons

5.1.1 The ChipIr terrestrial neutron facility

ChipIr is a beamline built at the second target station (TS2) of the ISIS spallation source at the Rutherford Appleton Laboratory, Didcot (UK) [181−184]. The beamline design is optimized to mimic the atmospheric neutron spectrum (up to 800 MeV) with an acceleration factor of up to 10^9 for ground-level applications. The facility is specifically tailored for testing radiation effects on electronic components and systems. In Figure 5.1 the layout of the ChipIr facility is shown. The beam enters the room through a hole in the backward wall, as visible in Figure 5.2. Two remote-controlled optical tables are available in the irradiation room for the setup installation. During the test campaign, the front table closer to the beam aperture was used for the DUTs installation. Additional technical information can be found in the ChipIr webpage [185].

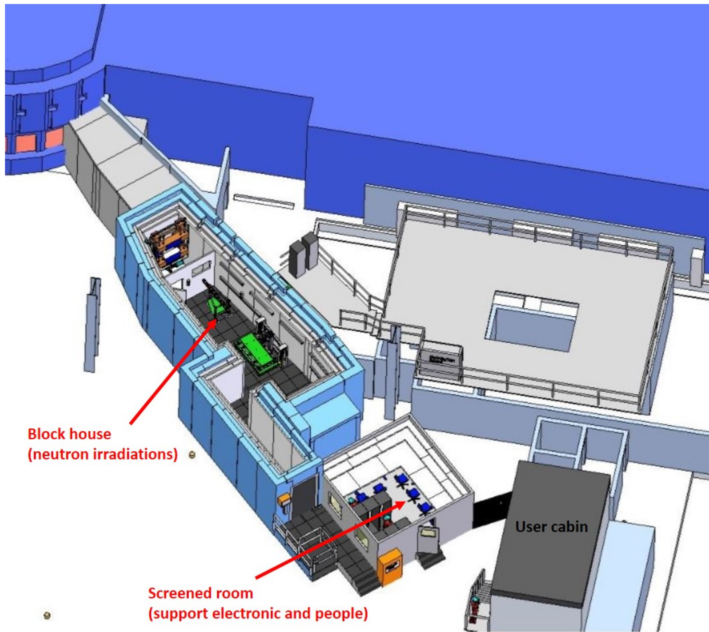


Figure 5.1: ChipIr facility layout, after [185].

5.1.2 Terrestrial neutron beam

The spallation neutrons delivered in ChipIr are produced from the collisions of the high-energetic protons (i.e., 800 MeV protons extracted from the synchrotron in a beam of 40 μA and pulsed at 10 Hz) with a tungsten target. The fast neutron (En > 1 MeV) beam is then collided with a secondary scatterer, which allows to optimize the hard atmospheric-like spectrum and to minimize the gamma-ray flux. The resulting fast neutron spectrum is similar to the atmospheric one [82] with energies up to 800 MeV [181], see Figure 5.3. The neutron flux has been studied by different methods and details of its spectral distribution and hardness can be found in [186, 187]. The neutrons are delivered into ChipIr according to the time structure of the ISIS source; i.e., pulsed at 10 Hz, with two 70-ns-wide bunches separated 360 ns apart. Immediately in front of the exit

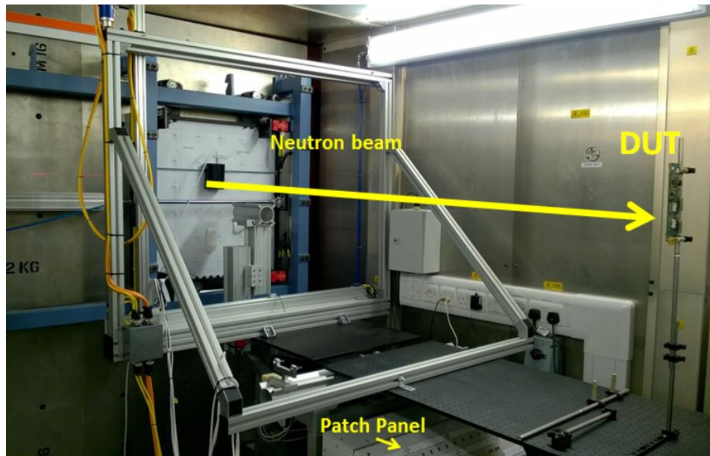


Figure 5.2: ChipIr experimental all, after [185].

window, a silicon diode measures pulse per pulse the energy deposition, which is used to retrieve the neutron fluence. A correction factor is applied to take into account the distance between the DUT position and the diode, since the beam may be attenuated by the air. A collimator system allows for selecting beams of different sizes. During the current test campaign, the flux of neutrons above 10 MeV was determined as $5.6{\cdot}10^6$ $\text{cm}^{-2}\text{s}^{-1}$ at the testing position, with a beam size of $10{\cdot}10$ cm^2.

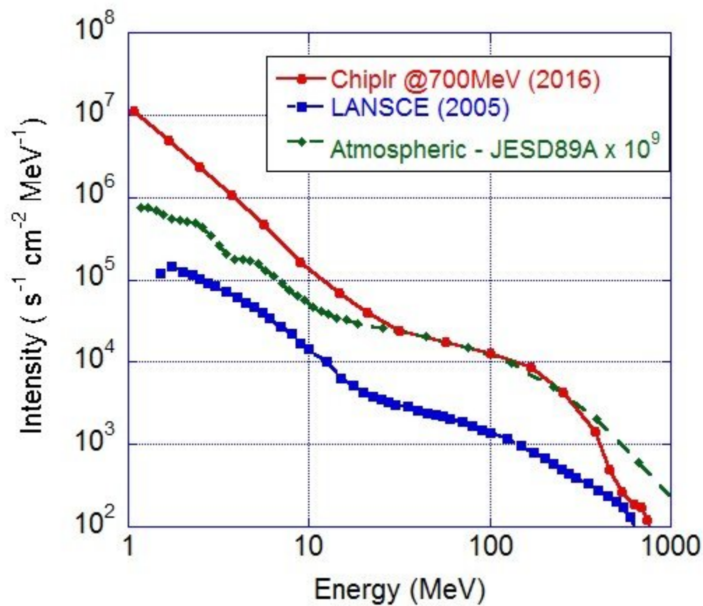


Figure 5.3: The ChipIr neutron spectrum (up to 800 MeV) compared to the atmospheric [82] and LANSCE spectra. Reprinted from [181]. © 2018, Cazzaniga *et al.*, licensed under CC BY 3.0.

5.2 Experimental setup and method

The objective of the test ChipIr campaign was to investigate the effect of terrestrial-neutron irradiation on different SiC MOSFETs technologies available on the market. Accelerated SEB tests were performed to calculate the cross sections and Failure in Time (FIT) rates. Additionally, the devices that did not exhibit destructive failure during exposure were characterized and their operational reliability was studied.

Several samples were selected from the commercial technologies. The references and the corresponding technical information are listed in Table 5.1. All the devices are rated for 1.2 kV and mounted in a TO-247 package. The first three and the last two devices have similar values of $R_{DS(on)}$. The first three DUTs were chosen following the requirements for the IA application at CERN, described in Section 2.3.4. The references were selected with three different architectures: planar, trench and double trench, as described in Section 2.2.3. In particular, the $CoolSiC^{TM}$ MOSFETs from Infineon have a trench gate structure [31], whereas the devices from Rohm have a double trench design, with trench gate and trench source. For the trench gate devices, the channel is formed vertically, which allows the vertical conduction of current and the reduction of $R_{DS(on)}$. All the other references have a planar gate structure, as described in Section 2.2.3. Schematics of the three architectures are shown in Figure 2.9.

Table 5.1: Commercial SiC vertical power MOSFETs tested with terrestrial neutrons at ChipIr. Three gate architectures were used: planar (pl.), trench (tr.) and double trench (d. tr.).

DUT	Manufacturer	Gen.	$R_{DS(on)}$ [mΩ]	V_{DS} [kV]	$I_{D@25}$ [A]	Gate [V]	BV_{DSS}
C2M0025120D*	Cree/Wolfspeed	II	25	1.2	250	pl.	1720
SCT3030KL*	Rohm	III	30	1.2	180	d. tr.	1926
SCTWA50N120	ST Micr.	II	59	1.2	130	pl.	1520
IMW120R090M1H*	Infineon	V	90	1.2	50	tr.	1483
MSC025SMA120B	Microsemi	II	25	1.2	275	pl.	1586

*Also tested with high-energy protons.

The setup was designed following the military standard regulations (MIL-STD-750E M1080.1) [83]. A maximum of 12 DUTs were installed in parallel on each board. A schematic layout of the setup is shown in Figure 5.4, where only 2 DUTs are illustrated for brevity. Two boards were stacked during each exposure to test a maximum of 24 DUTs. The two PCBs were placed at a distance of 58 cm and 76 cm from the beam aperture. The attenuation of the neutron beam in the first board was estimated to be negligible for the material used [183]. The gates were grounded directly on the boards, whereas two Keithley SMU model 2410s [188] (one channel, up to 1100 V), one for each board, were used to bias the drain and to monitor the total drain leakage as a sum of all devices. A stiffening capacitor of 10 nF was installed between the drain and the ground of each DUT, in order to limit the momentary voltage drop at the SMU output during current transients and supply sufficient amount of charge during a destructive event. The devices were connected in parallel to the high voltage, but each of them had an individual current limiting resistor of 860 kΩ between the drain and the SMU output. This guaranteed the isolation of the device after a failure and the continuous application of high voltage to all other devices. Each step increase in the total current monitored was counted as a failure

($\Delta I_{DS} = 1.27$ mA). This value corresponds to a short circuit on the DUT, when the total voltage is applied across the protection resistor. For each reference, three irradiations were performed on pristine devices at V_{DS} of 1100 V, 976 V and 846 V, which are $\sim$ 92 %, $\sim$ 81 % and 72 % of the maximum rated voltage (1.2 kV), respectively. With the gate directly grounded on the board, $V_{GS} = 0$ V during the exposure, therefore the DUTs were in off-state and the gate current was not monitored during the run. The test was stopped when 50% - 70% of devices failed or when a fluence of $2.8 \cdot 10^{10}$ n/cm^2 was reached. Figure 5.5 shows an example of the online measurement recorded during the irradiation of Rohm devices exposed at 1100 V.

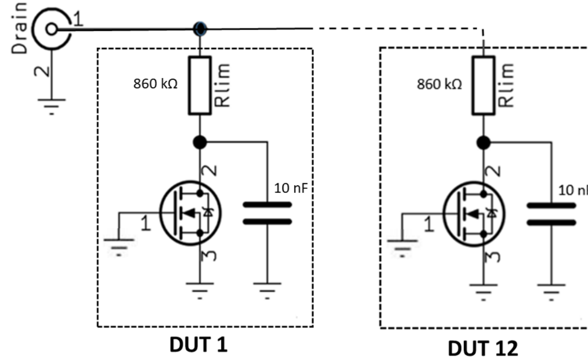


Figure 5.4: Electrical schematic of the experimental setup. For brevity, only two out of the twelve DUTs are represented. Two boards were used for each run, for a maximum of 24 DUTs exposed. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

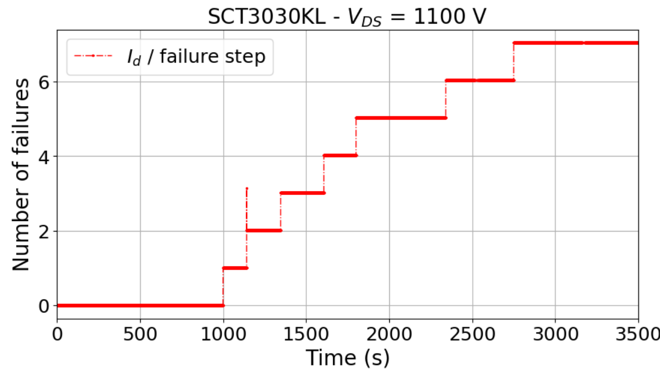


Figure 5.5: Online measurement of Rohm devices (SCT3030KL) exposed at 1100 V. In order to highlight the number of failures during the run, the I_D is divided by the failure step size. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

To investigate the damage, some DUTs were characterized after the irradiation using a Keithley Parametric Curve Tracer PCT-4B [189]. The breakdown voltage (BV_{DSS}) measurements were also conducted using a Keithley SMU 2657A [190] on the drain and a Keithley SMU 2636B [191] on the gate and the source terminals. For a pristine DUT, the BV_{DSS} is the voltage at which the reverse-biased body-drift diode breaks down causing significant current to flow between source and drain due to the avalanche multiplication process, as explained in Section 2.1.6.

5.3 Neutron irradiation results and discussion

5.3.1 Failure cross-sections and FIT rates

A standard 2-parameter Weibull distribution [192] was used to determine the reliability parameters and calculate the failure cross-sections (σ_{SEB}) and FIT rates for the tested references. The cumulative fraction of failed devices was calculated as a function of the neutron fluence; the 2-parameter Weibull distribution was fit to the data using a maximum likelihood estimation (MLE) method [193]. Two parameters were obtained from this analysis: the shape parameter β, which is an indicator of the failure mechanism, and the scale parameter η. For stochastic neutron failures $\beta = 1$ is expected, as representative of random events. The mean time between failures (MTBF) and the SEB cross-sections (σ_{SEB}) were calculated as:

$$\begin{aligned} MTBF &= \eta\,\Gamma(1+\frac{1}{\beta}) \quad when \quad \beta \neq 1 \\ MTBF &= \eta \quad when \quad \beta = 1 \\ \sigma_{SEB} &= \frac{1}{MTBF} \end{aligned} \tag{5.1}$$

A Poisson distribution dominated by the count statistics was considered to calculate the error bars. The uncertainty over the fluence was evaluated to be negligible with respect to the number of events. The upper and lower limits were calculated as:

$$\begin{aligned} Err_{high} &= \frac{N_{high}}{N_{SEB} * MTBF} \\ Err_{low} &= \frac{N_{low}}{N_{SEB} * MTBF} \end{aligned} \tag{5.2}$$

where N_{low} and N_{high} were obtained from the chi-square distribution with a confidence level of 95 %. The FIT rates were calculated considering 10^9 hours of operation and a cosmic-ray-induced neutron flux of 13 n/(cm^2h) for energies above 10 MeV (reference conditions at sea level in NYC from JEDEC JESD89A [82]). The error bars were calculated using the same conversion factor. During some runs, multiple SEBs were observed at the same time. They were considered as a single event to assure the independence between the SEB, and the total number of DUTs considered in the analysis was reduced

All the parameters (i.e. β, η, MTBF, σ_{SEB}) were calculated for each run of each reference and are reported in Table II in Paper III [32]. These results are graphically represented below. The failure cross-sections are visible in Figure 5.6 (a) as a function of the bias during the irradiation. In Figure 5.6 (b) the FIT rates are shown for the tested references, whereas in Figure 5.6 (c) the FIT rates are normalized with the active area and scaled by the avalanche breakdown voltage, such that a ratio of 1 would indicate that the critical field was reached, as suggested in [134]. A common trend is observed for all the devices and highlighted by the gray shadow. The trench MOSFETs (i.e. IMW120R090M1H and SCT3030KL) appear to have lower FIT rates with respect to the planar architecture. In particular, the double-trench device (SCT3030KL), which has the highest avalanche breakdown voltage, has the best performance. Finally, only two failures occurred for SCT3030KL exposed at V_{DS} = 1100 V; such low statistics explains why the cross-sections and FIT results do not increase with respect to the run at V_{DS} = 976 V.

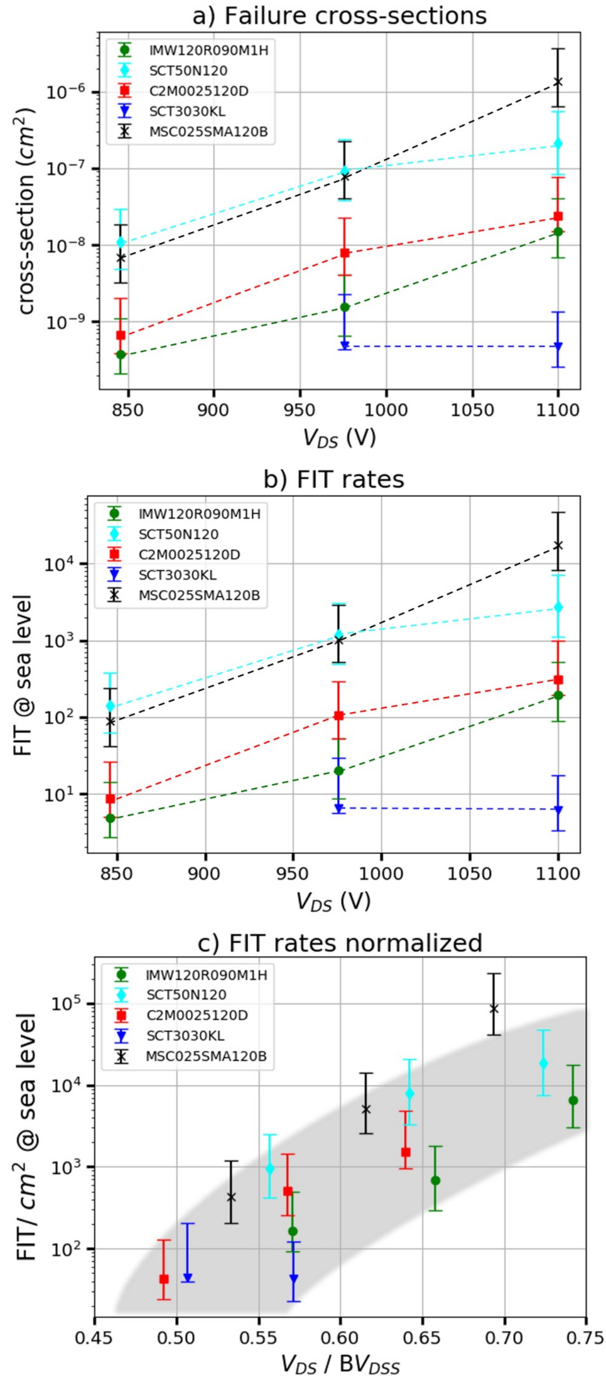


Figure 5.6: Results from the terrestrial neutron irradiations of commercial SiC MOSFETs from different suppliers. a) Failure cross-sections. b) FIT rates. c) FIT rates scaled by avalanche voltage and normalized with the active area. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

5.3.2 Post-irradiation measurement: breakdown voltage

Post-irradiation measurements were performed for some irradiated devices (fluence up to 2.8×10^{10} n/cm^2). Depending on the technology, they showed more or less severe effect. The full discussion of results is presented in Section III B of Paper III.

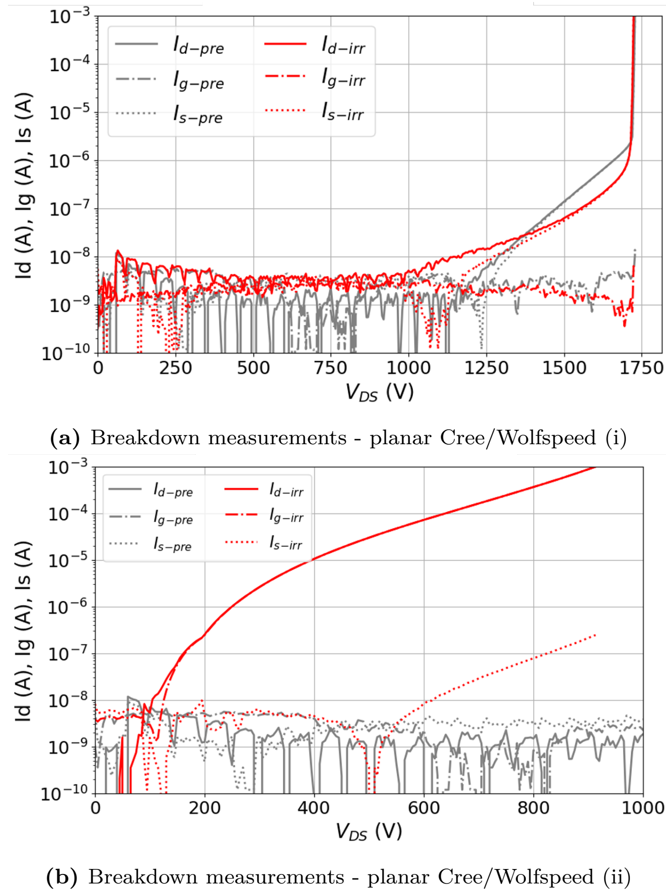
The results are compared for three references tested at 976 V: planar gate from Cree/Wolfspeed (C2M0025120D), trench gate from Infineon (IMW120R090M1H) and double trench gate from Rohm (SCT3030KL). BV_{DSS} measurements of the irradiated devices were performed at $V_{GS} = 0$ V and stopped at the V_{DS} corresponding to $I_D = 1.00$ mA. This level was defined as the point for breakdown voltage, however at this current level the device is still protected from a permanent breakdown of the body diode. The studied references showed three common scenarios:

- i) no differences observed with respect to a pristine device: no leakage current increase, neither degradation of the blocking capability of the MOSFETs.
- ii) partial degradation of the device, which exhibited I_G and I_D orders of magnitude higher with respect to the pristine level. However, the current paths (drain-to-gate vs drain-to-source contributions) differ among the three references.
- iii) ohmic trend of I_D caused by destructive SEB during the exposure.

Leakage currents measurements (i.e., I_D, I_G and I_S) are reported in the paper as a function of the V_{DS} for the three references and compared with pristine results. As an example, the results for scenarios (i) and (ii) are shown in Figure 5.7 for the planar device from Cree/Wolfspeed (C2M0025120D), as shown in the paper.

5.3.3 Post-irradiation measurement: gate rupture

The current path differs among the devices which exhibited partial degradation, with higher I_G and I_D (ii). In order to investigate this effect, I_D-V_{GS} and I_G-V_{GS} measurements were performed at ($V_{DS} = 1$ V). Figure 5.8 summarizes the results. For the planar device (C2M0025120D) although the gate leakage is higher with respect to the pristine level, the gate oxide is still operable and the channel is still controlled by the gate voltage. The planar structure exhibits a partial gate rupture with very high I_G and I_D and a gate-drain current path. This signature is the same as observed when degradation is induced by heavy-ion exposure (i.e. SELC), as discussed in Chapter 4 and reported in [130, 146]. Conversely, for the trench (IMW120R090M1H) and double-trench (SCT3030KL) devices, the gate oxide was found to be heavily damaged and not operable anymore. In fact, no positive drain current flows in these devices as the channel is in off-state, showing the signature of a complete gate rupture. However, a statistical study of this effect would be needed before generalizing these conclusions to all trench and planar devices.



(a) Breakdown measurements - planar Cree/Wolfspeed (i)

(b) Breakdown measurements - planar Cree/Wolfspeed (ii)

Figure 5.7: Post-irradiation BV_{DSS} measurements at $V_{GS} = 0$ V, with a maximum I_D current of 1 mA. Examples from two DUTs from Cree/Wolfspeed: (a) no failure observed and no damage with respect to a pristine device (i); (b) no failure observed, but partial degradation of the device (ii). Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

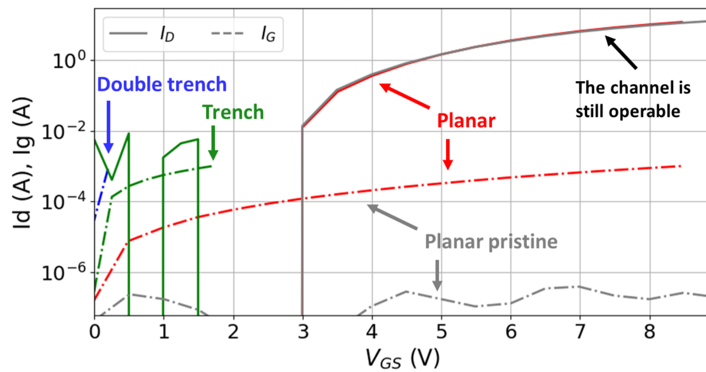


Figure 5.8: Post-irradiation $I_D V_{GS}$ and $I_G V_{GS}$ measurements performed at $V_{DS} = 1$ V. For the trench and double-trench devices, the gate oxide is heavily damaged and not operable anymore. Conversely, the gate is still operable for the planar device and the channel controllable by the gate voltage. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

5.3.4 Latent damage

The integrity of the gate oxide might be affected even though a device may not show any measurable damage during the irradiation. Breakdown voltage measurements were performed after applying positive and negative V_{GS}, for devices belonging to categories (i) and (ii). The measurement details and the results are reported in the paper and discussed for the three references mentioned before. As an example, the measurements for the two devices from Cree/Wolfspeed presented in Figure 5.7 are shown. For the device belonging to category (i), as in Figure 5.9 (a) no difference was observed in the leakage currents and in the breakdown point after these cycles. The small differences in the gate leakage current are caused by the sensitivity of the instrument. Hence, these devices are operable after the neutron irradiation, the leakage current is still within specification (i.e., $I_G < 100$ nA) and no latent damage is observed after applying the gate bias. The same was concluded for the trench and the double-trench devices.

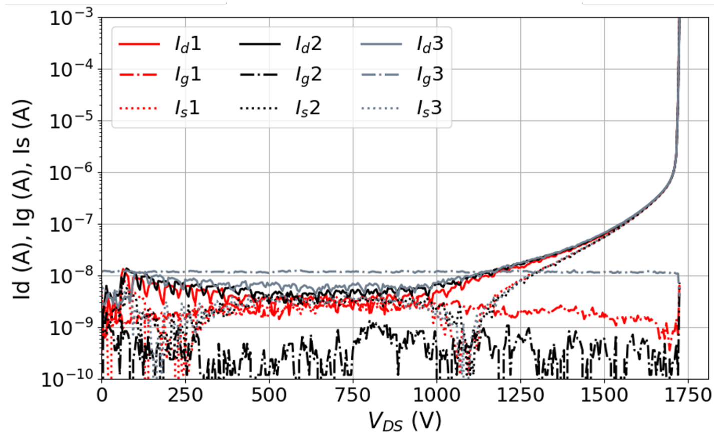
Differently, for the degraded device with partial gate rupture (ii), as in Figure 5.9 (b), after the stress at negative V_{GS}, the I_S decreased, meaning that higher current is flowing to the drain-gate path, rather than into the source pad, and therefore the gate damage increased.

5.3.5 Discussion

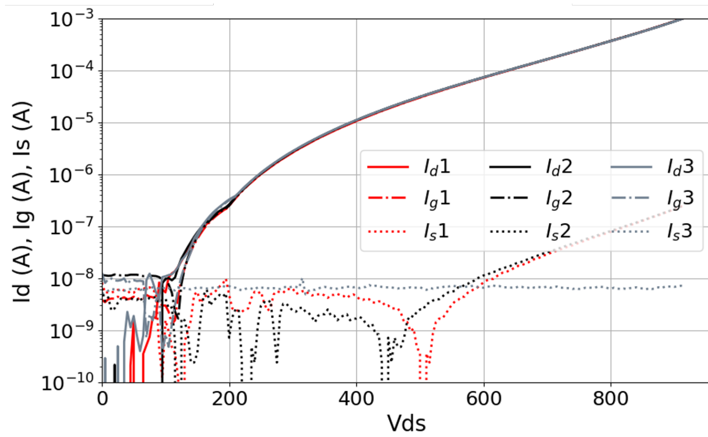
The post-irradiation analysis identified three different responses commonly observed in each of the three architectures. Considering the degraded devices (ii), the planar-gate architecture exhibited a partial gate rupture mechanism, characterized by very high I_{DG}. This effect was observed to be similar to the SELC degradation induced by heavy ions, already discussed in Chapter 4. Conversely, the trench and double-trench architectures appeared to be more sensitive to a complete gate rupture.

A model for an enhanced gate leakage current in Si devices exposed to heavy ions, was previously presented by Scheick *et al.* [112]. It states that the displacement damage caused by the ions create a significant number of damage sites in the oxide; in correspondence to these defects there is a reduced potential barrier, which allows the tunneling of electrons from the trapping sites in the oxide into the conduction band. Similarly, a model for early defects in SiO_2/SiC was discussed in [194] and attributed to the presence of defects in the oxide bulk. Considering the partial degradation observed for some devices (ii), one hypothesis explaining this effect is that neutrons are inducing defects in the gate oxide through displacement damage, and consequently these damage sites are responsible for the increased gate leakage current. The density and distribution of oxide defects in a pristine device depend on the oxide process, and can be considered as a by-product of the SiO_2 oxide growth on SiC. Therefore, the initial distribution of defects is different among devices produced by different manufacturers. However, the role of the initial defects in SEEs should be further investigated. A second hypothesis is related to the degradation effect which is observed for SiC devices exposed to heavy ions. In fact, the recoiling atoms created by neutron interactions with the SiC crystal lattice could have sufficiently high LET to induce SELC. However, dedicated experimental studies and numerical simulations are needed in order to further investigate the two hypotheses. Furthermore, the confirmation of this effect with a different setup would also be beneficial.

Finally, all the devices whose I_D in off-state exceeded 1.27 mA were counted as failed. Consequently, the FITs and the failure cross-section analysis include both the failure mechanism indicated as SEB (iii) and the degradation with partial or complete gate



(a) PIGS test - planar Cree/Wolfspeed (i)



(b) PIGS test - planar Cree/Wolfspeed (ii))

Figure 5.9: Breakdown voltage measurements after the post irradiation gate stress test. In red is the first cycle, reporting the measurement just after the irradiation. In black is the second cycle, performed after applying a positive V_{GS} up to the rated voltage (i.e. 15 V for Cree, 18 V for Infineon and 22 V for Rohm). In gray is the third cycle, measured after applying V_{GS} = -5 V. Reprinted from [32]. © 2021, Martinella *et al.*, licensed under CC BY 4.0.

rupture (ii) with the latter also considered not operable from an application point of view having the leakage current out of specifications. Comparing the normalized FIT rates for the planar device from Cree (C2M0025120D) reported in 5.6 (c) with the one discussed by Lichtenwalner *et al.* in the literature [134], our results are between a factor of 10 - 30 higher. A possible explanation for this difference might be found in the contribution of the degraded devices.

Finally, the experiments were carried out using a specific reference from each manufacturer, and further analysis is needed before extrapolating the results to other devices.

5.4 Proton experiments

Two test campaigns were performed with high-energy protons at the KVI-Center for Advanced Radiation Technology (KVI-CART) and at the Proton Irradiation Facility (PIF) at the Paul Scherrer Institute (PSI). The purpose was to identify the maximum V_{DS} at which no SEB are observed reaching a target fluence of 10^{11} protons/cm^2. During the PSI-PIF experiment, the effect of the angle between the beam incidence and the device surface was also investigated. Commercial SiC power MOSFETs with planar, trench and double-trench architecture were selected from different suppliers as DUTs.

5.4.1 Experimental facilities and setup

KVI-CART is located in Groningen, The Netherlands. The proton beam, provided by the AGOR cyclotron, was selected with an energy of 190 MeV/proton and a squared beam spot size of 2×2 cm^2. Two boards were used, each of them hosted 4 DUTs. During each irradiation, one single device was biased and exposed to the beam in a TO-247 package. The DUT was connected through BNC cables to one Keithley SMU 2410 and one Keithley SMU 2636, which were controlled via GPIB-USB and permitted to bias drain and gate respectively, and to measure the leakage current. The source was directly grounded on the board. For each run, a constant V_{DS} was applied during the exposure, whereas $V_{GS} = 0$ V, in order to keep the DUT in off-state. If a SEB was observed during the exposure, another pristine DUT was selected and the V_{DS} was lowered by 50 V for the new run. To switch between devices, an Arduino Uno multiplexer board controlled the SMUs signal to different DUTs. The equipment was placed in a shelter of the irradiation room and connected through a long USB cable to a laptop in the control room. The total length of the BNC cable was 10 m. Pictures of the setup are shown in 5.10. For each run, the irradiation was performed until a maximum fluence of 10^{11} protons/cm^2, with an uncertainty of 10%. The fluence was recorded during the irradiation using a simple digital counter based on an Arduino Leonardo microcontroller board, having the flux information provided as +5 V TTL pulses. The same setup was used to perform the characterisation before and after the run. If the DUT survived, no differences were observed with the pristine values for the following measurements:

- $I_D V_{DS}$ and $I_G V_{DS}$ with V_{DS} = [0 V - 1000 V] and V_{GS}= 0 V;
- $I_D V_{GS}$ and $I_G V_{GS}$ with V_{GS} = [0 V - 5 V] and V_{DS}= 1 V;

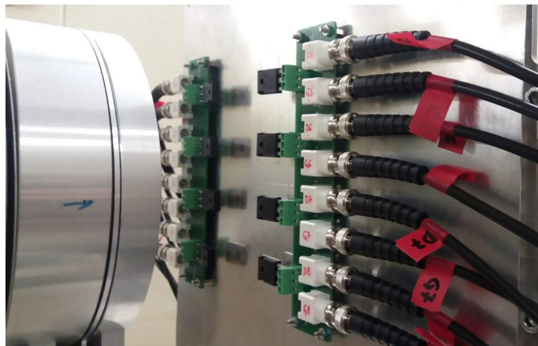


Figure 5.10: Each board used at KVI hosted 4 DUTs singularly biased for gate and drain.

The PSI-PIF facility is located in Villigen, Switzerland. The proton beam is provided by the PROSCAN accelerator and, by the primary energy degrader, the beam energy can be set between 230 MeV and 74 MeV. For the purpose of this experiment, the beam was selected with an energy of 200 MeV and a flatness area of 5 cm diameter (ϕ), with uncertainty of 10 %. The experiment was performed using the same setup as described for the neutron test in 5.2. In this case, the board was redesigned to host a maximum of 4 DUTs in a circular area of 4.5 cm diameter. The devices were biased in parallel at a constant V_{DS}, while monitoring the sum of all the I_{DS}, whereas the gate was directly grounded on the board. A step of a fixed size in the drain current (i.e., $I_{DS} = 1.27$ A), was counted as a SEB failure.

Initially, the beam was used with a normal incidence with respect to the DUT surface (i.e., $\Theta = 0°$) and the irradiations were performed up to a fluence of 10^{11} protons/cm^2. If a failure occurred, the run was repeated substituting the DUTs and lowering the V_{DS} of 50 V. Once the safe operative V_{DS} was identified, the procedure was repeated with the device tilted of 90 degrees, in order to have a parallel incidence of the beam with respect to the DUT surface (i.e. $\Theta = 90°$). The purpose was to investigate the effect of different angles of incidence of the proton beam on trench and planar devices.

The characteristics of the two experiments are reported in Table 5.2.

Table 5.2: Characteristics of the KVI-CART and PSI-PIF experiments.

		Beam			
Facility	Energy	Dimension	Shape	Setup	Incidence
KVI-CART	190 MeV	2x2 cm^2	square	single DUT	0°
PSI-PIF	200 MeV	Φ=5 cm	circular	multiple DUTs	0°, 90°

5.4.2 Proton results

The V_{DS} at which no failure was identified for the different conditions, are listed in Table 5.3. In some cases, only a range is indicated, as it was not possible to identify an accurate value due to the limited number of devices or beam time. The column labelled "DUTs" indicates the number of devices which survived at that specific voltage.

Similarly as for the neutrons, the trench devices appear to be more robust with respect to the planar ones, having the best performance with the double trench MOSFET from Rohm (no failure at $V_{DS} = 900$ V for $\Theta = 0°$). However, as showed in Table 5.1, even though the DUTs are all rated for 1.2 kV, the Rohm device has a much higher breakdown point ($\sim$ 1.9 kV), which could have an influence on the SEB tolerance. Furthermore, from the first results obtained from the PSI experiment, a beam with a normal incidence appears to be the worse-case scenario both for planar and trench devices. However, these experiments have been carried out with a limited number of devices and additional data would be needed in order to increase the statistics and confirm the observed results.

Table 5.3: Summary of the proton irradiations performed at KVI and PSI. In all the cases the accumulated total fluence was 10^{11} protons/cm^2.

Reference	Manufacturer	Gen.	$R_{DS(on)}$ [mΩ]	V_{DS} [kV]	$I_{D@25}$ [A]	Gate	KVI-CART DUTs	KVI-CART V_{DS} [V]	PSI-PIF DUTs	PSI-PIF $V_{DS-\Theta}$=0° [V]	PSI-PIF $V_{DS-\Theta}$=90° [V]
C2M0080120D	Cree/Wolf.	II	80	1.2	36	planar	3	600	-	-	-
C2M0025120D*	Cree/Wolf.	II	25	1.2	63	planar	4	650	4	600	800
C3M0065090D	Cree/Wolf.	III	65	0.9	36	planar	3	500	-	-	-
SCT3030KL*	Rohm	III	30	1.2	180	double tr.	3	900-1000	4	900	1100
IMW120R090M1H*	Infineon	V	90	1.2	50	trench	-	-	3	650-750	800-1000

*Also tested with atmospheric neutrons.

5.5 Summary of proton and neutron effects

Commercial devices with planar-gate, trench-gate and double-trench architectures were tested with atmospheric-neutrons and high-energy protons. The results lead to the following conclusions:

- With both atmospheric-neutrons and high-energy protons, the trench MOSFETs were observed to be less sensitive to SEB failure with respect to the planar ones. The double-trench architecture, which has also the highest breakdown voltage, was the most robust in both cases.
- Considering the terrestrial-neutron experiment, five different commercial devices were irradiated. Cross-section and FIT rates were calculated for DUTs which resulted out of specifications after the test ($I_G > 10^{-9}$ A). The post-irradiation analyses were performed on three tested references over five: planar DUTs from Cree (C2M0025120D), trench DUTs from Infineon (IMW120R090M1H) and a double-trench DUTs from Rohm (SCT3030KL). Three different scenarios where commonly observed for the different architectures analysed: (i) no damage with respect to a pristine device, (ii) partial degradation with higher gate and drain leakage current, (iii) ohmic trend of the leakage current caused by a SEB. Among the degraded devices (ii), the trench and double-trench DUTs exhibited a complete gate rupture. Conversely, a partial gate rupture was observed for the planar reference, which exhibited a gate-drain leakage path as previously observed for the same devices showing SELC after heavy-ion irradiation. The gate damage in these devices was observed to increase after PIGS tests. Overall, the degradation effect observed in devices from category (ii) requires further investigation; the confirmation of this effect with a different setup would also be beneficial. Based on the available data, two hypotheses were proposed for the enhanced gate current: the first is based on displacement damage caused by the neutrons in the gate oxide, whereas the second involves SELC caused by the recoiling atoms generated by the neutron interactions.
- In the case of proton irradiation, the post-irradiation analysis was performed only for devices which survived the test at KVI-CART (i.e. irradiated one at the time). In this case, no differences were observed in the I-V characteristics with respect to a pristine part. However, the devices which failed during the exposure and the devices tested at PSI-PIF with the same setup as the neutron test were not analysed, therefore it cannot be excluded that partial degradation was induced also by proton irradiation.
- From the proton experiment at PSI-PIF, it was observed that for all three architectures, the normal incidence of the beam represents the worse-case scenario with respect to a parallel incidence. However, higher statistics are needed to confirm the results.
- The tested devices were selected following the requirements for the inductive adder application at CERN described in Section 2.3.4. Among the selected references, the double-trench device from Rohm (SCT3030KL) was identified as the most interesting solution, being the most robust to SEB for the tested conditions. A safe operative voltage was identified with protons at V_{DS} = 900 V (V_{GS} = 0 V, $\Theta = 0°$, fluence = 10^{11} protons/cm^2). However, the gate rupture observed with atmospheric-neutrons requires further investigation before considering this device for applications in the high-energy accelerators at CERN.

6 Summary

6.1 Lessons learned from the experimental campaigns

This first section provides the reader with a list of suggestions/observations collected during the preparation and the completion of different test campaigns. The idea is to highlight a few aspects which should be treated with particular attention when testing SiC power MOSFETs for SEEs.

- When testing with heavy-ions, as soon as the SiC device starts to exhibit degradation, when the V_{DS} is applied at the beginning of the run, the current is observed to reach a certain level and then decrease with time. A possible cause of this effect might be a coupling of the DUT impedance in series with the feedback resistor of the SMU ammeter. This creates a RC-circuit that requires a finite time to charge the capacitance of the DUT. When testing with heavy ions, enough time has to pass between the start of the bias and the start of the irradiation, in order to charge the capacitor of the DUT and reach the steady-state condition. Depending on the magnitude of degradation, it might take from a few seconds to a few minutes. If the irradiation is started prematurely, the heavy-ion induced degradation is partially masked by the charging effect, resulting in an apparently lower degradation rate.
- When testing a MOSFET, it is important to monitor at least two of the three terminals in order to figure out the current path. In the standards this is not specified, and in the past very often radiation tests were performed grounding the gate terminal directly on the board. When testing Si MOSFETs with heavy ions, this might not make a difference, whereas with SiC devices monitoring only one terminal hides information about the underlying degradation mechanism.
- The protection circuit typically used for non-destructive multiple SEB testing with Si MOSFETs, as reported in the MIL-STD-750E M1080.1 [83], cannot be used for SiC testing. In fact, the energy stored in the device is sufficient to cause the SEB even though a limiting resistor is used, inducing the destructive failure of the part. Hence, the SEB test has to be considered a destructive test and a large number of devices is required in order to acquire sufficient statistics.
- During some experiments with heavy ions, not reported in this work, limiting resistors were used at the gate and drain terminal. In particular, the gate resistor which was installed between the gate terminal and the ground, caused a problematic effect as soon as the DUT started to be degraded. Over a certain level, the increasing gate current induced by degradation caused a voltage drop over the resistor which set the device in an on-state condition during the irradiation. Hence, in general, attention should be paid on the resistance between the gate terminal and the ground.

6.2 Conclusions and outlook

This work presented an overview of the results obtained along a four-year research on the SEE mechanisms in SiC power MOSFETs. The effects of heavy-ion, high-energy proton and terrestrial-neutron irradiations were studied on different commercial technologies, providing information to assess the reliability of SiC MOSFETs for space, avionic and high-energy accelerator applications.

The research initially focused on the non-catastrophic effects induced by heavy-ion irradiation. In fact, even though the devices can be de-rated at sufficiently low voltage to protect from the destructive SEB failure, permanent leakage current degradation (named SELC) and latent damage can still hamper the device operation, representing a significant risk to the part reliability. A minimum LET is required to observe these effects, and ions with LET > 7.7 MeVcm^2/mg were used in this work. The experiments were performed with planar devices from the 2nd and 3rd generation from Cree/Wolfspeed, and the 80 mΩ from the 2nd generation was considered as the reference device. The heavy-ion-induced SEEs observed during this research were graphically summarized as function of the ion LET and the drain-source bias during the exposure; five different regions of damage with respective thresholds can be identified.

Papers I and II focused on the leakage current degradation, whose mechanism was not fully explained yet [130, 146]. The effect of heavy ions was investigated through broad-beam and microbeam experiments; the latter was performed with a focal spot of 500 nm and a step size of ~ 1 μm, allowing the precise identification of the ion-strike location. Two mechanisms of degradation were identified in SiC MOSFETs. Initially, at a sufficiently high drain-source bias, a permanent increase in drain-gate leakage current (I_{DG}) is observed during the exposure, with a current path between gate-drain terminals and a linear proportionality to the fluence. The microbeam studies indicated the JFET and the adjacent channels as the sensitive regions involved in this damage. The Quantum Point Contact (QPC) model was proposed to explain the enhanced leakage currents, involving the generation of conductive paths in the gate oxide which behave as point contacts between the gate and the substrate [175]. The threshold for this effect varies with the ion LET and the device generation.

The second mechanism of degradation is observed for drain-source voltages higher than a certain threshold (i.e., $V_{DS} \geq 350$ V for the studied devices). The I_{DG} keeps increasing linearly with the fluence, whereas the drain-source current (I_{DS}) increases with larger magnitude. From the microbeam study, the p-n junction was identified as the sensitive region for this type of degradation, and it was suggested to be the same as the one observed in SiC diodes. The threshold for this effect is least influenced by ion LET and device breakdown voltage with respect to the threshold for the first type of degradation, leading to the conclusion that this mechanism may involve properties of the SiC material. The recent results from numerical simulations [151], suggested that Joule heating is responsible for the damage. The molecular dynamics simulations [140] of SiC diodes showed that the thermal transient results in a phase change in the SiC lattice at voltages lower than the ones required for a destructive failure. Based on these findings, in this work we proposed that the leakage current through the p-n junction is the result of permanent extended defects (ED) caused by the excessive lattice temperature. These EDs could be amorphous pockets, clusters, stacking faults, dislocations, different SiC solid-phase (polytype) inclusions, etc., whose nature could be further investigated by optical methods.

Two mechanisms of latent damage were observed, involving the gate-oxide and the SiC

crystal lattice, as discussed in Paper IV. The first is observed in the sub-degradation region at different drain-source bias depending on the ion LET. Even though no clear signature is observed during the exposure, it always leads to oxide breakdown during the post-irradiation-gate stress (PIGS). A target fluence of 10^6 ions/cm^2 was used to identify the V_{DS} threshold voltages for gate latent damage and to assess the oxide reliability for different ion species and LETs. The second latent damage was observed in the pre-SEB region, where the second mechanism of degradation is dominant, and the very high I_{DS} leakage current leads to device failure in the post-irradiation V_{DS} sweep. After the irradiation, when drain-source bias is applied, the localized power density induces an increase of temperature, which ultimately causes the sublimation of the SiC crystal as shown from the SEM-FIB analysis. This effect confirms that devices with increased leakage experience accelerated damage, resulting in a much earlier device failure.

SEB studies were performed with lighter particles, such as atmospheric-like neutrons and high-energy protons. Commercial technologies with planar-gate, trench-gate and double-trench (trench source and gate) architectures were used for these experiments. The double-trench devices from Rohm showed the highest tolerance to SEB failure with both terrestrial neutrons and protons. However, even though all the devices were rated for the same voltage, the Rohm ones have a much higher breakdown point, which could also play a role in the SEB tolerance.

The results from the neutron study are discussed in Paper III, where failure cross-sections and FIT rates were calculated for the tested references [32]. The post-irradiation analysis of the failure mode highlighted different magnitudes of damage in the tested devices. In particular, some devices did not exhibit an ohmic trend (as in the case of SEB failure), but enhanced gate and drain leakage currents which went out of specification. Among these devices, a partial gate rupture signature was observed in the planar devices similar to the partial degradation induced by heavy ions. Differently, the trench architectures showed a complete gate rupture.

This study underlined the physical mechanisms of SEEs experienced by the current commercial SiC MOSFET technologies in different radiation environments. The results pave the way for the explanation of the degradation mechanisms induced by heavy ions, providing some information for the mitigation by design of the described effects. However, the data were obtained from specific commercial SiC MOSFETs and, even though they could qualitatively be extended to other references, further analysis is needed before extrapolating the threshold voltages and failure cross-sections to devices with different architectures or those produced by other manufacturers.

As much as the research reported in this doctoral thesis contributed in understanding the SEE mechanisms in SiC MOSFETs, multiple open questions still remain around the degradation mechanism and the nature of the defects created by radiation in the SiC crystal structure. Possible further studies aimed at shedding light on these open queries include optical investigation of the irradiated samples and numerical simulations of the radiation interaction in the SiC crystal, to identify the LET and angular distribution of the reaction products. Finally, as there is not as much knowledge available for SEEs in SiC trench and double-trench MOSFETs as for the planar ones, dedicated radiation tests and numerical simulations are necessary to clarify the SEE mechanisms in these architectures.

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Included articles

Publication I

C. Martinella, R. Stark, T. Ziemann, R. G. Alia, Y. Kadi, U. Grossner, A. Javanainen, "Current Transport Mechanism for Heavy-Ion Degraded SiC MOSFETs", *IEEE Trans Nucl. Sci.*, vol 66, no. 7, pp. 1702-1709, Mar. 2019.

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Current Transport Mechanism for Heavy-Ion Degraded SiC MOSFETs

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***Abstract*— High sensitivity of SiC power MOSFETs has been observed under heavy ion irradiation, leading to permanent increase of drain and gate leakage currents. Electrical post-irradiation analysis confirmed the degradation of the gate oxide and the blocking capability of the devices. At low drain bias, the leakage path forms between drain and gate, while at higher bias the heavy ion induced leakage path is mostly from drain to source. An electrical model is proposed to explain the current transport mechanism for heavy-ion degraded SiC power MOSFETs.**

***Index Terms*— SiC power MOSFETs, heavy ion irradiation, gate leakage, single event effects.**

I. Introduction

Wide band-gap semiconductor, such as silicon-carbide (SiC) are very attractive for power devices due to their physical properties. The wide energy bandgap of 3.23 eV (4H SiC at room temperature) allows SiC devices to operate at high voltage, high temperatures and switching frequencies while achieving lower conduction losses in comparison to silicon [1], [2]. SiC devices are expected to be used in harsh environments, indeed it is considered as promising technology for space and accelerator applications, such as the injection kicker pulse generator for the Future Circular Collider [3].

Recently, various studies were performed to investigate the radiation tolerance of SiC devices. High sensitivity has been noticed under heavy ion irradiation and a unique Single Event Effect (SEE) phenomenon has been observed in plain Schottky diodes, junction barrier Schottky diodes [4], [5] and SiC power MOSFETs [6], [7]. While silicon-based power MOSFETs typically directly experience catastrophic failure such as Single Event Gate Rupture (SEGR) or Single Event Burnout (SEB). SiC power MOSFETs, instead, are shown to exhibit three characteristic regions as a function of the drain-source bias conditions during the exposure, as visible in Fig. 1 [6].

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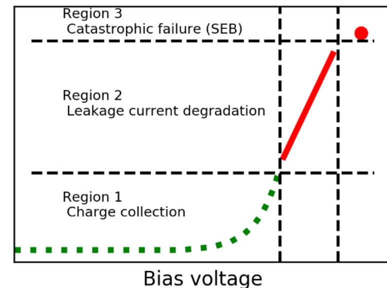

Fig. 1. Three characteristic regions of damage for SiC power devices as a function of the drain-source bias during the heavy ion irradiation.

The first non-destructive region occurs at low bias voltages. In this region, the ion-induced charge is collected with a similar multiplication mechanism as in Si MOSFETs and no permanent damage is observed in the device. The second region occurs at higher bias, where a unique phenomenon is observed for SiC devices, causing permanent degradation resulting in increased leakage currents with increasing heavy ion fluence. The damage is not catastrophic, but the device operation may become limited. In the third region, at sufficiently high bias, a SEB occurs leading to a catastrophic failure of the device. The mechanism triggering the SEB in SiC MOSFETs is still under study. Different hypotheses have been formulated.

Witulski et al. [7] investigated the SEB through experimental measurements and TCAD simulations. Their work concludes that at sufficiently high current generated by the ion strike and applied bias, the parasitic bipolar junction transistor (BJT) which is an intrinsic part of the device structure, turns on, resulting in the catastrophic SEB. This mechanism is very similar to the SEB in silicon-based power MOSFETs.

In the same work, experimental measurements of SEB threshold voltages versus heavy-ions LET for 1200 V SiC MOSFETs are reported and compared with previous results based on the works of *Mizuta et al.* [6] and *Lauenstein et al.* [8]. In their work, all the MOSFETs exhibit catastrophic failure at bias voltage significantly lower than the rated 1200 V when exposed to heavy ions with LET values above 10 $MeV/(mg/cm^2)$. Conversely, at LET values below 10 $MeV/(mg/cm^2)$, SEB occurs at higher voltages and the region for ion-induced degradation (region 2 above) becomes narrower. Finally, at very low LET values, there is a direct transition from region 1 to region 3 as drain bias is increased, hence no permanent non-destructive leakage current increase is observed for light ions, including protons.

Shoji et al. studied the neutron-induced SEB in SiC power diodes [9] and SiC power MOSFETs [10] through experiments and TCAD simulations, concluding, differently, that an SEB can occur in a diode structure without activating the parasitic npn transitor. They claim that the catastrophic failure occurs due to a shift in the peak electric field in the n^-drift/n^+ interface and punch-through of the electric field to the cathode at the device surface. Through TCAD simulations, *Shoji et al.* demonstrated similar mechanism in SiC power MOSFETs as a shift in the peak electric field and a punch-through at the n^+ source diffusion region.

Additionally, *Asai et al.* [11] performed studies with neutrons, concluding that there exists no consistent difference in SEB tolerance between SiC diodes and SiC MOSFETs and that the conventional SEB mechanisms developed in Si MOSFETs, such as parasitic bipolar transistor and tunneling assisted avalanche multiplication mechanism, may be suppressed in SiC devices [12].

For SiC MOSFETs the previous studies have mostly concentrated on the SEB and the permanent increase in the drain leakage. The ion-induced gate damage (such as SEGR) in these devices has not been previously discussed in that detail. For silicon power MOSFETs instead, the ion-induced effect in the gate oxide has been studied quite widely previously [13]. For SEGR the mechanism has been concluded as following. The primary ionizing ion generates electron-hole-pairs along the path through the oxide and the semiconductor, creating a track of ionized plasma in the active layer of the device. For an n-type device in off-state with a positive V_{DS}, electrons move towards the drain (in VD-MOSFETs represented by the backside substrate and contact), while a high concentration of holes is created at the Si/SiO_2 interface. Mirror charges are then induced at the gate and this creates a transient field across the oxide in addition to the applied field [14] [15]. Furthermore, the critical field required for the oxide breakdown is thought to be decreased by the ionization within the oxide induced by the impinging particle. The oxide response in Si power MOSFETs was described for the first time in [16].

A detailed description of SEGR mechanisms caused by heavy ions in Si Power MOSFETs is given in [17]. The important ion beam characteristics for inducing SEGR are the Linear Energy Transfer (LET) and the total energy deposited in the epitaxial layer (including the epi/substrate interface region).

Finally, three different types of SEGR modes have been proposed for Si power MOSFETs [18]; the micro-break, the thermal runaway and the avalanche breakdown. The proposed model for an enhanced gate current associated with a micro-break is that oxide defects from displacement damage caused by the ion hit create a significant number of damage sites at which there is a reduced potential barrier, permitting the tunneling of electrons from trapping sites in the oxide into the conduction band.

In this paper, we focus on the second region of degradation as shown in Fig.1, investigating the permanent non-catastrophic damage observed in SiC power MOSFETs during heavy ion irradiations. The results from the irradiation experiment and the electrical analysis are reported and discussed. The degradation rates were also calculated for all the tested devices and observed to be independent on the prior degradation. Finally, a mechanism describing the radiation induced leakage paths within the device structure is proposed and combined with simulations using an equivalent circuit to model this leakage.

II. Experimental Methods

A. Experimental Setup

The heavy ion experiments were performed at the RADiation Effects Facility (RADEF) in the Accelerator Laboratory of the University of Jyväskylä, Finland. Three types of 4H-SiC MOSFETs from the manufacturer Cree/Wolfspeed, available as bare die (CPM2-1200-0025B, CPM2-1200-0080B, and CPM2-1200-0160B), were selected as devices under test (DUTs). All three DUTs are rated for $V_{DS} = 1200\,V$, but differ in $R_{DS(on)}$ (25 mΩ, 80 mΩ, and 160 mΩ, respectively). All three types of devices are of the 2nd generation, and the different $R_{DS(on)}$ have been achieved by adjusting the active area in the die. This work discusses mostly the results for the 80 mΩ irradiations.

Bare die were used in order to directly expose the chip surface to the beam to allow sufficient penetration of the heavy ions through the sensitive layers of the device, without being stopped in the package materials.

The die were mounted on custom FR-4 carrier boards with gold (ENIG) surface using standard SAC 305 solder paste. While the drain connection was made by the large soldered bottom pad, the gate and source were connected by aluminum wire bonds with 300 µm diameter. To minimize shadowing by the wires, only a single source wire was used. Each board housed 5 die individually biased with BNC connectors for gate and drain. Keithley Source Measure Unit models 2636 (two channels, up to 200V) and 2410 (one channel, up to 1100V) were used for biasing gate and drain respectively.

TABLE I
CHARACTERISTICS OF THE ION SPECIES USED IN THIS STUDY

Ion	Energy [MeV]	Energy/ nucleon [MeV/amu]	LET^{SRIM} @surface [MeV/mg/cm^2]	Range SiC^{SRIM} [µm]
$^{56}Fe^{+15}$	523	9.33	20.05	65.63
$^{82}Kr^{+22}$	768	9.36	33.75	63.89
$^{131}Xe^{+35}$	1217	9.29	62.39	61.43

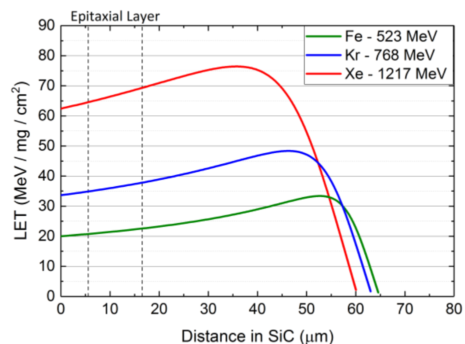

Fig. 2. Bragg curves as function of the penetration depth with SiC.

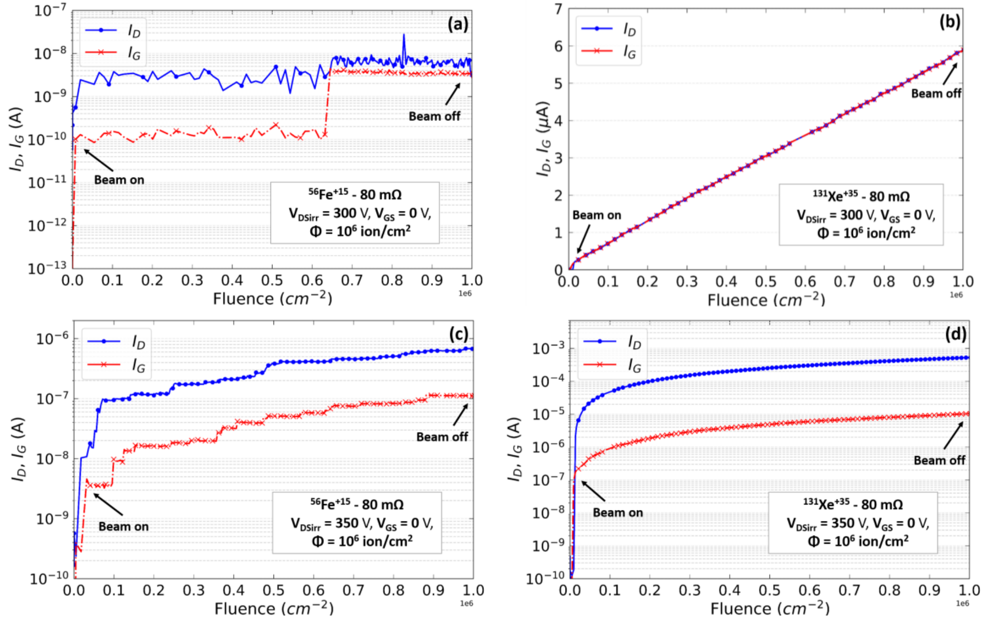

Fig. 3. Equal rate of increase in the gate and drain leakage currents during the irradiation at V_{DSirr} = 300 V with $^{56}Fe^{+15}$ (a) and $^{131}Xe^{+35}$ (b). Each step in the leakage currents is caused by a single incident heavy ion. The y-axis in figure (b) is in linear scale and μA unit. At 350 V and above, the drain leakage increases with higher rate than the gate leakage, as visible during $^{56}Fe^{+15}$ (c) and $^{131}Xe^{+35}$ (d) irradiation. The fluence in each case was 10^6 ions/cm^2 with an uncertainty of +10%.

B. Heavy Ion Irradiation Tests

The boards were mounted in a vacuum chamber and the die exposed to a fluence of 1x10^6 ions/cm^2 during the test runs, while bias voltages were kept constant. The heavy ion species used during the test were $^{131}Xe^{+35}$, $^{82}Kr^{+22}$ and $^{56}Fe^{+15}$, with an energy per nucleon of ~ 9.3 MeV/amu. The ion characteristics are listed in Table 1. While the gate voltage V_{GS} was set to 0 V to hold the device in off state, the drain voltage V_{DS} was set to constant positive value during the irradiation and increased after each run until the device was considered broken due to the degradation. The I_D-V_{DS} and I_G-V_{GS} curves were measured after each run. The beams were at normal incidence to the DUT surface. All the irradiations and the I-V characterizations were performed at room temperature.

The ion LET versus the penetration depth in SiC was estimated with ECIF (European Component Irradiation Facility) Cocktail Calculator [19]. The Bragg curves for each ion species used in the tests are reported in Fig. 2. The epitaxial layer is highlighted in the figure by vertical dashed lines and it extends from 5 µm until 18 µm from the die surface. This confirms that the energy deposition is well defined within the active layer and the ions penetrate deep enough in the device structure to meet the worst-case energy deposition criterion as discussed in [20]. The main source of uncertainty is due to the fluence measurement and, in general, for the RADEF facility an error of +10% is considered.

C. Degradation Rate and Post Irradiation Analysis

The die were irradiated at different V_{DS} bias conditions and the drain and gate leakage currents were measured during the exposure. The degradation rate is defined as the difference between the leakage current measured at the end of the run (after exposure to the beam) and at the beginning of it (before exposure) normalized by the fluence and the active area of the die. The active area was calculated from the microscope images as the metallized area subtracted with the gate pad and the gate conductors. The shadowing effect due to the bond wires was estimated, obtaining an active area of 19.92 mm^2 for the 25 mΩ, 5.74 mm^2 for the 80 mΩ and 2.75 mm^2 for the 160 mΩ die.

Moreover, electrical analysis of the die was performed before and after the irradiation at the Advanced Power Semiconductor Laboratory (APS) at ETH Zurich, using a wafer probe station MPI TS200-HP connected with a measurement equipment Keithley PCT-4B.

III. RESULTS

A. Current Measurements During Irradiation

Drain and gate leakage currents were monitored during the exposure of the DUTs. If the device degradation was not severe at the end of the run, the V_{DS} was increased, while V_{GS} was kept constant at 0 V. At sufficiently high V_{DS} bias, the same increase in absolute value of the drain and the gate leakage currents were observed during the exposure. The threshold drain-source voltage to observe degradation was determined at $V_{DS\,irr}$ = 300 V, 200 V and 120 V during the irradiation with $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ respectively. Fig. 3 presents the absolute values of I_D and I_G as a function of exposure time for two pristine 80 mΩ DUTs irradiated at V_{DS} = 300 V with $^{56}Fe^{+15}$ (a) and $^{131}Xe^{+35}$ (b). Each step in the current is caused by a single

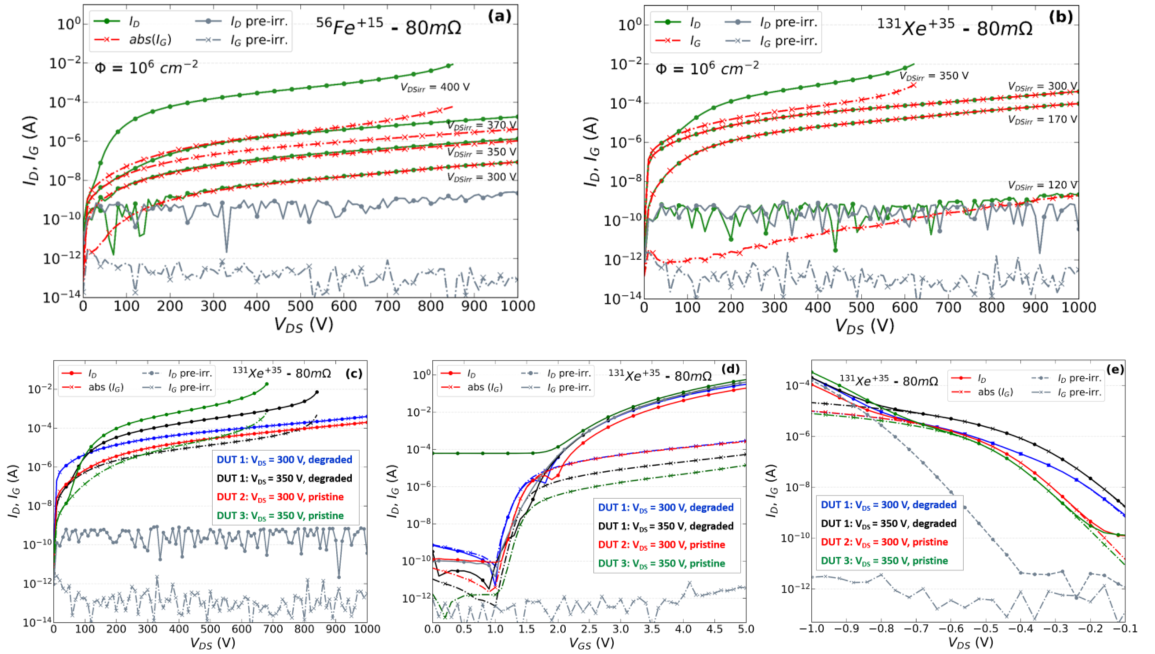

Fig 4. Post-irradiation I_DV_{DS} and I_GV_{DS} curves for 80 mΩ DUTs irradiated with $^{56}Fe^{+15}$ (a) and $^{131}Xe^{+35}$ (b). The drain-source bias during the irradiation are reported in the I_DV_{DS} graph as V_{DSirr}. Comparison of I_DV_{DS} and I_GV_{DS} (c), transfer characteristic (d) and body diode (e) for three DUTs exposed to $^{131}Xe^{+35}$ at $V_{DSirr} = 300\,V$ and $V_{DSirr} = 350\,V$ as pristine die or after prior degradation from previous irradiation at lower V_{DSirr}.

incident ion. For $^{131}Xe^{+35}$ the individual steps are less distinguishable due to high ion flux with respect to the speed of the current monitoring, hence only linear increase in leakage with increasing ion fluence is observed.

Conversely, during the runs at $V_{DSirr} \geq 350\,V$, with all the devices and all the ions, the drain leakage was observed to increase at higher rate than the gate leakage. This behavior is illustrated in Fig. 3 (c, d) by showing the $^{56}Fe^{+15}$ and $^{131}Xe^{+35}$ results respectively, but the same trend was measured also with $^{82}Kr^{+22}$ which has an intermediate LET. From the tests it is observed that the ion-induced leakage path is from drain to gate for $V_{DSirr} \leq 350\,V$, while at higher irradiation bias the leakage current is divided between drain-gate and drain-source paths, as discussed in more details below.

B. Post-Irradiation measurements at RADEF and prior degradation effect

The drain and gate leakage were measured promptly after each run in absence of the beam, sweeping V_{DS} from 0 V to 1000 V with $V_{GS} = 0\,V$ and V_{GS} from 0 V to 5 V with $V_{DS} = 1\,V$ respectively. Permanent damage was observed in the post characteristics for devices tested with bias voltages above the degradation threshold. For all the DUTs the gate was permanently damaged and the blocking capability of the device degraded with increased V_{DSirr} during the test. In general, no latent defect damage was observed. If there was no damage during the exposure, it was not measured as well during the post-irradiation stressing the DUTs up to $V_{GS} = 5\,V$.

In Fig. 4 the I_D and I_G as a function of V_{DS}, measured after each run, are shown for two 80 mΩ DUTs exposed to multiple irradiations with $^{56}Fe^{+15}$ (a) and $^{131}Xe^{+35}$ (b) beams. The history of the consecutive exposures is shown on the graph as V_{DSirr}. In the case of $^{56}Fe^{+15}$ the die was exposed also at $V_{DSirr} = 340\,V, 360\,V$, but the results are not shown here in order to have a more readable graph. The data for $^{82}Kr^{+22}$ are also not presented here, but they are consistent with the results reported for $^{56}Fe^{+15}$ and $^{131}Xe^{+}$.

These measurements confirm the trend that was already observed during the irradiation. Indeed, it is clearly visible that for the DUTs exposed to the beams at $V_{DSirr} < 350\,V$, the observed drain and gate leakages are due to a direct path between drain and gate, as confirmed by the equal leakage currents values ($|I_D| = |I_G|$). Conversely, for the DUTs irradiated at $V_{DSirr} \geq 350$ V, the drain and gate currents are equal at low V_{DS} values, but at higher V_{DS} the current starts to flow from drain to source through the channel ($|I_D| > |I_G|$). The effect depends on the applied drain-source bias during the irradiation and on the ion LET values. Although the results are not discussed in this work, the same mechanism was observed also during the irradiation of the 25 mΩ and 160 mΩ die of the 2nd Generation Cree/Wolfspeed, which have different active area, but the same vertical cell structure.

Most of the tests were performed exposing the same DUT to consecutive irradiation runs. In order to analyse the effect of the degradation induced by the previous irradiations at lower voltage, the test was repeated with $^{56}Fe^{+15}$ and $^{131}Xe^{+35}$ beams using pristine die and exposing them for a single run at $V_{DSirr} = 300\,V$ and $V_{DSirr} \geq 350\,V$. Three DUTs were selected for the analysis with $^{131}Xe^{+35}$: DUT 1 was exposed to $^{131}Xe^{+35}$ at $V_{DSirr} = 120$ V, 170 V, 300 V, 350 V (same die as in Fig. 4 (b)),

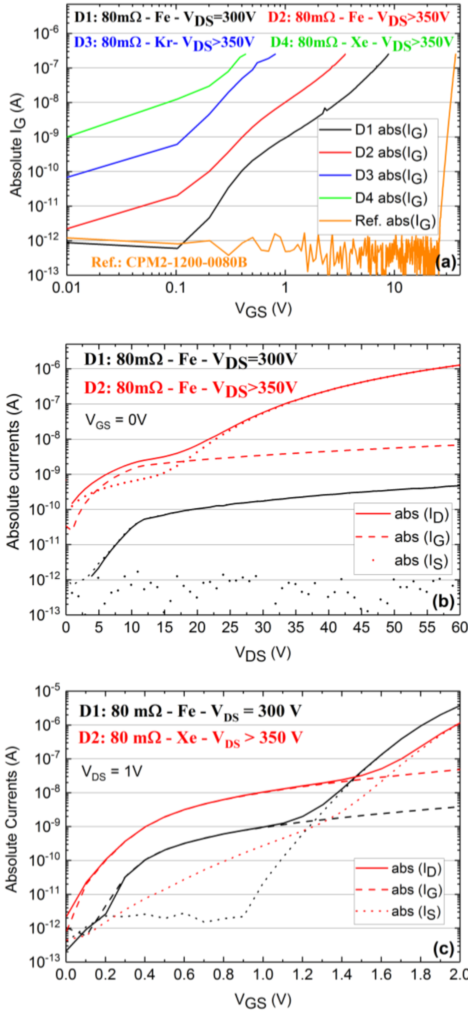

Fig. 5. (a) $I_G V_{GS}$ measurements for irradiated devices in comparison with a reference measurements of a CPM2-1200-0080B die. (b) $I_D V_{DS}$, $I_G V_{DS}$, $I_S V_{DS}$ current measurements ($V_{GS} = 0\,V$) (c) $I_D V_{GS}$, $I_G V_{GS}$, $I_S V_{GS}$ current measurements ($V_{DS} = 1\,V$).

while DUT 2 and DUT 3 were exposed only for a single run at $V_{DSirr} = 300$ V and $V_{DSirr} \geq 350$ V respectively. Similarly it was done for $^{56}Fe^{+15}$, but the second pristine die was exposed to $V_{DSirr} = 370\,V$. All the irradiations were done with a fluence of 10^6 ion/cm^2.

In Fig. 4 (c, d, e) the measurements are shown for the DUTs irradiated with $^{131}Xe^{+35}$. It is clearly visible in Fig. 4 (c) that the same characteristics are observed for the device already degraded as for the pristine die exposed to a single run. This result confirms that the current path within a degraded device is not affected by the prior damage history of the device, but it depends only on the drain-source bias during the irradiation (V_{DSirr}). Moreover, in Fig. 4 (d) it can be seen that the transfer characteristics for the irradiated die are still comparable with the reference values (i.e. DUT 1 is used as reference example and the difference is mostly caused by part-to-part variation). For DUT3 the transfer characteristics differs from that of the other devices probably because of some electrical stress induced effects during the post characterization. Finally, the body diode characteristic are presented in Fig. 4 (e). Here again the leakage path through the gate is evident at the lower V_{DS} values where $|I_D| = |I_G|$, while at sufficiently high reverse voltage, the diode characteristics become dominant and the path is then through the body and it is comparable with the reference measurements for the pristine device (the differences again are caused by part-to-part variation). The measurements for $^{56}Fe^{+15}$ confirm the same trend, concluding that no induced effect on the current path within a heavy ion degraded die was observed due to the prior irradiation history.

C. *Post-Irradiation analysis.*

After the irradiation tests, some of the die were electrically characterized at the APS Laboratory at ETH Zurich using a wafer probe station and measuring simultaneously the I_G, I_D and I_S. The results in this section compare measurements of 3 DUTs tested at $V_{DSirr} \geq 350\,V$ with $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ and a DUT tested at $V_{DSirr} = 300\,V$ with $^{56}Fe^{+15}$. For the latter DUT, the testing was stopped after the first exposure that induced degradation in the die, with only a single visible step in the drain and gate leakage.

In Fig. 5 (a) the gate leakage current measurements of the 4 DUTs in comparison with a reference measurement of a pristine CPM2-1200-0080B die are shown. It confirms that the gate oxide was heavily damaged during the irradiations and that the degradation is higher with increasing LET and drain-source bias voltage. Moreover, to not induce further damage in the device, the maximum measurable current was $I_G = 10^{-7}$ A. This value was reached at lower V_{GS} with increasing damage.

The current analysis presented in Fig. 5 (b) was performed increasing V_{DS} until a drain current threshold level of 1mA was reached. In this case also the source current I_S was measured, confirming the different current paths in devices tested at $V_{DSirr} = 300\,V$ and $V_{DSirr} \geq 350\,V$, as discussed earlier.

Similar analysis is reported in Fig. 5 (c) as a function of V_{GS} with $V_{DS} = 1\,V$. At low V_{GS}, the drain current flows from drain to gate, while at higher V_{GS} it flows from drain to source. This leads to the conclusion that the channel can still be controlled at V_{GS} below the V_{GS} breakdown voltage, although the gate leakage is very high. Hence, the assumption that the I_D is flowing through the channel and not through the base part of the MOSFET is confirmed.

D. *Degradation Rate*

The degradation rates as a function of the drain-source bias(V_{DSirr}) during the irradiation are presented in Fig. 6 (a) for the 25 mΩ , 80 mΩ and 160 mΩ DUTs irradiated with $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ (the results refer to one DUT for each case). The permanent increase of the drain leakage during the ion exposure was normalized by the fluence and the active area of the die, as described previously.

In general, at V_{DSirr} values above the degradation threshold, the degradation rate increases with increasing V_{DSirr}. Focusing on the $^{131}Xe^{+35}$ results, there is a sudden change in the bias dependent trend of the degradation rate as observed in Fig 6 (a)

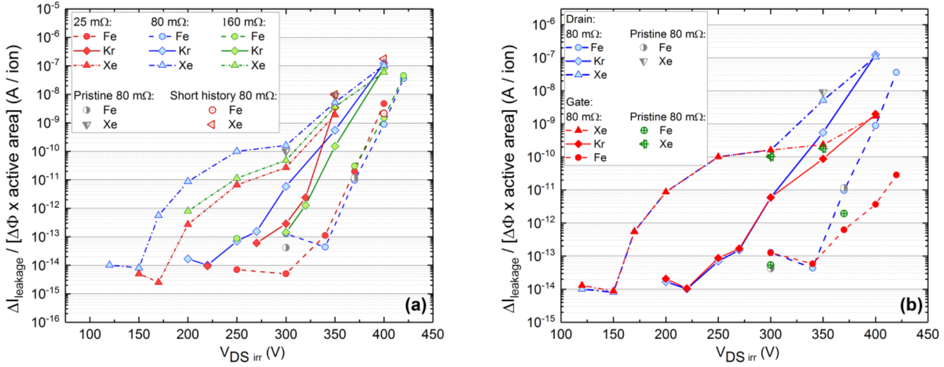

Fig. 6. (a) Rate of heavy ion induced increase in drain leakage current as a function of the drain-source bias during the irradiation. The results refer to a single DUT for the 25 mΩ, 80 mΩ and 160 mΩ. For the pristine 80 mΩ a different DUT was used for each irradiation. The short history 80 mΩ reports the results for the same DUTs exposed first as pristine at $V_{DSirr} = 300\,V$. (b) Magnified views of (a) considering heavy ion variation for the 80 mΩ die and comparison between the drain and the gate degradation rate.

at 300 V. This suggests that there can be two different mechanisms depending on the V_{DSirr}, as seen during the experiment. Moreover, approaching the SEB threshold at approximately 500 V [7], the dependence of the degradation rate on the LET becomes less distinctive.

Furthermore, the degradation rates for a die exposed to multiple consecutive runs and pristine die exposed only to a single run (as explained earlier) are at the same magnitude. Additionally, the same die tested as pristine at $V_{DSirr} = 300\,V$, were exposed for two more runs (at $V_{DSirr} = 350\,V, 400\,V$ for $^{131}Xe^{+35}$ and $V_{DSirr} = 370\,V$ for $^{56}Fe^{+15}$). The results for these die with a shorter prior degradation history are again at the same magnitude as all the other results. This leads to the conclusion that the prior degradation does not affect the degradation rate. This observation could suggest that also the SEB threshold is not affected by the prior damage, however further studies are needed in order to verify the hypothesis.

A magnified view of the degradation rates for gate and drain leakage considering the LET variations for the 80 mΩ die is shown in Fig. 6 (b). A clear superimposition of the drain and the gate degradation is observed until $V_{DSirr} = 300\,V$, independently from the prior degradation. At $V_{DSirr} \geq 350\,V$, the gate degradation diverges from the drain response, showing a common behavior independent from the heavy ion LET.

IV. Current Transport Model for Heavy-Ion Degraded SiC MOSFETs

A heavy ion strike can induce damage at the gate interface and create a leakage path through the oxide in the neck side. From the experimental results and from the electrical post-irradiation analysis, the heavy ion induced current path through the degraded device was schematized as follows.

At low V_{DS} the current flows from drain to gate, exhibiting a linear dependence on the applied bias. Hence, the current voltage characteristics can be modeled by a simple resistor. This resistor can be considered to have two components R_{ox} and R_{epi} ($R_{epi} \ll R_{ox}$) that represent the oxide resistance and the epilayer resistance, respectively. The effect of temperature variation during operation was not considered for the estimation. Moreover, in a pristine device the oxide leakage current is negligible ($R_{ox} \sim \infty$), hence the leakage flows through the body resistance R_{Body}. As observed from the experimental results, this is not the case of a degraded device, concluding that:

$$\begin{cases} R_{ox} \gg R_{Body} \text{ (pristine device)} \\ R_{Body} \gg R_{ox} \text{ (degraded device)} \end{cases} \quad (1)$$

At higher V_{DS}, the leakage path was observed to be mostly from drain to source, with a lower contribution of leakage from drain to gate. It was hypothesized that the leakage through the gate oxide generates a voltage drop sufficient to partially open the channel, setting the MOSFET in a condition of "partial on-state", sufficient to allow the current flowing to the source.

The electrical equivalent for the current transport is illustrated in Fig. 8 and is proposed to describe the heavy ion degraded device at $V_{DS} < 100\,V$. The very small part of the channel that opens as a consequence of the radiation induced leakage in the gate is modelled with a MOSFET named RADMOS. The gate terminal of the RADMOS is controlled by the potential generated in the gate oxide of the DUT. The total

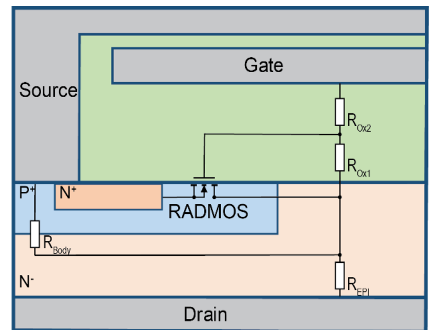

Fig. 7. Electrical equivalent for the heavy-ion induced current transport model in a degraded SiC power VD-MOSFET, valid at $V_{DS} < 100\,V$.

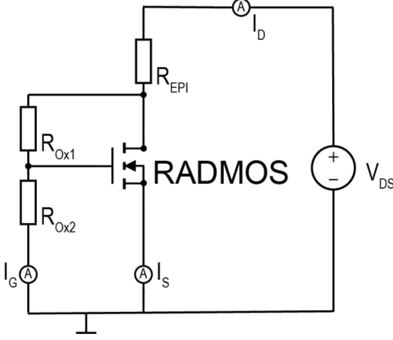

Fig. 8. Schematic layout proposed to describe the current transport in the heavy ion degraded device. The model was used to perform electrical simulations at $V_{DS} < 100\ V$.

resistance of the gate was divided in $R_{ox1} + R_{ox2}$ in order to simulate the potential gradient inside the oxide. At sufficiently high current flowing in the gate oxide, the $V_{GS-RADMOS} > V_{th-RADMOS}$, the channel is partially opened and the currents start to flow to the source.

To confirm this hypothesis, fits for the I_D, I_S, I_G measurements of the 80 mΩ device irradiated with $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ were done. For $V_{DS} < 100\,V$, it was confirmed that the I_G follows a linear behavior (i.e. ohmic), while the I_D and I_S follow a quadratic behavior characteristic of a MOSFET in on state. From the fit was found the following equation for I_S:

$$I_S = \frac{1}{2} K \left(\frac{V_{DS}}{B} - 2.6\right)^2 (1 + \lambda V_{DS}) \qquad (2)$$

where $B = (R_{ox1} + R_{ox2})/R_{ox2}$, K is the transconductance and $\lambda = \frac{\Delta L}{L}$ where L is the channel length. The fits were done for all the DUTs and the parameters are listed in Table II.

TABLE II
PARAMETERS USED FOR THE SIMULATIONS

Ion	R_{oxide} [Ω]	B	K [S]	λ
$^{56}Fe^{+15}$	8.82×10^9	9.5	1.80×10^{-7}	$1{,}16 \times 10^{-3}$
$^{82}Kr^{+22}$	3.13×10^8	10.4	3.70×10^{-7}	3.24×10^{-3}
$^{131}Xe^{+35}$	1.52×10^8	11.2	2.40×10^{-7}	1.21×10^{-2}

An electrical model to describe the degraded device is proposed in Fig. 8 and it was used to perform simulations with the parameters extracted from the fit. For all the cases, $V_{th-RADMOS} = 2.6\,V$ was used as first approximation, which is the typical V_{th} for the pristine device. The comparison between the measurements, the fit and the simulation results are reported in Fig. 9 for the DUTs exposed to $^{56}Fe^{+15}$ (a), $^{82}Kr^{+22}$ (b) and $^{131}Xe^{+35}$ (c) beams. For $V_{DS} < 100\,V$, there is a very good agreement between the measurements, the fit and the electrical model proposed in Fig. 8. The results confirm the linear ohmic behavior for I_G and the MOSFET behavior for I_D and I_S above the threshold voltage.

For $V_{DS} > 100\,V$, another current transport mechanism, not fully explained by the model above, becomes dominant. The I_D and I_G start to follow an exponential behavior. A linear

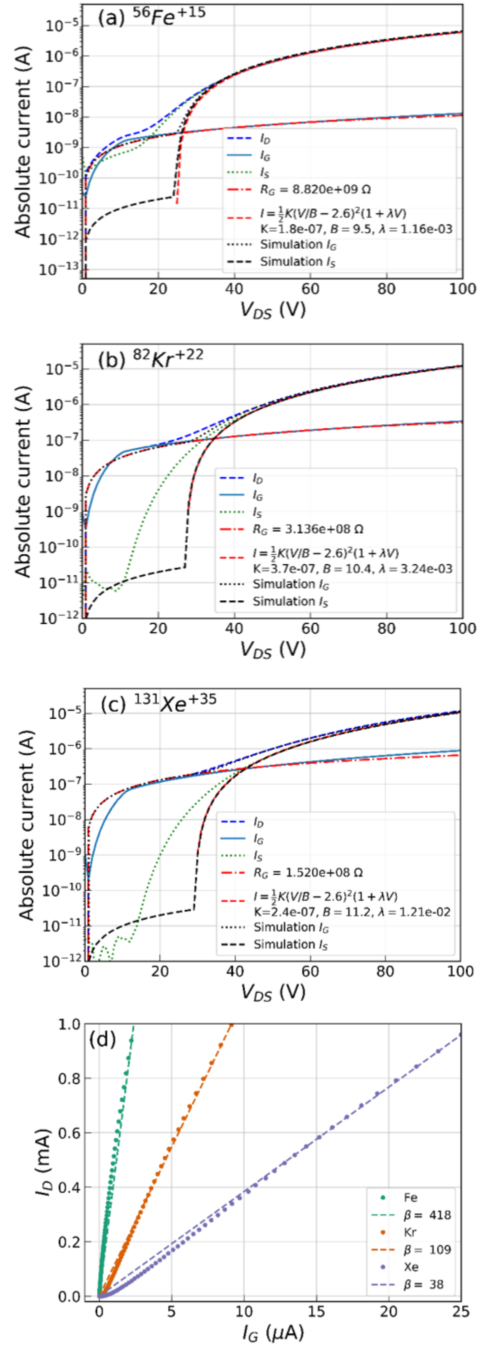

Fig. 9. Comparison of measurements, fit and simulations of I_D, I_G, I_S as function of the V_{DS}. The model for the simulation is valid until V_{DS} = 100 V The results are shown for $^{56}Fe^{+15}$ (a), $^{82}Kr^{+22}$ (b) and $^{131}Xe^{+35}$ (c). For V_{DS} > 100 V, the behaviour becomes exponential and there is a linear proportionality between I_D and I_G (d). The current amplification β depends on the heavy ion induced degradation.

dependency is observed between I_D and I_G currents, as visible in Fig 9 (d). The current amplifications, defined as β, are reported on the graph and they are dependent on the heavy ion induced degradation. However, the current amplifications measured do not involve the parasitic n-p-n BJT typically associated with the SEB in power MOSFETs [7].

Although a detailed discussion of the SEB mechanisms is beyond the scope of the present article and the focus of the work is on the non-destructive degradation region, this secondary transistor observed in the sub-region of the SEB is different from the parasitic BJT described in the literature. However, the current amplification observed at $V_{DS} > 100\,V$, could bring some suggestions on the description of the SEB phenomenon.

Finally, it has to be noticed that the observed charge transport mechanisms in ion-degraded SiC MOSFETs are different from those in SiC Schottky power diodes [21]. Indeed, in the case of ion-degraded SiC Schottky diodes, the charge transport is governed by the space charge limited current.

V. Conclusions

The ion-induced damage in the SiC power MOSFETs depends on the LET and the drain-source bias during the exposure. For all the DUTs, permanent increase in drain and gate leakage currents and degradation of the blocking capability were observed. Although no V_{th} shift was observed in the DUTs, the gate oxide was strongly affected in all the cases, and it was already damaged after the irradiation at $V_{DSirr} = 300V$, $200\,V$ and $120\,V$ respectively with $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$.

The results show that the ion-induced leakage path during the irradiation is from drain to gate when the irradiation bias is below 350 V. Above this bias voltage, the leakage current is divided between drain-gate and drain-source paths. Moreover, within the region studied ($300 \leq V_{DSirr} \leq 350\,V$), the leakage current path and the gate and drain degradation rate were observed to be independent on the prior degradation.

An electrical model is proposed to explain the current transport in the degraded SiC power MOSFETs. A current control phenomenon is described, leading first to the activation of the secondary MOSFET induced by radiation in the channel area (RADMOS) then, at $V_{DS} > 100V$, to an exponential behavior, with a linear dependence between I_D and I_G currents.

The mechanisms described here do not involve the parasitic n-p-n BJT, the intrinsic part of the device typically associated with catastrophic SEB in power MOSFETs [7]. However, the radiation induced secondary transistor as in the model proposed in this work, could bring some hints on the description of the SEB physical mechanisms.

Moreover, the charge transport model proposed for SiC power MOSFETs is also different from the one previously observed in SiC Schottky power diodes, where the charge transport is governed by the space charge limited current.

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Publication II

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Heavy-Ion Microbeam Studies of Single Event Leakage Current Mechanism in SiC VD-MOSFETs

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***Abstract*— Heavy-ion microbeams are employed for probing the radiation-sensitive regions in commercial SiC VD-MOSFETs with micrometer accuracy. By scanning the beam spot over the die, a spatial periodicity was observed in the leakage current degradation, reflecting the striped structure of the power MOSFET investigated. Two different mechanisms were observed for degradation. At low drain bias (gate and source grounded) only the gate-oxide (at JFET or neck region) is contributing in the ion-induced leakage current. For exposures at drain-source bias voltages higher than a specific threshold, additional higher drain leakage current is observed in the p-n junction region. This provides useful insights for the understanding of basic phenomena of Single Event Effects in SiC power devices.**

***Index Terms*— SiC VD-MOSFET, heavy-ion, single event effect, microbeam, leakage current degradation, SELC**

I. Introduction

Silicon carbide (SiC) is a wide bandgap material of great interest for high power and high temperature electronic applications, including space [1], [2] and accelerators [3]. Higher breakdown field and thermal conductivity makes SiC a very attractive material for power electronics compared to silicon [4], [5]. However, like their silicon counterparts, SiC power devices (MOSFETs and diodes) are sensitive to Single Event Effects (SEE). In particular, a unique SEE signature is observed in SiC power devices under heavy-ion irradiation [6]- [9]. For power MOSFETs, single ions can cause permanent degradation that leads to a gradual increased leakage in both drain and gate currents with increasing heavy ion fluence. This damage is not catastrophic, but the device operation may be altered, which complicates the assessment of radiation tolerance in these parts. This effect is here refereed to as Single Event Leakage Current (SELC).

The heavy-ion induced degradation in SiC MOSFETs was previously studied in [9]. It was observed that the gate area is the most vulnerable part within the MOSFET structure. The results show that the ion-induced leakage path forms from drain to gate when the irradiation bias is below a certain threshold voltage (about 30% of the maximum voltage or $V_{DS\,irr} = 350\,V$ for the 80 mΩ die from the 2nd Gen. Cree/Wolfspeed studied in the paper). Above this bias voltage, a permanent and more severe damage is caused in the MOSFETs and the leakage current is divided between drain-gate and drain-source paths. Also, the leakage current path and the gate and drain degradation rate were observed to be independent of the prior degradation. Based on the experimental results, an electrical equivalent circuit model was proposed in [9] to explain the current transport in the degraded SiC VD-MOSFETs.

SiC power MOSFETs are also sensitive to Single Event Burnout. Numerous experiments and simulations have been performed to study the SEB in SiC power devices for space and terrestrial environments [10]-[19]. Due to the similarities in results on SiC MOSFETs and diodes, it has been hypothesized that, the conventional SEB mechanisms developed in Si MOSFETs, such as parasitic bipolar transistor and tunneling assisted avalanche multiplication mechanism [20], may be suppressed in SiC devices. Indeed, there is no parasitic n-p-n BJT in the diode structure.

In order to extend the exploration of the physical mechanisms of ion-induced failure in SiC VD-MOSFETs, experiments were performed at the UNILAC micro-probe line at the Helmholtzzentrum für Schwerionenforschung (GSI) in Darmstadt (Germany). Au and Ca ion beams were used for the experiment. The focused beam (or microbeam) irradiation allows micron-accurate localization of the radiation-sensitive regions providing unique information for a deeper physical understanding of the SEE mechanisms in SiC technology. Different regions of the die were exposed to the heavy-ion microbeam and the ion-induced steps in the gate and drain

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TABLE I
LIST OF DEVICES UNDER TEST

Reference	Gen.	$R_{DS(on)}$ [mΩ]	V_{DS} [V]	$I_{D @ 25}$ [A]	#DUTs
CPM2-1200-0025B	II	25	1200	98	3
CPM2-1200-0080B	II	80	1200	36	7
CPM3-0900-0065B	III	65	900	36	6

TABLE II
CHARACTERISTICS OF THE ION SPECIES

Ion	LET [MeVcm²/mg]	Range [μm]	Window size [X x Y μm²]	ΔX [μm]	ΔY [μm]
Au	94	35.4	55x50	1.1	1.56
Ca	17	29.7	30x25	0.93	1.56

leakage current were analyzed as a function of the x-y coordinate within the scanned frame. The striped structure of the die was clearly recognizable and different sensitive regions were identified for different drain-source bias during the exposure, providing insight into the SELC mechanism. Two different responses to the ion strikes were observed in the monitored leakage currents. First, below a certain threshold voltage (about 30% of the maximum rated voltage or $V_{DS\,irr} > 350\,V$ for the 2nd Gen. Cree/Wolfspeed) only the gate region (above JFET region) was observed to be sensitive to SELC. Secondly, increasing the bias during the exposure ($V_{DS\,irr} > 350\,V$), higher sensitivity was measured in the p-n junction region of the vertical MOSFET.

Finally, it is hypothesised that the latter response in the observed SELC, is caused by the appearance of extended defects, generated by an ion initiated thermal stress, that consequently degrade the p-n junction area.

II. Heavy ion micro-probe experiment

A. The heavy ion micro-probe facility

The GSI's heavy ion micro-probe facility is situated at the end of the linear accelerator UNILAC. The ions enter the microbeam line through object slits assuring a beam free of scattered particles [21]. The beam is focused to a focal spot of about 500 nm in diameter by means of magnetic quadrupole lenses and it is moved in the focal plane using deflecting magnets, situated downstream of the focusing lenses. The single hits are discriminated by a channel electron multiplier (CEM) which detects the secondary electrons emitted by the materials due to the ion hit. To ensure the irradiation with a preset number of particles and to avoid double hits at the same position, a fast electrostatic beam switch, situated in front of the object slits, is controlled by the hit detection system. When a hit is detected, the microbeam is switched off and the probe moves to the new coordinates.

The irradiation is performed under vacuum and an optical microscope situated in the chamber allows a precise definition of the area to be scanned with the ion beam.

B. Experimental setup

Second and third generation vertical double-diffused power MOSFETs (VD-MOSFETs), available in bare die, from the manufacturer Cree/Wolfspeed were used as Devices Under Test (DUTs). Bare die were chosen in order to avoid the laborious decapsulation process, and directly expose the chip surface to the beam to allow sufficient penetration of the heavy ions through the sensitive active layers of the device, without being stopped in the package materials [22]. The references and the technical information of the tested devices are listed in Table I.

Three die individually biased via BNC connectors for gate and drain were mounted on a custom FR-4 carrier board with gold (ENIG) surface using standard SAC 305 solder paste. The gate and source were connected by aluminum wire bonds with 300 μm diameter and only a single wire was used to reduce the shadowing effect [22]. The drain connection was made onto the carrier board by the large soldered bottom pad. No capacitors or resistors were installed between the contacts. Keithley Source Measure Units, models 2636 (two channels, up to 200V) and 2410 (one channel, up to 1100V), were used during the irradiation to bias gate and drain, respectively, and to monitor the leakage currents. The cumulative count of heavy-ions hitting the device was recorded during the irradiation using a simple digital counter based on an Arduino Leonardo microcontroller board.

C. Heavy ion microbeam irradiation

Au and Ca ions with an energy of 4.8 MeV/amu and Linear Energy Transfer (LET) values of respectively 94 and 17 MeVcm²/mg were used in the experiments. Each DUT was irradiated several times scanning the beam spot in different pristine regions of the die until the drain leakage current reached a level of several 100 microamperes. Multiple DUTs were tested during the test campaigns. In the case of Au, a scanning area with a size of 55x50 μm² was selected for each irradiation and a total of 1600 ions in each scan was used. For the Ca-beam, 520 ions were used with a scanning area of 30x25 μm². The average distance between the steps in each, X and Y, direction, for both configurations was on the order of ~1 μm (see Table II for details). During the irradiation, the gate voltage V_{GS} was set to 0 V to hold the device in off-state, while the drain voltage V_{DS} was set to a constant positive value. Different values for the drain bias were used.

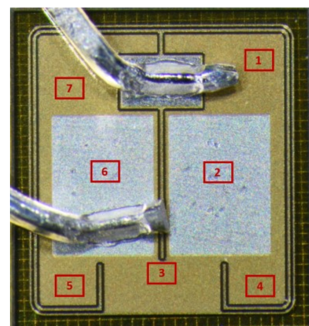

Fig. 1. Regions of the 80 mΩ die irradiated with Au beam (not to scale).

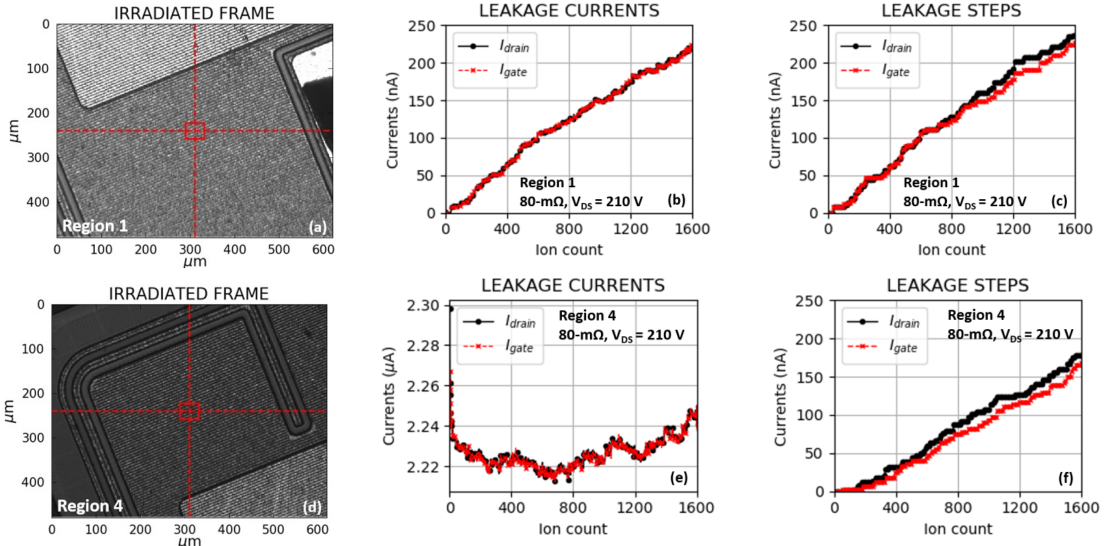

Fig. 2. Au irradiation in Region 1 and 4 of an 80 mΩ at $V_{DS\,irr} = 210\,V$. The exact location of the irradiation is identified by the window frame on the microscope images respectively in (a) and (d). The drain and gate leakage currents increases are shown in (b) and (e) (for a pristine device, the leakage currents are on the order of 10 pA), while in (c) and (f) is the cumulative sum of the radiation induces leakage steps.

III. Experimental Results

A. Exposure of different areas of the 80 mΩ DUT

In this work, the presented results are for the 80 mΩ die from the 2nd Gen. Cree/Wolfspeed, but similar considerations are valid also for the 25 mΩ and 65 mΩ DUTs. For an exemplary 80 mΩ DUT, the irradiated regions are indicated in Fig. 1 (not to scale). During Au irradiation, gradual permanent degradation (SELC) in the device was observed at $V_{DS\,irr} > 150\,V$ (~12.5% of the rated voltage). At drain biases below 350 V (~30% of the rated voltage), the magnitude and degradation rate of the leakage currents, for both drain and gate, were equal. Similarly it was observed for the 25 mΩ, while for the 65 mΩ devices from the 3rd Gen., equal gate and drain current were observed at $V_{DS\,irr} < 320\,V$ (~35% rated voltage).

Two examples for an 80 mΩ die exposed to Au beam in region 1 and 4 at $V_{DS\,irr} = 210\,V$ are shown in Fig. 2. The corresponding positions of the scanning areas are visible on the micrographs in Figs. 2 (a) and (d). The leakage current evolution during the irradiations are shown in Figs. 2 (b) and (e). The heavy-ion induced steps were analysed from the leakage current evolution by using a threshold step height of 2.5 nA to filter the background noise and are reported in Figs. 2 (c) and (f).

The total degradation induced by the ion exposures in regions 1-7 at $V_{DS\,irr} = 210\,V$ were calculated using two different methods and are listed in Table III. In the first method, the total radiation induced degradation was calculated summing all the leakage current steps higher than 2.5 nA. In the second method, instead, the induced degradation was calculated from the I_D-V_D and I_G-V_D measurements performed before and after each run (at $V_{GS} = 0\,V$), considering the leakage current increase at $V_{DS\,irr} = 210\,V$. The sequence of exposures is the same as reported in the table lines. Generally, the second method gives higher results since additional leakage current increase was caused by the stress induced during the post-irradiation IV measurements. The activation of latent damage in the gate oxide due to the post-irradiation electrical stress was previously discussed in [23]. Overall, the response is in the order of a few hundreds of nA and it is consistent between the different areas of the die (as expected). However, some differences are still visible. It has to be considered that not all the ions hitting the device during the scanning within the same window frame cause a permanent increase in leakage current. Also, a pristine area was selected for each irradiation and the position of the window to be irradiated was not exactly the same with respect to the device structure between different runs (i.e., number of stripes covered by the window). The combination of these effects could be a reason for the different responses observed. Also, the SMU range was automatically selected during the measurements leading to different measurement sensitivity

TABLE III
CURRENT DEGRADATION IN DIFFERENT REGIONS

Region *	ΔI_D / ΔI_G (nA) 1st method	ΔI_D / ΔI_G (nA) 2st method
1	237 / 226	192 / 191
2	221 / 215	396 / 396
3	140 / 122	419 / 418
4	178 / 168	344 / 341
5	157 / 166	311 / 313
6	262 / 239	361 / 362
7	366 / 356	555 / 555

* 80 mΩ die exposed to Au-beam at $V_{DS\,irr} = 210\,V$

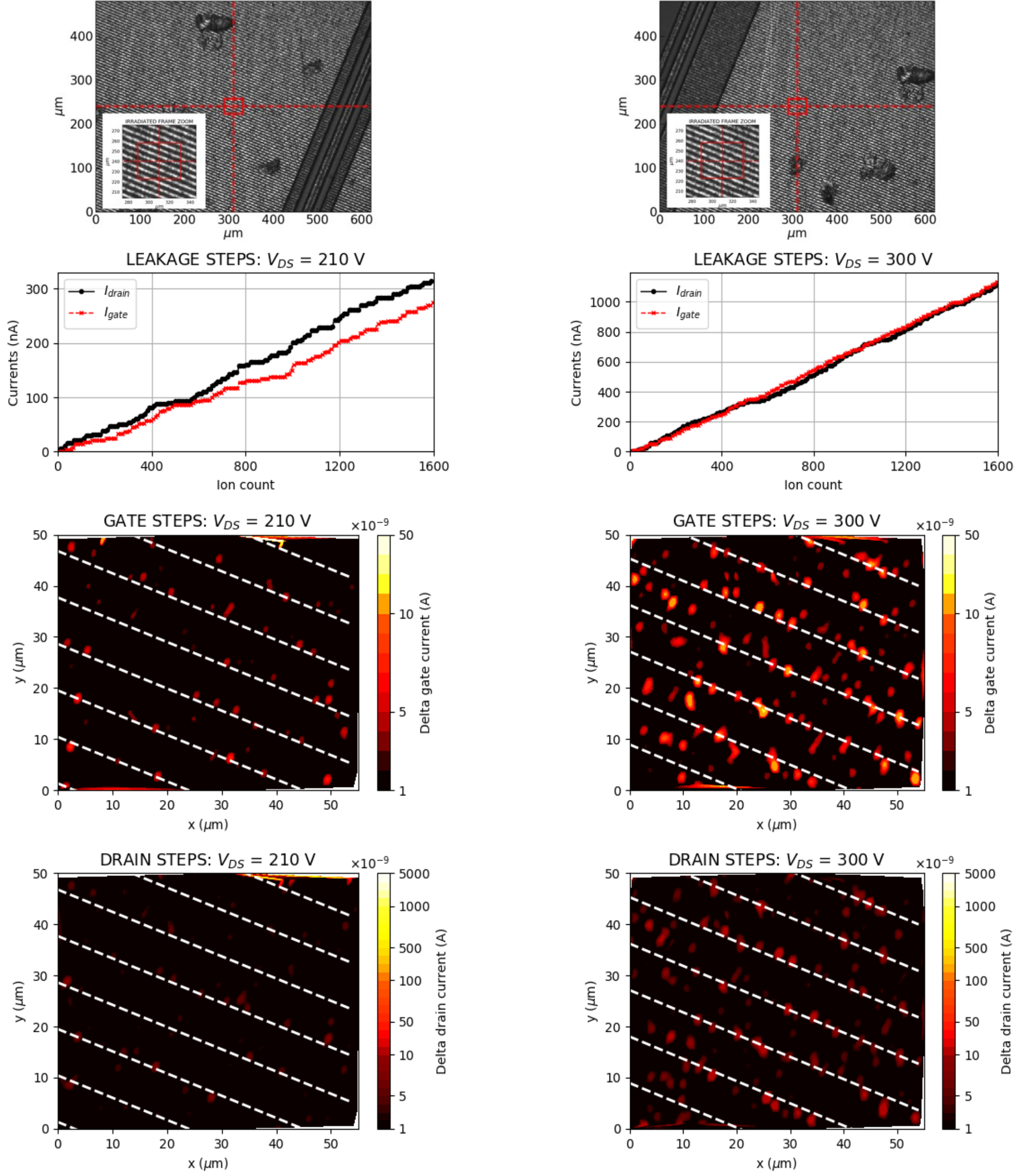

Fig. 3. All the runs refer to region 2 of an 80 mΩ DUT. On the left: $V_{DS\,irr} = 210\,V$, on the right: $V_{DS\,irr} = 300\,V$. From the top: 1) the frame selected for the irradiation in region 2 is visible on top of the microscope image; 2) drain and gate leakage current evolution during the irradiation; 3) and 4) the gate and the drain current steps are respectively represented as a function of the scanner position. The gate stripes were plotted within a distance of 9.1 µm, based on the technological information in 3) and 4) and they are comparable with the stripes in the zoom visible in 1).

during the runs due to the elevated baseline for the leakage current caused by the degradation induced by the radiation.

B. *Sensitive areas for gate and drain SELC*

In order to define the sensitive regions for gate and drain SELC and its dependence on the drain-source bias during the exposure, some runs were analyzed in more detail. The results are reported for an 80 mΩ DUT exposed to Au particles in region 2 at four different $V_{DS\,irr}$ conditions. The runs were performed consecutively with the same DUT and the results are shown in Fig. 3 for $V_{DS\,irr} = 210\,V$ and $V_{DS\,irr} = 300\,V$ and in Fig. 4 for $V_{DS\,irr} = 350\,V$ and $V_{DS\,irr} = 400\,V$. An optical

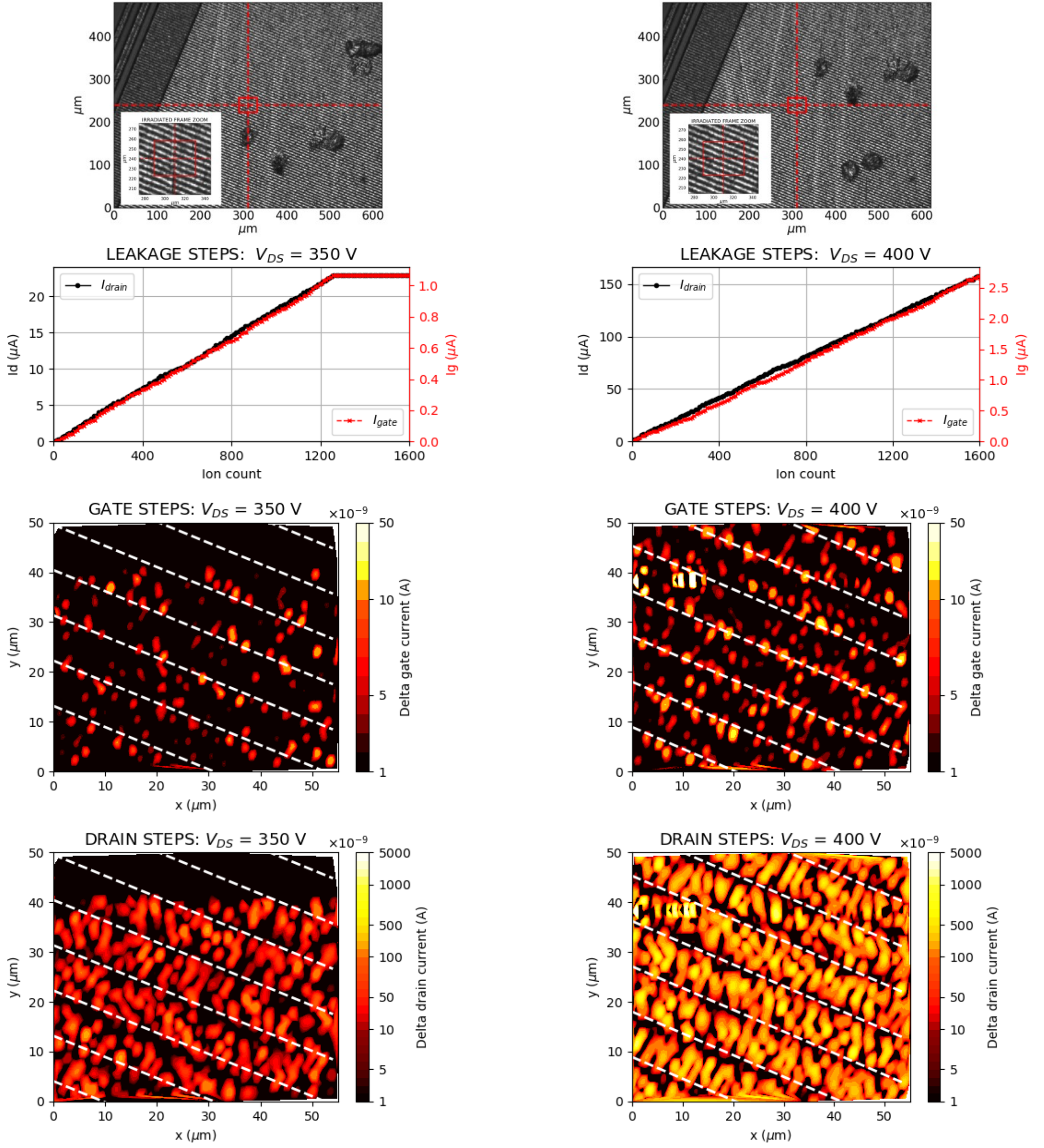

Fig. 4. All the runs refer to region 2 of an 80 mΩ DUT. On the left: $V_{DS\,irr} = 350\ V$, on the right: $V_{DS\,irr} = 400\ V$. From the top: 1) the frame selected for the irradiation in region 2 is visible on top of the microscope image; 2) drain and gate leakage current evolutions during the irradiation; 3) and 4) the gate and the drain current steps are respectively represented as a function of the scanner position. The gate stripes were plotted within a distance of 9.1 μm, based on the technological information in 3) and 4) and they are comparable with the stripes in the zoom visible in 1).

microscope was used to select the scanning area to be irradiated and the exact positions are shown in the first panel from the top. A pristine area was selected for each new run. During the exposure, I_D and I_G were monitored and the leakage current step evolutions calculated using a threshold of 2.5 nA. The data are presented in the second row of graphs. For the runs at 350 V and 400 V, separate axes are used for I_D and I_G, due to the higher degradation rate for the drain current. Also, in the irradiation at 350 V only a total of 1200 ions were used in the scan, due to a problem with the beam scanner during the exposure. Unfortunately, this was noticed only afterwards and the run was not repeated. For the irradiations performed at $V_{DS\,irr} < 350\ V$,

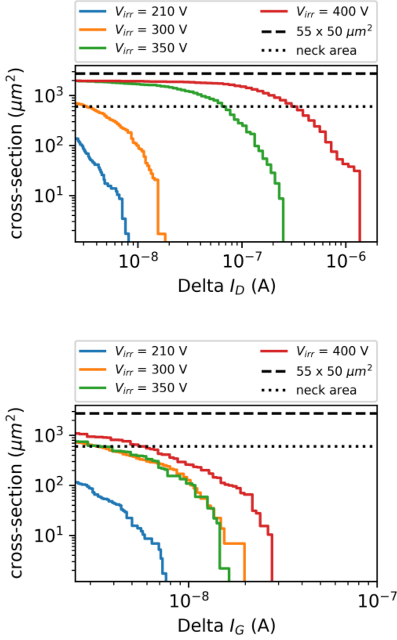

Fig. 5. Complementary cumulative distribution function for the measured cross-section of the gate and drain SELC at different drain-source bias during the irradiation. For reference, the size of the exposure window and the estimated transistor's neck area (or JFET region) are illustrated in the graphs.

as discussed in [9] and as mentioned earlier, the leakage current path is from drain to gate, i.e., $\Delta I_D \approx \Delta I_G$. For $V_{DS\,irr} > 350\,V$, instead, the leakage paths are divided between drain-gate and drain-source path. For both gate and drain, the current steps induced by the heavy ions were analyzed as a function of the scanner position within the scanning area used in the run. The amplitude of each radiation-induced step was calculated using a threshold value of 2.5 nA for I_D and I_G. If the step was lower than the threshold, it was set to 0 A to filter the noise. Moreover, the SMUs were usually logging data at a slower rate than the ion strikes arrived (especially for low leakage values), therefore for some ion counts no current data is available. In the analysis, the delta currents are set to 0 A for these ion strike locations. Successively, the data for the scanner position logged as CAMAC standard (Computer-Aided Measurement And Control) were converted into ASCII format and, then, into x-y coordinates (using µm units) inside the irradiated frame. Finally, each leakage step was associated with the corresponding scanner position and heat maps were generated for the gate and drain degradation for each run, as presented in the third and fourth row graphs of Figs 3 and 4. Additionally, the gate stripes within a distance of 9.1 µm are indicated with dotted lines to guide the eye, based on the technological information available for the device. For each run, the stripes were aligned with the degradation observed in the gate heat map, assuming the sensitive region for the gate leakage current being in the oxide of the gate stack. The striped structure of the die is clearly visible in the heat map and comparable with the one in the microscope image. Indeed, the periodicity in the lateral response observed in the leakage current degradation analysis reflects the periodicity of the striped structure. This result confirms that the entire MOSFET cell is not uniformly sensitive to SELC, but the response strongly depends on the ion strike location. In general, the sensitive region enlarges with increasing $V_{DS\ irr}$. In particular, for the irradiations at $V_{DS\,irr} < 350\,V$ (Fig. 3), the sensitive regions are aligned with the gate stripes in the neck area (JFET region) for both gate and drain heat maps. However, at $V_{DS\,irr} > 350\,V$ (Fig. 4) the sensitive areas for gate degradation are still aligned with the same regions, but those for the drain leakage degradation are now between the gate stripes, i.e., in the p-implanted body-diode region of the VD-MOSFET. This result supports the hypothesis that at increasing drain-source bias during the exposure and approaching the SEB threshold (~500 V), the body diode area is contributing to the current amplification process.

C. Cumulative distribution function for gate and drain SELC

The cross sections for SELC probabilities in different biasing conditions can be represented using complementary cumulative distribution functions (CCDF) for the measured gate and drain steps. The CCDFs for the four $V_{DS\ irr}$ conditions discussed earlier are shown in Fig. 5. Each bin represents the probability of the heavy-ion-induced step with a height above a given x-axis value. The distribution was normalized with the total number of ions in the run and the bin width. The probability to measure higher degradation steps increases with increasing drain-source bias during the exposure, as expected. Indeed, at $V_{DS\,irr} = 400\,V$, the maximum step height for drain and gate current were $\Delta I_D = 1.5x10^{-6}\,A$ and $\Delta I_G = 2.9x10^{-8}$ A, respectively. The size of the exposure window and the estimated transistor's neck region (within this window) are illustrated in the graphs. For the gate leakage the probability saturates to values close to the neck area (or JFET region). Probably the most sensitive areas for gate degradation are those close to the channel, but the resolution is not high enough to explicitly see that ($\Delta X = 1.1\,\mu m$).

D. Test methodology

During the experiments, an initial overshoot and subsequent levelling in the leakage current were observed once the DUT had been degraded to a certain level. In the run shown in Fig. 2 (b) the device exposed to the beam was pristine, while in the run in Fig. 2 (e) the part was already damaged. In the latter case, the leakage current was on the order of µA. Comparing the current evolutions, for the degraded part (Fig 2 (e)), higher current values are measured promptly after the V_{DS} bias was applied, followed by an immediate decrease of the current over the increase of the ion count. During the experiments, the irradiation started before the system reached the steady state condition, so the increase in the ion-induced leakage current was partially masked by this effect of overshoot and its levelling. In order to get rid of this effect in the analysis, the total degradation was then calculated summing all the leakage current steps over 2.5 nA, instead of considering the delta between the final and the initial value of the current. However, this effect has been identified as part of a testing methodology for future work. Unfortunately, due to the limited number of

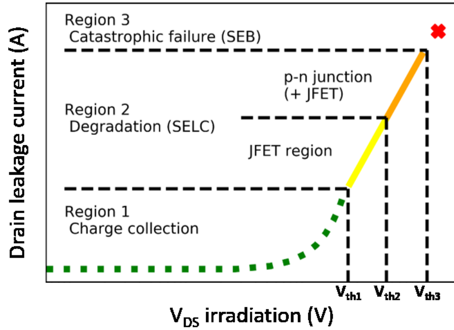

Fig. 6. Three characteristic regions of damage for SiC power MOSFETs as a function of the drain-source bias during the heavy ion irradiation. Two sub-regions are identified for degradation (region 2). Firstly, between V_{th1} and V_{th2}, the area underneath the gate (JFET or neck region) is the most sensitive for SELC. The second mechanism is newly added at biases higher than V_{th2}, when higher SELC is measured in the p-n junction area, but a smaller leakage remains also through the gate oxide.

tested devices still operable, it was not possible to obtain detailed conclusions and further investigation is needed to better understand the origin of this behavior. However, we suggest a possible explanation due to a thermal effect in the ion-induced damage area within the device. In a degraded DUT, the current can be considered to flow through very small damage sites (i.e., 10 – 100 nm size) causing very high current densities at localised leaky points. Once the bias is set, the temperature in these local spots increases very rapidly due to the high current density. If the conductivity of the leaky region is inversely proportional to temperature similarly to metals, then it could explain the observed behaviour in the leakage current promptly after applying the bias voltage. Additional studies are needed to validate this hypothesis.

Finally, since the work was performed in the context of the basic mechanism research, it was decided to avoid installing any additional capacitances to limit the external influences on the observed results. Therefore, the setup used was different from the one recommended by the military standard (MIL- STD-750 M1080).

IV. Discussion on SELC mechanism

The microbeam results confirm that two different mechanisms are governing the SELC, involving different areas of the MOSFET structure. One mechanism is attributed to oxide damage (above the JFET or neck region) that results in leakage path between drain and gate. The other degradation mechanism is triggered when the bias applied during the exposure is sufficiently high to reach certain electrical conditions within the pn-junction. These different areas for ion induced drain leakage response are illustrated in Fig. 6, where the three regions discussed in [9] are updated with the new considerations. At low bias voltages, the ion-induced charge is collected with a similar multiplication mechanism as in Si MOSFETs and no permanent damage is observed in the device. At higher bias, two sub-regions are identified for degradation. Firstly, between V_{th1} and V_{th2}, the area underneath the gate (JFET area) is the most sensitive for SELC. More precisely, the channel area should also be included in this considerations. The second mechanism is observed at biases higher than V_{th2}, when higher SELC is measured in the p-n junction region, but a smaller leakage remains also through the gate oxide. In the third region, at sufficiently high bias above V_{th3}, a catastrophic Single Event Burnout failure occurs.

Concerning the first mechanism of degradation, similarities are found with Si power MOSFETs soft oxide breakdown which was previously discussed in [23] and [24]. The increase of the leakage current was explained though the Quantum Point Contact (QPC) model. According to this theory, conductive paths are generated in the oxide which behave as point contacts between the gate and the substrate [25]. Similarities are found also with the precursor ion damage mechanism in Si MOS structures with thin oxides as described in [26]. This mechanism was described as an unrelated effect with respect to SEGR.

For the second SELC mechanism via p-n junction, a common explanation for SiC power MOSFETs and JBS diodes is proposed. Experimental data previously presented in [10], suggested that a common mechanism is responsible for leakage current degradation in SiC power MOSFETs and junction barrier Schottky (JBS) diodes when exposed to heavy ions. Technology Computer-Aided Design (TCAD) simulations of the two structures were also discussed in [10]. Ion-induced highly localised energy pulses were demonstrated and are proposed as a common mechanism for SELC degradation in SiC power MOSFETs and JBS diodes. However, no TCAD simulations were reported yet concerning the difference observed experimentally for heavy-ion irradiations at $V_{DS\,irr} < 350\,V$ and $V_{DS\,irr} > 350\,V$. Moreover, in [27] molecular dynamics (MD) simulations of heavy ion induced defects for SiC Schottky diodes has been performed. The structure of the ion track was obtained after the first 100 ps when the energy has already dissipated into the bulk and the atoms in the core of the track have cooled down. The results suggest that the combination of the ionization of the impinging ion and the applied bias, can result in prompt Joule heating that leads into amorphous regions within the material. Indeed, the energy deposited via Joule heating is sufficient to cause a phase transition in the material, which is unlikely to recrystallize back completely, leaving permanent structural modification in SiC lattice, as suggested in [28].

It is hypothesized that the common mechanism described in [10] for SELC in JBS diodes and SiC power MOSFETs, only involves the SELC through the p-n junction, therefore observed for voltage bias higher than V_{th2} ($V_{DS\,irr} > 350\,V$ for the studied DUTs). The SELC via p-n junction originates from the thermal stress induced by the highly located power dissipation. The thermal transient and excessive lattice temperature, probably causes the formation of permanent extended defects (EDs), which remain after the switch off of the irradiated device; e.g., MD simulations showed that amorphous region along the ion track appears starting from certain values of applied V_{DS} [27]. However, MD simulations now give rather qualitative results and there were no experimental studies yet to investigate the sites of heavy-ion impact. For this reason, the material modifications induced by the heavy-ion strike in biased SiC power devices, are still a matter of discussion. Those EDs can be amorphous pockets, different dislocations, stacking faults, different SiC solid phase (polytype) inclusions, clusters,

etc. More could be stated about the ED nature investigating the irradiated structure by electron microscopy and optical methods [29]-[31]. However, it should be clearly stated that the experiments were performed using a specific device type from one manufacturer; as both design as well as the resulting efficient carrier concentration in the specific areas will vary between device types and manufacturers, the results cannot be transferred to all SiC power devices without further analysis.

Finally, the role of the p-n junction degradation under SEB conditions needs to be further investigated taking into account also other types of devices from different manufacturers.

V. Conclusions

A unique SEE signature named Single Event Leakage Current (SELC) is observed in SiC power devices under heavy-ion irradiation. Micro-probe experiments were performed at GSI in Darmstadt (Germany) with Au and Ca ion beams in order to study the SELC mechanism. 2nd and 3rd generation commercial SiC VD-MOSFETs from the manufacturer Cree/Wolfspeed were used as DUTs.

Different regions of the die were exposed to heavy ions and detailed analyses were done for the 2nd Gen. 80 mΩ devices. The response to heavy ions was observed to be homogenous over the scanned areas around the die (as shown in Fig.1).

The ion-induced steps in the gate and drain leakage current were plotted as a function of the x-y coordinate within the frame scanned by the microprobe. A comparison was made for irradiations with Au at different drain-source bias during the exposure. The striped structure of the die is clearly visible in the gate and drain SELC heat maps. Two mechanisms involving different areas of the MOSFET structure were observed for the heavy-ion induced degradation. Firstly, at lower bias, the area underneath the gate (JFET or neck region) is the most sensitive for SELC. The second mechanism gets activated at higher biases and stronger SELC response is observed in the p-n junction region (smaller leakage contribution remains through the gate oxide).

For the first mechanism, similarities are found with the Si power MOSFETs soft oxide breakdown, previously explained with the QPC model. Concerning the second mechanism of degradation, it is discussed that at sufficiently high bias, the highly localized power dissipation caused by the heavy-ion strike generates a thermal transient and excessive lattice temperature. The thermal stress causes the formation of permanent extended defects (EDs) which degrade the p-n junction. For example, MD simulations showed that the amorphous region along the ion track appears above certain values of applied V_{DS}. However, the material modifications induced by the heavy-ion strike in biased SiC power devices are still a matter of discussion and the nature of the EDs should be further investigated.

Finally, it is hypothesized that SELC is the manifestation of the same mechanism in JBS diodes and SiC power MOSFETs only when it involves the SELC through the p-n junction of the MOSFET, therefore for voltage bias higher than a certain threshold ($V_{DS\,irr} > 350\ V$ for the studied DUTs).

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Publication III

C. Martinella, R. G. Alia, A. Coronetti, C. Cazzaniga, M. Kastriotou, Y. Kadi, R. Gaillard, U. Grossner, A. Javanainen, "Impact of Terrestrial Neutrons on the Reliability of SiC VD-MOSFET Technologies", *IEEE Trans Nucl. Sci.* vol 68, no. 5, pp. 634-641, May 2021.

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Impact of Terrestrial Neutrons on the Reliability of SiC VD-MOSFET Technologies

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***Abstract*—Accelerated terrestrial neutron irradiations were performed on different commercial SiC power MOSFETs with planar, trench and double-trench architectures. The results were used to calculate the failure cross-sections and the failure in time (FIT) rates at sea level. Enhanced gate and drain leakage were observed in some devices which did not exhibit a destructive failure during the exposure. In particular, a different mechanism was observed for planar and trench gate MOSFETs, the first showing a partial gate rupture with a leakage path mostly between drain and gate, similar to what was previously observed with heavy-ions, while the second exhibiting a complete gate rupture. The observed failure mechanisms and the post irradiation gate stress (PIGS) tests are discussed for the different technologies.**

***Index Terms*— Silicon Carbide, Power MOSFETs, neutrons, Single Event Effects, Single Event Burnout, gate damage**

I. Introduction

Wide bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have gained popularity in recent years. Between them, SiC is the most mature technology and has become a viable alternative to Silicon-based power devices in high-efficiency and high-power density applications [1-2]. The higher breakdown field and thermal conductivity make SiC a very attractive material for different ground applications, such as automotive and solar inverters, but also for the avionics and space industries [3-4]. Moreover, SiC is considered as a promising technology for accelerator applications [5-6]. However, SiC devices are known to be susceptible to Single Event Burnout (SEB), Single Event Gate Rupture (SEGR) and Single Event Leakage Current (SELC). SEB and SEGR are caused, among others, by high-energy neutrons [7-15], while SELC has been reported only with heavy-ions [16-20].

The high-energy neutrons originate from cosmic ray interactions with the atmosphere. These include solar event particles (SEPs) originated by dynamic solar activity and galactic cosmic rays (GCRs) created by events outside the solar system, such as the explosion of galactic nuclei and supernova, pulsars and stellar flares [21-23]. These particles (i.e., 92% protons, 6% alpha particles and 2% heavier atomic nuclei) are responsible for Single Event Effects (SEEs) observed in electronics used in space. The particles that are not deviated or trapped by the magnetic field enter the Earth's atmosphere and, upon interacting with, e.g., oxygen and nitrogen atoms, create a shower of secondary particles. These interactions result in neutrons, protons, muons, pions and electromagnetic waves [22]. Some particles decay or are absorbed, while others travel further in the atmosphere, causing a cascade through spallation reactions. Due to the charge neutrality and the abundance, this gives rise to a high flux of secondary neutrons traveling vast distances in the atmosphere. The peak of neutron intensity occurs at about 10-25 km, which is critical for avionic applications, being the altitude of many commercial airplane flights [21]. Below, there is a net loss of total particles in the cascades, having a flux which drops two orders of magnitude at sea level, with a neutron flux of less than 25 n/(cm^{2}h) for energies higher than 1 MeV [22]. Data centers and the Si power electronics community have reported failures and upsets at sea

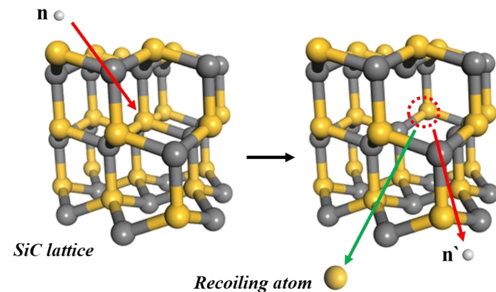

Fig. 1. By the elastic and inelastic scattering with the 4H-SiC lattice, the atmospheric neutrons produce recoiling atoms (i.e., α, C, Si, Mg, Al) which generate ionizing tracks inside the power MOSFET.

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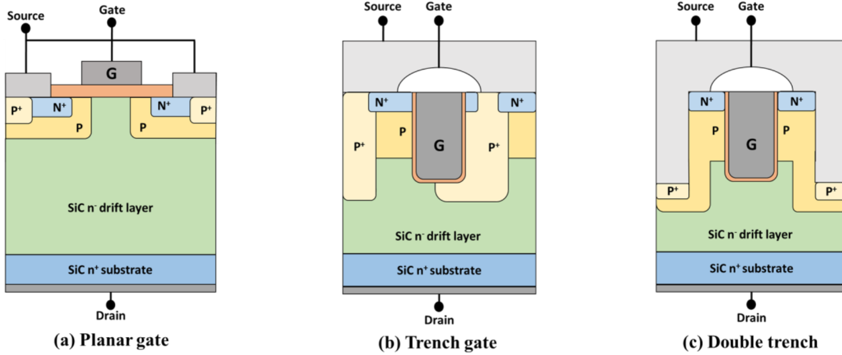

Fig. 2. Schematics of the three architectures of SiC power MOSFETs tested in this work: (a) planar gate, (b) trench gate from Infineon and (c) double trench (trench source and trench gate) from Rohm. Picture remake after the original from Siemieniec *et al.* [30].

level [24-27]. Additionally, due to the exponential increase of neutron flux with increasing altitudes, problems can be encountered for applications at higher altitudes, for example on a mountain top [23].

Furthermore, neutrons can cause issues for electronic systems installed in high-energy accelerators, such as the Large Hadron Collider (LHC) complex and its future upgrade High Luminosity LHC (HL-LHC) at CERN, Geneva [28]. Here, commercial SiC power MOSFETs have been considered for the design of a prototype inductive adder (IA) to be used as a pulse generator for the injection kicker magnets [5-6].

The physics of neutron induced SEB in SiC power devices has been previously studied, and an explanation for this destructive effect was suggested in [7]. Although neutrons are non-ionizing particles, the recoiling atoms, generated from their elastic or inelastic scattering with the lattice atoms, can indirectly give rise to ionization and create a large number of electron and hole (e–h) pairs along their trajectories. This event is followed by a hole impact ionization with associated multiplication factors and a consequent thermal transient and excessive lattice temperatures. This leads to local lattice sublimation and formation of voids, resulting in the loss of device blocking ability, hence a destructive failure. A schematic of the neutron interaction with the 4H-SiC lattice is shown in Fig. 1. Finally, it was reported that no consistent differences have been observed in the SEB tolerance for SiC MOSFETs and SiC diodes [8]. This supports the hypothesis that the conventional mechanisms underlying SEB in Si MOSFETs, such as parasitic bipolar junction transistor (BJT) and tunneling assisted avalanche multiplication mechanisms [29], may be suppressed in SiC devices, where the current gain of the parasitic BJT is lower. Indeed, there is no similar parasitic BJT structure in the diode design.

In this work, we investigate the effect of neutron irradiation on different commercial SiC power MOSFETs produced by different manufacturers. The devices were selected with three different types of design: planar gate, trench gate and double trench, where the last has a trench gate and source [30]. The schematics of the three architectures are shown in Fig. 2. The radiation sensitivity is discussed for the different technologies. Experiments were performed at ChipIr, the beamline at the Rutherford Appleton Laboratory (U.K.) providing an atmospheric-like neutron environment. During the irradiations, destructive failures were observed and the failure cross-sections and FIT rates are presented for the tested references. Additionally, from the post-irradiation analysis, the latent damage and the impact of gate rupture in planar and trench gate design are discussed highlighting the differences among these device types and the dependence of the failure type on the technology. Finally, the results for the post-irradiation gate stress (PIGS), performed as recommended by the MIL-STD-750, test method 1080 [31], are also presented.

II. Neutron Irradiation Experiment

A. The ChipIr terrestrial neutron facility

ChipIr is a beamline built at the second target station (TS2) of the ISIS spallation source at the Rutherford Appleton Laboratory, UK [32-34]. The facility is specifically tailored for testing radiation effects on electronic components and systems. The beamline design is optimized to mimic the atmospheric neutron spectrum (up to 800 MeV) with an acceleration factor of up to 10^9 for ground-level applications. The neutrons delivered to the ChipIr facility are emitted from the spallation of high-energy protons with a tungsten target (i.e., 800 MeV protons extracted from the synchrotron with beam current of 40 μA and pulsed at 10 Hz). The neutrons are delivered to ChipIr according to the time structure of the ISIS source, i.e., in 10 Hz pulses, with two 70-ns-wide bunches separated 360 ns apart. A silicon diode, placed in front of the testing position, measures the energy distribution of single pulses. This is used to retrieve the neutron fluence at the device under test (DUT) location knowing the detection efficiency and, by means of a correction factor function of the distance between the diode and the DUT position, which takes into account the beam divergence. During the test campaign, the measured flux of neutrons above 10 MeV was 5.6 x 10^6 $cm^{-2}s^{-1}$ at the testing position. A collimator system allows for selecting beams of different sizes. For the current experiment, a beam size of 10 cm x 10 cm was used.

TABLE I
LIST OF DEVICES UNDER TEST

Reference	Man.	$R_{DS(on)}$ [mΩ]	V_{DS} [kV]	$I_{D @ 25}$ [A]	BV_{DSS} [kV]	Gate	#DUTs
C2M0025120D	Cree/ Wolfspeed	25	1.2	250	1720	planar	51
SCT3030KL	Rohm	30	1.2	180	1926	double trench	48
MSC025SMA120B	Microsemi	25	1.2	275	1586	planar	50
SCTWA50N120	ST-Micr.	59	1.2	130	1520	planar	66
IMW120R090M1H	Infineon	90	1.2	50	1483	trench	65

B. *Experimental method*

The aim of this study is to investigate the effect of atmospheric-like neutrons on different commercial SiC MOSFET technologies. Accelerated testing of Single Event Burnout (SEB) by using terrestrial neutrons was performed. The obtained data were used to calculate the effect cross sections and failure in time (FIT) rates at ground level. Additionally, the devices that did not exhibit destructive failure during exposure were characterized and their operational reliability was studied.

Several samples were selected from the commercially available SiC VD-MOSFET technologies. The references and the corresponding technical information are listed in Table I. All the devices are rated for 1.2 kV and they are mounted in a TO-247 package. The devices were irradiated in their original packaging. The first three devices were selected with similar values of $R_{DS\ (ON)}$ among them, and the same was done for the last two devices. The references were selected with different design: planar, trench and double trench. In particular, the DUTs from Infineon have a trench gate structure [35], whereas the Rohm have a double trench design, with trench gate and trench source. For the trench gate devices, the channel is formed vertically, which allows the current to flow vertically while reducing the $R_{DS(ON)}$ [36]. All the other references have a planar gate structure.

The test setup was designed following the military standard specifications (MIL-STD-750E M1080.1) [31]. Each test board can host a maximum of 12 devices in parallel. A schematic layout of the setup is presented in Fig. 3, where two DUTs are illustrated for brevity. Two boards were stacked to test up to 24 DUTs for each run. They were installed at a distance of 58 cm and 76 cm from the beam aperture, respectively. The attenuation of the neutron beam in the first board was estimated to be negligible for the material used in the tested boards [37]. Two Keithley Source Measurement Unit (SMU) model 2410s (one channel, up to 1100 V), one for each board, were used to bias the drain and to monitor the total leakage currents as a sum of all devices. The gates were grounded directly on the board. A stiffening capacitor of 10 nF was installed between the drain and the ground for each DUT, in order to supply sufficient amount of charge during a destructive event. Moreover, it also limited the momentary voltage drop at the SMU output during current transients. The devices were connected in parallel to the high voltage, but each of them had an individual current limiting resistor of 860 kΩ between the drain and the SMU output. This guaranteed the isolation of the device after a failure and the continuous application of high voltage to all other devices. Each step increase in the total current measured by the SMU was accounted as a failure ($\Delta I_{DS} = 1.27\ mA$). This value corresponds to a short circuit on the DUT and the total voltage is applied across the protection resistor. In Fig. 4 an example of the online measurements recorded during an exposure run is shown. The results are presented for Rohm SCT3030KL devices exposed at 1100 V. Here, the measured drain current

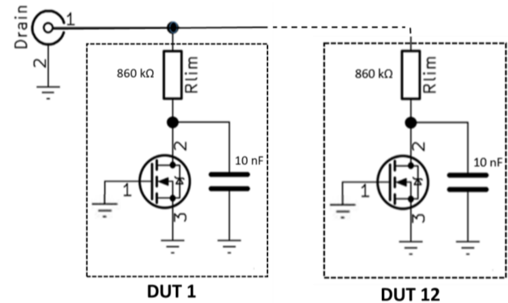

Fig. 3. Schematic layout of the setup. Only two DUTs out of 12 hosted by a single board are illustrated here for brevity.

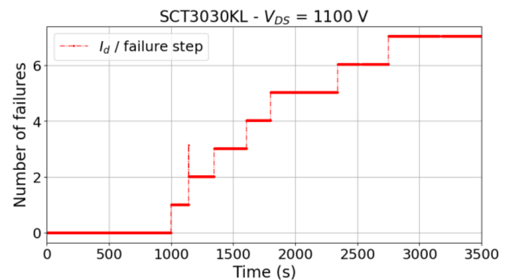

Fig. 4. Example of online measurement for Rohm devices (SCT3030KL) exposed at 1100 V. The drain current measured during the exposure is divided by the failure step size in order to highlight the number of failures during the run.

TABLE II
FAILURE ANALYSIS

Reference	Man.	$V_{DS\ irradiation}$ [V]	β	η [n/cm²]	Failed / Total DUT	σ_{SEB} [cm²]	MTBF [h]
C2M0025120D	Cree/ Wolfspeed	1100	0.70	3.31×10^{7}	6 / 13	2.39×10^{-8}	4.18×10^{7}
		976	0.67	9.43×10^{7}	11 / 20	8.04×10^{-9}	1.24×10^{8}
		846	0.97	1.47×10^{9}	8 / 18	6.71×10^{-10}	1.49×10^{9}
SCT3030KL	ROHM	1100	1.14	2.24×10^{9}	9 / 24	4.69×10^{-10}	2.13×10^{9}
		976	4.02	2.24×10^{9}	2 / 24	4.93×10^{-10}	2.03×10^{9}
MSC025SMA120B	Microsemi	1100	1.54	8.12×10^{5}	13 / 13	1.37×10^{-6}	7.31×10^{5}
		976	1.12	1.31×10^{7}	11 / 15	7.96×10^{-8}	1.26×10^{7}
		846	0.85	1.34×10^{8}	13 / 22	6.85×10^{-9}	1.46×10^{8}
SCTWA50N120	ST-Micr.	1100	0.85	4.33×10^{6}	19 / 20	2.13×10^{-7}	4.69×10^{6}
		976	1.05	1.13×10^{7}	17 / 22	9.06×10^{-8}	1.10×10^{7}
		846	1.04	9.32×10^{7}	15 / 24	1.09×10^{-8}	9.15×10^{7}
IMW120R090M1H	Infineon	1100	0.91	6.41×10^{7}	14 / 17	1.50×10^{-8}	6.67×10^{7}
		976	0.82	5.83×10^{8}	16 / 24	1.54×10^{-9}	6.49×10^{8}
		846	0.93	2.60×10^{9}	8 / 24	3.73×10^{-10}	2.68×10^{9}

was divided by the failure step size ($\Delta I_{DS} = 1.27\ mA$) in order to highlight the number of failures during the run.

For each reference, three irradiations were performed on pristine devices at V_{DS} of 1100 V, 976 V and 846 V, which are ~ 92 %, ~ 81 % and 72 % of the maximum rated voltage (1.2 kV) respectively. During the irradiation $V_{GS} = 0\ V$ to keep the device in off-state. The gate current was not monitored during the run. The test was stopped when 50% - 70% of devices failed or when a fluence of 2.8×10^{10} n/cm² was reached.

Some of the DUTs were characterized after the irradiation using a Keithley Parametric Curve Tracer PCT-4B in order to investigate the radiation-induced damage. In addition, breakdown voltage (BVdss) measurements were conducted using a Keithley SMU 2657A on the drain and a Keithley SMU 2636B on the gate and the source terminals. For a pristine device, the BV_{DSS} is the voltage at which the reverse-biased body-drift diode breaks down causing significant current to flow between source and drain due to the avalanche multiplication process.

III. Experimental Results

A. *Weibull distribution analysis and FIT rates*

In order to calculate the SEB cross-sections and the FIT rates, reliability parameters were determined using a standard 2-parameter Weibull distribution [23]. The cumulative fraction of failed devices was calculated as a function of the neutron fluence; a 2-parameter Weibull distribution was fit to the data using a maximum likelihood estimation (MLE) method [38]. Two parameters were extracted from this analysis: β, called the shape parameter, which is an indicator of the failure mechanism, and η, which is the scale parameter. Weibull distributions with β < 1 have an early-life failure, which decreases with time, while distributions with β > 1 have a failure rate that increases with time, also known as wear-out failures. For stochastic neutron failures $\beta = 1$ is expected, as representative of random events. The mean time between failures (MTBF) and the SEB cross-sections (σ_{SEB}) were calculated as (1):

$$MTBF = \eta \times \Gamma\left(1 + \frac{1}{\beta}\right) \text{ when } \beta \neq 1$$
$$MTBF = \eta \text{ when } \beta = 1 \quad (1)$$
$$\sigma_{SEB} = \frac{1}{MTBF}$$

The error bars were calculated considering a Poisson distribution dominated by the count statistics. The uncertainty over the fluence was considered negligible with respect to the number of events. The upper and lower limits were calculated as in (2), where N_{low} and N_{high} were obtained from the chi-square distribution with a confidence level of 95%:

$$Err_{high} = \frac{N_{high}}{N_{SEB} * MTBF}$$
$$Err_{low} = \frac{N_{low}}{N_{SEB} * MTBF} \quad (2)$$

The FIT rates were calculated considering 10^{9} h of operations and a cosmic-ray-induced neutron flux of 13 n/(cm² h) for energies above 10 MeV (reference conditions at sea level in NYC from JEDEC JESD89A standard). The same conversion factor was used also for the error bars as described above for cross-sections.

In Table II the parameters extracted from the analysis are listed for the tested references. In the case of Rohm, the tests were performed only at 1100 V and 976 V. In some runs, multiple SEBs were observed at the same time. For the analysis, they were considered as a single event, in order to assure the independence between the SEB events. Therefore, the total number of tested DUTs was reduced.

The failure cross-sections are shown in Fig. 5 (a) as a function of the bias during the irradiation. In Fig. 5 (b) the FIT rates are shown for the tested references, while in Fig. 5 (c) the FIT rates are normalized with the active area and scaled by the avalanche breakdown voltage, such that a ratio of 1 would indicate that the critical field was reached. This approach was

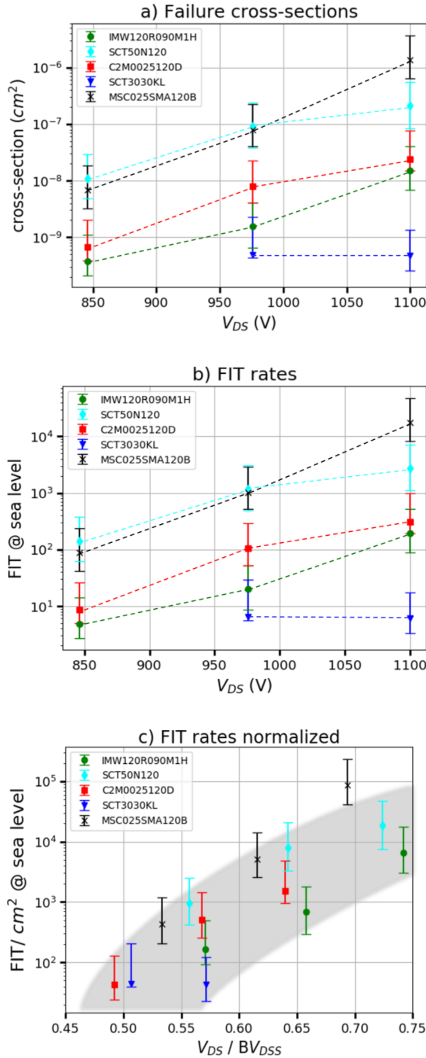

Fig. 5. a) Failure cross-sections of SiC MOSFETs from different suppliers as a function of the bias during the terrestrial neutron irradiations. b) FIT rates for 10^9 hours of operation. c) FIT rates scaled by avalanche voltage and normalized with the active area.

suggested and previously discussed in [9]. A common trend is observed for all the devices and highlighted by the gray shadow. The trench MOSFETs (i.e., IMW120R090M1H and SCT3030KL) appear to have lower FIT rates if compared to the planar architecture. In particular, the double-trench device (SCT3030KL), which has the highest avalanche breakdown voltage, has the best performance.

B. Post-irradiation measurements: breakdown voltage

Post-irradiation measurements were performed for some devices, which showed more or less severe effects depending on the technology. In this and the following sections, the measurements are discussed for the three tested architectures: planar gate from Cree/Wolfspeed (i.e., C2M0025120D), trench gate from Infineon (i.e., IMW120R090M1H) and double trench from Rohm (i.e., SCT3030KL). As an example, the results are compared for the references tested at 976 V. BV_{DSS} measurements of the irradiated devices were performed at $V_{GS} = 0\,V$ and stopped at the V_{DS} corresponding to $I_D = 1.00\,mA$, which is defined as the breakdown voltage. At this current level, the device is still protected from a permanent breakdown of the body diode. Three different responses were identified for all the studied references: i) no damage observed with respect to a pristine device; ii) partial degradation of the device, which exhibited higher gate and drain leakage currents; iii) ohmic trend of the leakage current caused by SEB. Examples of the leakage currents (I_D, I_G and I_S) are reported as a function of the drain-source bias (V_{DS}) for the three references in Fig. 6. The top and the bottom panels show respectively the measurements for the i) and the ii) scenarios described above. A measurement of a pristine device for each reference is given in gray for comparison. In Fig. 6 (a), (b), (c), the measurements are all in the same range as the pristine device, and the small differences observed are caused by part-to-part variation (i.e., the pristine device is not the same part as the irradiated one, but belongs to the same lot). For these devices, no damage was induced by the neutron exposure and no leakage current increase is observed, neither degradation of the blocking capability of the MOSFETs. Differently, a clear degradation was induced by the neutron exposure in the devices reported in Fig. 6 (d), Fig. 6 (e) and Fig. 6 (f). The leakage currents are orders of magnitudes higher with respect to the pristine level for all the three devices, however, the current paths (drain-to-gate vs drain-to-source contributions) differ among them.

Finally, the measurements for (iii) are not reported, but from the ohmic trend of the leakage current, it was concluded that the devices failed through an SEB during the exposure.

C. Post-irradiation measurements: gate damage

In order to investigate the different leakage path observed for (ii), I_D-V_{GS} and I_G-V_{GS} measurements were performed at $V_{DS} = 1$ V. The results are presented in Fig. 7, which shows that the gate oxide is still operable for the planar device (C2M0025120D) and the channel is still controlled by the gate voltage, but the gate leakage is higher with respect to the pristine level. The device exhibits a partial gate rupture with very high gate and drain leakage current and a gate-drain current path. This effect is similar to the degradation induced by heavy-ion exposure (i.e., SELC), previously reported in [18-19]. Conversely, repeating the measurement for the double-trench (SCT3030KL) and the trench (IMW120R090M1H) devices, the gate oxide was found to be heavily damaged and not operable anymore. Indeed, the channel is in off-state for these devices and no positive drain current flows. From these observations, it was concluded that the damage in the trench devices has the signature of a complete gate rupture.

D. Latent damage: PIGS test

Even though a device may not show any measurable damage during the irradiation, as for category (i), the integrity of its gate oxide might be affected. In order to study the effect of latent

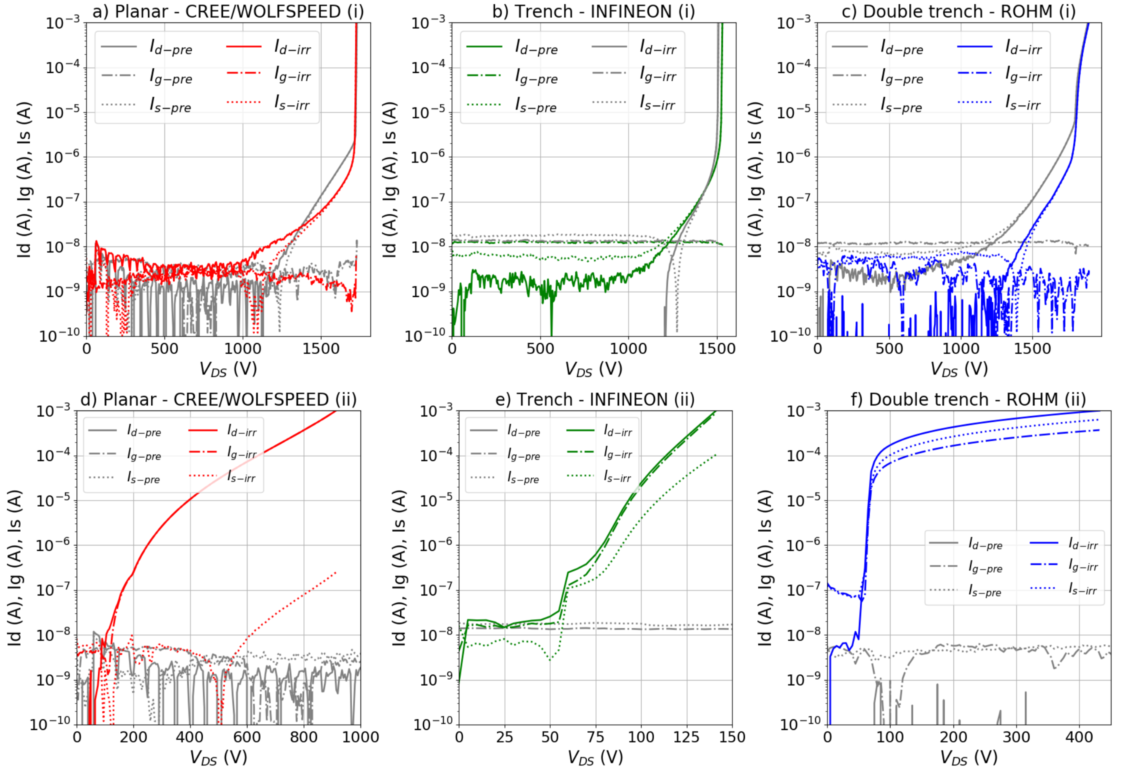

Fig. 6. Different responses were observed in the devices exposed to neutrons: i) no failure observed and no damage with respect to a pristine device, as in a), b) and c); ii) no failure observed, but partial degradation of the device, as in d), e), and f). The measurements of the leakage currents (I_D, I_G, I_S) were performed at $V_{GS} = 0\ V$ and with a maximum I_D current of 1 mA.

damage on the gate oxide integrity and on the blocking capability, breakdown voltage measurements were repeated after applying positive and negative voltage bias at the gate oxide, following the PIGS test as recommended in MIL-STD-750, test method 1080 [31]. The V_{GS} was first swept positively up to the rated value for each reference (i.e., +15 V for Cree/Wolfspeed, +18 V for Infineon and + 22 V for Rohm) or until a leakage current of 1 mA was measured. Secondly, a $V_{GS} = -5\ V$ was then applied at the gate oxide. The results are shown in Fig. 8 (a), (b), and (c) for the three devices discussed before in Fig. 6 (a), (b), and (c) respectively, which did not exhibit any measurable damage after the exposure (i). No difference was observed in the breakdown point and in the leakage currents after these cycles. The small differences in the gate leakage current might be due to the instrument sensitivity. Hence, these devices are operable after the neutron irradiation, the leakage current is still within the specification (i.e., $I_G < 100\ nA$) and no latent damage is observed after applying the gate bias.

However, for the degraded device (ii) previously presented in Fig. 6 (d), after the stress at negative V_{GS}, the I_S decreased, meaning that higher current is flowing to the drain-gate path, rather than into the source pad, as shown in Fig. 8. (d). This is evidence of an increased gate damage induced by the negative gate bias.

IV. Discussion

From the results presented, three different scenarios where commonly observed for the different architectures analysed. Considering the FIT normalized with the active area and scaled by the breakdown voltage, the trench devices showed a better performance to SEB with respect to the planar ones, with the double-trench architecture as the most robust. However, part of the trench and double-trench devices exhibited a complete gate rupture. Conversely, a partial gate rupture was observed for the planar reference analysed, which exhibited a current leakage path between gate and drain as previously observed for planar gate devices suffering from SELC after heavy-ion irradiation. Additionally, for the device with the gate partially ruptured, the gate damage increased after the PIGS test, which was already reported for devices suffering from SELC after heavy-ion experiments [39].

A model for an enhanced gate current associated with a leakage was previously presented for Si devices and heavy-ion irradiation. It states that the oxide defects from displacement damage caused by the ions create a significant number of damage sites at which there is a reduced potential barrier, permitting the tunneling of electrons from trapping sites in the oxide into the conduction band [40]. Similarly, a model for early defects in SiO_2/SiC was discussed in [41] and attributed

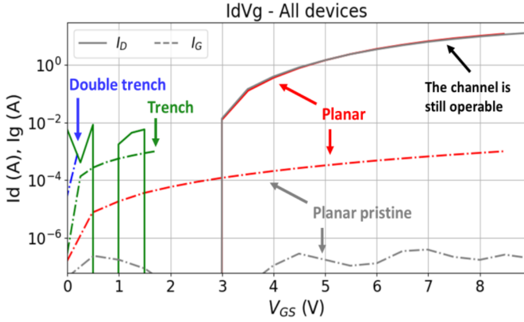

Fig. 7. I_D-V_{GS} and I_G-V_{GS} measurements performed at V_{DS} = 1 V. The gate oxide is still operable for the planar Cree/Wolfspeed device (C2M0025120D) and the channel is still controlled by the gate voltage. Conversely, the gate oxide is heavily damaged and not operable anymore for the trench and double-trench structures.

to the presence of defects in the oxide bulk. It is hypothesized that, through displacement damage, neutrons are inducing defects in the gate oxide, which are responsible of the increased gate leakage current. Furthermore, the density and distribution of oxide defects in a pristine device depend on the oxide process and can be considered as a by-product of the SiO_2 oxide growth on SiC, therefore different among devices produced by different manufacturers.

Finally, it should be noted that the setup used during the experiment was counting as a failure event all the devices whose I_D leakage current in off-state exceeded 1.27 mA. Therefore, the FITs and the failure cross-section analysis includes both the failure mechanism indicated as SEB (iii) and degradation with partial or complete gate rupture (ii), with the latter also considered not operable from an application point of view due to the very high leakage currents.

V. Conclusions

Results from accelerated terrestrial neutron experiments were presented for different commercial SiC technologies with planar, trench and double-trench architectures.

Different failure mechanisms were observed from the post-irradiation analysis of the irradiated devices, and three different responses were commonly identified for each of the three architectures: (i) no damage observed with respect to a pristine device, (ii) partial degradation of the device, which exhibited high leakage currents, (iii) SEB (i.e., ohmic trend of the leakage current). Categories (ii) and (iii) were considered failed devices from an application point of view. Failure cross-sections and FIT rates were calculated for these devices. MOSFETs with a trench structure appear to be less sensitive to neutron-induced failures with respect to the planar ones. The double trench-architecture, which has also the higher breakdown voltage, was observed to be the most robust.

Examples were reported and discussed for the degraded devices (ii) and the impact of gate rupture was discussed for the three designs. The planar-gate architecture exhibited a partial gate rupture mechanism, probably induced by displacement

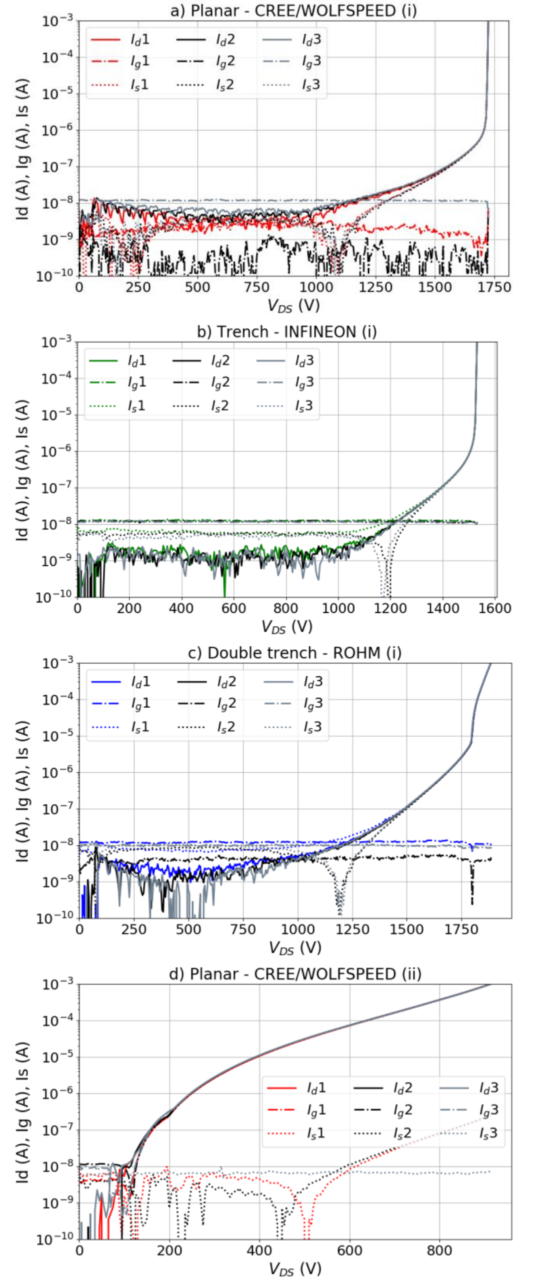

Fig. 8. Breakdown voltage measurements after the post irradiation gate stress (PIGS) test. The results are reported for the planar (a), trench (b) and double-trench (c) DUTs, which did not show any damage during the exposure (i), and for the planar DUT (d) which was partially degraded (ii). The first cycle reports the measurement just after the irradiation, while the second and the third represent the measurements repeated after applying a positive V_{GS} up to the rated voltage and a negative V_{GS} of -5 V, respectively.

damage and characterized by very high leakage currents with a gate-drain current path. This effect was observed to be similar to the SELC degradation induced by heavy-ions, already discussed for the same reference, but reported here for neutron irradiation. The trench and double-trench architecture, instead, appeared to be more sensitive to a complete gate rupture.

However, it should be clearly stated that the experiments were performed using a specific device type from each manufacturer. Both the design as well as the resulting efficient carrier concentration in the specific areas will vary between device types and generation from the same manufacturer; therefore, the results cannot be extrapolated to all SiC power devices without further analysis.

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Publication IV

C. Martinella, P. Natzke, R. G. Alia, Y. Kadi, M. Rossi, J. Jaatinen, H. Kettunen, U. Grossner, A. Javanainen, "Heavy-ion Induced Single Event Effects and Latent Damages in SiC Power MOSFETs", submitted for publication to *Microelectron. Reliab.*, Jun. 2021

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