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Impact of Terrestrial Neutrons on the Reliability of SiC VD-MOSFET Technologies

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***Abstract*—Accelerated terrestrial neutron irradiations were performed on different commercial SiC power MOSFETs with planar, trench and double-trench architectures. The results were used to calculate the failure cross-sections and the failure in time (FIT) rates at sea level. Enhanced gate and drain leakage were observed in some devices which did not exhibit a destructive failure during the exposure. In particular, a different mechanism was observed for planar and trench gate MOSFETs, the first showing a partial gate rupture with a leakage path mostly between drain and gate, similar to what was previously observed with heavy-ions, while the second exhibiting a complete gate rupture. The observed failure mechanisms and the post irradiation gate stress (PIGS) tests are discussed for the different technologies.**

***Index Terms*— Silicon Carbide, Power MOSFETs, neutrons, Single Event Effects, Single Event Burnout, gate damage**

I. Introduction

Wide bandgap materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) have gained popularity in recent years. Between them, SiC is the most mature technology and has become a viable alternative to Silicon-based power devices in high-efficiency and high-power density applications [1-2]. The higher breakdown field and thermal conductivity make SiC a very attractive material for different ground applications, such as automotive and solar inverters, but also for the avionics and space industries [3-4]. Moreover, SiC is considered as a promising technology for accelerator applications [5-6]. However, SiC devices are known to be susceptible to Single Event Burnout (SEB), Single Event Gate Rupture (SEGR) and Single Event Leakage Current (SELC). SEB and SEGR are caused, among others, by high-energy neutrons [7-15], while SELC has been reported only with heavy-ions [16-20].

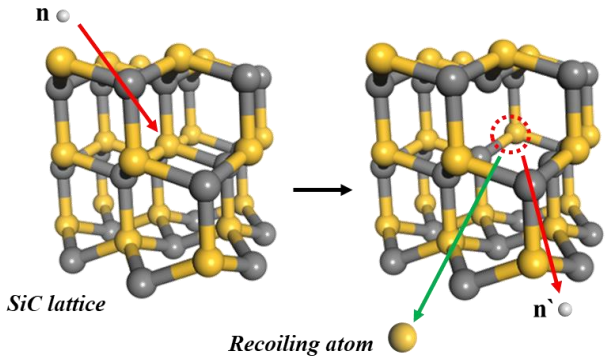

Fig. 1. By the elastic and inelastic scattering with the 4H-SiC lattice, the atmospheric neutrons produce recoiling atoms (i.e., α, C, Si, Mg, Al) which generate ionizing tracks inside the power MOSFET.

The high-energy neutrons originate from cosmic ray interactions with the atmosphere. These include solar event particles (SEPs) originated by dynamic solar activity and galactic cosmic rays (GCRs) created by events outside the solar system, such as the explosion of galactic nuclei and supernova, pulsars and stellar flares [21-23]. These particles (i.e., 92% protons, 6% alpha particles and 2% heavier atomic nuclei) are responsible for Single Event Effects (SEEs) observed in electronics used in space. The particles that are not deviated or trapped by the magnetic field enter the Earth's atmosphere and, upon interacting with, e.g., oxygen and nitrogen atoms, create a shower of secondary particles. These interactions result in neutrons, protons, muons, pions and electromagnetic waves [22]. Some particles decay or are absorbed, while others travel further in the atmosphere, causing a cascade through spallation reactions. Due to the charge neutrality and the abundance, this gives rise to a high flux of secondary neutrons traveling vast distances in the atmosphere. The peak of neutron intensity occurs at about 10-25 km, which is critical for avionic applications, being the altitude of many commercial airplane flights [21]. Below, there is a net loss of total particles in the cascades, having a flux which drops two orders of magnitude at sea level, with a neutron flux of less than 25 n/(cm^{2}h) for energies higher than 1 MeV [22]. Data centers and the Si power electronics community have reported failures and upsets at sea

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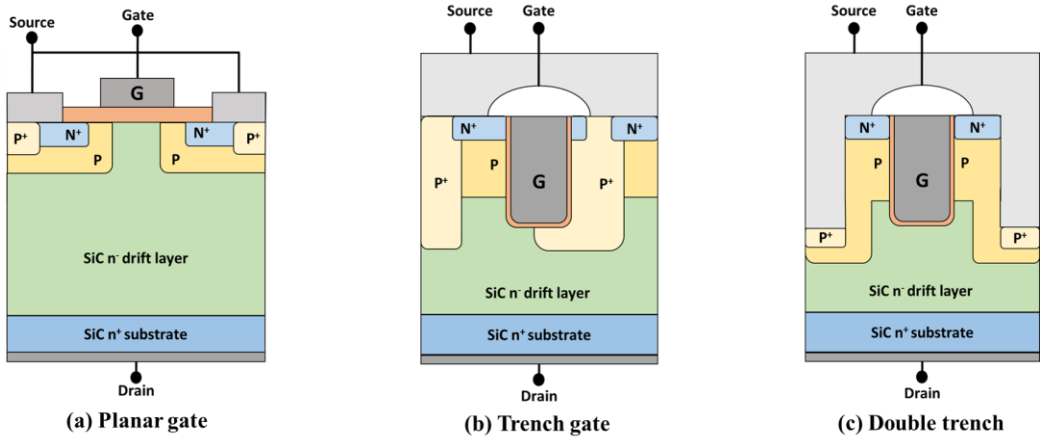

Fig. 2. Schematics of the three architectures of SiC power MOSFETs tested in this work: (a) planar gate, (b) trench gate from Infineon and (c) double trench (trench source and trench gate) from Rohm. Picture remake after the original from Siemieniec *et al.* [30].

level [24-27]. Additionally, due to the exponential increase of neutron flux with increasing altitudes, problems can be encountered for applications at higher altitudes, for example on a mountain top [23].

Furthermore, neutrons can cause issues for electronic systems installed in high-energy accelerators, such as the Large Hadron Collider (LHC) complex and its future upgrade High Luminosity LHC (HL-LHC) at CERN, Geneva [28]. Here, commercial SiC power MOSFETs have been considered for the design of a prototype inductive adder (IA) to be used as a pulse generator for the injection kicker magnets [5-6].

The physics of neutron induced SEB in SiC power devices has been previously studied, and an explanation for this destructive effect was suggested in [7]. Although neutrons are non-ionizing particles, the recoiling atoms, generated from their elastic or inelastic scattering with the lattice atoms, can indirectly give rise to ionization and create a large number of electron and hole (e–h) pairs along their trajectories. This event is followed by a hole impact ionization with associated multiplication factors and a consequent thermal transient and excessive lattice temperatures. This leads to local lattice sublimation and formation of voids, resulting in the loss of device blocking ability, hence a destructive failure. A schematic of the neutron interaction with the 4H-SiC lattice is shown in Fig. 1. Finally, it was reported that no consistent differences have been observed in the SEB tolerance for SiC MOSFETs and SiC diodes [8]. This supports the hypothesis that the conventional mechanisms underlying SEB in Si MOSFETs, such as parasitic bipolar junction transistor (BJT) and tunneling assisted avalanche multiplication mechanisms [29], may be suppressed in SiC devices, where the current gain of the parasitic BJT is lower. Indeed, there is no similar parasitic BJT structure in the diode design.

In this work, we investigate the effect of neutron irradiation on different commercial SiC power MOSFETs produced by different manufacturers. The devices were selected with three different types of design: planar gate, trench gate and double trench, where the last has a trench gate and source [30]. The schematics of the three architectures are shown in Fig. 2. The radiation sensitivity is discussed for the different technologies. Experiments were performed at ChipIr, the beamline at the Rutherford Appleton Laboratory (U.K.) providing an atmospheric-like neutron environment. During the irradiations, destructive failures were observed and the failure cross-sections and FIT rates are presented for the tested references. Additionally, from the post-irradiation analysis, the latent damage and the impact of gate rupture in planar and trench gate design are discussed highlighting the differences among these device types and the dependence of the failure type on the technology. Finally, the results for the post-irradiation gate stress (PIGS), performed as recommended by the MIL-STD-750, test method 1080 [31], are also presented.

II. Neutron Irradiation Experiment

A. The ChipIr terrestrial neutron facility

ChipIr is a beamline built at the second target station (TS2) of the ISIS spallation source at the Rutherford Appleton Laboratory, UK [32-34]. The facility is specifically tailored for testing radiation effects on electronic components and systems. The beamline design is optimized to mimic the atmospheric neutron spectrum (up to 800 MeV) with an acceleration factor of up to 10^9 for ground-level applications. The neutrons delivered to the ChipIr facility are emitted from the spallation of high-energy protons with a tungsten target (i.e., 800 MeV protons extracted from the synchrotron with beam current of 40 μA and pulsed at 10 Hz). The neutrons are delivered to ChipIr according to the time structure of the ISIS source, i.e., in 10 Hz pulses, with two 70-ns-wide bunches separated 360 ns apart. A silicon diode, placed in front of the testing position, measures the energy distribution of single pulses. This is used to retrieve the neutron fluence at the device under test (DUT) location knowing the detection efficiency and, by means of a correction factor function of the distance between the diode and the DUT position, which takes into account the beam divergence. During the test campaign, the measured flux of neutrons above 10 MeV was 5.6 x 10^6 $cm^{-2}s^{-1}$ at the testing position. A collimator system allows for selecting beams of different sizes. For the current experiment, a beam size of 10 cm x 10 cm was used.

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TABLE I
LIST OF DEVICES UNDER TEST

Reference	Man.	$R_{DS(on)}$ [mΩ]	V_{DS} [kV]	$I_{D\ @\ 25^{\circ}}$ [A]	BV_{DSS} [kV]	Gate	#DUTs
C2M0025120D	Cree/ Wolfspeed	25	1.2	250	1720	planar	51
SCT3030KL	Rohm	30	1.2	180	1926	double trench	48
MSC025SMA120B	Microsemi	25	1.2	275	1586	planar	50
SCTWA50N120	ST-Micr.	59	1.2	130	1520	planar	66
IMW120R090M1H	Infineon	90	1.2	50	1483	trench	65

B. *Experimental method*

The aim of this study is to investigate the effect of atmospheric-like neutrons on different commercial SiC MOSFET technologies. Accelerated testing of Single Event Burnout (SEB) by using terrestrial neutrons was performed. The obtained data were used to calculate the effect cross sections and failure in time (FIT) rates at ground level. Additionally, the devices that did not exhibit destructive failure during exposure were characterized and their operational reliability was studied.

Several samples were selected from the commercially available SiC VD-MOSFET technologies. The references and the corresponding technical information are listed in Table I. All the devices are rated for 1.2 kV and they are mounted in a TO-247 package. The devices were irradiated in their original packaging. The first three devices were selected with similar values of $R_{DS\ (ON)}$ among them, and the same was done for the last two devices. The references were selected with different design: planar, trench and double trench. In particular, the DUTs from Infineon have a trench gate structure [35], whereas the Rohm have a double trench design, with trench gate and trench source. For the trench gate devices, the channel is formed vertically, which allows the current to flow vertically while reducing the $R_{DS(ON)}$ [36]. All the other references have a planar gate structure.

The test setup was designed following the military standard specifications (MIL-STD-750E M1080.1) [31]. Each test board can host a maximum of 12 devices in parallel. A schematic layout of the setup is presented in Fig. 3, where two DUTs are illustrated for brevity. Two boards were stacked to test up to 24 DUTs for each run. They were installed at a distance of 58 cm and 76 cm from the beam aperture, respectively. The attenuation of the neutron beam in the first board was estimated to be negligible for the material used in the tested boards [37]. Two Keithley Source Measurement Unit (SMU) model 2410s (one channel, up to 1100 V), one for each board, were used to bias the drain and to monitor the total leakage currents as a sum of all devices. The gates were grounded directly on the board. A stiffening capacitor of 10 nF was installed between the drain and the ground for each DUT, in order to supply sufficient amount of charge during a destructive event. Moreover, it also

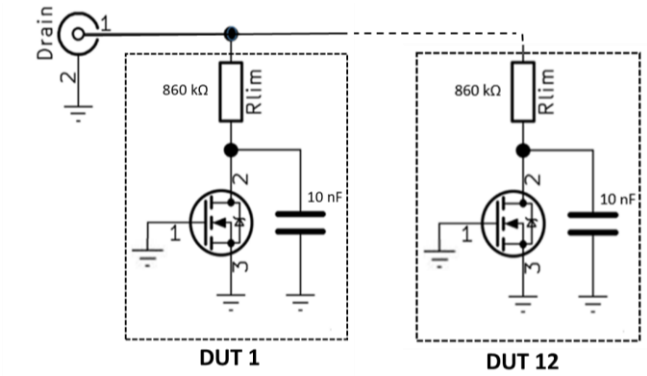

Fig. 3. Schematic layout of the setup. Only two DUTs out of 12 hosted by a single board are illustrated here for brevity.

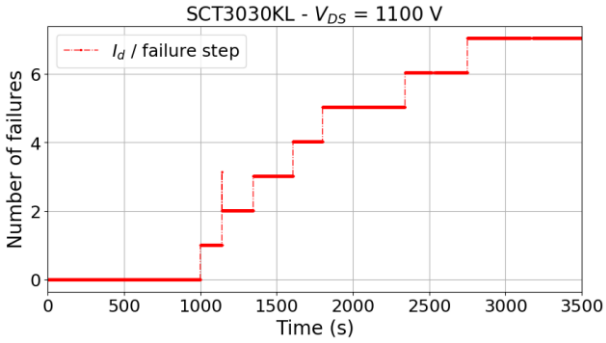

Fig. 4. Example of online measurement for Rohm devices (SCT3030KL) exposed at 1100 V. The drain current measured during the exposure is divided by the failure step size in order to highlight the number of failures during the run.

limited the momentary voltage drop at the SMU output during current transients. The devices were connected in parallel to the high voltage, but each of them had an individual current limiting resistor of 860 kΩ between the drain and the SMU output. This guaranteed the isolation of the device after a failure and the continuous application of high voltage to all other devices. Each step increase in the total current measured by the SMU was accounted as a failure ($\Delta I_{DS} = 1.27\ mA$). This value corresponds to a short circuit on the DUT and the total voltage is applied across the protection resistor. In Fig. 4 an example of the online measurements recorded during an exposure run is shown. The results are presented for Rohm SCT3030KL devices exposed at 1100 V. Here, the measured drain current

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TABLE II
FAILURE ANALYSIS

Reference	Man.	$V_{DS\ irradiation}$ [V]	β	η [n/cm^2]	Failed / Total DUT	σ_{SEB} [cm^2]	MTBF [h]
C2M0025120D	Cree/ Wolfspeed	1100	0.70	3.31 x 10^7	6 / 13	2.39 x 10^{-8}	4.18 x 10^7
		976	0.67	9.43 x 10^7	11 / 20	8.04 x 10^{-9}	1.24 x 10^8
		846	0.97	1.47 x 10^9	8 / 18	6.71 x 10^{-10}	1.49 x 10^9
SCT3030KL	ROHM	1100	1.14	2.24 x 10^9	9 / 24	4.69 x 10^{-10}	2.13 x 10^9
		976	4.02	2.24 x 10^9	2 / 24	4.93 x 10^{-10}	2.03 x 10^9
MSC025SMA120B	Microsemi	1100	1.54	8.12 x 10^5	13 / 13	1.37 x 10^{-6}	7.31 x 10^5
		976	1.12	1.31 x 10^7	11 / 15	7.96 x 10^{-8}	1.26 x 10^7
		846	0.85	1.34 x 10^8	13 / 22	6.85 x 10^{-9}	1.46 x 10^8
SCTWA50N120	ST-Micr.	1100	0.85	4.33 x 10^6	19 / 20	2.13 x 10^{-7}	4.69 x 10^6
		976	1.05	1.13 x 10^7	17 / 22	9.06 x 10^{-8}	1.10 x 10^7
		846	1.04	9.32 x 10^7	15 / 24	1.09 x 10^{-8}	9.15 x 10^7
IMW120R090M1H	Infineon	1100	0.91	6.41 x 10^7	14 / 17	1.50 x 10^{-8}	6.67 x 10^7
		976	0.82	5.83 x 10^8	16 / 24	1.54 x 10^{-9}	6.49 x 10^8
		846	0.93	2.60 x 10^9	8 / 24	3.73 x 10^{-10}	2.68 x 10^9

was divided by the failure step size ($\Delta I_{DS} = 1.27\ mA$) in order to highlight the number of failures during the run.

For each reference, three irradiations were performed on pristine devices at V_{DS} of 1100 V, 976 V and 846 V, which are ~ 92 %, ~ 81 % and 72 % of the maximum rated voltage (1.2 kV) respectively. During the irradiation $V_{GS} = 0\ V$ to keep the device in off-state. The gate current was not monitored during the run. The test was stopped when 50% - 70% of devices failed or when a fluence of 2.8 x 10^{10} n/cm^2 was reached.

Some of the DUTs were characterized after the irradiation using a Keithley Parametric Curve Tracer PCT-4B in order to investigate the radiation-induced damage. In addition, breakdown voltage (BVdss) measurements were conducted using a Keithley SMU 2657A on the drain and a Keithley SMU 2636B on the gate and the source terminals. For a pristine device, the BV_{DSS} is the voltage at which the reverse-biased body-drift diode breaks down causing significant current to flow between source and drain due to the avalanche multiplication process.

III. Experimental results

A. Weibull distribution analysis and FIT rates

In order to calculate the SEB cross-sections and the FIT rates, reliability parameters were determined using a standard 2-parameter Weibull distribution [23]. The cumulative fraction of failed devices was calculated as a function of the neutron fluence; a 2-parameter Weibull distribution was fit to the data using a maximum likelihood estimation (MLE) method [38]. Two parameters were extracted from this analysis: β, called the shape parameter, which is an indicator of the failure mechanism, and η, which is the scale parameter. Weibull distributions with $\beta < 1$ have an early-life failure, which decreases with time, while distributions with $\beta > 1$ have a failure rate that increases with time, also known as wear-out failures. For stochastic neutron failures $\beta = 1$ is expected, as representative of random events. The mean time between failures (MTBF) and the SEB cross-sections (σ_{SEB}) were calculated as (1):

$$MTBF = \eta \times \Gamma\left(1 + \frac{1}{\beta}\right) \text{ when } \beta \neq 1$$
$$MTBF = \eta \text{ when } \beta = 1 \qquad (1)$$
$$\sigma_{SEB} = \frac{1}{MTBF}$$

The error bars were calculated considering a Poisson distribution dominated by the count statistics. The uncertainty over the fluence was considered negligible with respect to the number of events. The upper and lower limits were calculated as in (2), where N_{low} and N_{high} were obtained from the chi-square distribution with a confidence level of 95%:

$$Err_{high} = \frac{N_{high}}{N_{SEB} * MTBF}$$
$$Err_{low} = \frac{N_{low}}{N_{SEB} * MTBF} \qquad (2)$$

The FIT rates were calculated considering 10^9 h of operations and a cosmic-ray-induced neutron flux of 13 n/(cm^2 h) for energies above 10 MeV (reference conditions at sea level in NYC from JEDEC JESD89A standard). The same conversion factor was used also for the error bars as described above for cross-sections.

In Table II the parameters extracted from the analysis are listed for the tested references. In the case of Rohm, the tests were performed only at 1100 V and 976 V. In some runs, multiple SEBs were observed at the same time. For the analysis, they were considered as a single event, in order to assure the independence between the SEB events. Therefore, the total number of tested DUTs was reduced.

The failure cross-sections are shown in Fig. 5 (a) as a function of the bias during the irradiation. In Fig. 5 (b) the FIT rates are shown for the tested references, while in Fig. 5 (c) the FIT rates are normalized with the active area and scaled by the avalanche breakdown voltage, such that a ratio of 1 would indicate that the critical field was reached. This approach was

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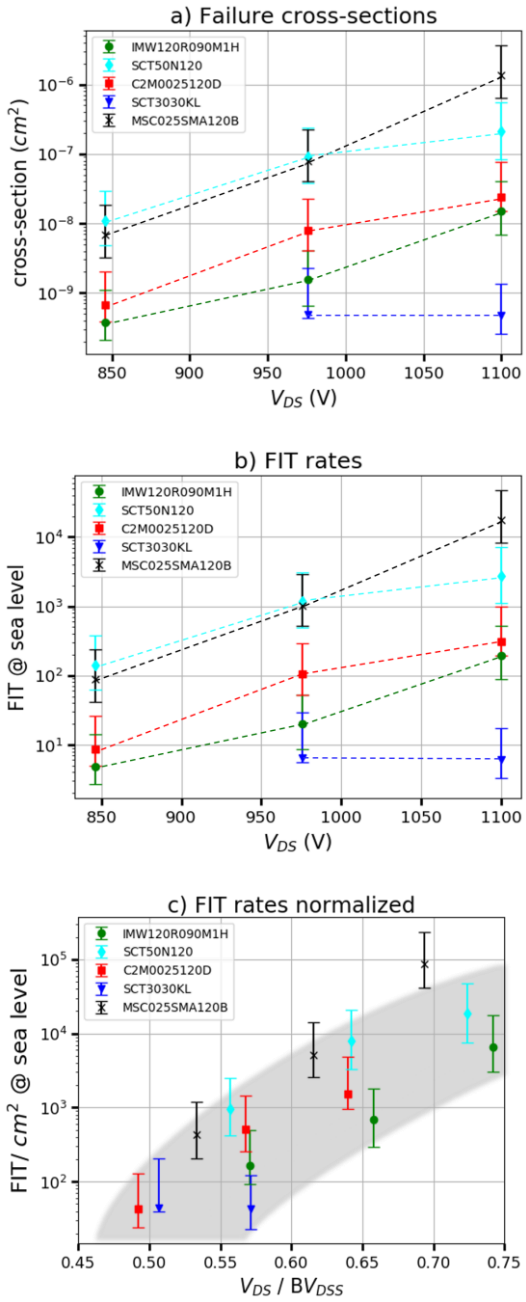

Fig. 5. a) Failure cross-sections of SiC MOSFETs from different suppliers as a function of the bias during the terrestrial neutron irradiations. b) FIT rates for 10^9 hours of operation. c) FIT rates scaled by avalanche voltage and normalized with the active area.

suggested and previously discussed in [9]. A common trend is observed for all the devices and highlighted by the gray shadow. The trench MOSFETs (i.e., IMW120R090M1H and SCT3030KL) appear to have lower FIT rates if compared to the planar architecture. In particular, the double-trench device (SCT3030KL), which has the highest avalanche breakdown voltage, has the best performance.

B. Post-irradiation measurements: breakdown voltage

Post-irradiation measurements were performed for some devices, which showed more or less severe effects depending on the technology. In this and the following sections, the measurements are discussed for the three tested architectures: planar gate from Cree/Wolfspeed (i.e., C2M0025120D), trench gate from Infineon (i.e., IMW120R090M1H) and double trench from Rohm (i.e., SCT3030KL). As an example, the results are compared for the references tested at 976 V. BV_{DSS} measurements of the irradiated devices were performed at $V_{GS} = 0\,V$ and stopped at the V_{DS} corresponding to $I_D = 1.00\,mA$, which is defined as the breakdown voltage. At this current level, the device is still protected from a permanent breakdown of the body diode. Three different responses were identified for all the studied references: i) no damage observed with respect to a pristine device; ii) partial degradation of the device, which exhibited higher gate and drain leakage currents; iii) ohmic trend of the leakage current caused by SEB. Examples of the leakage currents (I_D, I_G and I_S) are reported as a function of the drain-source bias (V_{DS}) for the three references in Fig. 6. The top and the bottom panels show respectively the measurements for the i) and the ii) scenarios described above. A measurement of a pristine device for each reference is given in gray for comparison. In Fig. 6 (a), (b), (c), the measurements are all in the same range as the pristine device, and the small differences observed are caused by part-to-part variation (i.e., the pristine device is not the same part as the irradiated one, but belongs to the same lot). For these devices, no damage was induced by the neutron exposure and no leakage current increase is observed, neither degradation of the blocking capability of the MOSFETs. Differently, a clear degradation was induced by the neutron exposure in the devices reported in Fig. 6 (d), Fig. 6 (e) and Fig. 6 (f). The leakage currents are orders of magnitudes higher with respect to the pristine level for all the three devices, however, the current paths (drain-to-gate vs drain-to-source contributions) differ among them.

Finally, the measurements for (iii) are not reported, but from the ohmic trend of the leakage current, it was concluded that the devices failed through an SEB during the exposure.

C. Post-irradiation measurements: gate damage

In order to investigate the different leakage path observed for (ii), I_D-V_{GS} and I_G-V_{GS} measurements were performed at V_{DS} = 1 V. The results are presented in Fig. 7, which shows that the gate oxide is still operable for the planar device (C2M0025120D) and the channel is still controlled by the gate voltage, but the gate leakage is higher with respect to the pristine level. The device exhibits a partial gate rupture with very high gate and drain leakage current and a gate-drain current path. This effect is similar to the degradation induced by heavy-ion exposure (i.e., SELC), previously reported in [18-19]. Conversely, repeating the measurement for the double-trench (SCT3030KL) and the trench (IMW120R090M1H) devices, the gate oxide was found to be heavily damaged and not operable anymore. Indeed, the channel is in off-state for these devices and no positive drain current flows. From these observations, it was concluded that the damage in the trench devices has the signature of a complete gate rupture.

D. Latent damage: PIGS test

Even though a device may not show any measurable damage during the irradiation, as for category (i), the integrity of its gate oxide might be affected. In order to study the effect of latent

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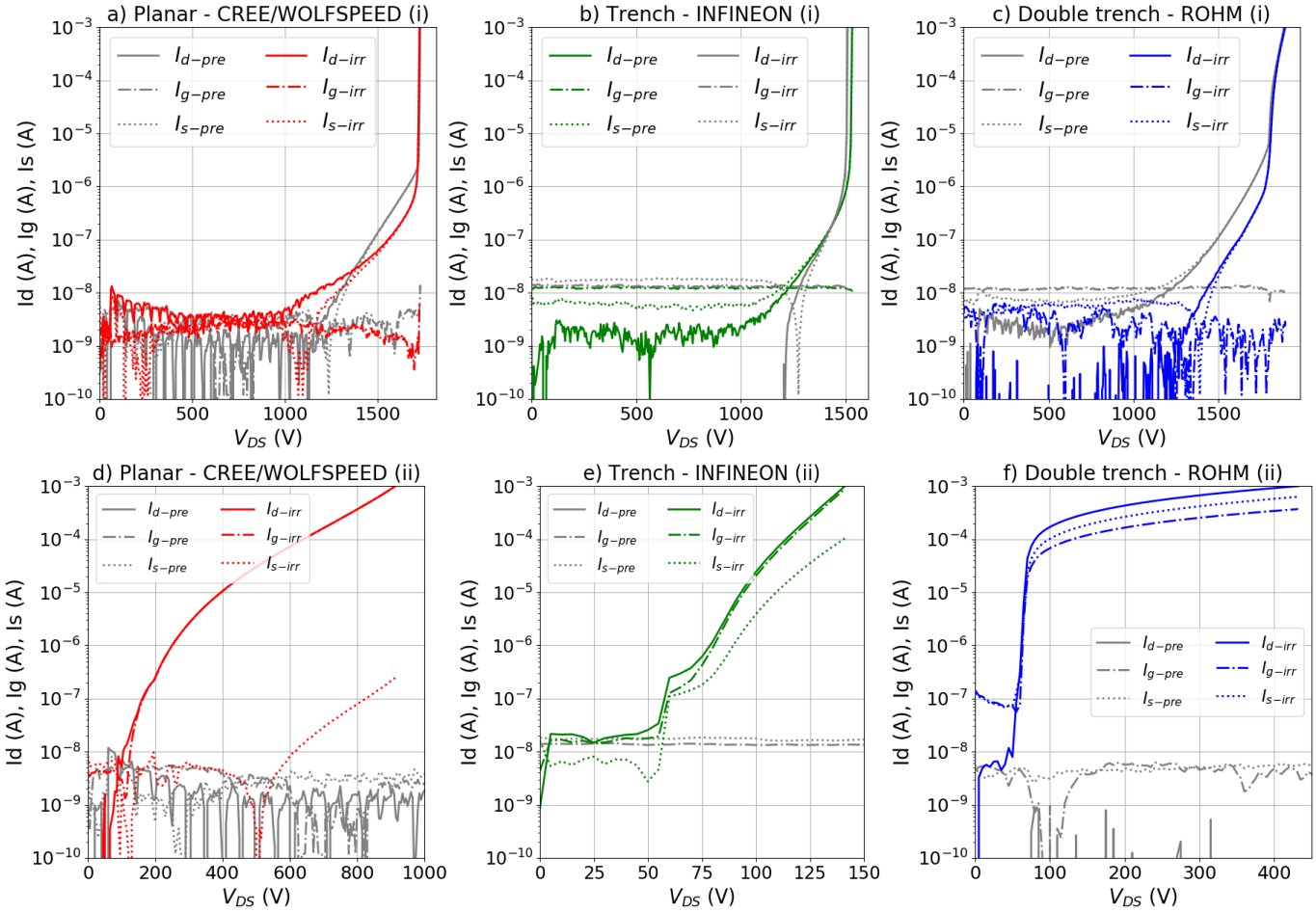

Fig. 6. Different responses were observed in the devices exposed to neutrons: i) no failure observed and no damage with respect to a pristine device, as in a), b) and c); ii) no failure observed, but partial degradation of the device, as in d), e), and f). The measurements of the leakage currents (I_D, I_G, I_S) were performed at $V_{GS} = 0\ V$ and with a maximum I_D current of 1 mA.

damage on the gate oxide integrity and on the blocking capability, breakdown voltage measurements were repeated after applying positive and negative voltage bias at the gate oxide, following the PIGS test as recommended in MIL-STD-750, test method 1080 [31]. The V_{GS} was first swept positively up to the rated value for each reference (i.e., +15 V for Cree/Wolfspeed, +18 V for Infineon and + 22 V for Rohm) or until a leakage current of 1 mA was measured. Secondly, a $V_{GS} = -5\ V$ was then applied at the gate oxide. The results are shown in Fig. 8 (a), (b), and (c) for the three devices discussed before in Fig. 6 (a), (b), and (c) respectively, which did not exhibit any measurable damage after the exposure (i). No difference was observed in the breakdown point and in the leakage currents after these cycles. The small differences in the gate leakage current might be due to the instrument sensitivity. Hence, these devices are operable after the neutron irradiation, the leakage current is still within the specification (i.e., $I_G < 100\ nA$) and no latent damage is observed after applying the gate bias.

However, for the degraded device (ii) previously presented in Fig. 6 (d), after the stress at negative V_{GS}, the I_S decreased, meaning that higher current is flowing to the drain-gate path, rather than into the source pad, as shown in Fig. 8. (d). This is evidence of an increased gate damage induced by the negative gate bias.

IV. Discussion

From the results presented, three different scenarios where commonly observed for the different architectures analysed. Considering the FIT normalized with the active area and scaled by the breakdown voltage, the trench devices showed a better performance to SEB with respect to the planar ones, with the double-trench architecture as the most robust. However, part of the trench and double-trench devices exhibited a complete gate rupture. Conversely, a partial gate rupture was observed for the planar reference analysed, which exhibited a current leakage path between gate and drain as previously observed for planar gate devices suffering from SELC after heavy-ion irradiation. Additionally, for the device with the gate partially ruptured, the gate damage increased after the PIGS test, which was already reported for devices suffering from SELC after heavy-ion experiments [39].

A model for an enhanced gate current associated with a leakage was previously presented for Si devices and heavy-ion irradiation. It states that the oxide defects from displacement damage caused by the ions create a significant number of damage sites at which there is a reduced potential barrier, permitting the tunneling of electrons from trapping sites in the oxide into the conduction band [40]. Similarly, a model for early defects in SiO_2/SiC was discussed in [41] and attributed

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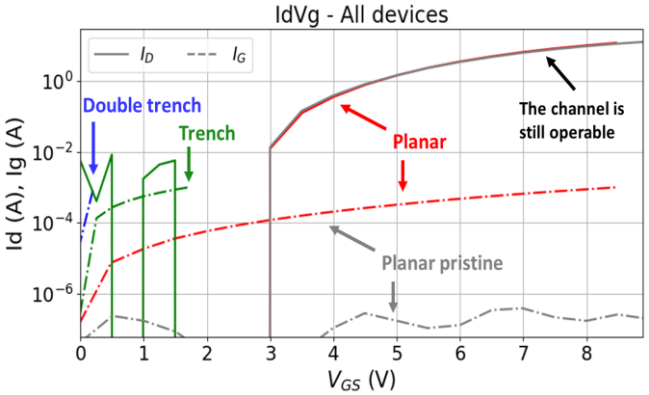

Fig. 7. I_D-V_{GS} and I_G-V_{GS} measurements performed at V_{DS} = 1 V. The gate oxide is still operable for the planar Cree/Wolfspeed device (C2M0025120D) and the channel is still controlled by the gate voltage. Conversely, the gate oxide is heavily damaged and not operable anymore for the trench and double-trench structures.

to the presence of defects in the oxide bulk. It is hypothesized that, through displacement damage, neutrons are inducing defects in the gate oxide, which are responsible of the increased gate leakage current. Furthermore, the density and distribution of oxide defects in a pristine device depend on the oxide process and can be considered as a by-product of the SiO_2 oxide growth on SiC, therefore different among devices produced by different manufacturers.

Finally, it should be noted that the setup used during the experiment was counting as a failure event all the devices whose I_D leakage current in off-state exceeded 1.27 mA. Therefore, the FITs and the failure cross-section analysis includes both the failure mechanism indicated as SEB (iii) and degradation with partial or complete gate rupture (ii), with the latter also considered not operable from an application point of view due to the very high leakage currents.

V. Conclusions

Results from accelerated terrestrial neutron experiments were presented for different commercial SiC technologies with planar, trench and double-trench architectures.

Different failure mechanisms were observed from the post-irradiation analysis of the irradiated devices, and three different responses were commonly identified for each of the three architectures: (i) no damage observed with respect to a pristine device, (ii) partial degradation of the device, which exhibited high leakage currents, (iii) SEB (i.e., ohmic trend of the leakage current). Categories (ii) and (iii) were considered failed devices from an application point of view. Failure cross-sections and FIT rates were calculated for these devices. MOSFETs with a trench structure appear to be less sensitive to neutron-induced failures with respect to the planar ones. The double trench-architecture, which has also the higher breakdown voltage, was observed to be the most robust.

Examples were reported and discussed for the degraded devices (ii) and the impact of gate rupture was discussed for the three designs. The planar-gate architecture exhibited a partial gate rupture mechanism, probably induced by displacement

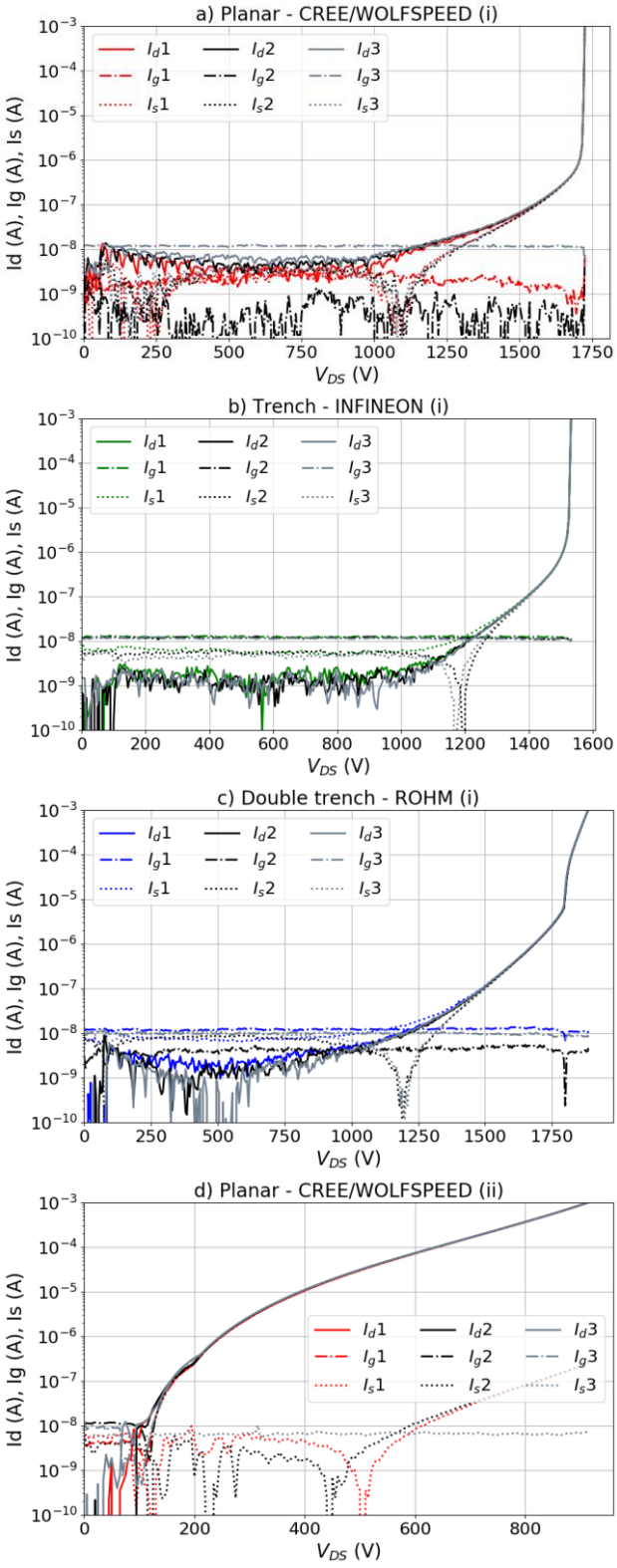

Fig. 8. Breakdown voltage measurements after the post irradiation gate stress (PIGS) test. The results are reported for the planar (a), trench (b) and double-trench (c) DUTs, which did not show any damage during the exposure (i), and for the planar DUT (d) which was partially degraded (ii). The first cycle reports the measurement just after the irradiation, while the second and the third represent the measurements repeated after applying a positive V_{GS} up to the rated voltage and a negative V_{GS} of -5 V, respectively.

damage and characterized by very high leakage currents with a gate-drain current path. This effect was observed to be similar to the SELC degradation induced by heavy-ions, already discussed for the same reference, but reported here for neutron irradiation. The trench and double-trench architecture, instead, appeared to be more sensitive to a complete gate rupture.

However, it should be clearly stated that the experiments were performed using a specific device type from each manufacturer. Both the design as well as the resulting efficient carrier concentration in the specific areas will vary between device types and generation from the same manufacturer; therefore, the results cannot be extrapolated to all SiC power devices without further analysis.

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