This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

Enhanced Charge Collection in SiC Power MOSFETs Demonstrated by Pulse-Laser Two-Photon Absorption SEE Experiments

Robert A. Johnson III, *Student Member*, IEEE, Arthur F. Witulski, *Senior Member,* IEEE, Dennis R. Ball, *Member,* IEEE, Kenneth F. Galloway, *Fellow*, IEEE, Andrew L. Sternberg, *Member*, IEEE, Enxia Zhang, *Senior Member*, IEEE, Landen D. Ryder, *Student Member,* IEEE, Robert A. Reed, *Fellow*, IEEE, Ronald D. Schrimpf, *Fellow*, IEEE, John A. Kozub, Jean-Marie Lauenstein, *Member*, IEEE, and Arto Javanainen, *Member*, IEEE

***Abstract*— A two-photon absorption technique is used to understand the mechanisms of single-event effects in silicon carbide power MOSFETs and power junction barrier Schottky diodes. The MOSFETs and diodes have similar structures enabling identification of effects associated specifically with the parasitic bipolar structure that is present in the MOSFETs, but not the diodes. The collected charge in the diodes varies only with laser depth, whereas it varies with depth and lateral position in the MOSFETs. Optical simulations demonstrate that the variations in collected charge observed are from the semiconductor device structure, and not from metal/passivation-induced reflection. The difference in the spatial dependence of collected charge between the MOSFET and diode is explained by bipolar amplification of the charge carriers in the MOSFETs. TCAD device simulations extend this analysis to heavy ion-induced charge collection. In addition, there is discussion comparing this analysis with experimental results from prior works that show enhanced charge collection resulting from heavy ion irradiation.**

***Index Terms*— pulse height analysis, Schottky diodes, Silicon carbide, single-event effects, two-photon absorption, vertical MOSFET**

I. Introduction

SILICON carbide (SiC) is an excellent material for power devices. It boasts a higher breakdown field and thermal conductivity than silicon, which permits devices with equivalent breakdown voltages, current ratings, and on-state resistances to be made smaller in SiC than in silicon [1]. This benefit is of importance both for terrestrial and space power systems.

Silicon power metal oxide field effect transistors (MOSFETs) are susceptible to catastrophic failure through both single-event gate rupture (SEGR) and single-event burnout (SEB), induced by protons, heavy ions, or neutrons. The mechanisms responsible for these events are well understood [2], [3]. Specifically, for SEBs in silicon, the failures are linked to a parasitic bipolar junction transistor (BJT) inherent in the structure of conventional vertical double-diffused metal oxide semiconductor (VDMOS) power FETs, as shown in Fig. 1. Further information on the structure and function of VDMOSFETs can be found at [4] These conclusions have been supported using pulsed-laser two-photon absorption backside testing with burnout protection circuits to map the regions where failure is most likely to occur [5], [6].

Silicon carbide power MOSFETs are also susceptible to both SEGR and SEB when exposed to energetic particles [7], and SEB has been examined for protons [7], heavy ions [8], and neutrons [9], [10]. In [8], heavy ion-induced charge-collection measurements on MOSFETs are presented. The charge-collection distributions isolate two separate mechanisms, one that results in constant charge collection with bias and one with increasing charge amplification with bias. The latter is hypothesized in the work to be the parasitic bipolar amplification associated with SEB in silicon power MOSFETs and inherent in the vertical MOSFET structure. In [11], technology computer-aided design (TCAD) simulations were used to show that a parasitic bipolar effect is present during SEB in SiC MOSFETs using structures modeled after the device used in this work.

Single-event effects can be created using pulsed-laser two-photon absorption (TPA) techniques [12]. It has been shown that SEB can be induced in SiC power diodes using TPA, and that the ability to induce SEB using TPA is dependent on diode reverse bias voltage and laser focus location within a device under test (DUT) [13].

In this work we investigate charge collection induced in SiC MOSFETs utilizing the two-photon laser technique through the backside of 1200 V devices SiC power MOSFETs to produce non-catastrophic transients. As a comparison, 1200 V SiC power diodes from the same manufacturer and technology are also tested. The similarity of the diodes to the MOSFETs permits isolation of MOSFET-specific

Manuscript submitted Oct 5th, 2018 and revised Jan 25th 2019, May 10th, 2019, June 9th 2019, and June 10th 2019; accepted June 11th 2019.

This work was supported by an Early Stage Innovations grant from NASA's Space Technology Research Grants Program, grant number NNX17AD09G, with additional support from the NASA Electronic Parts and Packaging Program.

Robert A. Johnson, Kenneth. F. Galloway, Arthur F. Witulski, Dennis R. Ball, Andrew L. Sternberg, Enxia Zhang, Robert A. Reed, Landen D. Ryder, John A. Kozub, and Ronald D. Schrimpf are with the Electrical Engineering and Computer Science Department, Vanderbilt University, Station B 351825, Nashville, TN 37235, USA, and the Institute for Space and Defense Electronics, Vanderbilt University, Nashville, TN 37235 USA (e-mail: robert.a.johnson@vanderbilt.edu)

Arto Javanainen is with the Department of Physics, University of Jyvaskyla, P.O. Box 35, FI-40014, University of Jyvaskyla, Finland (e-mail: arto.javanainen@jyu.fi)

Jean-Marie Lauenstein is with NASA/GSFC, Code 561.4, Greenbelt, MD 20771 USA (e-mail: jean.m.lauenstein@nasa.gov)

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

mechanisms from the results. Using TPA, positional dependence of these MOSFET-specific mechanisms is found. TCAD device simulations extend this analysis to heavy-ion induced charge collection and provide insight into the differences between the MOSFET and diode charge collection mechanisms. In addition, there is discussion comparing this analysis with experimental results from prior works that show enhanced charge collection resulting from heavy ion irradiation.

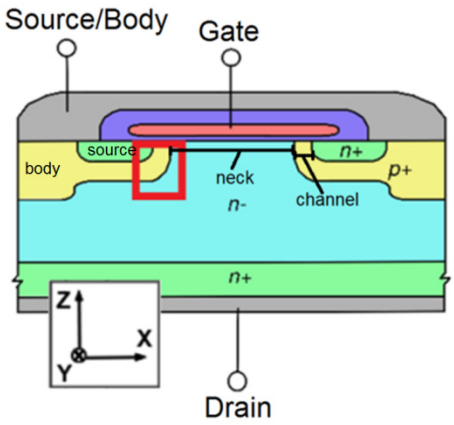
A. Experimental Conditions*Sample Devices*

The SiC power MOSFETs used in this experiment were CPM2-1200-0080B bare die from Wolfspeed, a CREE company. The MOSFETs' specifications are 1200 V, 80 mΩ, and 36 A for the blocking voltage, drain to source on resistance, and maximum drain to source current, respectively. The devices are enhancement-mode MOSFETS. The devices are fabricated on 4H SiC and consist of vertical MOSFETs symmetric along one axis while repeating along another, as shown in Figs. 1a and 1c. The stripes are repeated with a pitch of approximately 10 µm, determined by optical examination of the metal layers. The channel width is known to be approximately 1 µm and the epitaxial depth is known to be approximately 10 µm.

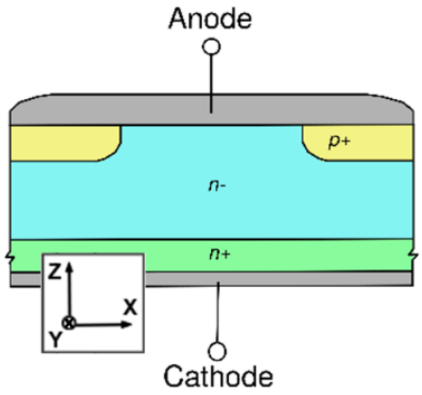
The SiC junction barrier Schottky (JBS) power diodes tested are CPW4-1200-S020B bare die also from Wolfspeed. The device specifications are 1200 V, and 20 A for the blocking voltage and maximum current, respectively. The diodes are made of 4H SiC and have similar doping densities and structure sizes to the MOSFETs, including the epitaxial depth of approximately 10 µm. The primary differences between the two are the lack of the gate and source structures within the diode and a hexagonal repeating geometry in the diode compared to the striped geometry in the MOSFET. Other device characteristics, including the dimensions of the hexagonal repeating geometry and overlayer composition, are not available to the public, and are not discernable optically due to the uniform topside metal layer.

B. *Device Preparation*

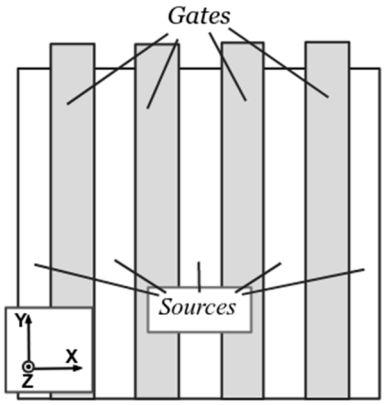
Each die was first polished until the backside metalization was completely removed, minimizing the reduction in SiC die thickness. They were mounted using silver epoxy into modified high-speed ceramic DIP40 packages with a hole drilled in to the package to allow access to the backside. The hole is sized to expose approximately 30% of the backside, which results in insignificant modification to the electric fields with bias compared to an unaltered die [5]. Gold bond wires connect the gate and source/body contacts to package pins, and the exposed die and bond wires were then coated in HumiSeal 1A33 to ensure safe operation of the device at biases over 100 V [14]. The drain contact is on the backside of the device and is attached directly to a package contact using silver epoxy. Each device underwent IV sweeps after packaging to verify normal operation.



(a)



(b)



(c)

Fig. 1. Depiction of the vertical power MOSFET and diode structure for the devices used. Fig. 1a is a cross section through the XZ plane of a MOSFET, Fig. 1b is a cross section through the XZ plane of a diode, and Fig 1c is a top-down view of the MOSFET below the metalization. The highlighted region of the cross section covers one of the parasitic bipolar transistors inherent in the device structure, and known to play a fundamental role in SEB occurrence in Si and SiC vertical power MOSFETs.

C. *Two-photon absorption technique for SiC devices*

Pulsed-laser TPA testing was conducted using Vanderbilt's tunable wavelength focused laser facility. For 4H SiC, which has a larger bandgap than Si (3.2-3.3 eV), the maximum wavelengths able to generate electron-hole pairs from single-photon and double-photon absorption are 375 nm and 650 nm, respectively. The laser was tuned to a wavelength of 481 nm,

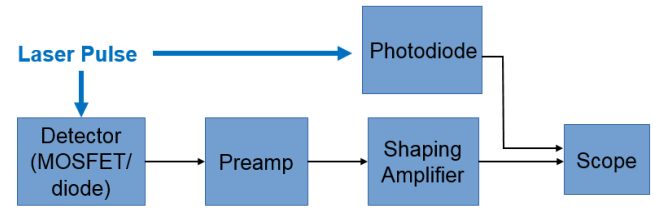
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

which equates to a photon energy of 2.58 eV. This wavelength has been used to generate SEB in 4H SiC diodes in prior testing [13].

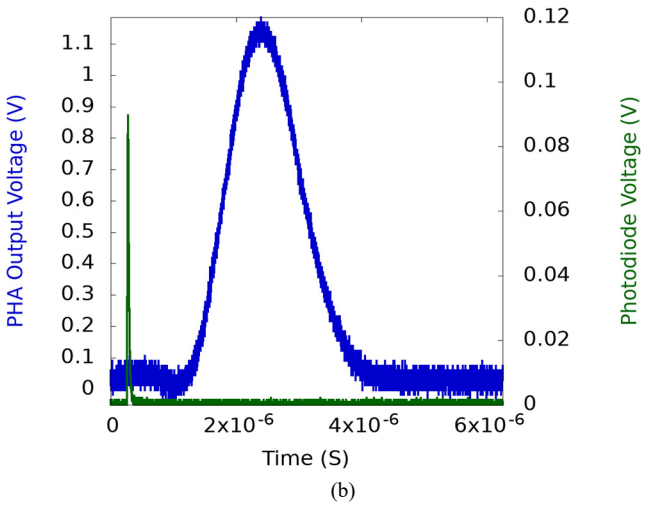
D. Charge Collection Measurements

Initial charge collection measurement efforts utilizing bias tees and a CT-2 current probe were unable to produce sufficient signal over environmental and device noise at biases below 200V, and above 200V both MOSFETs and diodes exhibited laser-pulse induced leakage current degradation. Due to these factors, pulse height analysis was used to complete charge collection measurements.

Fig. 2a shows a block diagram of the experimental setup used for charge collection measurements. This technique, known as pulse height analysis (PHA), is a well-established characterization method in nuclear spectroscopy and has been used for many years to measure charge-collection spectra from ionizing radiation events [15]. A device is exposed to an ionizing source while biased and the resulting charge transient from a heavy ion or laser pulse is integrated by a FET amplifier within the preamplifier. This output pulse has an amplitude proportional to the charge collected by the biased device. The shaping amplifier provides additional signal processing to aid in isolating transient peaks. The output of the shaping amplifier is then sent to an oscilloscope where it can be captured. The peak heights were converted to collected charge using the technique described in [15], [16].



(a)



(b)

Fig. 2. Fig. 2a provides a chart detailing the basic experimental setup and Fig. 2b. provides an example oscilloscope output.

The photodiode is used to measure the pulse-to-pulse variation of the laser energy using the same oscilloscope as the output of the amplifier. The voltage generated by the photodiode has not been mapped quantitatively to energy values at the laser wavelength used, but the pulse energy is estimated to be on the order of nanojoules based on the efficiency of the photodiode. This measurement therefore is used exclusively for verifying consistency of laser pulse energies during each run as well as providing a relative measure of deposited energy per pulse between runs. Within individual runs energy values remained fairly concentrated, but drift in energy throughout test days varied by as much as 50%. Pulses were produced at a frequency of 1 kilohertz, yielding a total power dissipation of only microwatts in each sample due to the laser. Transients caused by laser pulses are isolated from noise by triggering the oscilloscope on pulses of the photodiode signal, which is shown in Fig. 2b.

The MOSFETs are biased with the gate and source attached to a shared ground, and the diodes are reverse biased for all tests. The response to pulsed TPA was studied over bias and position of the laser spot. The location of the laser focus is recorded for each laser pulse and resulting oscilloscope output. During voltage sweeps, a Keithley 2410 Source Measure Unit (SMU) provides bias and this bias is also recorded on each pulse. Z=0 was set to the SiC-metal interface of each device by finding the laser focus depth with the most concentrated reflections off of the metal as viewed through a backside camera. This method produced results within a few microns of the actual SiC-metal interface, an error which does present itself when comparing the results of multiple devices as discussed later. While able to identify the striped structure of the MOSFET using both a frontside and backside camera, determining which stripes were associated with gate structures was not possible, necessitating later optical simulation to verify, presented in section IV. Initial tests were performed to determine the locations of maximum charge collection in both the diode and MOSFET. Once these charge-collection maxima locations were found the voltage sweeps were run at these locations for each device.

II. Experimental Results

Lateral sweeps (x-axis in Fig. 1c) of laser focus through the diode yielded insignificant variation in collected charge at a constant reverse bias and laser energy, as shown in Fig. 3. Fig. 4 presents a similar sweep in the MOSFET, where there is a periodic response with position. The period of the output is approximately 10 µm, which is consistent with the pitch of the gates within the MOSFET. These data suggest that the variation in structure in the MOSFET causes spatial variability in charge collection, but it was not possible to correlate the details of the device structure with peaks and troughs. We accomplish this by comparing the response of the diode to the MOSFET (described next).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

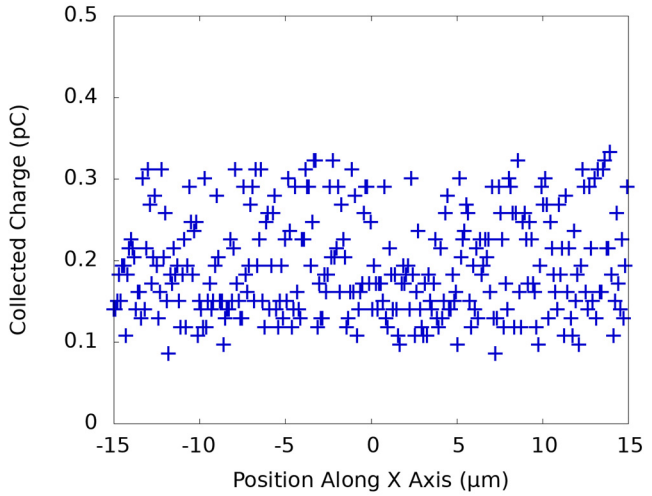


Fig. 3. Collected charge with a sweep of laser focus along the X axis in the diode. The diode was reverse biased at 50V.

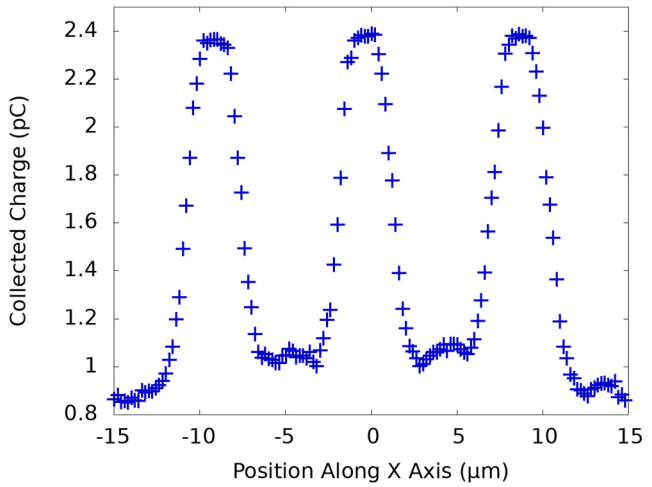
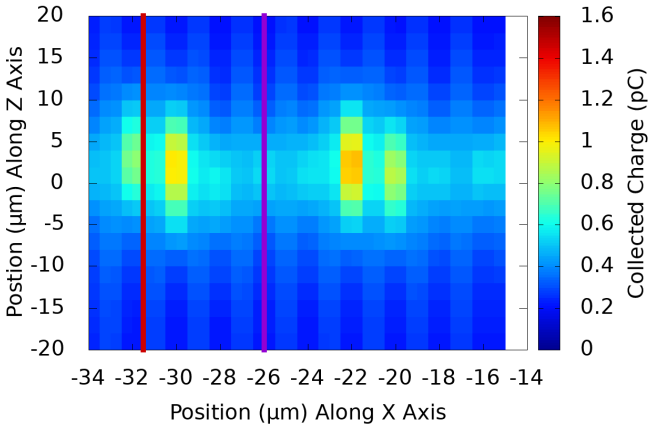


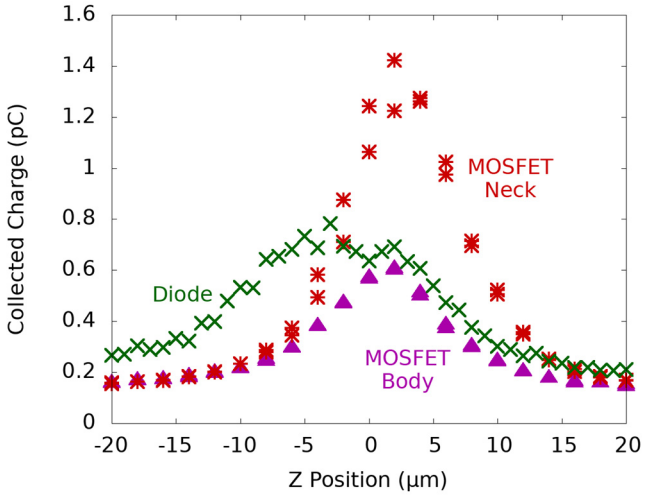
Fig. 4. Collected charge with a sweep of laser focus along X axis (across structures) in the MOSFET. Periodicity is the same as the observed pitch of device structures. The MOSFET was reverse-biased at 50V with the gate and source contacts grounded.

The diode structure (including the metal) is most similar to the region of the MOSFET underneath the source/metal contact (e.g., compare the left most region in Fig. 1a to that in Fig. 1b), and consequently the charge-collection response to a laser sweep perpendicular to the top surface of the die (z-direction as shown in Fig 1c) will be similar for the two devices in this region, enabling correlation of the peaks and troughs in Fig. 4 to physical structures of the MOSFET.

Fig. 5a shows a mapping of the collected charge for the MOSFET over two directions; the x-axis is perpendicular to the metal strips and z-axis is perpendicular to the top surface of the device; there are two device structures shown in this figure. Next, these data are sampled at two locations: x = -32 μm and x = -26 μm, indicated by the vertical lines in Fig. 5a and plotted in Fig. 5b. A vertical sweep in the diode is also plotted in Fig 5b. The distribution and amplitude of collected charge in the diode is very similar to that of the trough of the MOSFET in both distribution and amplitude. There is greater similarity in distribution between the two measurements within the MOSFET, however this is due to the limited accuracy of the method for setting z = 0, which only presents itself when comparing test results from multiple devices rather than within a device. From this data we conclude that the troughs occur under the shared source and body contacts of the MOSFET and the peaks occur under the gate-neck region.



(a)



(b)

Fig. 5. Fig 5a shows collected charge with a cross section sweep of laser focus along X and Z axes (across device structures and vertically) in the MOSFET. Fig. 5b shows stripes in the Z axis taken from the data in Fig. 5a at peaks and troughs along the X axis, as well as a sweep of the diode along the Z axis. The lines shown in Fig. 5a are where the data stripes in Fig.5b are taken. Data was acquired with the MOSFET and diode reverse-biased at 50V.

Fig. 6 contains a plot of charge collection as a function of voltage for both the MOSFET and diode focused at respective positional charge maxima; the MOSFET data are collected with the laser is focused at the gate-neck region, i.e., the location where charge amplification is expected. In order to prevent saturation of the PHA system when operating up to 300V, the laser energy was reduced below the energy of the pulses for positional sweeps at a 50V bias. The diode's response appears to follow a square root rule, which is expected. The MOSFET's response tracks the diode's response from 0 V up to 30 V, then appears to maintain a roughly linear relation. We will discuss this result in more detail in the discussion section.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

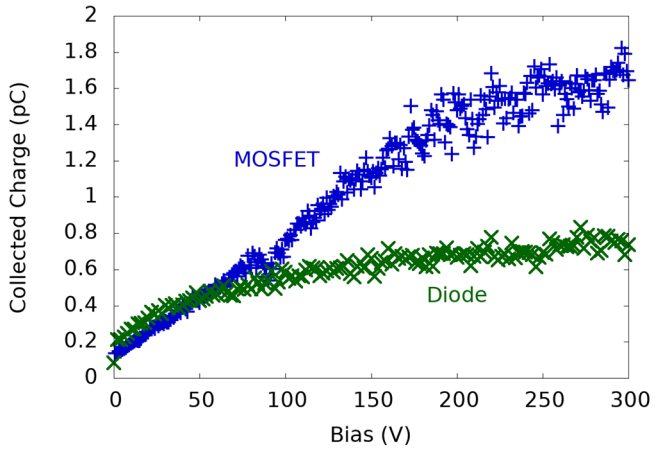


Fig. 6. Diode and MOSFET collected charge at reverse-biases between 0 and 300V. Due to variations in laser pulse energy throughout the day the diode received pulses with a similar distribution but 20% greater than the MOSFET, explaining the region between 0-60V where the diode collected charge is greater than the MOSFET. Due to limitations on laser availability, repetition of these experiments with less laser pulse energy drift have not occurred.

III. Optical Simulation

Charge collection in the MOSFET structure from backside illumination was considered in two regions: underneath the source and underneath the gate. Nominally, these structures are differentiated by the location of the metal contact relative to the SiC bulk, with the source region being a SiC/metal contact interface and the gate region having a polysilicon layer between the SiC and metal contact. In order to better elucidate the charge-collection mechanisms of the device, the role of material interfaces and reflections on the optical generation of carriers should be considered when comparing charge collection from the two regions.

Optical simulations were performed using Lumerical FDTD Solutions, a 3-D commercial nanophotonic software package, to calculate the optically generated carrier distribution from a laser pulse propagating from the backside of the device. Two structures were simulated for evaluation of interfacial reflections and the implication for charge generation: a bulk SiC layer with a metal interface, similar to a VDMOS source structure, and a bulk SiC layer with a polysilicon layer between the metal contact, similar to a VDMOS gate structure. The laser was focused at the interface of the SiC and the adjacent material, corresponding to a Z position of zero in the experimental results. Simulations were conducted with an operating wavelength of 481 nm. For an overfilled objective at this wavelength, Lumerical calculates a spot size with a full width half max diameter of 494 nm [17], [18]. Values for the complex refractive index of polysilicon ($n_{Poly\text{-}Si}$ = 4.42+.086i), the complex refractive index of SiC (n_{SiC} = 2.69), and the TPA coefficient of SiC (β_{SiC} = 10cm/GW) were taken from [19]-[21].

In both structures, light propagating from the backside through the SiC will interact with a material interface that will partially reflect and partially transmit light. The gate structure provides two material interfaces for consideration: the SiC/polysilicon interface and polysilicon/metal contact interface. For the stated refractive index values, the Fresnel reflection coefficient for the SiC/polysilicon interface indicates that <6% of the light incident on the interface is reflected back into the SiC. Although the majority of the light is transmitted through the SiC/polysilicon interface, polysilicon is extremely absorptive at this wavelength and, consequently, >99% of the light is absorbed within the polysilicon layer. Therefore, light that is not initially reflected at the SiC/polysilicon interface is almost completely absorbed by the polysilicon and does not significantly contribute to optical charge generation in the SiC. Accordingly, because the intensity of light reflected from the SiC/polysilicon interface is much lower than that reflected from the SiC/metal contact interface (>82%), there will be less optically generated charge in the SiC/polysilicon/metal contact structure (gate) than in the SiC/metal contact structure (source). The simulated spatial distribution of optically generated carriers in the SiC layer is shown in Fig. 7 for the source and gate regions under the same illumination conditions. In both geometries, the existence of interference fringes confirms the presence of reflections from the material interface contributing to charge deposition. Consistent with the aforementioned discussion, the optical carrier generation in the source region is larger than in the gate region. Furthermore, the spatial distribution shape affirms that reflections from the metal contact and etalon effects from the polysilicon layer in the gate structure are suppressed by absorption in the polysilicon. The full width half max diameter of the generated charge distribution is 350 nm.

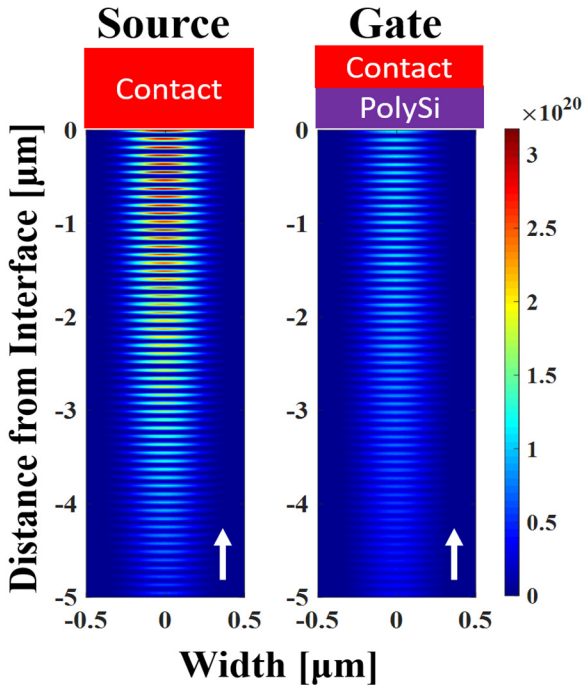


Fig. 7. Cross-section of optically generated carriers in SiC for bulk SiC with a metal contact (Source/Body) and bulk SiC with a polysilicon layer and metal contact (Gate) regions. In both simulations the interface between SiC and adjacent materials is defined at the zero line. The laser pulse propagates from the bottom (direction of white arrow) and is focused at the interface.

In order to quantitatively relate the optically generated charge profiles to collected charge, a charge transport model must be utilized. In this work, we focus on the general trends to gain insight and do not directly integrate optical and TCAD

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

simulations. Nevertheless, the optical simulation results depicted in Fig. 7 are important for understanding the charge collection mechanisms of the device by clarifying the impact of the material system on the optically generated charge. The implications of the interfacial reflections discussed earlier in this section enable the estimation of depth profiles of the optical generated charge for the two structures. Based on the results in Fig. 7, we expect the depth profile of the source structure would be only slightly different when focused below or beyond the surface interface. Moreover, the minimal reflections in the gate structure and significant absorption in the polysilicon layer would result in depth profiles for which significantly less optical charge generation exists when the laser focal position is above the SiC/polysilicon interface compared to below the interface. Fig. 5b provides experimental results that can be used as comparisons to these trends predicted from optical simulations. Since the structure of the diode and MOSFET body yielded higher charge carrier generation in the optical simulations than the MOSFET gate, the increase in collected charge when a laser is focused in the gate and neck regions suggests a non-optical process dominates the collected charge results in these regions.. The optical simulations demonstrate that the enhanced charge collection in the neck region is not due to enhanced optical generation from interfacial reflections.

IV. Extension to Heavy Ion Effects

A. Heavy ion TCAD Simulation

Previous TCAD simulations of the MOSFET used in this study have shown a position dependence on the collected charge with ion strikes at bias voltages high enough to induce SEB in hardware testing [11]. If there are sufficient carriers generated in the body to forward-bias the body/source junction, holes begin to flow into the source, forming a base current for the BJT. Simulations were only able to produce runaway associated with SEB if impact ionization was implemented in the MOSFET, indicating two complimentary charge amplification mechanisms. However, impact ionization was only seen in significant amounts at biases above 450V. At lower biases, changes in depletion region depth present in both the diode and MOSFET explain the variation in charge collection with bias in the diode (green curve), as seen in Fig. 6.

Given the similarity of the diodes and MOSFETs tested, the effects of depletion depth variation on the charge collection from the laser events are expected to be similar for both device types and have little or no measurable positional dependence in either device. The amount of charge collected in the diode defines the portion of charge collected in the MOSFET due to carrier generation in the depletion region. If the BJT plays a significant role in charge collection for SiC MOSFETs, there should be evidence of charge amplification at bias voltages sufficiently large to activate the BJT during a laser strike for specific strike locations. Specifically, amplification should occur when carriers are generated in a MOSFET channel.

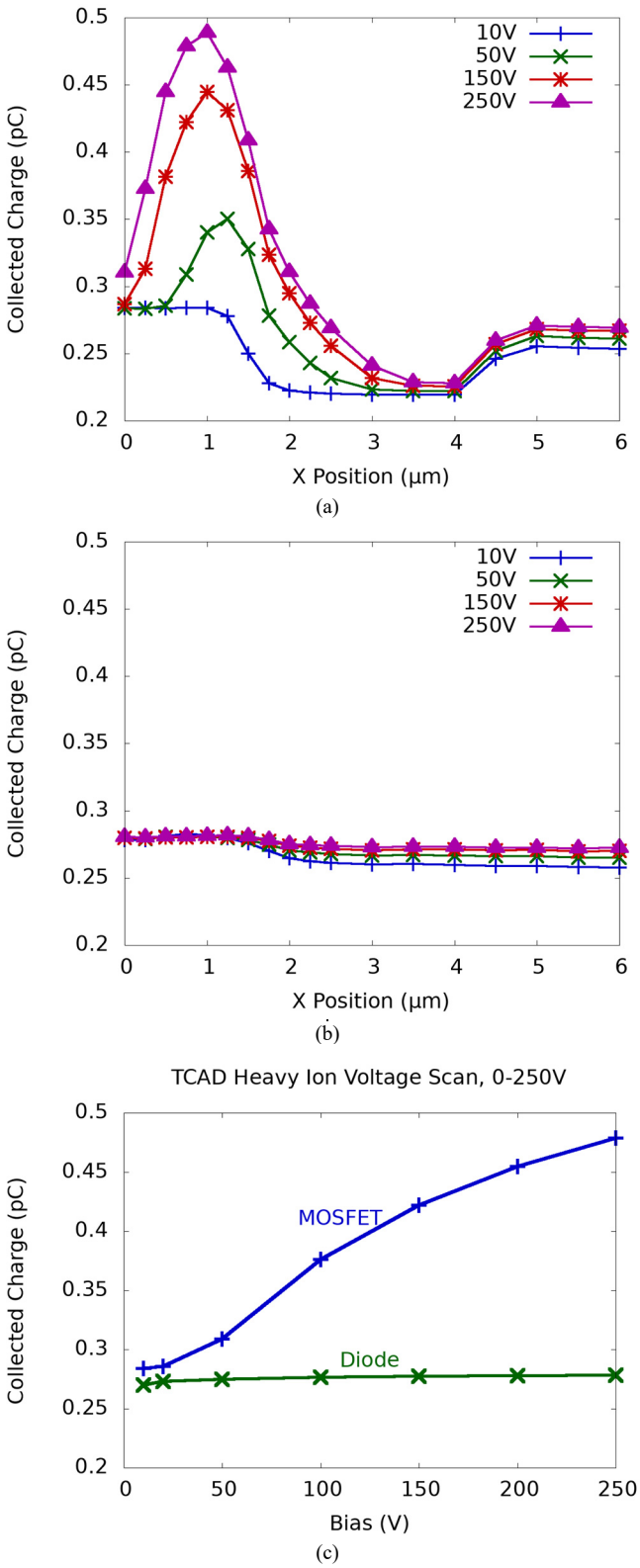


Fig. 8. TCAD simulations of collected charge in a MOSFET for a constant amount of deposited charge but varying location and bias are shown in Fig. 8a. Fig. 8b shows TCAD simulations of collected charge in a diode for a constant amount of deposited charge but varying location and bias. For Figs. 8a and 8b, a strike location of 0 is at the center of the epitaxial region near the surface between two p-doped regions. Fig. 8c shows TCAD simulations of collected charge in a MOSFET and diode for a constant amount of deposited charge and constant location but varying bias.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2019.2922883, IEEE Transactions on Nuclear Science

Fig. 4 suggests this, but has limited detail due to the full width half max charge distribution diameter of 350 nm, which is approximately a third of the channel width of 1 µm. Rather than a peak charge collection centered in each channel with a slight dip in charge collection in the center of the neck between channels, the distributions around both channels are unavoidably blurred across the neck, showing a single peak centered in each neck of each device stripe.

Fig. 8a shows 2D TCAD heavy ion simulations using Synopsys Sentaurus [22]. The ion strike has a Gaussian radius of 50 nm and an ion LET of 20 MeV-cm^2/mg passing through the top 2 µm of the epitaxial layer. This short path length isolates the effects of a parasitic bipolar from additional amplification due to impact ionization and generating additional charge at the epitaxial/drain interface, which would have minimal interaction with the intrinsic bipolar transistor. The ion strike location x = 0 is at the center of the device neck (see Fig. 1a and 1b), and stepped every 50 nm laterally across the surface of the device. For the MOSFET, x = 1 µm is the interface of the neck and channel. . At the test biases the depletion region takes up only the top 1-2 µm of the device, and only the charge deposited in this region ends up collected at the terminals. Collected charge as a function of position is shown in Figs. 8a and 8b for the MOSFET and diode, respectively. These results show a significant gain in collected charge for the MOSFET for a strike near the n+/p/n region, which is the parasitic BJT. With a 10 V bias in the MOSFET, the entire neck and channel are equally sensitive, with a drop off moving to the source and body. At higher biases, the electric field distributions around the channel-neck interface play an increasing role, and the amplification is centered on this interface rather than a drop off on the other side of the channel. In the diode, there is no n+/p/n region, and consequently, no parasitic BJT, and collected charge remains largely unchanged as a function of position.

Simulation results for collected charge at x = 0 and varying bias are shown in Fig. 8c. The diode and MOSFET collect similar amounts of charge at biases below 20 V. Below 20 V, the ion-induced carriers are not able to produce a sufficient base emitter voltage in the parasitic bipolar transistor to saturate it. At higher biases (effectively the collector bias in the parasitic BJT), the gain increases while the deposited charge stays the same. However, for the diode, the collected charge stays relatively constant.

B. Analysis of Previously Published Heavy Ion Data

As a final demonstration of parasitic bipolar amplification, we review similar charge collection measurements on the same MOSFET presented in [8]. The resulting charge collection distributions contain two primary maxima. The maximum with lower collected charge closely tracks the quantity of deposited charge, indicating that the first mechanism is simply ordinary charge collection at the terminals. Fig. 9 replots the second maximum collected charge values data from that paper as a function of bias for three different ion linear energy transfers (LET). (We note that the lower mode in the charge collection distribution did not depend on bias.) The horizontal lines represent the amount of charge generated in the epitaxial region for each ion LET. The maximum charge collected increases with bias for all three ion species used in that work, also the higher bias experiments show that more charge is collected than deposited. These effects were enhanced with increasing LET and increasing bias voltage.

As shown in Fig. 3, the diodes tested exhibited behavior consistent with the absence of charge carrier amplification dependent on position parallel to the SiC-metal interface of the device. However, MOSFETs demonstrated amplification dependent on laser focus position, seen in Fig. 4. For ion strikes of a constant LET, the only variable in strike conditions is the location of the strikes. Ions should all generate approximately the same charge in a device independent of strike location. If the resulting distribution of collected charge for all ion strikes contains multiple local maxima, there must be additional mechanisms that are only relevant for certain strike locations. Therefore results of Fig. 9 imply a positionally dependent mechanism in the MOSFET during heavy ion testing, as the data contains two primary local maxima at every ion species and bias. Since the gain in collected charge over deposited in the presented laser results is credited to bipolar amplification and is similar to the amplification seen in [8], and the TCAD simulation presented here and in [11], the second maxima in Fig. 9 are due the occasional ion strikes causing bipolar amplification of deposited charge in these SiC MOSFETs.

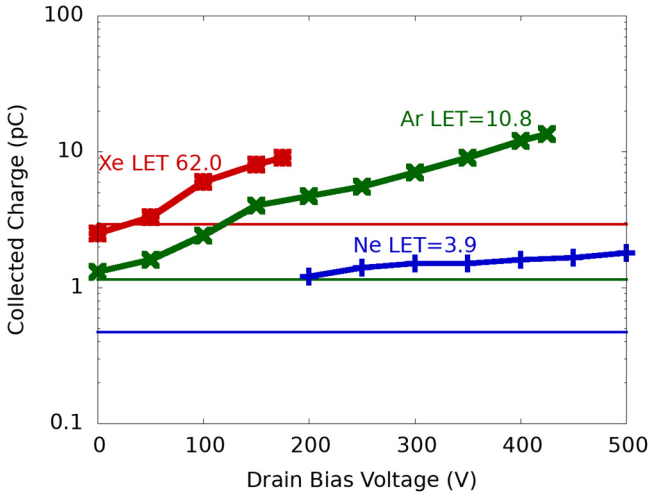


Fig. 9. Second peaks of collected charge as a function of the drain bias voltage below the bias voltage threshold for SEB [8] as well as horizontal lines showing the calculated deposited charge for each ion using an epitaxial depth of 10 µm. A distribution of charge collection values was collected for each bias and ion species, and the points shown are the higher of the two most frequent collected charge bins in each distribution.

V. Summary

Two-photon backside laser testing has been used to identify the source of bias-dependent charge collection amplification with localized ionization in SiC power MOSFETs and SiC power diodes. Peaks in charge collection were seen with movement of the laser focus between power MOSFET cells at a fixed depth. These peaks are not observed in similar measurements on SiC power diodes. Comparing the different responses of the diode and MOSFET, it is observed that when the laser is focused on the neck region of a MOSFET cell the greatest charge collection occurs. This agrees with prior simulated results [13]. The charge collection increases as the

bias voltage increases, supporting results seen in earlier work using heavy ions [8]. We conclude that the parasitic bipolar amplification inherent in the vertical SiC power MOSFET structure is the cause of these phenomena and is an important mechanism when SEB is observed in these devices.

ACKNOWLEDGMENT

We thank Dave Grider, Daniel Lichtenwalner, and Brett Hull at Wolfspeed for providing the die and important technical discussions.

REFERENCES

[1] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proc. IEEE*, vol. 90, no. 6, pp. 969–986, Nov. 2002.

[2] C. F. Wheatley, J. L. Titus, and D. I. Burton, "Single-Event Gate Rupture in Vertical Power MOSFETs; An Original Empirical Expression," *IEEE Trans. Nucl. Sci*., vol. 41, no. 6, pp. 2152–2159, Dec. 1994.

[3] M. Allenspach et al., "SEGR and SEB in n-channel power MOSFETs," *IEEE Trans. Nucl. Sci*., vol. 43, no. 6, pp. 2927–2931, Dec. 1996.

[4] B. J. Baliga, "Advanced Power MOSFET Concepts," in *Advanced Power MOSFET Concepts*, Springer, 2010, pp. 23–61.

[5] F. Miller et al., "Characterization of single-event burnout in power MOSFET using backside laser testing," *IEEE Trans. Nucl. Sci*., vol. 53, no. 6, pp. 3145–3152, Dec. 2006.

[6] F. Darracq et al., "Imaging the single event burnout sensitive volume of vertical power MOSFETs using the laser two-photon absorption technique," *Proc. Eur. Conf. Radiat. its Eff. Components Syst. RADECS*, pp. 434–441, Sept. 2011.

[7] M. C. Casey et al., "Single-Event Effects in Silicon Carbide Power Devices," *NEPP Electronic Technology Workshop*, 2013. [Online]. Available: https://ntrs.nasa.gov/archive/nasa/casi.ntrs.nasa.gov/20150017740.pdf.

[8] E. Mizuta, S. Kuboyama, H. Abe, Y. Iwata, and T. Tamura, "Investigation of single-event damages on silicon carbide (SiC) power MOSFETs," *IEEE Trans. Nucl. Sci*., vol. 61, no. 4, pp. 1924–1928, Jul. 2014.

[9] A. Akturk, R. Wilkins, J. Mcgarrity, and B. Gersey, "Single Event Effects in Si and SiC Power MOSFETs Due to Terrestrial Neutrons," *IEEE Trans. Nucl. Sci*., vol. 64, no. 1, pp. 529–535, Dec. 2017.

[10] K. Rashed, R. Wilkins, A. Akturk, R. C. Dwivedi, and B. B. Gersey, "Terrestrial neutron induced failure in silicon carbide power MOSFETs," *2014 IEEE Radiat. Eff. Data Work*., pp. 1–4, Jul. 2014.

[11] A. F. Witulski et al., "Single-Event Burnout Mechanisms in SiC Power MOSFETs," *IEEE Trans. Nucl. Sci*., vol. 65, no. 8, pp. 1951–1955, Jun. 2018.

[12] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Subbandgap laser-induced single event effects: Carrier generation via two-photon absorption," *IEEE Trans. Nucl. Sci*., vol. 49, no. 6, pp. 3002–3008, Dec. 2002.

[13] N. Mbaye, V. Pouget, F. Darracq, and D. Lewis, "Characterization and modeling of laser-induced single-event burn-out in SiC power diodes," *Microelectron. Reliab*., vol. 53, no. 9–11, pp. 1315–1319, Sept. 2013.

[14] "HumiSeal ® 1A33 Aerosol Conformal Coating Technical Data Sheet." Chase Electronic Coatings, pp. 1–2, 2002.

[15] R. A. Reed, P. J. Mcnulty, W. J. Beauvak, and D. R. Roth, "Charge collection spectroscopy," *IEEE Trans. Nucl. Sci*., vol. 40, no. 6, pp. 1880–1887, Dec. 1993.

[16] P. J. McNulty, W. J. Beauvais, and D. R. Roth, "Determination of SEU Parameters of NMOS and CMOS SRAMs," *IEEE Trans. Nucl. Sci*., vol. 38, no. 6, pp. 1463–1470, Dec. 1991.

[17] M. Mansuripur, "Distribution of light at and near the focus of high-numerical-aperture objectives," *J. Opt. Soc. Am. A*, vol. 3, no. 12, p. 2086-2093, Dec. 1986.

[18] M. Mansuripur, "Certain computational aspects of vector diffraction problems," *J. Opt. Soc. Am. A*, vol. 6, no. 6, pp. 786–805, Jun. 1989.

[19] D. E. Aspnes and A. A. Studna, "Dielectric functions and optical parameters of Si, Ge, GaP, GaAs, GaSb, InP, InAs, and InSb from 1.5 to 6.0 eV," *Phys. Rev. B*, vol. 27, no. 2, pp. 985-1009, Jan. 1983.

[20] S. Wang, M. Zhan, G. Wang, and H. Xuan, "4H-SiC: a new nonlinear material for midinfrared lasers," *Laser & Photonics Reviews*, vol. 7, pp. 831-838, Jul. 2013.

[21] V. Grivickas et al., "Two-Photon Spectroscopy of 4H-SiC by Using Laser Pulses at Below-Gap Frequencies," *Materials Science Forum*, vols. 457-460, pp. 605-608, Jun. 2004.

[22] "Synopsys TCAD Tools." [Online]. Available: https://www.synopsys.com/. [Accessed: 29-Apr-2019].