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Low-Power, Subthreshold Reference Circuits for the Space Environment: Evaluated with γ-rays, X-rays, Protons and Heavy Ions

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Abstract: The radiation tolerance of subthreshold reference circuits for space microelectronics is presented. The assessment is supported by measured results of total ionization dose and single event transient radiation-induced effects under γ-rays, X-rays, protons and heavy ions (silicon, krypton and xenon). A high total irradiation dose with different radiation sources was used to evaluate the proposed topologies for a wide range of applications operating in harsh environments similar to the space environment. The proposed custom designed integrated circuits (IC) circuits utilize only CMOS transistors, operating in the subthreshold regime, and poly-silicon resistors without using any external components such as compensation capacitors. The circuits are radiation hardened by design (RHBD) and they were fabricated using TowerJazz Semiconductor's 0.18 µm standard CMOS technology. The proposed voltage references are shown to be suitable for high-precision and low-power space applications. It is demonstrated that radiation hardened microelectronics operating in subthreshold regime are promising candidates for significantly reducing the size and cost of space missions due to reduced energy requirements.

Keywords: analog single-event transient (ASET); bandgap voltage reference (BGR); CMOS analog integrated circuits; gamma-rays; heavy-ions; ionization; protons; radiation hardening by design (RHBD); reference circuits; single-event effects (SEE); space electronics; total ionization dose (TID); voltage reference; X-rays

1. Introduction

Radiation-tolerant, high-accuracy, reference circuits are widely used in almost all circuits and systems that are intended for space applications. Analog and mixed-signal circuits and systems such as flash memories [1], ADCs, operational amplifiers, LDOs and DACs, require a stable and reliable reference voltage/current in order to perform within their specifications [2–5]. Any performance deviations of the reference voltage will consequently deteriorate the performance of all the subsequent circuits, leading to a malfunction or even failure of the overall system. Designing reference circuits that achieve a low temperature coefficient (TC) at a wide temperature range, whilst consuming little power, is challenging. Hence, when the supply voltage and power consumption specifications are very aggressive, the design has to operate within the subthreshold region, in which the non-linearities of the CMOS current components increase. Furthermore, in this region increased mismatch and process variations can be an issue. Nevertheless, it has been shown that it is possible to design and build an entire, mixed-signal, system-on-chip, operating predominantly in the subthreshold regime [6].

Traditional voltage reference circuits, such as the well known bandgap voltage reference (BGR), use the bipolar junction transistor (BJT) temperature dependence in order to generate a proportional to absolute temperature (PTAT) voltage, which is then utilized in order to produce a first-order temperature compensation scheme [2,7]. Subsequent approaches focus on partially canceling the BJT's base-emitter voltage non-linearities, in order to provide a higher-order, non-linear compensation [8–13]. The penalty of this approach is the higher design complexity and increased power consumption. More recently, low-power reference circuits utilize the metal oxide semiconductor (MOS) carrier mobility and threshold voltage temperature dependence in order to generate a first-order temperature-compensated reference voltage by summing a PTAT current and a complementary to absolute temperature (CTAT) current [14–17]. These circuits achieve low-power consumption but the TC is limited due to the non-linearities of MOS current components, which are higher when compared to the BJT ones.

Beyond the existing performance requirements of commercial applications, space microelectronics are required to be robust to the increased radiation levels of the space environment [5,18–27]. Hence, there is a lot of ongoing research activity to investigate the design of CMOS based analog, digital and mixed-signal, radiation tolerant circuits [28–45], including those that operate in the subthreshold regime [46–48].

Studies of the space industry have revealed that satellite/spacecraft size and cost can be significantly reduced by taking advantage of the inherent radiation hardness of modern CMOS commercial processes, in conjunction with radiation-hardening-by-design and low-power techniques [49,50]. Low-power is of major concern in space microelectronics, due to the isolation of the system and the limited available power.

One of the most promising solutions for achieving low-power consumption is to operate the devices in the subthreshold region. However, although designers can utilize well-known radiation hardening by design (RHBD) techniques, such as enclosed layout geometry transistors, it is not trivial to maintain good performance, when MOS transistors are biased in subthreshold. In this operating region, the transistor's drain-current is exponentially dependent on threshold voltage, therefore any deviations of the threshold voltage will severely impact the circuit's performance.

In this work, we've designed and characterized two custom subthreshold reference circuits [17,51]. In addition to achieving competitive performance for commercial applications, the proposed topologies are designed to be radiation tolerant so as to perform reliably in the space environment. The proposed reference circuits achieve high-order, non-linear curvature correction, which leads to an improved TC over a wide temperature range. In addition, the circuits perform reliably without failures and up to a certain extent with comparably low reference voltage variations when exposed to radiation such as γ-rays, X-rays, protons and heavy ions. The TC and TID performance are evaluated through fabricated silicon and experimental accelerated characterization results.

2. Radiation-Induced Effects in Subthreshold Circuits

Radiation-induced effects can be generally categorized into three kinds of radiation effects; those where the total ionization dose (TID) affects the devices properties, those where high-energy particles induce single event transients (SET) or device failures by dumping relatively large charges on critical nodes and those where the energetic particles cause displacement damage (DD) of the atomic lattice.

2.1. Total Ionization Dose Effects

When ionizing radiation impinges a material, such as Si and SiO_2, it loses energy (MeV/cm) which is absorbed by the material. The energy transfer, from high energy photons (i.e., γ-rays, X-rays) or charged particles (i.e., protons, electrons, α-particles, energetic heavy ions) towards the impinged material, is achieved through direct or indirect ionization mechanisms that generates electron–hole pairs. Ionizing radiation energy will extract electron–hole pairs from the material's atomic lattice. Some of the created electron–hole pairs will manage to recombine within a short time window; others, in the presence of an electric field, will escape recombination due to high mobility and will drift outside the gate oxide (within picoseconds) [52,53] towards the gate. This process will be triggered due to the gate electric field (assuming positive bias at the gate) or due to the built-in field. The holes (low mobility), that survived the recombination, will drift under the positive electric field of the gate towards the interface between gate oxide and silicon channel (Si/SiO_2 interface) [54,55], where charge trapping can occur. Other areas of CMOS processes, which are prone to charge trapping due to TID, are the shallow trench isolation and the deep trench isolation oxides.

In commercial CMOS processes, the gate oxide and isolation oxides (shallow trench isolation and deep trench isolation) which are structured by SiO_2 (insulator) are the most sensitive areas to be affected by ionizing radiation. The long-term charge trapping in the oxides will modify the electrical characteristics of the transistors and depends on total dose, dose rate, bias, time and temperature. The electrical characteristics that degrade include threshold voltage, carrier mobility, noise and leakage currents [41,56].

The threshold voltage shift (ΔV_{TH}) is proportional to the square of the oxide thickness (t_{ox}) up to a certain total dose as [57]:

$$\Delta V_{TH} \propto t_{ox}^2. \tag{1}$$

Above a certain dose, at which all the charge traps (oxide and interface states) are completely filled, the dependence becomes linear [57]:

$$\Delta V_{TH} \propto t_{ox} \tag{2}$$

The electrical characteristics that degrade will have different impact on a transistor/circuit operating in the subthreshold regime, compared to the same transistor/circuit designed in strong inversion regime. In order to identify the impact of radiation-induced effects in subthreshold regime, one has to explore the corresponding equations describing the MOS physics.

The threshold voltage shift (1) as well as the carriers mobility degradation (μ_{eff}) will modify the drain current (I_D) of an NMOS transistor operating in subthreshold/saturation such as:

$$I_D = K\mu C_{ox}(n-1)U_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{nU_T}\right), \tag{3}$$

where K is the transistor's size aspect ratio W_{eff}/L_{eff}, μ is the mobility of carriers in the device channel, C_{ox} is the oxide capacitance per unit area, n is the subthreshold slope factor, $U_T = kT/q$ is the thermal voltage, V_{GS} is the gate-source voltage, and V_{TH} is the transistor threshold voltage. From (3) it can be deduced that the radiation-induced mobility degradation has the same impact on I_D in a transistor that operates in subthreshold regime compared to one that operates in strong inversion. However, the radiation-induced threshold voltage shift will impact I_D exponentially in a subthreshold MOS

compared to a square law impact in a strong inversion MOS. In addition, the threshold voltage shift and the carriers mobility degradation will modify the transconductance (g_m) and the drain-source resistance (r_0) of a transistor operating in subthreshold/saturation through the I_D (neglecting the channel length modulation (λ)):

$$g_m = \frac{\delta I_D}{\delta V_{GS}} = \frac{I_D}{nU_T} \tag{4}$$

$$r_0 = \frac{1}{\lambda I_D}. \tag{5}$$

2.2. Displacement Damage Effects

High energy particles (∼1 MeV), can induce crystal defects such as atomic lattice displacement (bulk damage), where atoms are displaced from their proper locations [58–61]. However, there is considerable DD even below (∼1 MeV). This non-ionization effect is common when the impinging particle is electron, neutron or proton and can create Frenkel defects (vacancies or interstitials) [62]. The displacement damage will potentially degrade the minority carrier lifetime, the carrier mobility and the carrier concentration.

The non-ionizing energy loss (NIEL) which causes the displacement damage is mostly associated with bipolar transistors, whose operation depends on minority carrier lifetime [63]. However, the conduction of a MOS transistor operating in the subthreshold regime is due to the diffusion of minority carriers in the channel (caused by the lateral concentration gradient). Therefore, it is expected that displacement damage will affect the subthreshold MOS in a similar manner as a bipolar transistor.

2.3. Single Event Effects

Analog single-event transients (ASETs) are evanescent fluctuations of electrical charges in integrated circuits (IC). They may be observed when high-energy particles (alpha, protons and heavy ions), such as those found in the space environment (trapped particles in the Van Allen belts, solar energetic particles and galactic cosmic rays) [64], collide with analog ICs. When a high-energy particle penetrates the silicon substrate it ionizes the target material along its path. The ionized region is proximal to the ion path, generating a multitude of electron–hole pairs [65–68] in the vicinity of the ion track. Built-in electric fields or fields created by normal biasing conditions separate the pairs, leaving excess charge after the event. The excess charge injected at a sensitive circuit node can potentially disrupt the reliable functionality of the circuit, causing instantaneous or permanent failures.

Observable transients are most likely to occur when the impinging particles are heavy ions, such as silicon (Si), krypton (Kr) and xenon (Xe), which are high energy ions that have a high linear energy transfer (LET), and hence deposit more excess charge. The effect of the ASETs induced by these heavy ions on the desired signals, depends on the sensitivity of the particular analog circuit to the injected charge. The sensitivity is dependent on the circuit architecture, the devices' operating speed and the nominal operating voltage. Furthermore, as the technology nodes scale down, the decreased transistor geometries and thinner gate oxides, reduce the charge required to disrupt normal functionality, thus making the circuits more prone to ASETs. Thus in deep sub-micron technologies [69–71] ASETs are of major concern and impose critical issues for the microelectronic circuits reliability, while much ongoing research deals with characterizing the optimum circuit topologies, technology processes, devices and design approaches in order to mitigate ASETs in space applications [36,39,40,45,52,72–86].

3. Proposed Reference Circuits

In this work, two versions of low-power, subthreshold reference circuits were extensively assessed for the space environment. The design and analog performance tests for non-radiation environments was presented in [17,51,87]. This paper focuses on the radiation tolerance of two subthreshold topologies. The characterization experiments include measured results of the post-fabricated ICs

in a wide temperature sweep, as well as measured results after exposing the circuits to γ-rays, X-rays, protons and heavy ions (silicon, krypton and xenon).

The designs were fabricated using TowerJazz Semiconductor's CMOS 0.18 µm technology. Both circuits utilize enclosed layout geometries [88] for all key NMOS transistors. These use enclosed layout geometry since they are prone to leakage currents from positive charges that are trapped in the deep-trench isolation structure and attract negative charges from the substrate, that form a parasitic channel along the edges of a planar layout geometry. The PMOS transistors are not prone to this effect, since their charge carriers are holes and trapped positive charges in oxide structures decrease the leakage current. The presented circuits are MOS-based voltage references, operating in subthreshold, which combine individually-linearized PTAT and CTAT currents. The proposed topologies incorporate two different types of polysilicon resistors. These, when combined with a subthreshold NMOS transistor, lead to a high-order curvature correction of the reference voltage, giving better performance across a wide range of temperatures. The two topologies have a high-impedance node at the drain of MP_3 transistor of the core structure. In addition, the reference voltage (VR)1 topology has an extra high-impedance node at the drain of MP_6 transistor.

Subthreshold operation of circuits and systems would be extremely beneficial in space microelectronics due to the limited energy sources. However, subthreshold circuits have to prove their reliability for such missions, where several radiation sources impact their electrical parameters. Therefore, this work investigates the resilience of subthreshold circuits with high total doses for a wide range of radiation sources. The circuits under evaluation are designed using the standard radiation-hardening-by-design (RHBD) techniques such as, extensive guard-rings, minimum gate extension to avoid leakage from the channel edge due to shallow trench isolation (STI), small layout and specialized circuit architectures.

The first reference circuit [51] is a low-power, wide-temperature-range topology which achieves a low TC over a temperature range of 190 °C, whilst being biased at a low supply voltage of 0.75 V and consuming only 4 µW of power. The circuit's topology is shown in Figure 1 and its layout in Figure 2a. This circuit occupies an area of 0.039 mm^2.

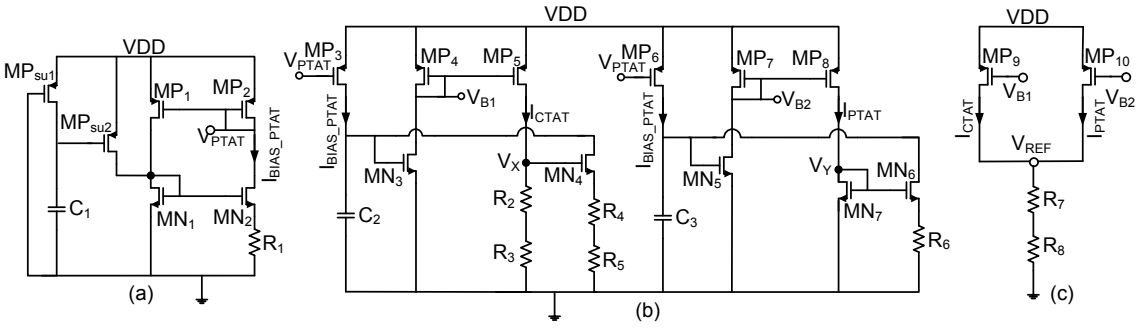


Figure 1. Schematic of the proposed voltage reference (VR1) [51]. (**a**) Proportional to absolute temperature (PTAT) current generator including a start up circuit, (**b**) main module utilizing the proposed novel method of high-order curvature correction of the reference voltage, (**c**) reference voltage output which sums the PTAT and complementary to absolute temperature (CTAT) curvature corrected currents.

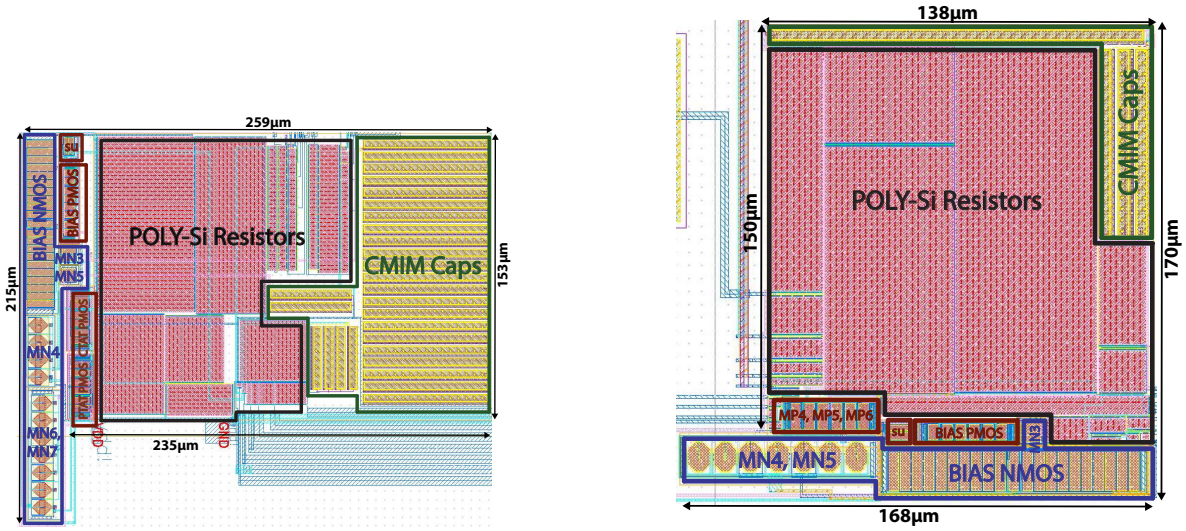
The reference output voltage is generated by summing I_{PTAT} and I_{CTAT} currents across a resistance. This voltage is equal to:

$$V_{REF} = (I_{PTAT} + I_{CTAT}) \times R_{7,8} \quad (6)$$

where $R_{x,y} = R_x + R_y$. A detailed expression of the first reference voltage (VR1) can be expressed as:

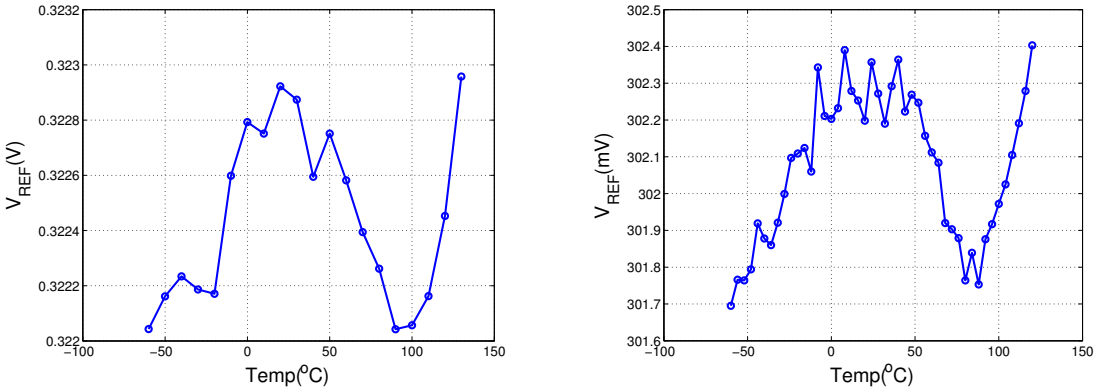
$$V_{REF} = R_{7,8} K_{MN7} I_0 \exp\left(\frac{V_{GS7} - V_{TH}}{n U_T}\right) + \frac{R_{7,8}}{R_{2,3}} V_{GS4} + \frac{R_{7,8} R_{4,5}}{R_1 R_{2,3}} U_T \ln\left(\frac{K_{MN2}}{K_{MN1}}\right). \quad (7)$$

The measured post-trimmed TC at a bias voltage of 0.75 V is 15 ppm/°C for an extended temperature range of 190 °C (−60 °C to 130 °C) and is shown in Figure 3a.



(**a**) (**b**)

Figure 2. Layout of the proposed voltage references. (**a**) Layout of VR1 [51]; (**b**) Layout of VR2 [17].



(**a**) (**b**)

Figure 3. Measured temperature coefficient (TC) of the two reference circuits. (**a**) Measured TC of 15 ppm/°C of the first reference circuit; (**b**) measured TC of 12.9 ppm/°C of the second reference circuit.

The second reference circuit [17] is also a low-power, wide-temperature-range, curvature-compensated topology. The proposed topology achieves a temperature sensitivity of 12.9 ppm/°C for a temperature range of 180 °C (−60 °C to 120 °C) at a bias voltage of 0.7 V, whilst consuming 2.7 µW. It occupies an area of 0.023 mm^2.

The schematic of the proposed design is illustrated in Figure 4 while the layout is shown in Figure 2b. The topology consists of three main modules. A PTAT circuit, including the start-up circuit (MP_{su1}, MP_{su2}, C_1), is shown in Figure 4a, which generates a PTAT current for supplying the module of Figure 4b [15,89]. Figure 4b shows the core module, where both the linear and the non-linear compensation predominantly takes place.

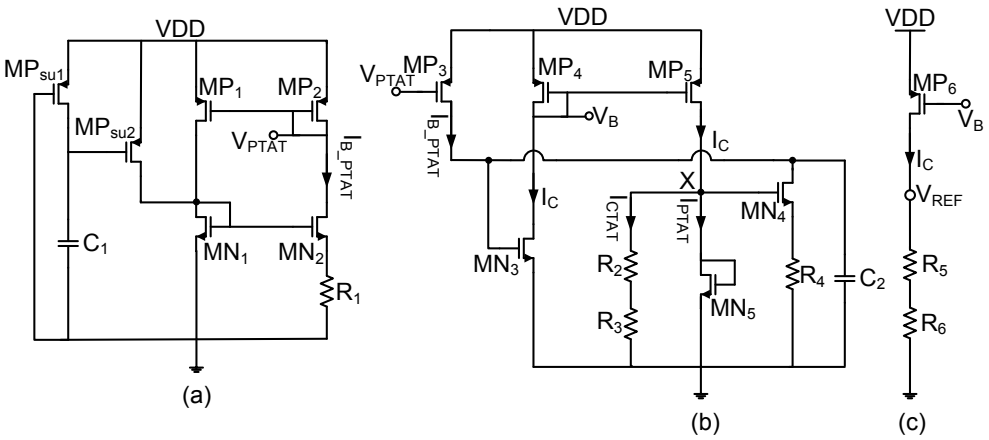


Figure 4. Schematic of the proposed voltage reference (VR2) [17]. (**a**) PTAT circuit including the start up (MPsu1, MPsu2,C1), (**b**) core module for implementing the high order compensation, (**c**) output stage to supply the reference voltage.

The reference voltage at the output of the proposed topology in Figure 4 can be expressed as:

$$V_{REF} = I_C \times R_{5,6}, \tag{8}$$

where $R_{x,y} = R_x + R_y$ and the current I_C consists of the currents through resistors R_2 and R_3, and the current through the transistor MN_5

The detailed equation for the second output reference voltage (VR2) is described by:

$$\begin{aligned} V_{REF} = \frac{V_{GS4}R_{5,6}}{R_{2,3}} + \frac{R_4R_{5,6}}{R_1R_{2,3}} \times U_T \ln\left(\frac{K_{MN2}}{K_{MN1}}\right) \\ + R_{5,6}K_{MN5}I_0 \exp\left(\frac{V_{GS5} - V_{TH}}{nU_T}\right), \end{aligned} \tag{9}$$

where I_0 is:

$$I_0 = \mu C_{ox}(n-1)U_T^2, \tag{10}$$

where μ is the mobility of carriers in the device channel, C_{ox} is the oxide capacitance per unit area and n is the subthreshold slope factor.

4. Experimental Measurements on SET Irradiation Effects (Heavy Ions)

The proposed reference circuits were characterized at Radiation Effects Facility (RADEF) at the University of Jyvaskyla, Finland, for ASETs. Heavy ions (Si, Kr and Xe) from RADEF's standard 9.3 MeV/µm cocktail beam were used in order to provide different LET characteristics, so as to extract their cross-section (σ). The circuit irradiations were performed in air with a Kapton foil thickness of 25 µm and air thickness of 5 mm. During irradiation, the circuits were biased at their nominal supply voltages and the ASETs were recorded using a high sampling-rate oscilloscope (Agilent Technologies, Inc., Santa Clara, California, United States, DSO9104A 1 GHz/20 GS/s). The oscilloscope was set to record all the transient segments above a threshold trigger level (12 mV). This level was higher than the reference circuit noise floor and it ensures that stray electromagnetic fields at the testing facilities would not trigger the oscilloscope.

The RADEF's heavy ions cocktail provided Si ions with a LET(Si) of ∼6.9 MeV·cm^2/mg, Kr ions with a LET(Si) of ∼36.1 MeV·cm^2/mg and Xe ions with a LET(Si) of ∼64.7 MeV·cm^2/mg. The charge deposited in the targeted material is greater at higher value of LET.

The cross-section, σ, is a metric to evaluate the resilience of the circuits under test when exposed to heavy-ions and can be expressed as:

$$\sigma = \frac{N_{ASET'S}}{\phi} \quad (\text{cm}^2), \tag{11}$$

where $N_{ASET'S}$ is the observed number of ASET events and ϕ is the uniform particle fluence (particles/cm^2).

The measured σ of the two voltage references are shown in Figure 5. The VR2 topology did not exhibit any sensitivity to Si ions, while an overall comparison shows that VR2 had less sensitivity compared to the VR1 circuit. The measured SET durations for the two circuits (VR1 and VR2) are shown in Figures 6–8 for silicon, krypton and xenon respectively. The VR2 circuit exhibits lower transients' duration compared to VR1.

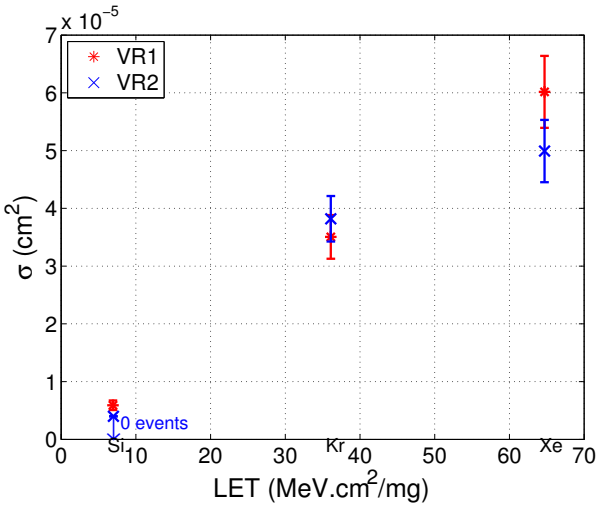


Figure 5. Measured Cross-Section of the two voltage reference circuits (VR_1 and VR_2) while exposed to silicon, krypton, and xenon ions.

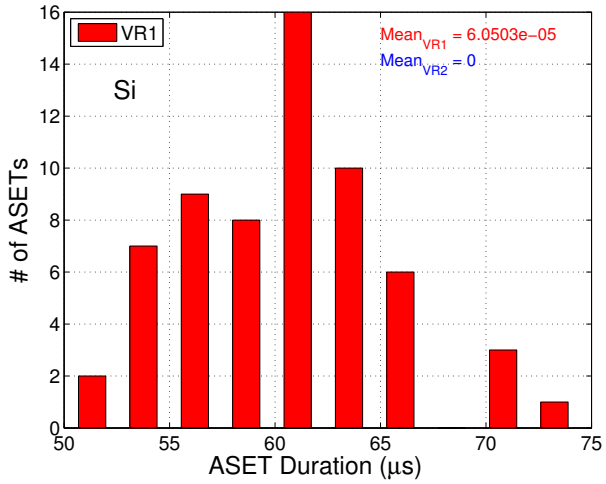


Figure 6. Measured number of ASETs versus ASETs duration for VR1 and VR2 circuits when exposed to Silicon.

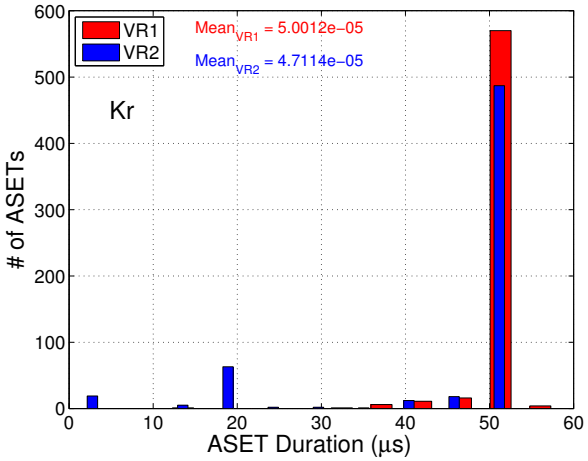


Figure 7. Measured number of ASETs versus ASETs duration for VR1 and VR2 circuits when exposed to Krypton.

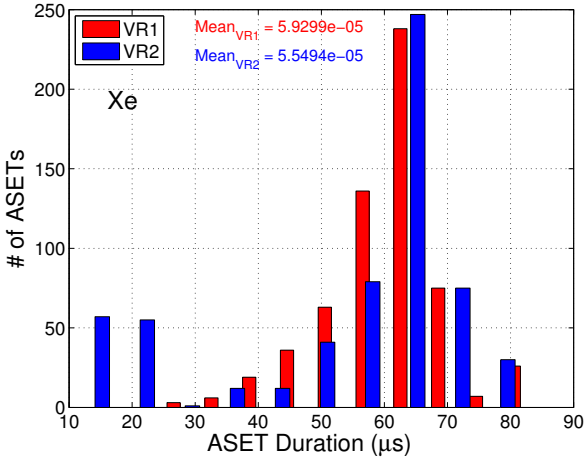


Figure 8. Measured number of ASETs versus ASETs duration for VR1 and VR2 circuits when exposed to Xenon.

The measured SET amplitudes for the two circuits (VR1 and VR2) are shown in Figures 9–11 for silicon, krypton and xenon respectively. The VR2 circuit exhibits smaller amplitudes compared to VR1.

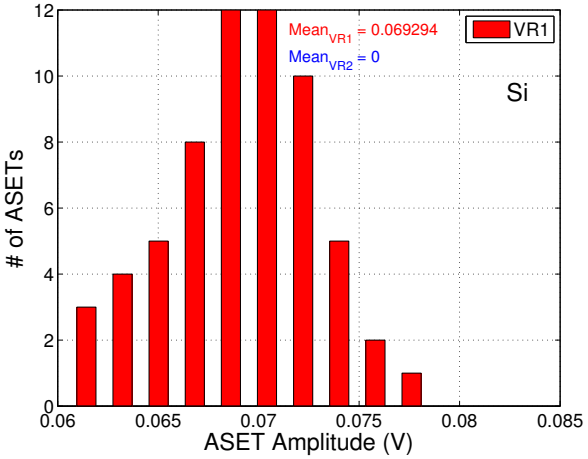


Figure 9. Measured number of ASETs versus ASETs peak amplitude for VR1 and VR2 circuits when exposed to Silicon.

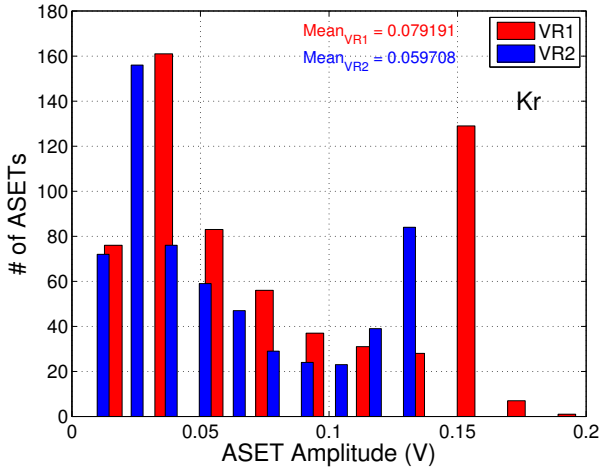


Figure 10. Measured number of ASETs versus ASETs peak amplitude for VR1 and VR2 circuits when exposed to Krypton.

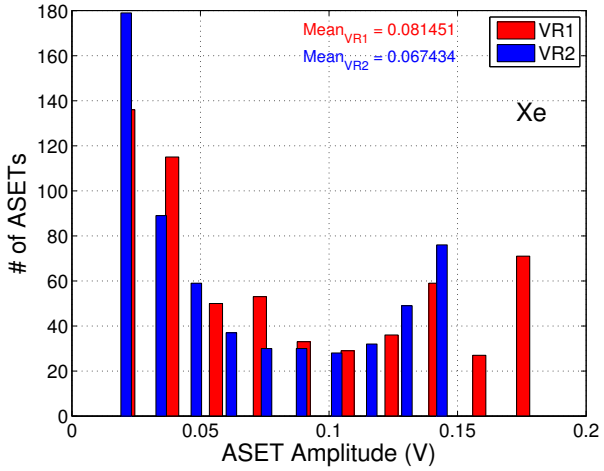


Figure 11. Measured number of ASETs versus ASET's peak amplitude for VR1 and VR2 circuits when exposed to Xenon.

The fact that VR2 outperforms VR1, in terms of σ, SETs' durations and amplitude, is possibly due to the smaller area of VR2 compared to VR1, since their circuit topology and operating conditions are very similar.

In general, the subthreshold circuits show somewhat higher sensitivity to heavy ions, in terms of σ and SETs' durations, compared to the strong inversion ones which were evaluated in previous work [90] by the authors. This is partly due to the lower supply voltage, which in turn needs less amount of deposited charge from the impinging ion in order to alter their nominal operating conditions of a particular circuit node. Furthermore, subthreshold circuits need more time to recover from a transient because of the lower current drive capability and the slower feedback. However, due to the limited bandwidth, longer transient durations are required in order to appear at the output, which gives subthreshold circuits an advantage. Part of the higher sensitivity could also be attributed to the larger silicon area of those topologies compared to the ones in [90]. The SETs' amplitudes in subthreshold and strong inversion circuits in [90] are comparable. This is probably due to the same reason described above, where the larger time constants of the subthreshold circuits tend to filter out some of the transients. An additional advantage of subthreshold circuits when exposed to heavy ions is that it is less probable to latch-up due to parasitic bipolar effect because of much smaller currents. This is a big advantage since parasitic bipolar effect could be fatal for a device and therefore an entire system.

5. Experimental Measurements on TID Irradiation Effects (γ-rays and X-rays)

In this section, a complete experimental characterization under γ-rays and X-rays TID induced effects was performed in order to evaluate the resilience of subthreshold reference circuit topologies against TID.

5.1. γ-ray Irradiation

The γ-ray irradiation was performed at the Radiation Physics Laboratory of the Universidade de Santiago de Compostela, using an AECL Theratron 780 Co-60 unit at room temperature. Dose rate and TID were monitored in real time by a 0.6 cm^3 therapy level ionization chamber connected to a reference class electrometer. The chamber and chips were positioned behind a 2 mm lead slab and 1 mm aluminium slab, to provide transient charge particle equilibrium in the gamma-ray field originating from the Co-60 source. Measured charge was converted to absorbed dose in air first, by employing the value of mean energy to produce a pair in air by a Co-60 beam (W_{Co60} = 33.97 J/C) and the mass of air enclosed in the chamber cavity with the appropriate correction due to ambient conditions. The correction factor between dose in air and dose in silicon inside the chips was calculated by Monte Carlo simulations (EGSnrc code) employing a realistic definition of geometries of the therapy unit, the ionization chamber and the chips.

Four chips from two different wafers (two chips from each wafer) were irradiated with γ-rays at a dose rate of 25 krad/h(Si) up to a total dose of 5.153 Mrad(Si), followed by room temperature annealing steps with the last annealing step measurement taken 25.97 h after the end of irradiation. The circuits under test were irradiated and measured at room temperature, with the supplies biased at nominal voltage during irradiation. The output voltages and current consumption of each circuit were measured at regular dose steps. The measured results of the relative output voltage are shown in Figure 12 for VR1 circuit and Figure 13 for VR2 circuit. Different wafers are expected to have some variation on device parameters, like threshold, voltage due to process variations. The measured results of the relative current consumption are shown in Figure 14 for VR1 circuit and Figure 15 for VR2 circuit.

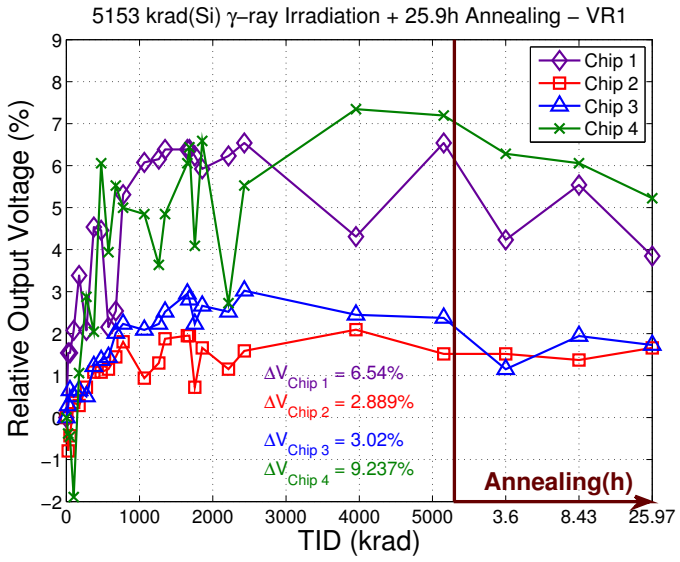


Figure 12. Relative output voltage (%) of the reference voltage (VR)1 when exposed to γ-rays at a dose rate of 25 krad/h(Si).

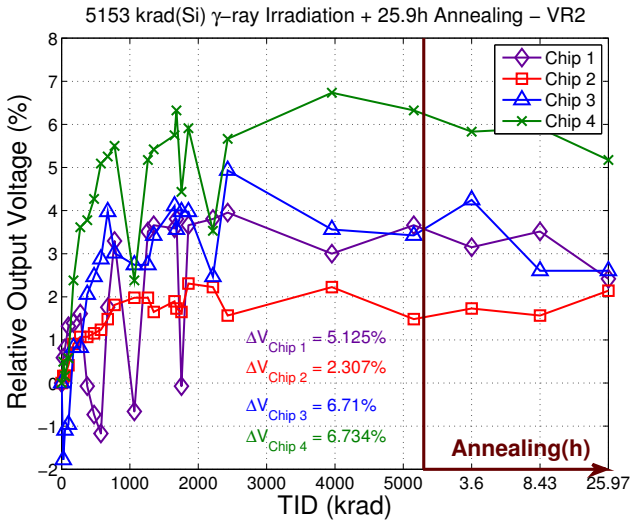


Figure 13. Relative output voltage (%) of the VR2 when exposed to γ-rays at a dose rate of 25 krad/h(Si).

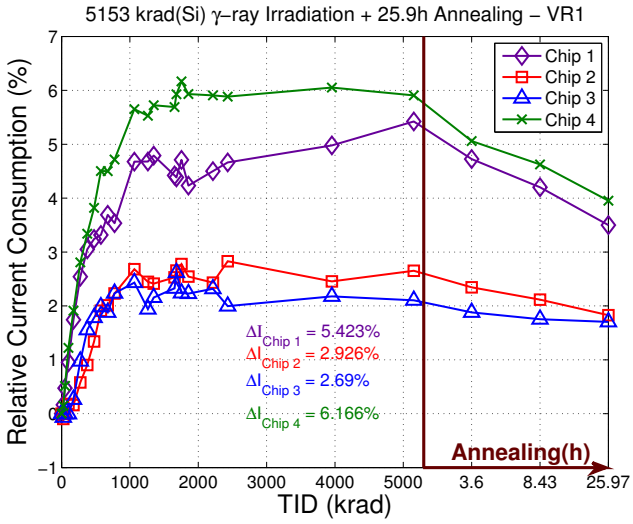


Figure 14. Relative current consumption (%) of the VR1 when exposed to γ-rays at a dose rate of 25 krad/h(Si).

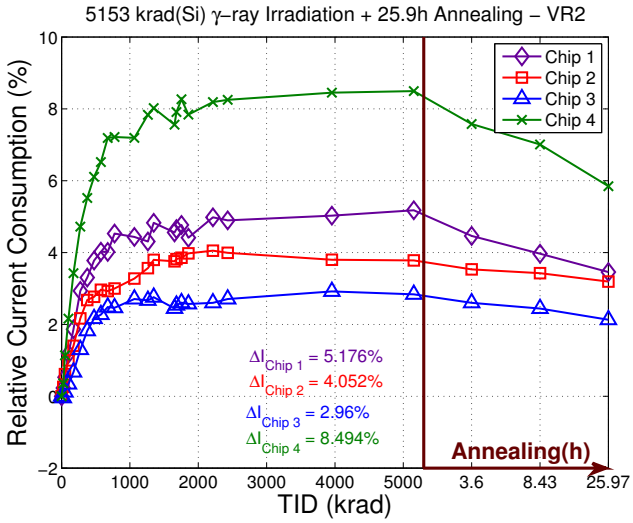


Figure 15. Relative current consumption (%) of the VR2 when exposed to γ-rays at a dose rate of 25 krad/h(Si).

The smallest output voltage variation is achieved by the VR2 circuit of chip 2 which is 2.307% and the highest by the VR1 circuit of chip 1 which is 9.237%. The two voltage references (VR1 and VR2) show comparable performance in terms of γ-rays irradiation TID effects, which for some of the chips is remarkable when considering the high total dose. The variation between different chips is due to the device mismatch within a circuit as well as due to process variation between different dies. Both circuits show a rising trend for total doses up to 1 Mrad, while for higher doses the output voltage remains almost unaffected. This could be explained by the competition between the interface state trapped charge and the oxide trapped charge. The interface state trapped charge occurs much slower and has a counterring effect in NMOS devices as opposed to the oxide trapped charge. Furthermore, when activated, interface trapped charge dominates the oxide trapped charge. The measured relative current consumption in Figures 14 and 15 show a similar trend with the relative output voltage variations. The current consumption variations are due to threshold voltage induced drain current variations as well as edge leakage currents due to STI trapped charge. During annealing at room temperature, the output voltage and current consumption partially recover. However, the interface trapped charge would need very high temperatures in order to anneal.

5.2. X-rays Irradiation

Two sessions of X-rays irradiation were performed. The first session was performed up to a total dose of 3.7 Mrad(Si) at the Radiation Physics Laboratory of the Universidade de Santiago de Compostela. The second session was performed up to a total dose of 80 Mrad(Si) at the Department of Information Engineering of the University of Padova. During both irradiation sessions all the circuits within the chips were biased at nominal supply voltage and their output reference voltages were measured at regular dose steps during irradiation.

5.2.1. X-ray Irradiation up to 3.17 Mrad(Si)

The irradiation was performed by a TW50 X-ray beam, delivered by an Oxford Instruments Neptune tube, with an added filtration by 1.1 mm of aluminum. X-ray beam outputs are generally measured by means of thin entrance window air filled ionization chambers. Conversion to absorbed dose to a relatively high atomic matter (high Z) medium like Silicon, surrounded by other higher than air Z materials, such as those present in a silicon chip, is not trivial. This is because the ratio of the absorbed dose to silicon and absorbed dose to air in the chamber varies sharply as a function of X-ray photon energy, due to enhanced photoelectric effect cross section. The beam output was characterized by measuring the X-ray spectrum and the exposure rate. The spectrum was measured with an AMPTEK CdTe scintillator connected to a MultiChannel Analyzer (MCA). The 50 keV tail was employed to calibrate the MCA in terms of photon energy. The exposure rate was measured with a PTW 23344 plate parallel X-ray chamber connected to an IBA DOSE-1 electrometer. The measured exposure rate was first converted to absorbed dose in air and then to absorbed dose in silicon in the area of the circuits under test. This was done by employing EGSnrc Monte Carlo code. The measured spectrum was used as the energy distribution of the Monte Carlo primary source. This spectrum was fine-tuned in order to reproduce experimental percent depth doses of the unfiltered 50 keV beam. A conversion factor was determined as the ratio of Monte Carlo absorbed dose in silicon inside the circuits under test and Monte Carlo absorbed dose to air inside the ionization chamber cavity.

In this first session, the two chips were irradiated with X-rays using a dose rate of 8.75 rad(Si)/s up to a total dose of 1.3 Mrad(Si) and then irradiated with a dose rate of 6.56 rad(Si)/s, up to a total dose of 3.173 Mrad(Si). The circuits were irradiated and measured at room temperature, with their supplies biased at nominal supply voltage. The output voltages as well as the current consumption were measured at regular dose steps during irradiation. Annealing steps at room temperature followed the irradiation, with the last annealing measurement taken 465 min after the end of irradiation. The measured results of the relative output voltage of the two chips of VR1 and VR2 reference circuits are shown in Figure 16 and their relative current consumption is shown in Figure 17.

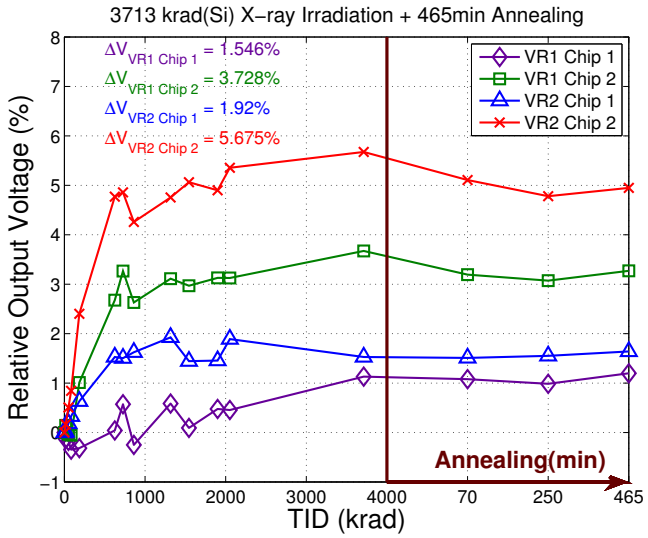


Figure 16. Relative output voltage (%) of the VR1 and VR2 when exposed to X-rays at a dose rate of 8.75 rad(Si)/s.

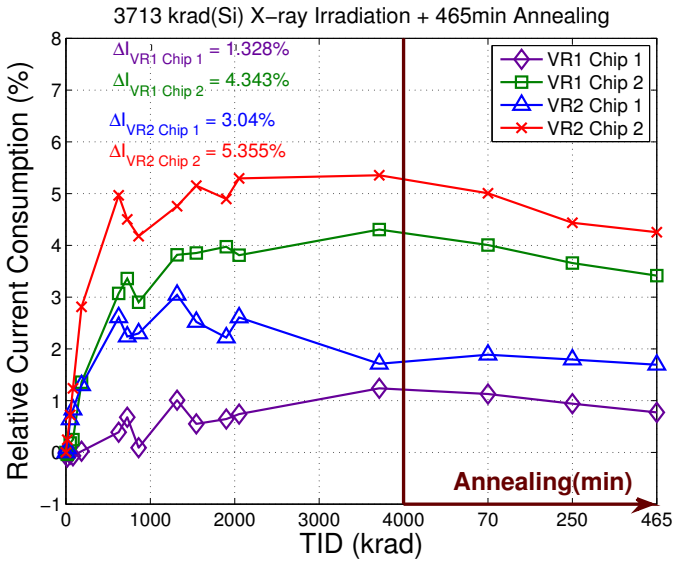


Figure 17. Relative current consumption (%) of the VR1 and VR2 when exposed to X-rays at a dose rate of 8.75 rad(Si)/s.

The smallest output voltage variation was achieved by the VR1 circuit of chip 1 which was 1.546% and the highest by the VR2 circuit of chip 2 which was 5.675%. The variation between different chips is again due to the process and mismatch variations between the circuits' devices. This can be justified by the fact that all the circuits of chip 1 demonstrated better performance than the ones of chip 2. Both circuits showed changing properties trend for total doses up to 800 krad, which then stabilizes at higher doses. This effect was in agreement with the γ-rays experiments and can be explained by the opposite effect of the interface state trapped charge and the oxide trapped charge on the device characteristics.

The measured relative current consumption in Figure 17 show almost identical trend with the relative output voltage variations. The current consumption variations can be attributed to the threshold voltage variation induced drain current variation as well as edge leakage currents due to STI trapped charge. During annealing at room temperature, the output voltage and current consumption of the VR1 and VR2 circuits of chip 2 (exhibited the highest TID variation) showed some recovering, while the corresponding circuits of chip 1 did not exhibit any significant change.

5.2.2. X-ray Irradiation up to 80 Mrad(Si)

In this session, a chip with the circuits under test was irradiated at a room temperature at the Department of Information Engineering of the University of Padova with 10-keV X-rays using a dose rate of 300 rad(Si)/s up to a total dose of 80 Mrad(Si). During irradiation both the circuits were biased at their nominal supply voltage. The output voltages were measured at regular dose steps during irradiation as well as during room temperature annealing, after the end of irradiation. The measured results for the relative output voltage are shown in Figure 18.

The two circuits showed similar performance to TID induced effects, where the smallest output voltage variation was achieved by the VR1 circuit which was 11.51% and the highest by the VR2 circuit which was 12.9%. The TID induced output voltage variations as shown in Figure 18 revealed an important outcome. Both circuits exhibited significant changes up to 10 Mrad, while for higher total doses they stabilized and then recovered significantly. This is in agreement with γ-rays and X-ray experiments and could again be explained by the competition between the interface state trapped charge and the oxide trapped charge. Another reason for this recovering during irradiation is the possible saturation of the oxide trapped charge first and then the interface trapped charge, which can be caused by the high total dose exposure. This can be supported by (1) and (2), where the irradiation induced rate of threshold voltage shift will reduce from square to linear dependence on oxide thickness. During annealing, at room temperature, the output voltage recovered at a higher rate.

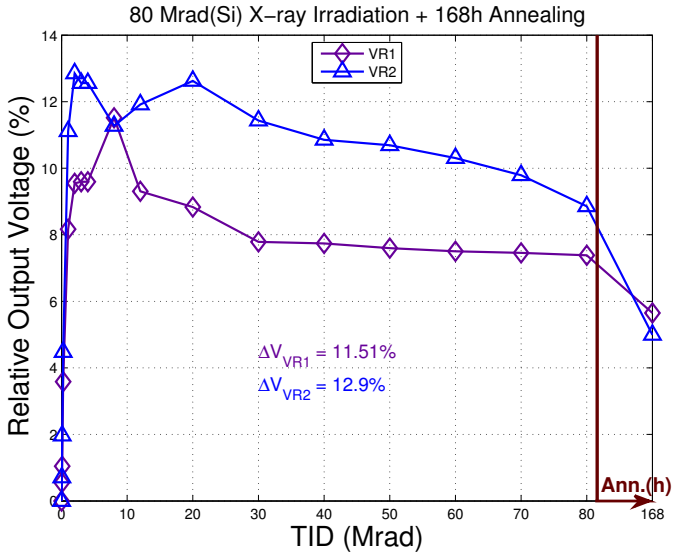


Figure 18. Relative output voltage (%) for the VR1 and VR2 when exposed to a 10 keV X-rays at a dose rate of 300 rad(Si)/s.

6. Experimental Measurements for TID and DD Irradiation Effects (Protons + X-rays and Protons)

The space radiation mixture is to a large extent composed from high-energy protons [91]. Therefore, in this section, the different topologies were irradiated with protons and X-rays and only-protons for the experimental characterization of DD/TID radiation-induced effects. These tests were required in order to classify the robustness of the subthreshold circuits in a more realistic scenario. It has to be noted that the effects induced by DD and TID interacted in a complicated fashion and were not simply additive [91].

6.1. Irradiation with Protons and X-rays

In this session the chip with the two circuits was irradiated with a 3 MeV proton beam in vacuum, with a flux of 10^9 p/cm^2·s, up to a fluence of 1.47×10^{12} p/cm^2, corresponding to a total ionizing dose of 2 Mrad(Si). This was followed by three days of room temperature annealing. The circuits were unbiased during irradiation and they were biased just after the end of the irradiation in order to measure their output voltage. Then, they were remeasured again after one week (168 h) of room temperature annealing. The results of this irradiation session are shown in Figure 19 for the relative output voltage versus TID.

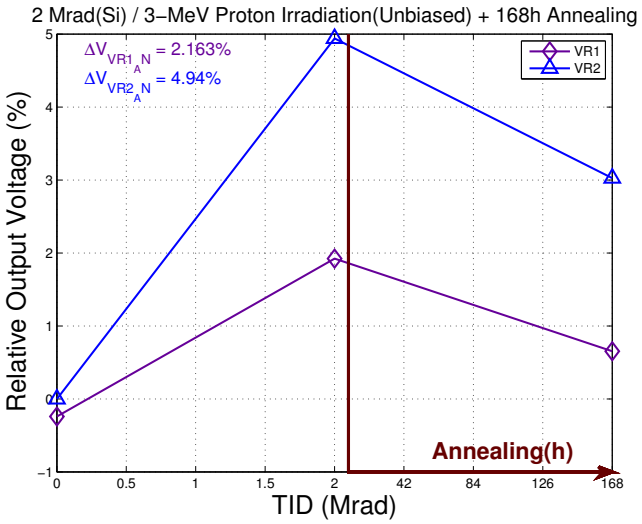


Figure 19. Relative output voltage (%) of the VR1 and VR2 when exposed to protons. The chips were irradiated unbiased with 3 MeV protons in vacuum, up to a fluence of 1.47×10^{12} p/cm^2 with a flux of 10^9 p/cm^2·s. This corresponds to a total ionizing dose of 2 Mrad(Si), followed by three days of annealing.

The same chip, that was irradiated with a total dose of 2 Mrad(Si) of protons, was further irradiated with 10 keV X-rays after the proton exposure and annealing step. The X-ray irradiation and subsequent annealing were performed at room temperature, with all the circuits biased at the nominal supply voltage. A total dose of 78 Mrad(Si) was delivered through this X-ray irradiation session, so that a total dose of 80 Mrad(Si) was accumulated on the device, using a dose rate of 300 rad(Si)/s. The output voltages were measured at regular dose steps during irradiation at room temperature. Annealing steps followed the irradiation at room temperature, with the last annealing measurement taken one month (720 h) after the end of irradiation.

The results of the proton and subsequent X-ray irradiation are shown in Figure 20. The total dose reported on the X-axis of Figure 20 is the sum of the proton and the subsequent X-rays irradiation.

The VR1 circuit topology shows more resilience in comparison to the VR2 topology. The differences of the output voltage in Figure 20 when compared to the same irradiation dose of Figure 18 is possibly due to displacement damage that was induced from the proton irradiation on the subthreshold biased transistors. A 3 MeV proton beam with such a high fluence (1.47×10^{12} p/cm^2) delivered both, TID as well as DD, for the equivalent dose of about two Mrad(Si). The conduction of a MOS transistor in sub-threshold regime was due to diffusion of minority carriers in the channel, where minority carrier lifetime was affected by DD in a similar manner as in bipolar transistors.

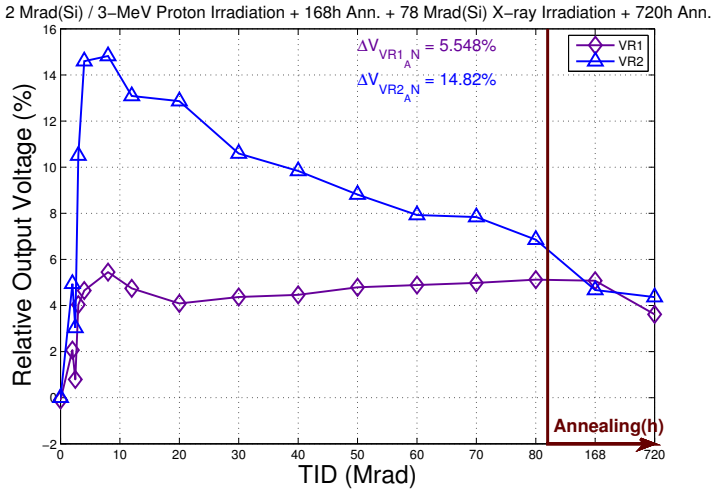


Figure 20. Relative output voltage (%) of the VR1 and VR2 when exposed to Protons and X-rays. The chips were irradiated unbiased with 3 MeV protons in vacuum, up to a total dose of 2 Mrad(Si), followed by three days of annealing. Then they were further irradiated with 10keV X-rays up to 78 Mrad(Si) with a dose rate of 300 rad(Si)/s. The dose reported on the x-axis is the sum of the proton and the subsequent X-ray irradiation which is 80 Mrad(Si).

6.2. Irradiation with Protons

In this irradiation session, another chip was irradiated in air with protons, at the Svedberg Laboratory in the University of Uppsala. The nominal primary proton energy was 180-MeV. In order to create a uniform proton field at the position of the chips under test, the primary proton beam was scattered by a Ta foil of 1.5 mm thickness. The chips were positioned at a distance of 200 cm from the foil. The average proton energy at the chips under test position amounted to 170.5-MeV. During irradiation, the incident proton beam was monitored by a telescope consisting of two scintillators, calibrated using a thin-film breakdown counter equipped with a fission foil. The telescope detected protons scattered by a stainless steel foil at the end of the vacuum pipe.

The chip was irradiated with the 170.5 MeV protons at the fluence of 3.9×10^{11} cm^{-2}. By the end of the experiment it had accumulated a total dose of 1400 krad(Si), at steps of 25 krad for low TID values, with wider steps for higher TID values, with an intermediate annealing step of 15 h. The irradiation and measurements were performed at room temperature with all the circuits biased at nominal supply voltage.

The output voltage of the circuits was measured at regular dose steps and is shown in Figure 21, where VR1 outperforms VR2. Both circuits show a considerable change for total doses up to 900 krad, which saturates at higher doses. This again agrees with the experimental sessions of γ-rays and X-rays and could be attributed to the same reasons explained above. The relative current consumption is shown in Figure 22 where the current consumption trend was identical with the relative output voltage variations trend. This is because the STI edge leakage current as well as the threshold voltage shift variations (gate oxide and interface states trapped charge) modify the current drained by the transistors and therefore the total current consumption of the circuits was modified accordingly. The current was increased mostly in the non-core NMOS transistors where planar layout was utilized. However, all transistors (including enclosed layout geometry ones) had small current variations due to threshold voltage shifts. During annealing both circuits show significant recovery in terms of output voltage as well as current consumption due to possible annealing of oxide trapped charge.

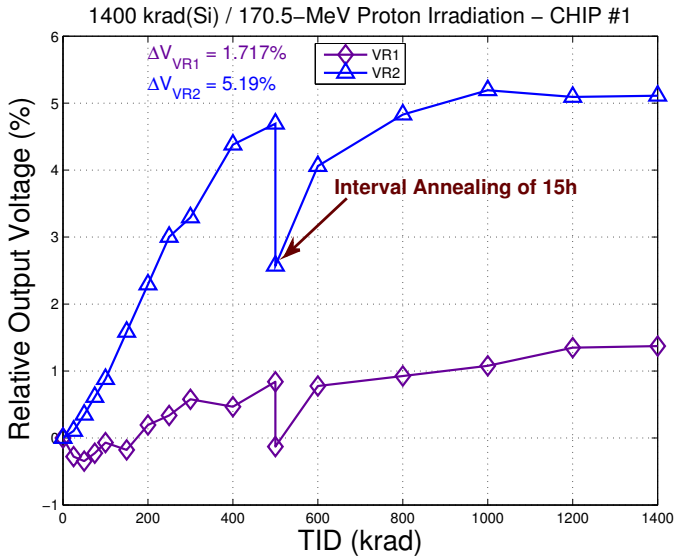


Figure 21. Relative output voltage change (%) of the VR1 and VR2 when exposed to 170.5-MeV Protons irradiation, accumulating a total dose of 1400 krad(Si) with a fluence of 3.9×10^{11} cm^{-2}. An interval annealing step at room temperature was performed at 500 krad(Si).

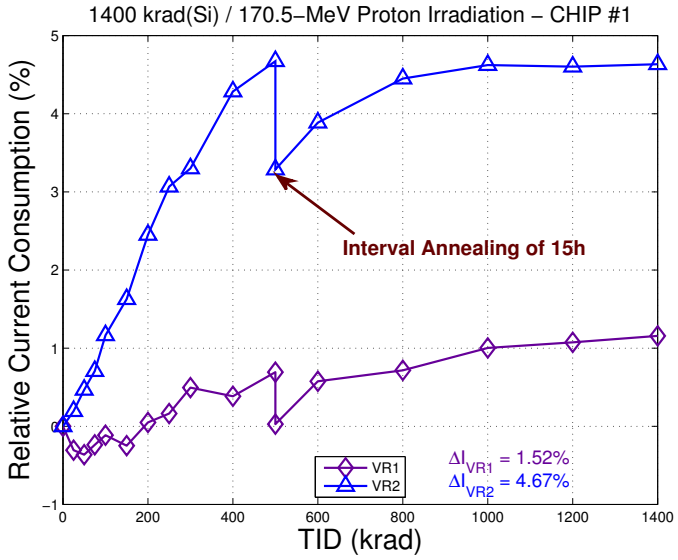


Figure 22. Relative change in current consumption (%) of the VR1 and VR2 when exposed to 170.5 MeV Proton irradiation, accumulating a total dose of 1400 krad(Si) with a fluence of 3.9×10^{11} cm^{-2}. An interval annealing step at room temperature was performed at 500 krad(Si).

7. Discussion on Subthreshold Radiation Effects

In this paper we have presented the results of radiation tests involving two subthreshold circuits. When comparing TID radiation-induced effects between subthreshold and strong inversion circuits, the major difference is the dependence of the drain current to threshold voltage shift. This dependence is exponential in subthreshold circuits as opposed to square-law dependence in strong inversion circuits. This is the major disadvantage of subthreshold circuits in radiation environment, however this disadvantage is rapidly diminishing in deep sub-micron semiconductor technologies, where according to (1) and (2) the oxide thickness reduction will diminish the radiation-induced threshold voltage shift. Thus, in deep sub-micron technologies, subthreshold circuits will potentially emerge as an attractive and promising solution for space microelectronics. The leakage currents due to trapped charge at the STI oxides will have more relative impact in subthreshold circuits compared to strong inversion

ones, since the actual current through the channel could be in the order of the STI induced leakage currents. However, this disadvantage, which concerns only NMOS devices, can be remedied by using enclosed layout geometry transistors at the layout level. On the other hand, the low-voltage operation of subthreshold circuits applies lower electric fields across the oxides. This will reduce the rate of electron–hole separation and increase the probability of recombination. Therefore, this induces lower trapped charge in the oxides and hence lower will be the radiation-induced threshold voltage shift and leakage current.

SETs usually originate from particle strikes which traverse reverse-biased pn-junctions or areas with strong electric fields. Built-in electric fields or fields created by normal biasing conditions separate the pairs, leaving excess charge after the event. This is particularly a problem at the transistor's drain terminal, especially with the deep submicron technologies, where the generated plasma of e-h pairs drifts apart because of the high electric fields across the depletion region. When comparing SET radiation-induced effects between subthreshold and strong inversion circuits, the major difference is the supply voltage. The gate oxide thickness (depends on the type of device that is selected) and the supply voltage, both affect the amount of energy needed in order to alter the transistor's normal operating conditions. Therefore, the lower supply voltage of subthreshold circuits will require less charge and therefore less energy from the impinging ion in order to alter its nominal state, which makes them more vulnerable compared to strong inversion circuits. On the other hand, the advantage of low-voltage operation of subthreshold circuits is the lower electric field across the pn-junctions which reduces the amount of separated e-h pairs as well as the charge collected at the impinged node. An additional advantage of subthreshold circuits is that it is not possible to form a BJT through the substrate (parasitic bipolar effect) after a heavy ion strike [46].

An important advantage of subthreshold regime, which applies in both TID and SET effects, is that the drain-source voltage for saturation is 4 kT $\approx$ 104 mV which, in contrast with strong inversion regime, is very low and independent of the gate-source voltage and threshold voltage. Therefore, in contrast with strong inversion regime, it is not easy to get a subthreshold transistor out of saturation region due to irradiation-induced effects. This has been proven throughout all the experimental sessions in this work, where there was not any complete functional failure observed, even in very high TID irradiation or heavy ion strikes.

8. Conclusions

A comprehensive evaluation of two subthreshold voltage reference circuits with respect to their resilience to SEE, TID and TID/DD was performed. The evaluation is supported by measured results with γ-rays, X-rays, protons and heavy ions. The high total doses applied in this range of experiments provide a complete evaluation of subthreshold circuits in the whole range of space applications, radiation physics instruments and medical applications.

The fact that VR2 outperforms VR1, in terms of σ, and SETs' durations and amplitude, is due to the smaller area of VR2 compared to VR1. The circuit topology and operating conditions of the two circuits are very similar, since VR2 combines two feedback loops within a single branch.

The critical nodes that affect the output voltage are those that generate I_{CTAT} and I_{PTAT}, namely nodes V_X and V_Y in VR1 and node X in VR2. The reason that the VR1 circuit outperforms the VR2 circuit in the TID experiments is because VR1's critical nodes have a slightly higher impedance than that of VR2, given that in VR2 the I_{CTAT} and I_{PTAT} appear in parallel at a single node X. Therefore if the TID reduced the threshold of MN_4 the change in voltage at node X will create a greater change in current at node X, given the lower impedance, when compared to the equivalent critical nodes in VR1. In VR1 the threshold change will influence MN_6 and MN_4, which influence the voltage at the higher impedance nodes V_X and V_Y, thus leading to smaller relative change in the output current and consequently reference voltage.

In general, the subthreshold reference circuits show promising performance for space applications, especially in high total doses where they stop deviating or partially recover towards their nominal

performance. It is also important that they do not show any signs of collapse or functional failure in any of the experiments, even in uncommonly high total ionization doses or heavy ion strikes. In addition, as expalined above, they will benefit from more advanced technology nodes with thinner gate oxides. These conclusions, along with their main advantage of low-power consumption, make subthreshold circuits candidates for future space missions due to significantly reducing the size, cost and power requirements of space applications. Therefore, there is still room to explore more in the future in terms of different types of circuits and devices.

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