Tunnel junction thermometry on three-dimensional phononic crystals

Master's thesis, December 19, 2018

Author:

Emmi Kirjanen

Supervisor:

Ilari Maasilta

UNIVERSITY OF JYVÄSKYLÄ
DEPARTMENT OF PHYSICS

Abstract

Kirjanen, Emmi
Tunnel junction thermometry on three-dimensional phononic crystals
Master's thesis
Department of Physics, University of Jyväskylä, 2018, 80 pages.

In this work three-dimensional periodic nanostructures, phononic crystals to be more exact, have been studied. Phononic crystals are analogous to photonic crystals. They can modify lattice vibrations such as sound and heat in a similar manner like photonic crystals affect light. Depending on the structure and the materials some frequencies can travel faster or slower, and some frequency ranges can be completely blocked. Blocked frequency ranges are called energy gaps as vibrations are not allowed to have those energies. Phononic crystals have a wide range in applications such as thermal insulation or contact, or selecting or guiding specific frequencies.

At low temperatures, the importance of thermal management is even more essential compared to room temperature. In addition, the frequency range of thermal phonons is modified. Because of this, this work focused on effects that are present at low temperatures. This in turn restricts the phononic crystal sample period close to nano- and micrometer range, and in addition, the measurement system for thermal conduction should be suitable for low temperatures. As planned for the measurements, nanofabricated tunnel junctions could serve as a local thermometer and a heater. Tunnel junctions are highly sensitive to temperature and their theory is well known and thermometry applications are widely used. A new challenge in this work is how to fabricate such a delicate system on top of a rough crystal surface.

There has already been notable breakthroughs with two-dimensional phononic crystals. In turn, in this project the scope is three-dimensional phononic crystals with selected fabrication techniques. The techniques are a combination of multiple previously studied methods. First, a negative photoresist and UV-lithography are used to make a template structure which in turn is used to control the crystal size and position. The crystal itself was made by utilizing colloidal crystallization from sub-micron sized polystyrene spheres. It was noticed that crystals formed mostly in the patterned sites leaving the photoresist surface clean. This makes the following metal deposition steps easier, as misplaced spheres could hinder the process. For the tunnel junction fabrication, a new positive photoresist layer was deposited and then patterned with laser lithography. SINIS tunnel junctions were evaporated by using two-angle deposition. In the junction aluminum served as the superconductor (S), copper as the normal metal (N), and aluminum oxide between them as the insulator

(I). The junction deposition was found to be successful even directly on top of the crystals when using wide and thick enough wiring.

Measurements that were carried out at low temperatures confirmed that the tunnel junction fabrication was successful, by the study of the characteristic current-voltage curves. The junctions would thus be suitable to be used as thermometers. In the first measurement, there was some nonideal behavior present. However, such effects were not repeated, and unfortunately, their cause is still not fully known. Nevertheless, the second measurement was in good agreement with theory in the whole voltage range. Thermal conduction measurements were unfortunately not yet carried out, but the advancements in this thesis should make them possible in the near future. Also, possibilities for a control sample have been investigated.

Keywords: Thesis, colloidal crystallization, polystyrene, phononic crystals, SINIS tunnel junction

Tiivistelmä

Kirjanen, Emmi
Tunneliliitosten käyttäminen lämpömittarina kolmiulotteisilla fononikiteillä
Pro gradu -tutkielma
Fysiikan laitos, Jyväskylän yliopisto, 2018, 80 sivua

Tässä työssä on tutkittu kolmiulotteisia periodisia nanorakenteita, tarkemmin sanottuna fononikiteitä. Fononikiteet voivat muokata kiteessä liikkuvia värähtelyitä, eli ääntä ja lämpöä, samaan tapaan kuin fotonikiteet vaikuttavat valoon. Riippuen kiteen rakenteesta ja materiaaleista, jotkin taajuudet voivat kulkeutua paremmin tai huonommin, tai jotkin niistä voivat olla täysin kiellettyjä kiteen sisällä. Jälkimmäistä tapausta kutsutaan energia-aukoksi, sillä fononeilla ei voi olla kyseisiä energioita. Fononikiteitä voidaan soveltaa esimerkiksi hyvän tai huonon lämmönjohtavuuden saavuttamiseksi, tiettyjen värähtelytaajuuksien vahvistamiseksi tai poistamiseksi, tai värähtelyjen ohjaamiseksi.

Matalissa lämpötiloissa lämmönjohtumisen kontrolloinnin tärkeys korostuu ja termisten fononien taajuusalue on pienempi verrattuna korkeampiin lämpötiloihin, joten tässä työssä ollaankin keskitytty matalissa lämpötiloissa havaittaviin efekteihin. Tämä asettaa näytteen periodin nano-mikrometrialueelle ja lämmönjohtumiseen käytettävän mittasysteemin tulisi olla mataliin lämpötiloihin soveltuva. Mittauksissa nanovalmistetut tunneliliitokset toimisivat lokaalina lämmittimenä ja lämpömittarina, joita voitaisiin käyttää kiteen ominaisuuksien tutkimiseen. Tunneliliitoksien herkkä lämpötilakäyttäytyminen on hyvin tunnettu ilmiö ja niitä ollaan käytetty paljon esimerkiksi kalvojen tutkimuksessa. Uutena haasteena kuitenkin on, miten kyseisten herkkien rakenteiden valmistaminen luonnistuu kolmiulotteisen pinnan päälle.

Kaksiulotteisten fononikiteiden osalta on jo tehty huomattavia edistysaskelia, joten tässä työssä on keskitytty vain kolmiulotteisten kiteiden valmistamiseen valitulla menetelmällä. Valmistusprosessissa on yhdistetty useita aiemmin tutkittuja menetelmiä. Ensin kiteelle tehtiin negatiivisesta fotoresististä sen sijaintia ja kokoa rajoittava rakenne UV-litografian avulla puhdistetun piipalan päälle. Itse kide valmistettiin itsejärjestyvyyttä hyödyntäen kolloidikiteytyksellä polystyreenipalloista, joiden halkaisija oli satojen nanometrien luokkaa. Kiteytysprosessissa havaittiin, että polystyreenipallot hakeutuvat mieluiten niille varattuihin kohtiin ja resistin pinta jää useimmiten hyvinkin puhtaaksi, mikä mahdollistaa metalloinnin tekemisen näytteen päälle. Metallisten liitosten tekemistä varten näytteen päälle levitettiin uusi, myöhemmin poistettava resistikerros, mihin valotettiin laser-litografialla haluttu kuvio.

Kuvioidun resistin ja kahden kulman höyrystyksen avulla pyrittiin valmistamaan pari SINIS tunneliliitoksia. Liitoksessa alumiini toimi suprajohteena (S) ja kupari normaalimetallina (N), ja höyrystyksien välissä alumiinin pintaan muodostettu alumiinioksidi toimi eristeenä (I). Höyrystyksistä havaittiin, että johtimet onnistuivat suoraan kiteen päälle, mikäli ne olivat tarpeeksi leveitä ja jos metallia höyrystettiin tarpeeksi paksulti.

Matalissa lämpötiloissa suoritetut mittaukset vahvistivat valmistetut metalloinnit tunneliliitoksiksi niiden tunnusomaisten virta-jännite-käyrien perusteella. Liitokset olisivat siis soveltuvia käytettäviksi lämpötilan mittaamiseen. Ensimmäisissä mittauksissa havaittiin kuitenkin myös poikkeuksellista käyttäytymistä, minkä lähteitä ei valitettavasti vielä ymmärretä. Efektiä ei kuitenkaan saatu toistettua toisissa mittauksissa, mitkä puolestaan noudattivat teoriaa huomattavan hyvin koko jännitealueella. Lämmönjohtumismittauksia ei valitettavasti ehditty vielä tehdä, mutta kaikki välineet sitä varten on nyt toteutettavissa. Myös mahdollisuuksia referenssinäytteen valmistamiseksi on tutkittu.

Avainsanat: Opinnäyte, kolloidikiteytys, polystyreeni, fononikiteet, SINIS tunneliliitos

Preface

The work presented in this thesis has been carried out at the Department of Physics and Nanoscience Center at the University of Jyväskylä. All of the fabrication steps were carried out inside the Nanoscience Center cleanroom facilities. I carried out research training (FYSS9470) alongside the Master's thesis project, and it is reported in this thesis. The aim of the research training was to cover as many sample fabrication steps from the beginning as time allowed and further work was continued as Master's thesis project. The research training is covered in sections 3.3-3.6.

First, I would like to thank my supervisor, Professor Ilari Maasilta for giving me an opportunity to work on such interesting topics and also for his guidance and ideas along the project. Moreover, I would like to thank Mr. Zhuoran Geng for all of his practical help with cleanroom equipment and beyond. Cooldowns were carried out by him and he guided me through the measurements, and he also did indium bonding to my samples. He kindly let me use his code to simulate simple theoretical curves presented in sections 4.3 and 4.5 and he performed the actual simulations for spin-split and -polarization effects which are presented in section 4.4. I would also like to thank Mr. Samuli Heiskanen for his help with the equipment and sharing his fabrication knowledge, especially used in evaporation. Thanks to Dr. Kimmo Kinnunen for lending his skills with bonding machine and to him along with Mr. Tarmo Suppula for their efforts in keeping the equipment working and labs in order. My gratitude goes also to current and former group members who have provided me with help and ideas, especially to Mr. Teemu Loippo for interesting fabrication discussions.

Most of all, I am thankful to my family and friends for their encouragement, especially to my parents Tommi and Pauliina Kirjanen and my fiancé Oskari Saarimäki for their support.

Jyväskylä, December 2018

Emmi Kirjanen

Contents

1 Introduction

Colloidal crystals have been widely used to make photonic crystals (PtCs). PtCs have a periodic structure with a varying dielectric constant. PtCs will have an effect on how light propagates inside the crystal, which will result in a complex photonic band structure. The band structure describes which wavelengths are able to travel inside the material, in which direction and with which speed. [1] Phononic crystals (PnCs) are analogous to PtCs, except that mechanical vibrations are modified instead of electromagnetic waves. In PnCs, the periodic structure has alternating densities of materials, as the name suggests, phonons are the quantum mechanical quantity for vibrations just like photons are for light. Likewise, PnCs can be fabricated from colloidal crystals. [2]

PnCs can be used to control how vibrations, and so also heat carried by them, are transmitted. They can block certain wavelengths completely or in certain directions. These restricted spectral regions are called band gaps. PnCs can hinder or enhance propagation by the modifications to the band structure. With these properties, it is possible to use PnCs for insulation or to make good thermal contact in the case of thermal transport. There are also some other novel ideas, such as guiding or focusing vibrations. [3] The properties of PnCs can be radically changed or fine tuned by altering the geometry, the material, the filling factor or the lattice constant. The effects of different structures have been studied a lot, both experimentally and computationally. [2, 4, 5]

While there has been a lot of focus on two-dimensional (2D) PnCs [6] and their possibilities, three-dimensional (3D) PnCs can also be used in similar ways. However, fabrication of 3D PnCs can sometimes prove to be challenging. One of the problems is of course how to fabricate good quality 3D periodic structure. Self-assembled colloidal crystals is a promising solution to that. Nevertheless, the optimization of the fabrication process can be crucial. In addition, with the usual self-assembly techniques, the crystal is usually deposited on top of the whole surface and it produces multiple domains instead of one single crystal. This can cause problems for measurements where usually single domain crystals are wanted. [7]

2D PnCs have been fabricated from different types of membranes by patterning them with hole arrays. However, whereas 2D PnCs can have a flat surface by default, the top of 3D PnC is rough when it is formed by colloidal crystallization. This can cause problems if some sort of fabrication on top of the structure is necessary for measurements. One such option is a nanofabricated heater-thermometer pair that can be used to measure the thermal conductance locally. [4] Restricting the place and

size of the crystal is also important for wire fabrication. In addition, the stability of the crystals is of concern, especially when using organic materials which can be vulnerable to many chemicals. Electron beam irradiation seems to be suitable to control polystyrene (PS) durability [8], which is also the material that is used in this study.

The aim of this study is first to reproduce the previous results by Tian et al. [8], then to optimize sample fabrication and continue it further to produce final devices for thermal transport studies. Before this work, 3D colloidal crystals have been fabricated from a PS microsphere suspension with a single-step vertical deposition. It has been possible to influence the crystal size and position with pre-crystallization lithographic methods, with either an etched silicon trough or with a patterned photoresist. From these two, photoresist seemed more promising so I continued with it. I tried the more straightforward method of using simple UV patterned resists instead of 3D lithography. In addition, as PS is vulnerable to harsh chemicals used in post-crystallization fabrication, I made sure what type of treatment is necessary. Afterward, I deposited metallic wiring in the form of superconductor - insulator - normal metal - insulator - superconductor (SINIS) heater-thermometer pairs, similar to Zen et al. [4] in design and materials. Novel combination of 3D lithography and electron beam evaporation was used. I investigated if fabrication is possible directly on top of the crystal, whether the junctions behave according to theory, and whether they are suitable to be used as thermometers. For the finished samples, thermal properties are planned to be measured at sub-Kelvin temperatures. These measurements could then be compared to results from a control sample with a continuous structure, and thus the effect of the 3D PnC could be determined.

2 Theoretical background

2.1 Thermal phononic crystals

2.1.1 Diffusive heat conduction

Thermal conductivity is a property of matter. It describes at which rate heat is transferred in a material. It can be defined as rate of heat flow per area ($\dot{q} = \dot{Q}/A$), given by the thermal conductivity coefficient times the temperature gradient ($\dot{q} = -\kappa\nabla T$), which is the differential form of Fourier's law. The thermal conductivity coefficient can easily be used to describe the properties of matter and it is usually temperature dependent. [9]

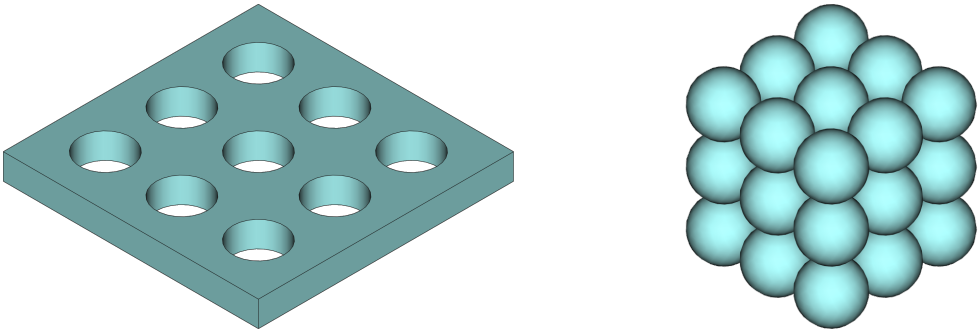
Heat is mainly carried by conduction electrons or by phonons in a solid. Phonons are the quantized lattice vibrations. Insulators lack conduction electrons so only phonons can carry heat in them. For most samples and temperatures phonon transport is a diffusive process, where phonons scatter from electrons, phonons or impurities. The kinetic model for thermal conductivity coefficient can then be written as:

$$\kappa = \frac{1}{3}\frac{C}{V_m}v\lambda \ , \tag{1}$$

where C is the specific heat, V_m is molar volume, v is the average velocity of heat carriers, and λ is the mean free path. Mean free path is the average distance that the heat carrier (a phonon in case of insulators) can travel before scattering. Some scattering processes are temperature dependent such as phonon-phonon scattering, while others are not, such as phonon-impurity scattering. The velocity of phonons, which is the velocity of sound for acoustic phonons, is temperature independent at low temperatures. The phononic specific heat can be calculated, and it is known to have T^3 dependence at low temperatures. This way it is possible to write an approximation for the phononic thermal conductivity coefficient:

$$\kappa_{ph} = \frac{1}{3}\frac{C_{ph}}{V_m}v_S\lambda_{ph}(T) \propto T^3\lambda_{ph}(T) \quad \text{at} \quad T \leq \theta_D/10 \ , \tag{2}$$

where θ_D stands for the Debye temperature, which means that the equation is valid for so called intermediate temperatures. For temperatures significantly lower than Debye temperature, the number of exited phonons is small and their wavelength is long, which means that most scattering processes become negligible. Phonons will scatter mostly at crystal boundaries which is a temperature independent process. For perfect crystals κ_{ph} then becomes T^3 dependent. [9]



(a) Two-dimensional. **(b)** Three-dimensional.

Figure 1. Examples of phononic crystal structures.

2.1.2 Ballistic heat conduction

Diffusive scattering leads to incoherence. This means that phonons will lose their phase during scattering. Instead, in coherent scattering the phase of phonons is preserved. Coherent scattering occurs at sample boundaries if the surface is smooth enough compared to the wavelength of the phonon. Coherent scattering combined with periodic structures makes it possible for phonons to interfere with each other either destructively or constructively. Multiple periods are required for the effect to show. The phonon band structure (phonon dispersion relations) is modified by interference, which turns usually diffusive particles to behave as phonon waves. As phonons are vibrations of the lattice, the elastic properties of materials affect the propagation, and thus the phononic band structure. Other determining factors are the shape and the arrangement of the periodic structure (crystal). Crystals that can be used to control phonon propagation are called phononic crystals. [10, 11]

Phononic crystals (PnCs) can be realized in many dimensions, some of which are presented in Figure 1. For example, one-dimensional layered structures, two-dimensional hole (or pillar) patterns on a plate, or three-dimensional such as spheres arranged in lattice can all serve as PnCs. However, in all three cases the periodicity of the PnC affects the possible formation of a band gap. The band gap is a range of frequencies, which do not support propagation inside the PnC. A partial band gap means that selected frequencies are prohibited only to some directions, and a complete band gap means that those frequencies can not propagate at all inside the PnC. Band gaps are mainly formed from Bragg interference which occurs at frequencies around c/a, where c is speed of phonons and a is period of PnC. This means that periodicity of PnC should be chosen according to which frequencies are the area of interest. For example, to control kHz frequencies periodicity in the order of cm is suitable, for GHz order of µm, and for THz order of 10 nm. [11, 12]

Both sound and heat are lattice vibrations which are carried by phonons. The only difference is the frequency range at which they propagate. Sound is carried by low-frequency phonons, in kHz range, and heat is carried by a wide range of higher

frequency phonons, THz range at room temperature. This makes experimental study of coherent thermal conductance challenging because of the fabrication difficulties of such delicate structures. It also gives high requirements for surface smoothness. [10, 11] To make experiments possible, the frequencies of thermal phonons should be made lower. One suggestion is to use an alloy material where there are a lot of high-frequency scatterers. This would restrict propagation of high-frequency phonons, and heat would have to be carried more by lower-frequency phonons. [13] Another solution, which will be the focus of this study, is to perform experiments at low temperatures, below 1 K. Low temperatures will increase the wavelength of the dominant thermal phonons and the main excitations will be in GHz range. [4]

2.1.3 Thermal phonon radiation

In order to study phonons, they must be introduced to the sample in controlled manner. At low temperatures there are only very few excited states because of the low thermal energy. In addition, the mean free path is not limited by phonon-phonon interactions. In insulators only phonons are in charge of the thermal conductance. However, thermal phonons can be generated by heating the sample with a metallic thin film. If a metal film is considered to have phonon distribution corresponding to temperature T_1 and it is treated as an isotropic material, the net phonon power emitted by the heater per area at low temperatures (much lower than Debye temperature) and with perfect matching conditions (emissivity = 1) can be written as:

$$\frac{P(T_1,T_0)}{A} = \frac{\pi^2}{120\hbar^3}\left(\frac{1}{c_l^2}+\frac{2}{c_t^2}\right)\cdot k_B^4\left(T_1^4 - T_0^4\right) \ , \tag{3}$$

where T_1 and T_0 are temperatures of heater and insulator, $\hbar$ is the reduced Planck constant, c_l and c_t are the longitudinal and transverse speeds of sound, and k_B is the Boltzmann constant. This is the phononic equivalent to the Stephan-Boltzmann law for photon thermal radiation. [14]

2.1.4 Two-dimensional phononic crystals

In general, two-dimensional (2D) phononic crystals can be realized with either periodic holes (or pillars) in one plane, as presented in Figure 1a. Hole structures are usually made from suspended thin films, as the thickness of the film also affects the phonon band structure. A band gap might even open only for a specific period to thickness ratio. [4] Silicon and its derivatives are common materials for such membranes. In the following, some advancements made with low-temperature 2D PnCs are reviewed.

The first report on coherent thermal conductance in 2D PnCs was made by Zen et al. [4]. In that study, silicon nitride membranes were used to make periodic structures with a square lattice array. The chosen periods were 970 nm and 2425 nm with a

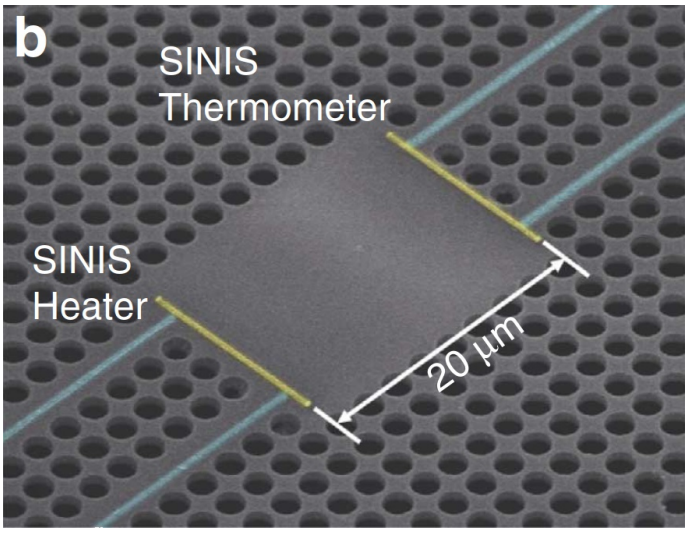


Figure 2. Fake color SEM image of 2D PnC sample with SINIS tunnel junctions. Yellow color represents copper and blue aluminum. [4]

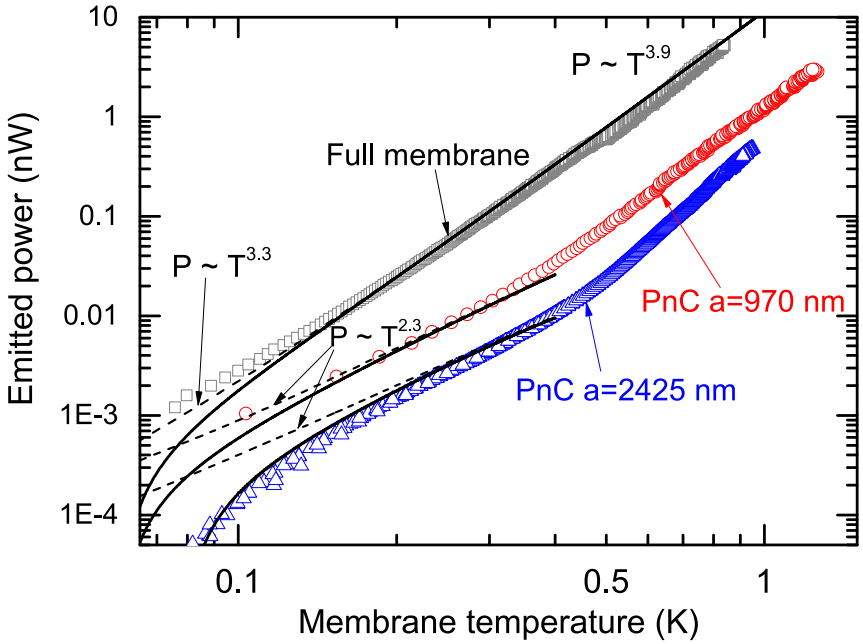


Figure 3. The emitted phonon power as a function of temperature for a full membrane and two 2D PnCs with different periods. [4]

membrane thickness of 485 nm. Finite element method (FEM) calculations were utilized to predict phonon dispersion relations. From the calculated band structures it was shown that the smaller period had a complete band gap in the dominant frequency range, and in addition, both periods had much flatter band structures compared to the full membrane, which will also affect thermal conductance. Despite different periodicities, both samples were fabricated with the same filling factor for easier comparison between the PnCs. If the filling factor is the same, and thus the surface to volume ratio, classical or ballistic heat conduction would predict the same values for both samples. However, for the case of the PnCs, the band structures modify the heat conduction and produce coherent changes. Measurements were carried out below 1 K where bulk scattering of phonons is negligible, and where the wavelength of thermal phonons is long. Thermometer-heater pairs of SINIS tunnel junctions were used to heat and measure the temperature locally in the middle of the sample. The principles and applications of SINIS junctions are explained in more detail in section 2.2. The sample with the larger period is presented in Figure 2, and the measurement results in Figure 3. It was found out that both PnC structures had a lower thermal conductance compared to the full membrane by one to two orders of magnitude. Despite the smaller period sample having the band gap in its band structure, the longer period showed a smaller thermal conductance. It can be said that dispersion relations as a whole are more important than band gaps when it comes to thermal conductance. In addition, as the two PnCs with the same filling factor had different thermal conductivities, it was confirmed that it can not be explained by ballistic conduction alone. Instead, the band structure modifications have to be taken into account. That is further confirmed, as the computational calculations for the thermal conductance fit the experiments really well.

Afterwards, silicon nitride membranes have been used for PnCs with longer periodicities. A periodicity of 4 µm was studied [15] with smaller SINIS junctions placed closer together compared to the previous study. Over two orders of magnitude reduction in thermal conductance was achieved compared to a full membrane. PnCs with periodicities of 4 µm, 8 µm, and 18 µm were also fabricated [16, 17] with again a different SINIS geometry and this time also heater/thermometer material. This was done in order to use the same heater geometry for all samples with different periodicities, as it was necessary to fit the wiring to all samples despite the holes having different sizes. It was again observed from the measurements that all PnCs had a lower thermal conductance compared to a full membrane. Interestingly, the middle periodicity, 8 µm, had the lowest value instead of the longest periodicity. This is believed to be due to increase in diffusive scattering with increasing period. That is because with increasing period the sample dimensions become large, comparable to the mean free path, and diffusive scattering could increase thermal conductance by starting to increase the group velocity. All of these silicon nitride membrane PnCs were measured at sub-Kelvin temperatures.

Later, coherent thermal effects of 2D PnCs have been experimented with different set-up by using thin silicon membranes as samples at 4 K temperatures and by

carrying measurements with an optical system. Effects of different geometries have been studied by Anufriev et al. [18], where they fabricated hole-arrays with hexagonal, square and honeycomb lattices. All geometries and periodicities showed lower thermal conductance compared to a full membrane. More than the lattice type, the period and the neck size seemed to have bigger effect on conductance. Measurements were also carried out at high temperature, 300 K, for comparison. Coherent thermal scattering was not demonstrated at such high temperatures where frequency of thermal carriers is much higher. Another interesting way to prove the coherent modifications in a periodic structure was used by Maire et al. [19] where they used a similar type of samples and measurement scheme as in [18]. They fabricated samples with a square lattice but also introduced disorder to samples by randomly shifting the positions of the holes. With increasing disorder the thermal conductance was found to be increasing, reaching a maximum value near 5 % disorder. By repeating the measurement at room temperature, the same effect was not present, and all PnCs had the same thermal conductivity despite the amount of disorder. That was interpreted to demonstrate that the coherent effects were present only at temperatures lower than 10 K. Similar conclusions were also reached by Lee et al. [20]

2.1.5 Three-dimensional phononic crystals

Three-dimensional (3D) thermal PnCs have proven to be more challenging to fabricate compared to lower dimensional PnCs. FEM modeling of simple cubic 3D polystyrene PnCs [21] has predicted modifications to band structures and even band gaps, and so 3D PnCs are expected to have big effects on thermal conductance. Visual presentation of such a crystal is in Figure 1b.

One attempt at a fabrication of a low temperature 3D PnC was made by Savytskyi [22]. He utilized the single-step vertical deposition method, which is explained in section 2.3.2. It was used to make close packed arrays of colloidal crystals formed from silicon dioxide microspheres. However, such crystal is very challenging for further fabrication steps. The surface is rough, and because of that, multiple coating materials and methods were attempted to make it smooth enough. There was also problems with the crystal breaking off during lift-off after metal deposition. Eventually, junction fabrication was made possible with a SU-8 negative photoresist coating between the crystal and the metal. Evaporated metal wires were long enough to travel from a crystal to clean silicon area where bonding to sample stage could be made. This was done because the crystal could still break easily in such a process. Thermal conductance was measured at sub-Kelvin temperatures with SINIS junction pair, and the power of the emitted heat was found to have $T^{4.15}$ dependence. However, no control sample was made so result could not be compared.

Meanwhile, advances have also been made with polystyrene (PS) microsphere colloidal crystals, by starting with the characterization of crystals formed by single-step vertical deposition [7] and followed by solving problems such as the weak nature of polymers

and roughness of the surface, resulting in successful integration of metallic wiring on top of crystals [8]. However, only simple wires were fabricated on top of crystals, and such samples can not be used for thermal transport measurements. A SINIS pair needs to be on top of a crystal, and in addition, the placement of bonding pads needs to be taken into account. Bonding directly on top of a crystal is most likely impossible with ultrasonic bonding techniques. Instead, positioning of the crystal must be controlled in a way that allows bonding outside of the crystal surface. The ways to control crystal position and size are explained in more detail in section 2.3.3. These challenges need to be addressed before measurements are possible. So far only one microsphere size has been used, with diameter 260 nm, but others are also possible.

2.2 SINIS thermometry

2.2.1 Superconductivity

Superconductivity is a property possessed by some elements and compounds. Characteristic properties of superconductors are the occurrence of perfect conductivity and perfect diamagnetism when the superconductor is cooled below its critical temperature, T_c. The critical temperature depends on the material. For example, for aluminum it is as low as $T_c \approx 1.2$ K. When wires are made from material which is in superconductive state, current can be transferred without losses. According to the Bardeen–Cooper–Schrieffer (BCS) theory, superconductivity is attributed to formation of Cooper pairs. Cooper pairs are formed from two bound electrons. These electrons have a lower energy than unpaired electrons. The formation of pairs causes an energy gap between the ground state and the excited states in superconductor. The gap is centered at the Fermi energy. The gap width is usually denoted with Δ, and a minimum energy of 2Δ is required to break a pair. Energies inside the gap are forbidden. [23]

2.2.2 Tunneling between superconductor and normal metal

One way to study superconductivity is to observe the tunneling to or from a superconductor. Tunneling is a quantum mechanical effect where electron is transferred from one metal to another through a barrier, which can be a thin insulating layer. This can be achieved by a small potential difference between metals or by thermal excitations. In the case of two normal metals with an insulator between them, the tunneling current is linear as a function of voltage across the junction. The effect of temperature is negligible as the electron distribution is similar on both sides of the insulator. However, if one of them is in the superconductive state, the current-voltage characteristics become highly non-linear. This is due to the energy gap in the superconductor which restricts the current at low voltages. The density of

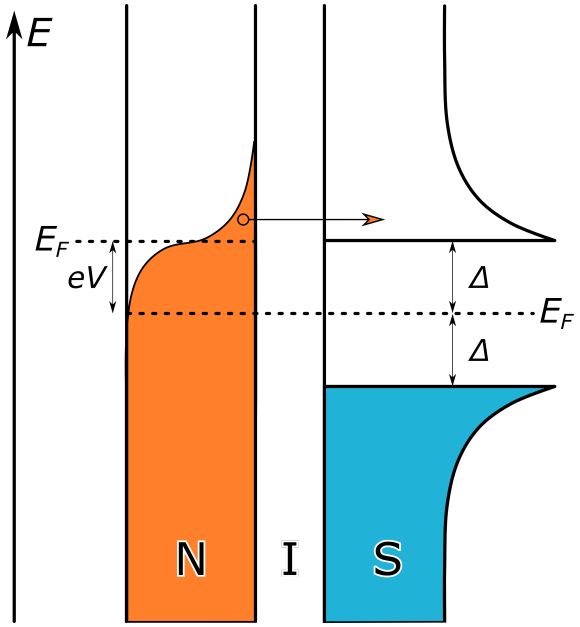


Figure 4. Energy diagram for a normal metal - insulator - superconductor (NIS) junction at finite temperature. Colored areas represent occupied states and white areas unoccupied states. V is the biasing of the junction.

states is also different compared to a normal metal, and the tunneling current-voltage characteristics are also temperature dependent. At absolute zero, the gap in the superconductor would block all current for voltages smaller than $|\Delta/e|$. The energies would all be inside the gap and at such forbidden. However, at higher temperatures there are some thermal excitations which can allow current to flow through even with sub-gap voltages. Depending on the temperature, there are different amount of thermal excitations. This makes tunneling current highly dependent on temperature with small voltages. [24]

This is further illustrated in Figure 4 where a NIS junction is presented in the form of an energy diagram. In the figure, the junction is biased with voltage V which lifts the energy of occupied states in normal metal higher allowing those electrons with high enough energy to tunnel to the unoccupied states in the superconductor.

2.2.3 SINIS junction current

In practice, NIS junctions can easily be fabricated in series forming symmetrical SINIS junctions, where there is a normal metal island between two superconductors separated by a thin insulating layer. An example is presented in Figure 2 where there is pair of SINIS junctions facing each other. SINIS junction behaves in a similar way as a single NIS junction with half of the applied voltage. The tunneling current can

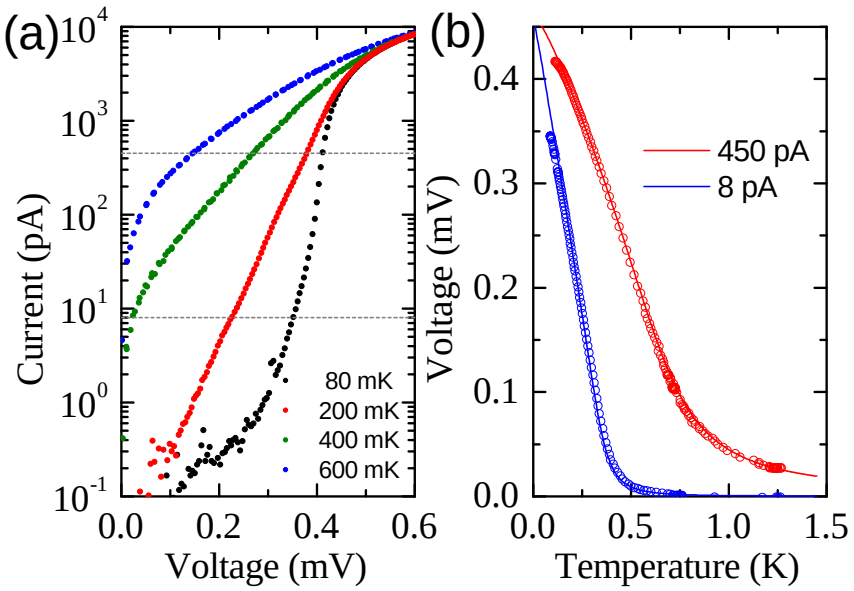


Figure 5. An example of SINIS junction thermometer characteristics. On the left side there are current-voltage curves at different bath temperatures, and on the right side there are voltage-temperature calibration curves for two different bias currents. [4]

be written as:

$$I(V) = \frac{1}{eR_T} \int_{-\infty}^{\infty} n_S(E, T_S) \left[f_N(E - eV/2, T_N) - f_N(E + eV/2, T_N) \right] dE \ , \qquad (4)$$

where e is elementary charge, R_T is the total tunneling resistance, n_S is density of states (DOS) of the superconductor, and f_N is the Fermi function which describes electron distribution in normal metal. Both n_S and f_N are temperature dependent, as T_S is the superconductor temperature and T_N is the normal metal temperature. V is the voltage across the whole junction pair. According to the BCS theory, the simplest model for the superconductor DOS can be described by:

$$n_S(E, T_S) = \begin{cases} \frac{|E|}{\sqrt{E^2 - \Delta(T_S)^2}} & \text{when } |E| > \Delta \\ 0 & \text{when } |E| < \Delta \end{cases} \ , \qquad (5)$$

which assumes that there are no states inside the gap. [4, 23] However, non-idealities can cause a small current even inside the gap, and this is present in all measurements. The non-ideal DOS can be expressed as:

$$n_S(E, T_S) = \left| \mathrm{Re} \left\{ \frac{E + i\Gamma}{\sqrt{(E + i\Gamma)^2 - \Delta(T_S)^2}} \right\} \right| \ , \qquad (6)$$

where Γ is the Dynes parameter. [4, 25]

The current across the SINIS junction given by equation (4) depends on voltage and temperature. If such junction is biased with constant current, the voltage will

depend only on temperature as the current is fixed. It is also important to note that equation (4) depends strongly only on the temperature of the normal metal, and not of the superconductor. The temperature dependent part of superconductor DOS in equation (6) is the gap size Δ which is essentially constant at temperatures that are much smaller than critical temperature T_c. This makes SINIS junctions excellent local thermometers, as ideally only the temperature of the small normal metal island affects the reading. Nevertheless, the temperature of the superconductor plays also a critical role when SINIS junctions are used as a thermometers. The T_c of the chosen superconductor limits the temperature range where it can be used, because above T_c the superconductor turns back into a normal metal. In the case of aluminum, it gives an upper limit of around 1 K. [4, 23]

An example of SINIS characteristics is presented in Figure 5. As it can be seen, the shape of the current-voltage curves is greatly affected by temperature at which they are measured. All parameters that are relevant to using SINIS junction as a thermometer can be self-consistently derived from the current-voltage curves. In thermometry measurements, the junction is typically biased with constant current which can be appropriately chosen from the current-voltage characteristics to cover the temperature range of interest. On the left side of Figure 5, the chosen current values are indicated with dotted lines. Multiple current values can be chosen to gain optimal sensitivity at high and at low temperatures. SINIS junction thermometers can be calibrated as presented on the right side of Figure 5, where the voltage across the junction was measured with a constant current bias, and the temperature was measured with a calibrated RuO (ruthenium oxide) thermometer. This is done to correct possible errors. After calibration, a SINIS junction can be used as a local thermometer. [4]

2.3 Colloidal crystals

2.3.1 Self-assembly in colloidal crystallization

Colloidal crystals are ordered arrays of colloidal spheres. They are typically formed from silica or polymer microspheres from a suspended solution by self-assembly. Highly uniform polymer microspheres can be produced by emulsion polymerization. They can be suspended either in water or some organic solvent, as long as they are insoluble to that solvent. [26] In this study, polystyrene microspheres are suspended in water.

Self-assembly is a bottom-up method which means that crystals are formed from smaller pieces that are independently stacked over each other. Most of the traditional lithographic methods are so called top-down methods. In top-down methods, a bigger piece is modified from outside into a wanted shape, such as how resist is modified by UV light or electron beam. However, self-assembly makes it possible to have small feature size and long range order relatively easily. [27]

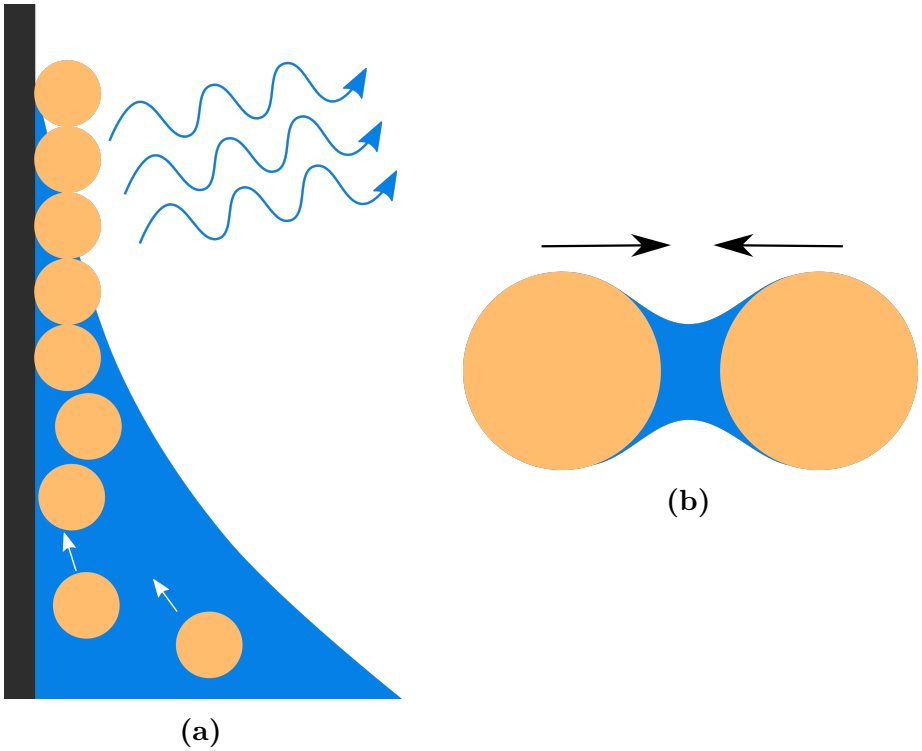


Figure 6. Simplified images related to vertical deposition. **(a)** Solvent flows to the substrate interface where it evaporates (blue arrows), and colloidal spheres move with the flow (white arrows). **(b)** Capillary neck formation between two colloidal spheres where solvent has been partially evaporated. Arrows indicate direction of attractive forces.

Colloidal crystals formed by self-assembly usually produce close packed geometries such as face-centered cubic (fcc) and hexagonal close packing (hcp), but other geometries are also possible. Colloidal crystallization is entropy-driven process, and there are multiple methods to initiate self-assembly of these colloids. One traditional method is to use gravitational sedimentation, where colloids slowly gather at the bottom of a container and form a crystal. However, the process is really slow and can take months. In addition, there is little control over morphology of the formed crystal and over the number of layers. Samples are usually also polycrystalline. Other possible methods include methods such as utilizing repulsive electrostatic forces, or growing crystals under physical confinement. [1, 26]

2.3.2 Crystallization by single-step vertical deposition

The effects of capillary forces and how colloids can gather at interfaces have been studied as well. In one set-up, colloids are laying on a horizontal surface, and the solvent is evaporated. When colloids are partially visible, they start gathering together and form a crystalline layer. This is explained to happen because of

Figure 7. Shape of the meniscus when water is in contact with hydrophilic surface (left) and hydrophobic surface (right).

capillary necks (Figure 6b) that form between spheres and pull them together during drying. [28] Capillary forces have also been utilized in vertical crystal growth where substrate is partially immersed in colloidal suspension perpendicular to the suspension surface. First, colloids flow to the meniscus by the solvent flux, as the solvent evaporates fastest at the contact line at the substrate-solvent-air interface. Then, at the interface, colloids form capillary necks with the substrate surface and with each other, and the crystal is formed. If the movement speed of the contact line is the same as the formation speed of the crystalline layer, a monolayer crystal is formed continuously, as the contact line moves downwards. [29] This is demonstrated in Figure 6a.

Vertical deposition can also be used to form multilayer crystals with same principles. Like in the monolayer formation, colloids gather to the meniscus by the solvent-flux, and are then pulled together by capillary forces. The already formed crystal acts as a filter for upcoming colloids. [30] The two most important and most easily varied factors in multilayer crystal formation are the movement speed of the meniscus and the concentration of the colloidal suspension. The slower the movement of the contact line, the more there is time for colloids to gather to the crystallization area. Likewise, the higher the concentration, the more there are colloids that go with the flow. [1, 31, 32]

There are different approaches to how to control the movement of the contact line. One way is to simply evaporate the solvent. [1] This can be further controlled by such things as humidity and temperature. Evaporation can also be countered by adding more solvent to the suspension at a constant rate. This way even slower speeds can be achieved. [33] However, by simple evaporation, the concentration of the suspension might not stay constant during the deposition process. It causes uneven crystal formation over the substrate by forming distinguishable regions. [34] This can be avoided by lifting the substrate from the suspension with a constant speed which is faster than the evaporation process. Thus the concentration will stay

constant during the whole crystal formation. The lifting speed can easily be varied with right equipment, and the thickness of the crystal can therefore be tuned. [1, 32]

In vertical deposition, the shape of meniscus plays an important role. It determines how colloids travel to the contact line and how much time they have to rearrange. The most important factor seems to be the substrate wetting as presented in Figure 7. The substrate must be hydrophilic for deposition to happen, if water is used in the colloidal suspension. Otherwise, the meniscus is shaped in such a way that colloids can not attach to the surface. The easiest way to alter the wetting of the substrate is to coat it with a hyrdophilic material, but other treatments are also possible. [26] The shape of the meniscus can also be altered by tilting the substrate compared to the suspension surface [35], or with topographical changes in the substrate [36].

In addition to the crystal thickness, the crystal quality is also of great interest. Vertical deposition is reported to produce large, uniform crystals. However, all sorts of defects can be found on colloidal crystals, such as dislocations, changes in crystalline structure and cracks. In vertical deposition, cracks are mainly produced during the drying process. The orientation of crystallites separated by a crack was found to be same, which means that the crack is formed after the crystallization. [34] On the other hand, the size distribution of colloidal particles seems to be important for long range ordering of the crystals. For microspheres with a wide size distribution, the crystalline order resembled amorphous instead of a close packed structure. [31]

Characterization of crystals show that domains separated by cracks are longer in the vertical direction, parallel to the growing direction. In addition, thicker crystals are found to produce larger domains. [31, 37] However, domain sizes are not uniform in one sample. Instead there is a lot of variation in the domain size. [7] Because of this, it can be challenging to make samples with appropriately sized crystals at wanted positions. In addition, thicker crystals can have especially bad adhesion with the substrate, which can cause flaking off or detachment from the surface during further fabrication steps. [8, 34]

2.3.3 Lithographically assisted self-assembly

Crystal growth can be modified by using a non-uniform substrate. The changes in the substrate surface affect the shape of the meniscus and also how colloids are attached to the substrate surface. For charged particles, charged regions on the substrate can affect the growth. For neutral particles, changes in surface wettability will affect the shape of the meniscus. As mentioned in the previous section, crystal growth will favor wettable surfaces over hydrophobic. Thus hydrophobic and hydrophilic areas can be patterned for example by depositing a thin layer of different materials. [30]

In addition to chemical or electrical properties of the substrate surface, topographical patterns can also affect crystal growth. Topographical pattern can be made with the same or a different material compared to the substrate. One solution is to etch troughs or pits into the substrate. The meniscus shape is different for etched

and non-etched parts, which can result in favored crystal formation at the deeper parts. [36] This can be further encouraged by depositing more hydrophilic material to the bottom of the etched containers. With an appropriately sized container, it is possible to enhance also the crystal domain size compared to a plain substrate with the same treatment. [7] However, with etched pits made from silicon and crystals made from colloidal polymers, it seems to be common for cracks to form between the container and the crystal. [7, 36] This can be problematic if a continuous structure is wanted to be fabricated from substrate surface to the crystal.

The shape of the assisting pattern also affects the resulting crystal. In the case of templated growth with a chemical pattern, the thickest crystal is formed in the middle of a hydrophilic area. In addition, lines parallel to the growing direction formed nice crystals, while perpendicular stripes were partially unfilled. This is because with parallel lines the meniscus shape is constant, and the crystal can form continuously. On the other hand, with alternating hydrophobic and hydrophilic stripes perpendicular to the growth direction, the meniscus has to flip between different types of surfaces. Also, if the patterned features are too narrow, the meniscus cannot adjust, and no crystal is grown on top of the hydrophilic area, or it is grown on top of the hydrophobic area. [30] In topographical assistance, it is possible to trap a single domain inside one pit, if it is made small enough. [7] However, the shape of a pit does not seem to affect the crack formation at the edge of the crystal. [36]

A promising solution to prevent crack formation is to use polymers to make the confining structure instead of etching. In the work by Tian et al. [8], crystal growth was controlled with a square-shaped container made from a resist. It was found out that while some crack formation was present, crystal edges were nicely in contact with the container.

2.3.4 Considerations with organic colloid materials

Polymer spheres, particularly polystyrene (PS) is a common material for colloidal particles used in crystallization. However, one problem with such materials is that their structure can be easily destroyed by heat or strong chemicals. This means that PS must be made more durable for it to withstand additional fabrication steps. One commercially widely used method with plastics and rubbers is to introduce cross-linking by ionizing radiation. It is a method that does not require any chemicals, and is usable for many different polymers with different chemical structures. It can also be used in addition to other cross-linking methods just to give extra strength to the material. Usually radiated materials maintain their shape better, are stronger and even have increased chemical resistance. There are many types of radiation that can be used to initiate the cross-linking, electron beam is one among them. [38]

In the work by Tian et al. [8], electron beam irradiation was used to control solubility of thin PS crystals to acetone. It was shown that with just high enough radiation

dose, PS spheres could survive immersion to acetone instead of being completely destroyed. This happened for doses between 60 µC/cm^2 and 170 µC/cm^2. Under doses of 2300 µC/cm^2, the solubility was highly tunable. Depending on the dose, the PS spheres would merge more or less together during acetone immersion. With higher doses than that, thin crystals would retain their shape. This is especially interesting, as FEM computational studies [21] have shown, thet the contact area between spheres in crystalline lattice can modify the phonon band structure. With a simple cubic (SC) lattice, the band gap would narrow and completely disappear by increasing the contact area.

It was also noted by Tian et al. [8] that thicker crystals might easily peel off even after the electron beam irradiation treatment. However, with a confining structure as explained in previous section, crystals can be trapped into a pit in the substrate. With lithographic assistance, even thicker crystals could stick to the substrate.

3 Fabrication

In this section all the sample fabrication details are presented. First there is an overview of the whole process and then separate steps are presented in chronological order. The research training is covered in sections 3.3-3.6.

3.1 Imaging and visualization

Optical images were taken with an Olympus BX51M optical microscope and a Q Imaging MicroPublisher 5.0 RTV camera. Scanning electron microscope (SEM) images were taken with a Raith eLine scanning electron microscope. It was controlled with the eline and smartSEM software. Both the usual flat and tilted sample stages were used. An aperture size of 30 µm and an acceleration voltage of 10 kV were used. Samples were sputter coated with gold before taking the SEM images. JEOL JFC-1100 ion sputter was used.

Optical and SEM images were edited with paint.net. Inkscape was used to make diagrams and Origin 2017 was used to plot graphs.

3.2 Overview of the fabrication

Three-dimensional PnCs were fabricated by combining many previously studied methods. The most important fabrication steps are presented in Figure 8. The numbers in the text represent the numbered steps in the figure. For preparation, the sample is first cut from a silicon wafer and cleaned (described in more detail in section 3.3). After that, 1) the silicon substrate is spin coated with SU-8 negative photoresist, and SU-8 is exposed with UV light by using a mask aligner. Chromium-glass-mask is used to shield 50 µm × 50 µm areas from exposure. 2) The unexposed resist is removed during development. It can be followed by a hard bake to make sure that the resist was fully cross-linked. Steps 1) and 2) are explained in section 3.4.

3) The sample is then ‘‘dipped’’ into a PS microsphere suspension and drawn out slowly using a stepper motor. The method is called single-step vertical deposition. In addition to the control with surface topography, silicon is more hydrophilic than the resist layer which gives control over the crystal growth. The dipping angle is perpendicular to the suspension surface. Step 3) is explained in section 3.5. 4) Crystals are hardened by electron beam irradiation with SEM. Step 4) is covered in section 3.6.

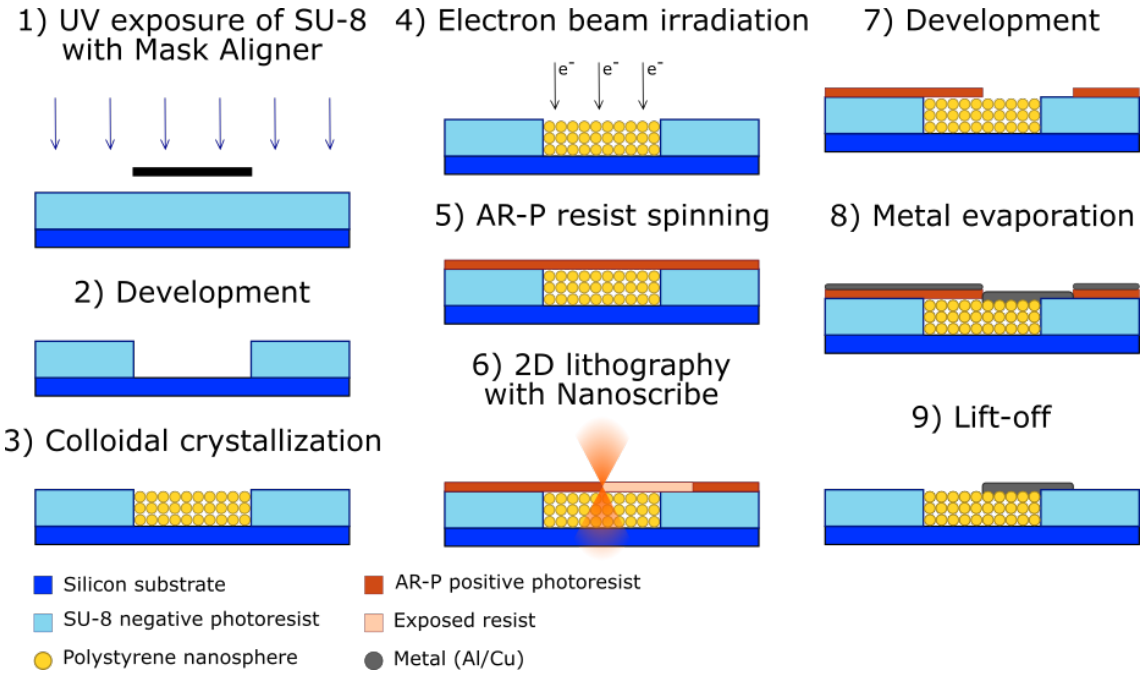


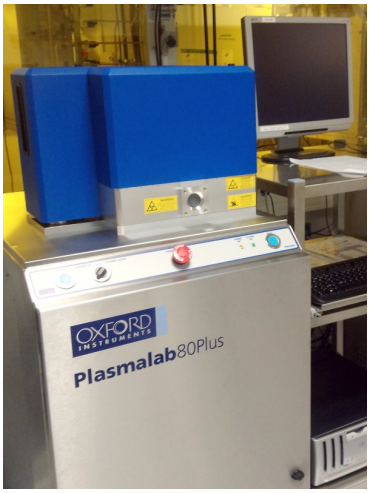
Figure 8. Simplified diagram of the fabrication steps after the preparation of the sample.

5) A thin layer of AR-P positive photoresist is spin coated on top of the sample. 6) The resist is patterned with Nanoscribe (3D lithography machine) which uses near infrared light and two-photon absorption to expose a chosen pattern. 7) The exposed resist is removed during development. 8) Metal is evaporated on top of the sample, first aluminum, then copper. Two angles are used, and aluminum is oxidized before copper deposition to make tunnel junctions. 9) Lift-off is carried out in hot acetone. It removes the AR-P resist and the deposited metal on top of it, leaving only patterned path left. Steps 5)-9) are covered in section 3.7. After this, the sample is ready to be attached to a sample stage and measurements can be carried out, which is discussed in section 4.

3.3 Preparation steps

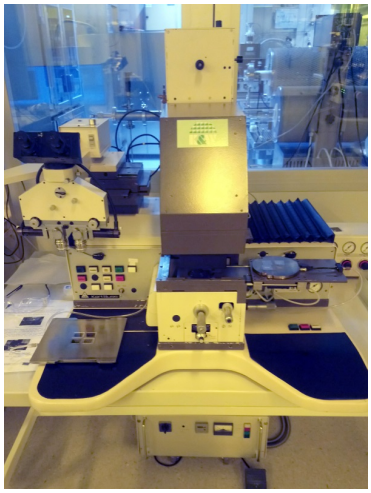
3.3.1 Cutting of silicon wafer

Samples were cut from 525 µm thick silicon wafers using diamond scribe. The sample size was around 8 mm × 8 mm, as that would be suitable for the sample stage that is used later during measurements. Also longer sample sizes were attempted to be used. This was because longer samples would have been useful for the colloidal crystallization by single-step vertical deposition, as explained in section 3.5. However, getting a uniform resist layer to a 8 mm × 16 mm sample appeared to be difficult. Positioning such a sample to the spin coater was hard because of the imbalance. In



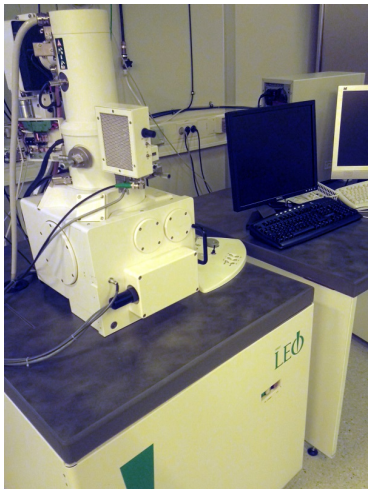
(a) RIE Oxford instruments Plasmalab80Plus.

(b) Laurell Model WS-650MZ-23NPPB spin coater.



(c) Karl-Suss MA45 UV mask aligner.

(d) KLA Tencor P-15 profilometer.



(e) LEO 1430 Scanning electron microscope.

(f) Nanoscribe Photonic Professional.

Figure 9. Some of the used equipment.

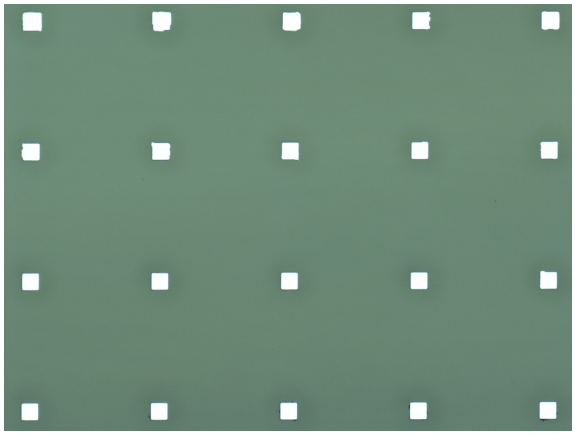


Figure 10. Optical micrograph of the chromium mask for photoresist patterning. Light areas are metal, dark areas are glass. One row is left out from the picture. Size of the squares is 50 µm × 50 µm.

addition, the longer chips might not rotate at an appropriate speed.

3.3.2 Cleaning of silicon chips

After cutting, the samples were cleaned with hot acetone. The surface was wiped with a cotton stick and the samples were sonicated for 4 minutes in FinnSonic m03 ultrasonic cleaner. Then they were rinsed with isopropanol (IPA) and dried with a nitrogen gas flow. Additional cleaning was done with O_2 plasma by using RIE Oxford instruments Plasmalab80Plus, shown in Figure 9a. The recipe had 50 sccm flow of O_2 at 40 mTorr with power of 200 W for 120 s.

3.4 Photoresist template

3.4.1 Mask used in template exposure

The mask used in making the photoresist template was a piece of glass patterned with chromium, and it is presented in Figure 10. The pattern had 50 µm × 50 µm square areas of approximately 100 nm thick chromium in 5 by 5 array with a 400 µm spacing. The fabrication of the mask was was not perfect, as can be seen from the figure. The edges have some surplus deposition. This was most likely caused by a too short lift-off time. Nevertheless, the mask was good enough as the shape of containers was not too crucial for the crystallization. Another mask used at the beginning of this project was similar. The only difference was that there were fever squares (3 by 3) and with smaller spacing (200 µm).

3.4.2 Materials and methods for template making

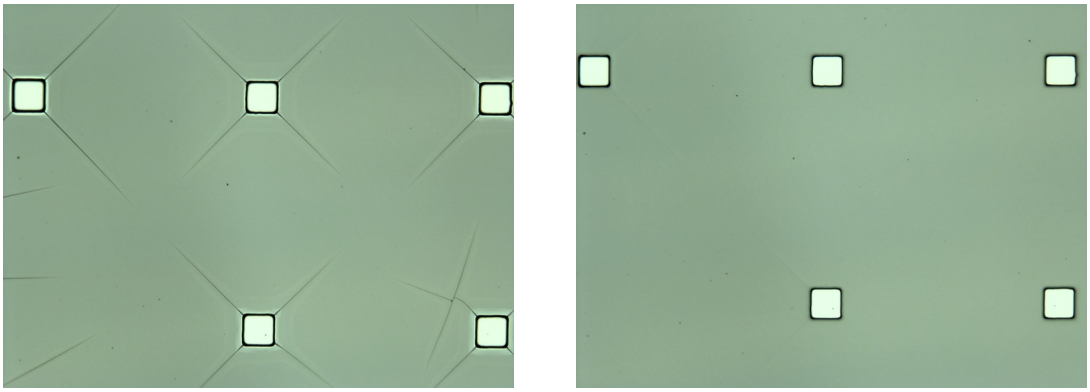
The first actual fabrication step was to make the confining structure from negative photoresist. SU-8 2002 (MicroChem) photoresist and Laurell Model WS-650MZ-23NPPB spin coater (Figure 9b) were used. Karl-Suss MA45 UV mask aligner (Figure 9c) was used for the exposure. The UV lamp was left to warm up beforehand, but it still had some fluctuations between different samples. Because of this, the exposure times discussed later are only a guideline. The most reliable way to make the contact between the sample and the mask was to simply place the mask on top of the sample with the metal side down. Immersion in L-ethyl lactate (Fluka Analytical) was used for the development. Developing was stopped with IPA, and samples were dried with nitrogen gas. For finished resist layers, KLA Tencor P-15 profilometer (Figure 9d) was used to measure the resist thicknesses. The system was controlled with Profiler Version 6.41 software. Usually thickness was measured from multiple positions for each sample, and an average was calculated.

The guidelines provided by the manufacturer [39] were followed. For SU-8 fabrication, the steps are: spin coating on top of a cleaned sample, soft bake to evaporate solvent, exposure with UV light (introduces chemical changes to resist), post exposure bake (actual cross-linking happens), development (unexposed resist is removed), and possible hard bake (makes resist more durable). The varied parameters were the spinning speed ($1500-7000$ rpm), the exposure time ($10-90$ s), and the development time ($10-120$ s). Spinning time was kept as 60 s. The baking times were kept as 1 min for soft bake, and 3 min for post exposure bake, both at 95 °C. The soft bake times were varied for multilayer samples.

Multiple periods are required to see the effects of PnCs. There was thus an interest to fabricate at least 10 layers thick crystals, so the resist layer also needed to be of appropriate thickness. For the spheres with diameter of 140 nm, around 1 µm thick resist would be suitable. Thicker layers were also attempted to allow for bigger spheres.

3.4.3 Photoresist template results

In the beginning, thicker resist layers were attempted. The aim was to get 10 µm thick resist. According to the SU-8 manual [39], one layer of 1500 rpm spin coated SU-8 2002 resist should give roughly 2.5 µm thick result. Thicker layers were aimed, but a slower spinning speed would not be a good option because the resist might not spread evenly. Instead, one attempt was to spin multiple layers on one chip with soft bakes between the layers. However, it was found that after the first layer the additional layers gave only a marginal addition to the total thickness. Overall, samples fabricated with a three-layer method had a thickness smaller than 3 µm, which is lot less than was expected. Even longer exposure times did not result in thicker resist layers. After the initial layer, the additional spin coated layers gave only $0.1-0.3$ µm increase to the total thickness. The soft baked SU-8 is probably



(a) Before hard bake. **(b)** After hard bake.

Figure 11. Optical microscope images of a sample with extremely cracked SU-8.

still fluid enough that the under layers are affected by additional spinning, and because of that, the increase in thickness is so small. Different underlayer (silicon or SU-8) could also affect the spin coating process. As the multilayer effectivity was so small, it was decided to use only one layer for the rest of the samples.

Occasionally, cracks could appear at the corners of patterned squares. One extreme case is shown in Figure 11a. This happened only with thicker resist layers (close to 3 µm) or with longer exposure times (over 45 s). Layers with thickness close to 1 µm did not seem to be as prone to crack formation. In addition, the adhesion of the resist layers seemed to be poor especially for shorter exposure times (under 30 s). Unsufficient sample cleaning before the resist spin coating can also cause poor adhesion. Some of the resist layers even started to peel off after crystallization. That is not good, as SU-8 should be durable enough to withstand later process steps. One possible solution for these problems was hard bake. In the hard bake, the developed sample is reheated. The effect of hard bake is presented in Figure 11. If heating and cool down are done slowly, it will anneal the cracks in resist. It will also make resist more durable. Slow heating and cooling were achieved simply by placing sample on top of a room-temperature hot plate instead of a pre-heated one and, likewise, the sample was kept on the hot plate after switching it off, instead of immediately removing it. As a downside, the hard bake might also affect the shapes of the patterned edges. Corners might become more rounded which is not necessarily wanted. The hard bake did not have notable effect on the thickness for resist layers when the original thickness was a couple of micrometers.

Overall, the geometry of the 8 mm × 16 mm samples proved to be difficult, especially when thinner layers were attempted. For thinner layers, faster rotation speeds were used during spin coating. Long, narrow samples had to be positioned carefully on top of a sample stage where there is a small area to make the vacuum contact to the sample for keeping the sample in place. However, such a non-traditional shape of the sample affects the spin coating. For the long samples, the SU-8 thickness was highly

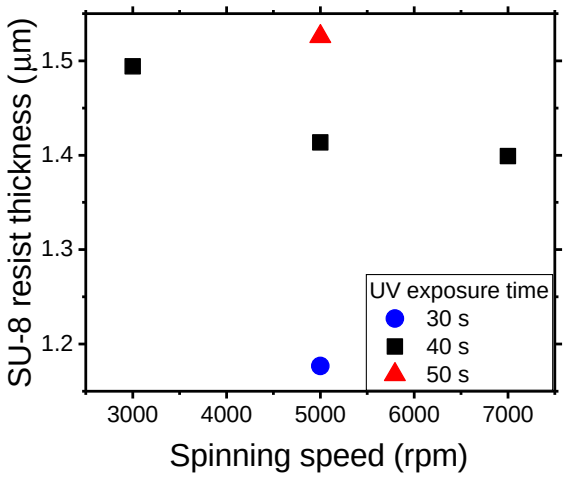
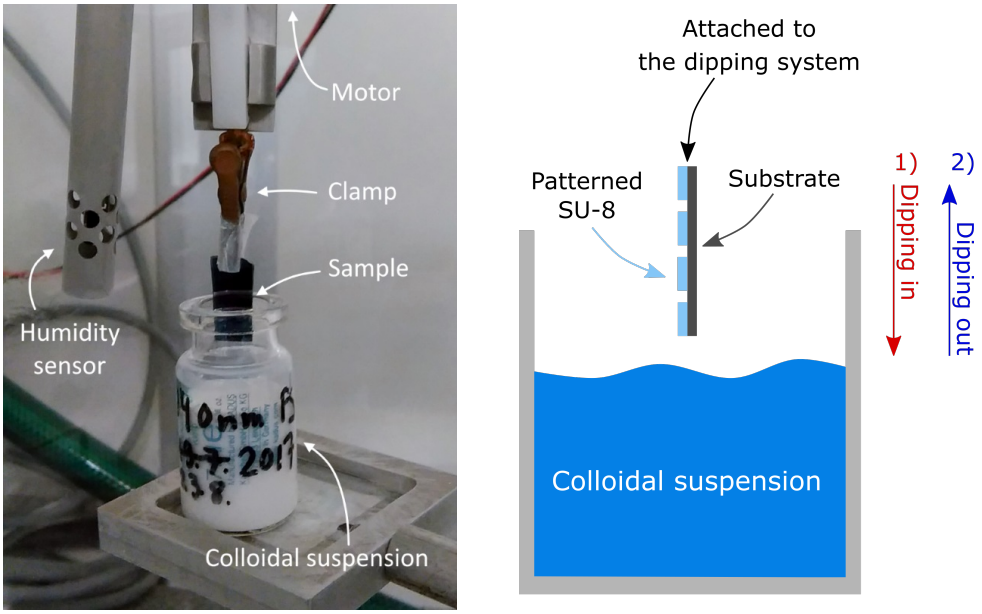


Figure 12. SU-8 thickness as a function of spinning speed with three different exposure times.

non-uniform. Oddly shaped contours were visible even to naked eye, and edge beads were really thick. In addition, resist thicknesses were highly non-reproducible with long samples, and they did not seem to follow the usual dependence on spinning speed and exposure time. Faster spinning speed did not necessarily result in a thinner resist. It is speculated that this could be because the vacuum head is relatively small compared to whole sample area, so it could not keep up with higher spinning speeds. The non-uniformity and non-reproducibility problems were solved by making the sample chips smaller and symmetric in both x- and y-directions, the size being 8 mm $\times$ 8 mm.

Some resist thickness calibration data is presented in Figure 12. For thinner resist layers spinning speed of 5000 rpm was mostly utilized to get a resist thickness that was close to 1 µm. As seen from the figure, faster spinning speeds did not make it notably thinner. Difference between 5000 and 7000 rpm with an exposure time of 40 s is under 20 nm. It was found, that especially with thicker layers, long exposure times produced deformations to corners of the patterned troughs. Long exposure times also made the final SU-8 layer thicker, as seen in Figure 12. However, with spinning speed of 5000 rpm the thickness seemed to saturate to 1.55 µm, and no thicker layers were produced with even longer exposure times. The exposure times of $30 - 40$ s produced best results as the deformities caused by overexposure appeared with longer exposure times. The development time did not affect the resist thickness by much, but it was also an important factor to sample quality. If the development time was too short, there were impurities that looked like white powder left on top of the sample. Development time of 1 min was found to be suitable.

The final recipe for the SU-8 step was to use 3 droplets of resist on top of 8 mm $\times$ 8 mm sized silicon chip for spin coating with spinning speed of 5000 rpm, soft bake time of 1 min, UV exposure time of 40 s, post exposure bake time of 3 min, and development time of 1 min. Both bakes were done at 95 °C. This resulted in roughly 1.4 ± 0.1 µm



(a) Photograph. **(b)** Diagram.

Figure 13. Vertical deposition or the so called ‘‘dipping’’ set-up. Sample is attached to a clamp which is connected to a motor. Motor controls the movement of the sample. Sample is first dipped in and then lifted up.

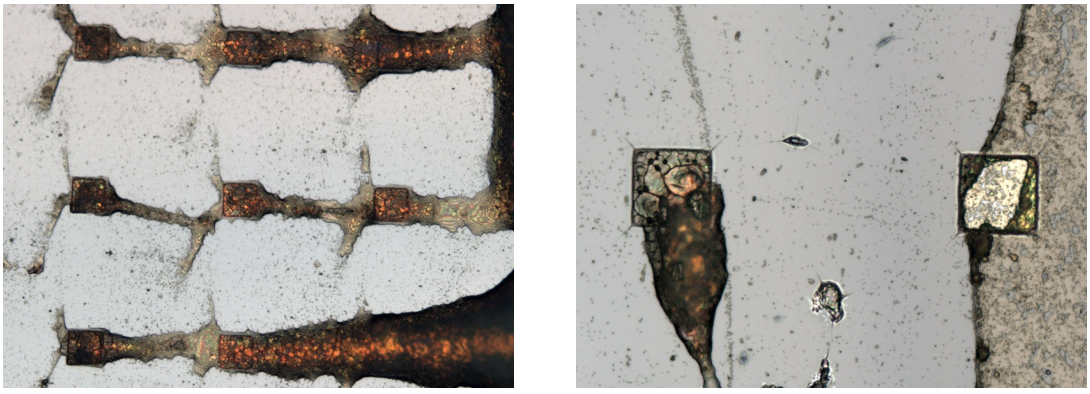
thick resist layer.

It should be noted that SU-8 2002 can be used only to produce resist layers with thicknesses around $1 - 3$ µm. For thicker or thinner layers, other concentrations of SU-8 should be used. If thicker samples are attempted in the future with a similar process, there might be a need for some adjustments. Thicker samples were more likely to form cracks. In addition, there should be more consideration to the shape of the side walls with thicker layers. Without filters, thicker layers might not produce vertical side walls, as the absorption of different wavelengths is not uniform through thicker layers [39, 40]. The top will absorb more which can result in an undercut structure or other deformations.

3.5 Colloidal crystallization

3.5.1 Materials and methods for single-step vertical deposition

Home-made set-up was used for colloidal crystallization by single-step vertical deposition, or the so called ‘‘dipping’’ process. The set-up had humidity and ventilation system connected to a chamber where dipping was carried out. The slowest lifting speed, 0.00675 mm/min, was always used. It was known to produce the best quality [7]. 260 nm and 140 nm diameter PS microsphere suspensions were used. Size distributions were ≤ 3 % CV and ≤ 6 % CV respectively. Both of them



(a) Crystals connected to each other. **(b)** Excess and detached crystals.

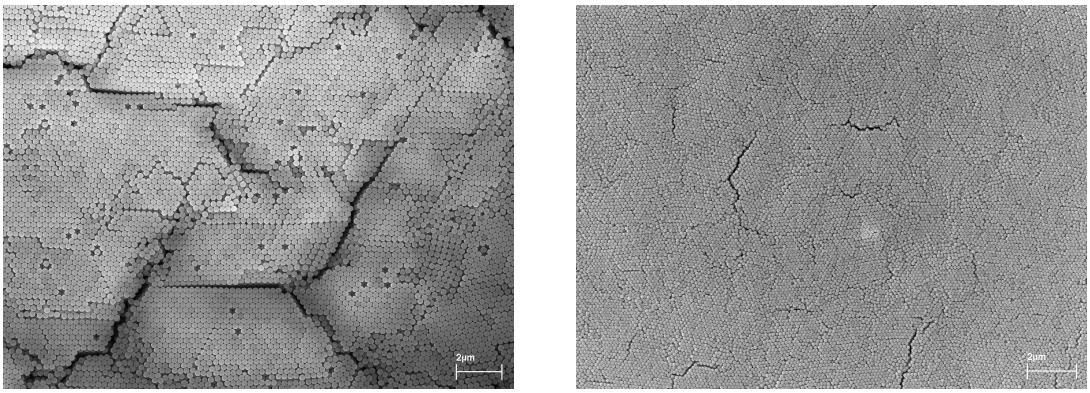
Figure 14. Optical micrographs of crystal deformities with 260 nm diameter microspheres. Square areas are 50 µm × 50 µm in both images.

were purchased from Duke Scientific Corporation and original suspensions were 10 % w/w in water. These were diluted with deionized water to get lower concentrations.

The dipping set-up and process is presented in Figure 13. First, the sample is attached to a clamp at one edge. In the case of smaller sample chips, those were first glued (with Marabu Fixogum) to a piece of plastic that was then attached to the clamp. A bottle with the PS suspension is positioned under the sample. The sample edge is driven closer to the suspension surface manually. After that, the equipment is programmed to quickly dip the sample in. This is done so that the wanted crystal positions are fully immersed in the suspension. Usually, the sample is dipped around 7 mm under the surface. After reaching the lowest position, the sample is slowly lifted up (''dipping out'') so that the whole sample rises over the suspension surface. After dipping, the sample is removed from the clamp and then rinsed with deionized water and dried with a nitrogen gas flow.

3.5.2 Crystallization results

The dipping speed was fixed so the other ways to control the crystal thickness were mainly the concentration of the suspension and the humidity of the chamber. The concentration was easily adjusted by diluting the original suspensions with water. However, humidity control was much more difficult. On one side of the dipping chamber, there is humidifier that is directed inside, and on the other side, there is a fan that ventilated excess humidity out. A humidity sensor was used to control a valve between the humidifier and the chamber, but the set-up was still very sensitive to the initial setting on the humidifier. Previous PS microsphere dipping experiments [7] were carried out without an additional humidifier. By those results, 1 % concentration of 260 nm diameter microspheres should be suitable for these samples. The humidifier was used in the beginning. It was also used in the previous dipping experiments with SiO_2 microspheres [22], as it made thinner crystals with



(a) 260 nm diameter microspheres. **(b)** 140 nm diameter microspheres.

Figure 15. SEM images of typical crystal surfaces. Scale bar is 2 µm long

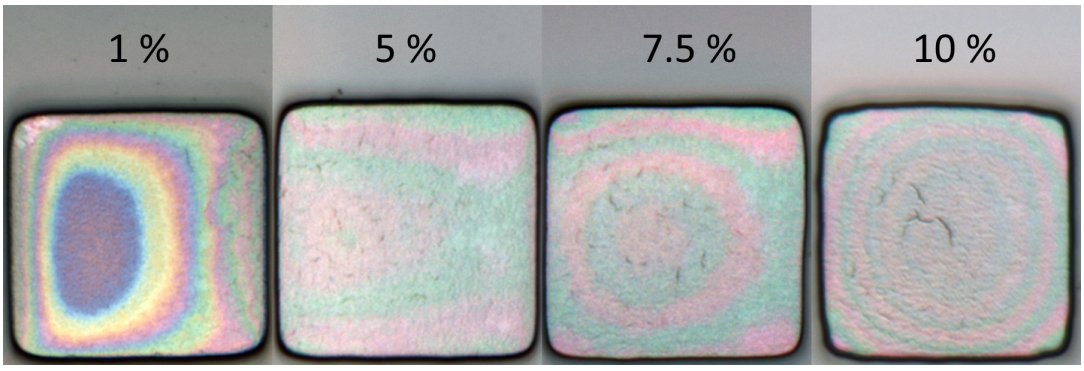
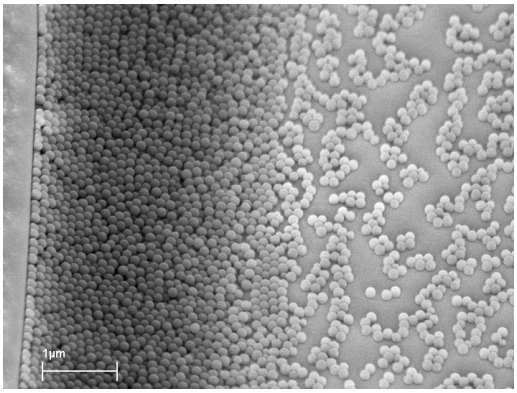
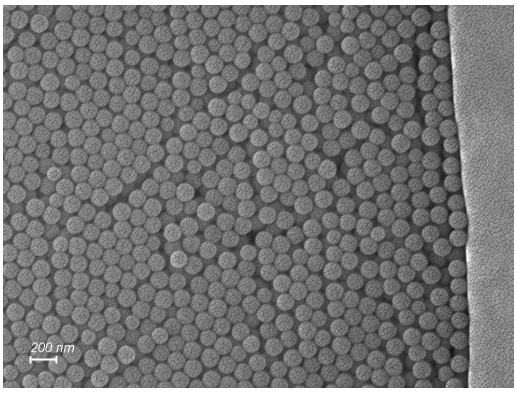


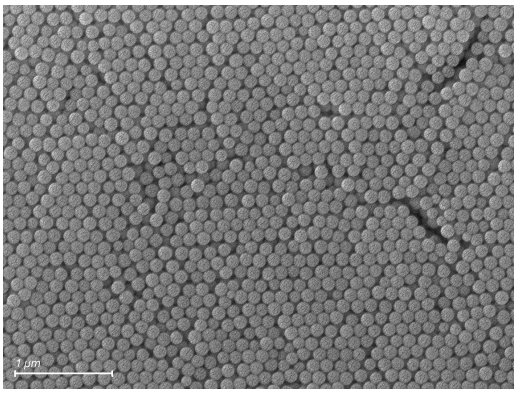
Figure 16. Optical microscope images of crystals formed from different concentrations of 140 nm diameter microspheres. All square shaped crystal sites are 50 µm × 50 µm.



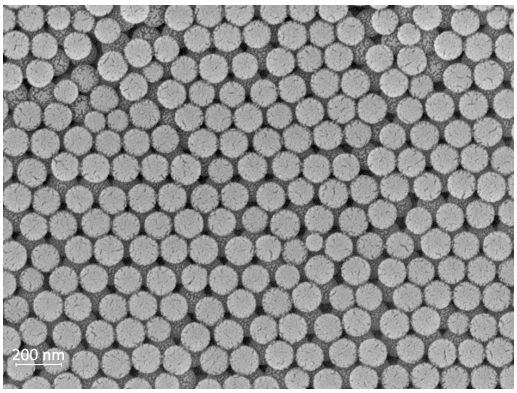
(a) Tilted image of partially filled trough. 1 % suspension.



(b) Crystal edge connected to SU-8 edge. 10 % suspension.



(c) Crystal surface. 10 % suspension.



(d) Crystal surface. 10 % suspension.

Figure 17. SEM images of crystals formed from 140 nm diameter microspheres.

better quality. However, it was realized that while fan was on, the PS suspension evaporated really fast. Fast evaporation increased the degeneration of the suspension and also made the actual concentration unknown. If the fan was turned off but humidifier left on, the chamber would be so full of water vapor that almost no crystallization could happen. In the end, more reliable results were gained by leaving both the fan and the humidifier off. Relative humidity was then between 33-45 %. It should be noted that some of the suspension would still evaporate during dipping, and later it was also found out that some crystal is also formed at the water-air interface, causing contamination of the suspension. PS is very hydrophobic, which can cause microspheres to attach to each other. Because of this, fresh suspensions are preferred to obtain the best quality.

In addition to the unreliability of the humidifier, there were also other challenges. When using the larger microsphere size, 260 nm, the produced crystals could easily grow also on top of the SU-8, despite it being much more hydrophobic than silicon. In addition, the produced crystals might occasionally get exceptionally large and thick and could cover the whole area, where SU-8 was patterned with pits or connect some of them, as seen in Figure 14a. If a pit was completely covered by a large crystal, the whole crystal would most likely detach away when rinsed with water, as shown in Figure 14b. The cause could be that during the dipping, the meniscus might not be able to adjust that well to changes in the surface when pits were close together, as the crystal usually got clumped over all of them. This was mostly countered by making a new mask where pits were further away from each other by growing the spacing between them from 200 µm to 400 µm. However, PS microspheres could still attach to SU-8 and overly large crystals could form. When there were crystals of appropriate thickness, the surface had multiple domains with clear cracks between them, as seen in Figure 15a. Some additional optical microscope images are also presented in Figures 18a, 18c and 18e. Cracks could be in the way of metal deposition, in addition to the unclean surface. It was then decided to try a smaller microsphere size instead, as there might have been some contamination in the suspension that caused the problems.

It was clear that with 140 nm diameter microspheres the same concentrations would not work as with the 260 nm spheres. Suspensions with only 1 % concentration could not even cover the bottom of the troughs, as presented in Figure 17a. An optical image of the same crystal is presented in Figure 16 on the far left. Dipping tests were carried out with varying concentrations ranging from 1 % to 10 %. Visual examples of the tests are presented in Figure 16. As can be seen from the images, crystals formed from the smaller sphere size were much less prone to cracking. The amount of cracks would slightly increase by the increase of concentration (and by the increase in thickness) as seen in the figure. The highest concentration would produce thickest crystals, so it was used in further dipping experiments. It was estimated to produce a thickness of around 1 µm by profilometer measurements. Even with the highest concentration, there were no similar problems of huge crystals on top of pits as with the bigger sphere size. Occasionally, a crystal could be deposited even on

top of SU-8, but it usually appeared only at sample edges.

By comparing the crystal surfaces of bigger and smaller sphere size presented in Figure 15, it can be confirmed that smaller spheres produced less cracks. In addition, cracks also were thinner. However, smaller spheres did not show as prominent long range order as larger spheres. This could simply be a property of smaller spheres. Smaller spheres also had a wider variance in the size distribution, which is also known to affect crystal quality. The short range order of crystals formed from smaller spheres is better presented in Figures 17c and 17d. While bigger sphere size was more likely to produce cracks, it was also more likely to produce cracks between the crystal and the SU-8. The smaller sphere size formed a contact with the SU-8 edge consistently most of the time as presented in Figure 17b.

3.6 Electron beam irradiation

3.6.1 Preliminary solubility test for crystals

As a preliminary test, it was experimented how different chemicals would affect un-treated PS crystals. This was to make sure if the hardening process is necessary or not. Acetone is known to dissolve PS, so other possible chemicals were chosen for the test.

There is a possibility that the crystal surface is too rough for lithography. In that case a smoothing layer might be needed. SU-8 has been previously used for this purpose [22]. Cyclopentanone is used as a solvent in SU-8 2000 series, so it was chosen as one of the tested chemicals. Cyclopentanone from Fluka Analytical was used. The sample was kept in solvent for 10 min.

The other two tested chemicals are also related to lithography. One is a developer used in laser lithography and the other one is a remover, which is used for lift-off after metal deposition. They were AR 300-47 and AR 300-76 respectively, both from Allresist. The sample was kept in developer for 2 min, as the developing step is usually fast, and 30 min in remover, as lift-off usually takes time.

After keeping the sample in the tested solution, it was rinsed with IPA and dried with a nitrogen gas flow. Separate samples were used for each solvent.

3.6.2 Crystal solubility results

Results from the preliminary test are presented in Figure 18. As it can be seen from Figures 18a and 18b, cyclopentanone dissolved PS, while SU-8 suffered only mild damage.

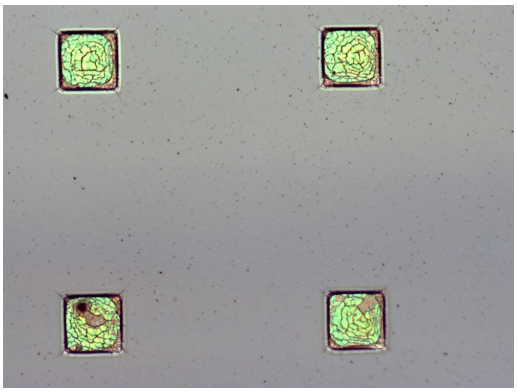
On the other hand, the AR 300-47 developer had more interesting effect, as seen in Figures 18c and 18d. After the treatment, the crystals looked darker or more ‘‘muddy’’, and they lost the bright color they had before. The bright opalescent color results from the effect of the ordered crystal on light, acting as a photonic crystal as opposed to phononic. In addition, the sample surface around the crystals looked dirtier than before. This would suggest that the developer had some sort of effect on at least the crystal surface. It probably removed some parts of it. This was confirmed with SEM imaging, presented in Figure 19. The PS microspheres do not seem to have any ordered structure anymore, which is the reason for the change in the color. There did not seem to be any places with ordered structure at least on the surface. There were also lots of PS microspheres on top of the SU-8. It can be concluded that AR 300-47 developer can detach PS microspheres from the crystalline structure. If the immersion time had been longer, there might have been even more drastic effects, for example the whole crystals could have been removed. However, interestingly, at least for the 2 min immersion time, there did not seem to be any effects on the PS microsphere size or shape.

The AR 300-76 remover had the biggest effects, and those are presented in Figures 18e and 18f. The whole SU-8 resist layer had peeled off, and only very small fragments of crystals had stayed attached to the substrate. The sample might have had just slight adhesion problems, but nevertheless, such strong effects were still kind of alarming. SU-8 should be durable enough to survive the lift-off. Luckily, AR 300-76 remover can be replaced with acetone for lift-off.

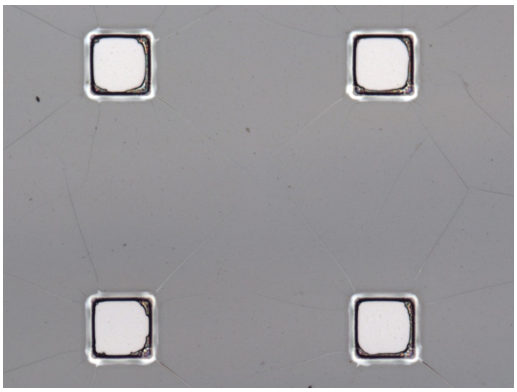
As a conclusion, none of the three chemicals is compatible with non-treated PS microsphere crystals. Hardening of PS is necessary, and after that it should be durable enough to withstand the rest of the fabrication steps.

3.6.3 Materials and methods for electron beam irradiation

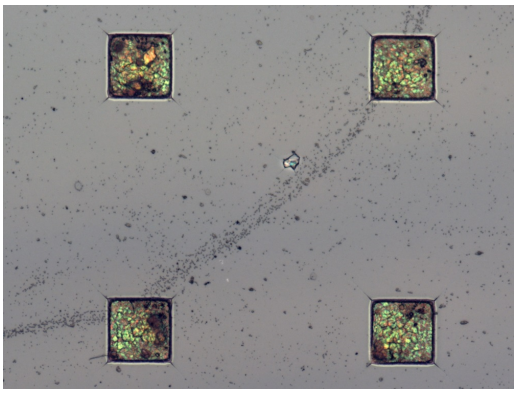
LEO 1430 Scanning electron microscope (Figure 9e) was used in electron beam irradiation. The electron beam irradiation resembled the traditional electron beam lithography, except that much higher doses were used. Samples were not coated with a conducting material so they would start charging very fast. Because of this, the imaging must be done quickly. The positioning of the sample is not exact so a pattern was made with 80 × 80 µm square to ensure that the whole crystal will be exposed, even if the alignment is not exactly right. Each crystal was aligned separately and then exposed. An aperture size of 10 µm, an acceleration voltage of 30 kV, a spot size around 700, and a current around few nA was used. After



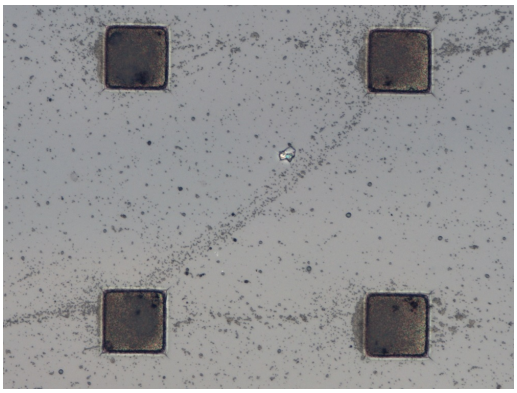
(a) Before cyclopentanone.



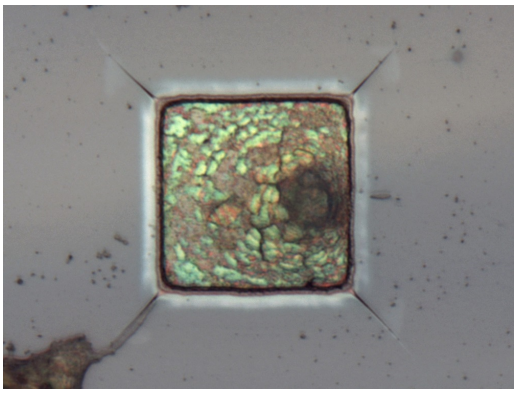
(b) After cyclopentanone.



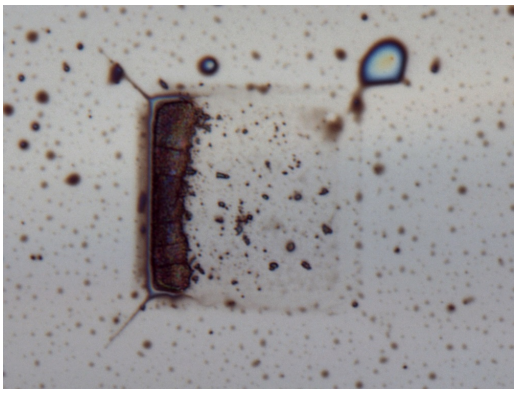
(c) Before AR 300-47 developer.



(d) After AR 300-47 developer.



(e) Before AR 300-76 remover.



(f) After AR 300-76 remover.

Figure 18. Optical micrographs of the effects of different solvents on samples. Square areas are 50 µm × 50 µm in all images.

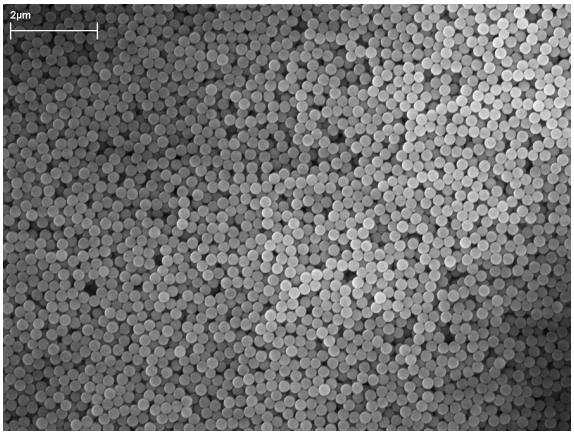


Figure 19. SEM image of sample after immersion to AR 300-47 developer. Scale bar is 2 µm.

irradiation, samples were immersed in acetone, then rinsed with IPA and dried with a nitrogen gas flow before the next fabrication step.

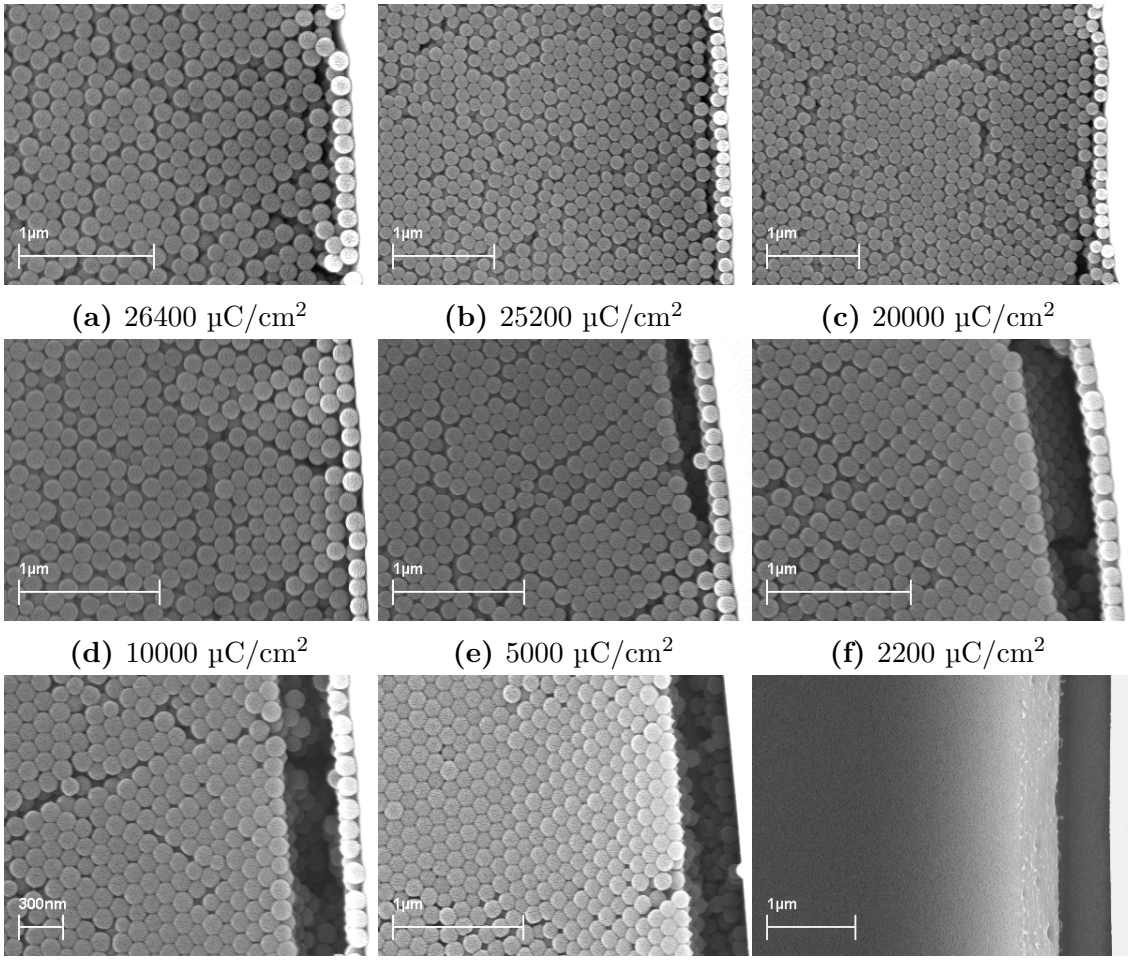
3.6.4 Electron beam irradiation dose test results

The previous thorough dose tests [8] were carried out for much thinner PS microsphere crystals, only 1-2 layers thick. A new test was therefore done to find out suitable dose of irradiation for thicker crystals. Previously, doses over 2000 µC/cm^2 had been enough to harden thinner crystals. In this dose test, doses from 500 µC/cm^2 to 26400 µC/cm^2 were used. All test crystals were on the same chip, and relatively uniform with each other.

Results of the dose test are presented in Figure 20. For doses 10000 µC/cm^2 and higher (Figures 20a-20d), there does not seem to be any difference. Crystals have retained their structure and PS spheres still have a round shape. For lower doses, PS spheres start to merge together (Figures 20e-20h). The lower the dose, the more crystal is deformed. As PS spheres merge together, the crystal becomes denser and a crack is formed between the crystal and the SU-8 resist edge. In addition to deep cracks at the edges, the middle parts of crystals also started to show an increasing amount of small cracks with decreasing dose, though it is not presented in the figures. The crystals with no irradiation, shown in Figure 20i, seemed to merge into mostly continuous material and also shrunk forming cracks between PS and SU-8.

Additional tilted image of low-dose crystal is presented in Figure 21. In this figure, the crystal edge is visible. As it can be seen, the PS spheres have deformed into a droplet shape at the edge. Most likely they have been in contact with the SU-8, and then gotten ripped apart from it, which has caused the contact area to stuck out.

As a conclusion, doses lower than 10000 µC/cm^2 are not enough to harden around 1 µm thick PS crystals. Too low doses cause PS spheres to deform and start to



(a) 26400 μC/cm^2 **(b)** 25200 μC/cm^2 **(c)** 20000 μC/cm^2

(d) 10000 μC/cm^2 **(e)** 5000 μC/cm^2 **(f)** 2200 μC/cm^2

(g) 1000 μC/cm^2 **(h)** 500 μC/cm^2 **(i)** Non-treated

Figure 20. SEM images of crystals with different doses of electron beam irradiation after immersion to acetone.

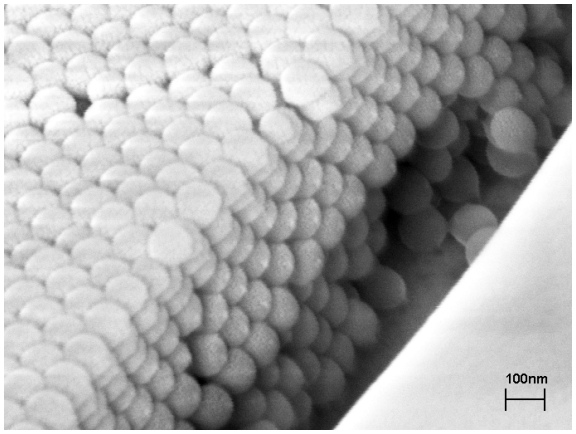


Figure 21. SEM image of low-dose irritated crystal from tilted angle. Scale bar is 100 nm.

merge together when exposed to harsh chemicals. The lower the dose, the bigger the effect. On the other hand, higher doses do not seem to have any difference. Doses over 20000 µC/cm^2 were thus used to harden the crystals before the next fabrication step to make sure that PS was fully cross-linked.

3.7 SINIS fabrication

3.7.1 Three-dimensional laser lithography

Three-dimensional laser lithography utilizes two-photon absorption. It is highly dependent on the intensity of the light, so the exposure will only happen at the focus point of the laser. To make patterns one defines parameters, selects different modes, and gives a path which the laser will travel. This path will define what kind of structure is made. MathWorks Matlab R2015b program was used to generate patterns used in the lithography to determine the path for the laser. Narrower exposed paths were designed with only a single line, and could be made narrower or wider with different values for the laser power. The widest exposed paths were designed with multiple parallel lines close to each other in the x-y-plane. For most patterns, the lines were repeated in z-direction with a 0.6 µm spacing to make sure that the exposure is done through the whole resist layer (thickness around 2 µm). This is demonstrated in Figure 24c. The piezo writing area is 300 µm × 300 µm, which gives some restrictions to possible patterns. Inside this area, movement can be controlled very accurately. The stage can also be moved mechanically without piezo scanners, but it is not as accurate, so some overlap for the write fields is required. An overlap of a few µm was usually enough.

First, the sample is spin coated with AR-P 3120 positive photoresist (Allresist). Bidtec Model:SP100 spin coater was used. The spinning speed was 1500 rpm and duration 90 s. Two layers were coated with bake times of 40 s and 60 s respectively, both at 100 °C. A single layer produced thickness of approximately 800 nm so the total thickness should be around 1.6 µm. Nanoscribe Photonic Professional 3D laser lithography machine (Figure 9f) was used to pattern the resist, and it was controlled with the NanoWrite program. The program uses .gwl files to read the wanted parameters and pattern. DeScribe program was used to check the patterns before exposure. The selected objective was Zeiss LD Plan-Neofluar 63x/0.75 Korr.

The spin coated sample is first glued to a sample holder with Marabu Fixogum. After the glue has dried, the sample holder is put in its place in such a way that the sample goes upside down, as the microscope objective is under the sample holder, and we cannot write through the opaque Si substrate. An inverted z-axis setting must also be used. An air-gap objective is used, so no immersion material is required. Nanoscribe finds an interface from the contrast of the materials, and in this case the interface is found between the air and the resist. The interface was found separately for each individual crystal, and it was additionally adjusted to make sure that it

(a) Chambers and monitors. **(b)** Rotatable sample stage.

Figure 22. UHV evaporator system.

was inside the resist. This was done by manually moving the objective closer to the sample. Transformation of coordinates was performed with three markers by measuring positions of different crystals and using knowledge of the SU-8 pattern to correct sample alignment. Tilt correction was performed with measurement from 9 points. Different values for laser power ($50 - 80$ %) were tested, otherwise the parameters are as represented in Appendix A.1, which shows an example of a typical code used for the exposure.

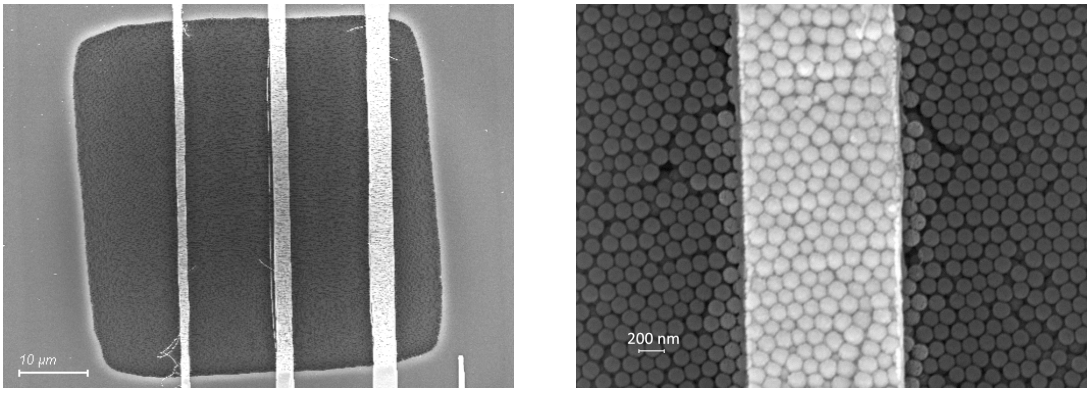
After the exposure, the sample is developed with a 1:1 mixture of deionized water and AR 300-47 developer (Allresist) for 60 s, then rinsed with deionized water and dried with a nitrogen flow. To remove the resist residues from patterned areas, oxygen plasma cleaning was used. The same machine was used as in the cleaning step (section 3.3.2), but with a gentler recipe. The recipe had 50 sccm flow of O_2 at 40 mTorr with a power of 60 W for 30 s.

3.7.2 Evaporation and lift-off

UHV (ultra high vacuum) evaporator system was used for the deposition, and it is shown in Figure 22a. First, the sample is attached to a stage with a clamp as presented in Figure 22b. It is important to make sure that the pattern is correctly aligned with the stage edge. The sample is loaded into the vacuum chamber via a load lock.

An electron beam is used to heat a metal source inside a crucible. Aluminum, copper, gold and titanium were available, among others. A wire test evaporation was made with gold with a thin titanium layer underneath, as explained in more detail in section 3.7.4. The actual SINIS junctions were made by depositing aluminum as a superconductor first, and then copper as a normal metal from two different angles, as explained in more detail in section 3.7.6.

After the evaporation and unloading process, the sample is detached from the sample



(a) Whole crystal. **(b)** Zoom-in.

Figure 23. Gold test wires on top of PnC crystal. Narrowest wire, as presented in b), is 1.2 µm wide.

stage and placed into hot acetone for lift-off. Hot acetone is used to remove the resist. The deposited metals on top of the resist will also be removed, so only metal that is attached directly to the sample surface will remain. The lift-off is enhanced by using a syringe to cause a stronger flow of acetone to the sample. It is finished by rinsing the sample with IPA and drying it with nitrogen gas.

3.7.3 Test design with straight wires

As a preliminary test, a pattern with only simple, straight lines was designed. The pattern had a few parallel wires to test different widths. Some of them had only single write-field line (the left one in Figure 23a), while some had multiple lines close together (the middle and right one in Figure 23a). The test was used to determine if metal deposition would be possible directly on top of the crystal surface. Bonding pads were also designed to be connected to some of the wires, so it was possible to test if the wires are conducting.

3.7.4 Test deposition with gold

A test evaporation was done with three angle evaporation: first in two tilted angles, 45° and −45° (compared to surface normal, along the pattern lines), which is recommended to ensure better step coverage, and then perpendicular to sample surface (0°). First, a thin layer of titanium was deposited from these angles, with thicknesses of 4 nm, 4 nm and 5 nm respectively, to ensure better adhesion for gold. Then the same was repeated for gold but with thicker layers, 10 nm, 10 nm and 40 nm respectively.

It was found out from the tests that even with only two AR-P resist layers (with total thickness of 1.6 µm), writing with focus at interface surface level was not enough to

expose through the whole resist layer. If the deposition was done on top of a partially exposed pattern, wires broke easily as there was no contact to the sample surface. Therefore, the exposure interface was adjusted by manually lifting the objective closer to sample surface. 1 µm adjustment still had occasional problems, but with a 2 µm adjustment, the exposure seemed to work well.

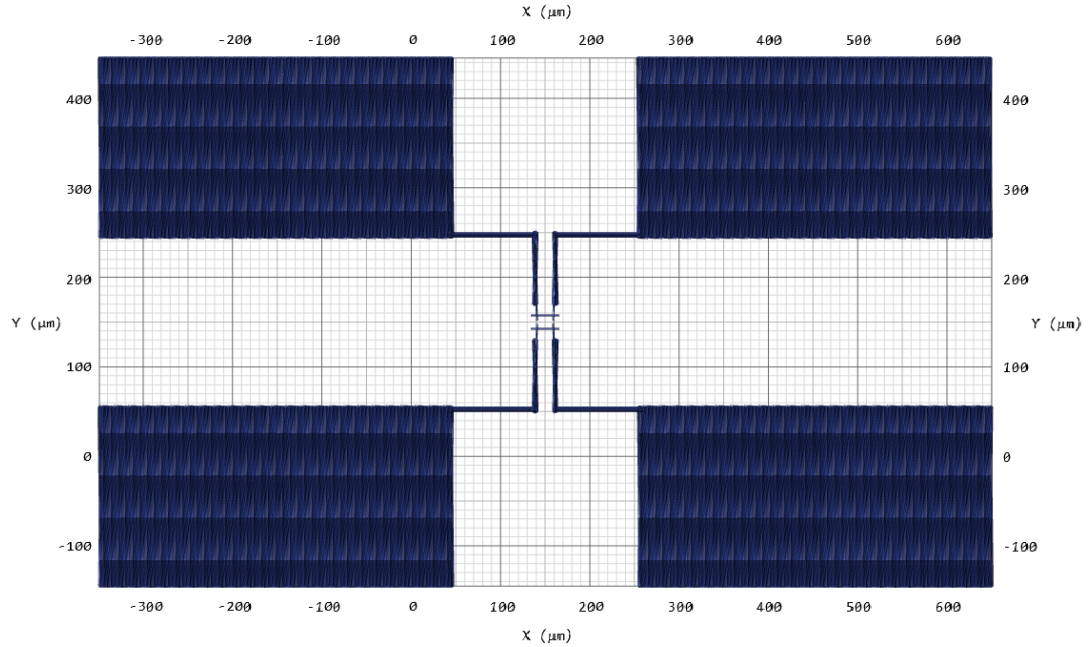
One of the tested samples is presented in Figure 23. It was found that the more the pattern was repeated along the z-axis, the smoother is the wire. The one in Figure 23 had four layers in the resist pattern. However, this might also make the wires slightly wider.

The resistances of the wires were measured to see if the deposition was successful. All wires which were measured were conducting. Resistances were in the range of $100 - 300\ \Omega$. Thinnest wire which conductance was measured was 1 µm wide. It was made with 80 % power and as a single line along z-axis, with a 1 µm adjustment in z-direction.

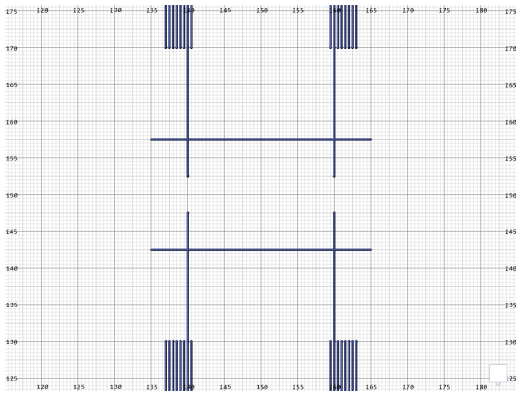
3.7.5 SINIS pattern design

The actual pattern was designed for two different metals to be deposited from two different angle sets. The aim was to fabricate two mirrored SINIS junctions against each other (Figure 24). These junctions should fit inside the 50 µm × 50 µm crystals, and wires should continue further away on top of SU-8 and connect to bonding pads. The connecting wires were made wider than the thin junction wires. The bonding pads were $200 - 400$ µm wide and tall. Both mesh style pads and full metal pads were tested. The only difference in fabrication between these two was the spacing between parallel lines. The pads would later be used to connect the junctions to measurement system.

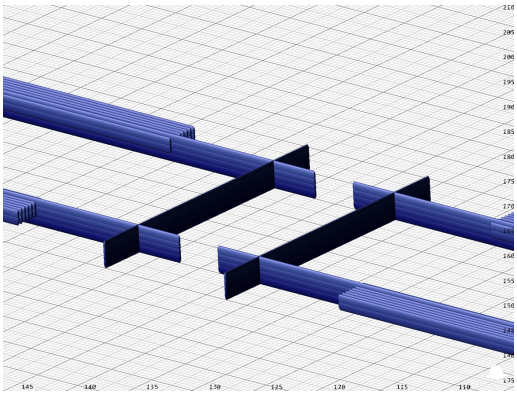
The SINIS lithography design is presented in Figure 24. As can be seen from the image, the junction has perpendicular lines for the two different metals (Al, Cu). The lines extend beyond the crossing point by 5 µm to make sure that metal is evaporated to the cross-section area even from high angles. During adjustments of the pattern desing, wires were made wider close to the crystal edge to ensure better step coverage between the crystal and the SU-8. The exposed areas are removed during the development, which results in a pattern presented in Figure 25. As can be seen, the resist can block line of sight to the sample surface if it is positioned appropriately. This is taken advantage of during deposition.



(a) Top view of the full pattern. The bonding pads are in full metal style.



(b) Top view of the junction.



(c) Tilted view of the junction.

Figure 24. DeScribe view of the SINIS pattern design. In the figures y-axis corresponds to direction of aluminum deposition and x-axis copper deposition. Scale is in micrometers.

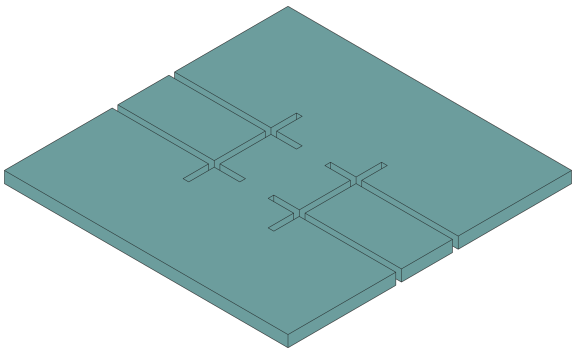


Figure 25. 3D visualization of patterned resist.

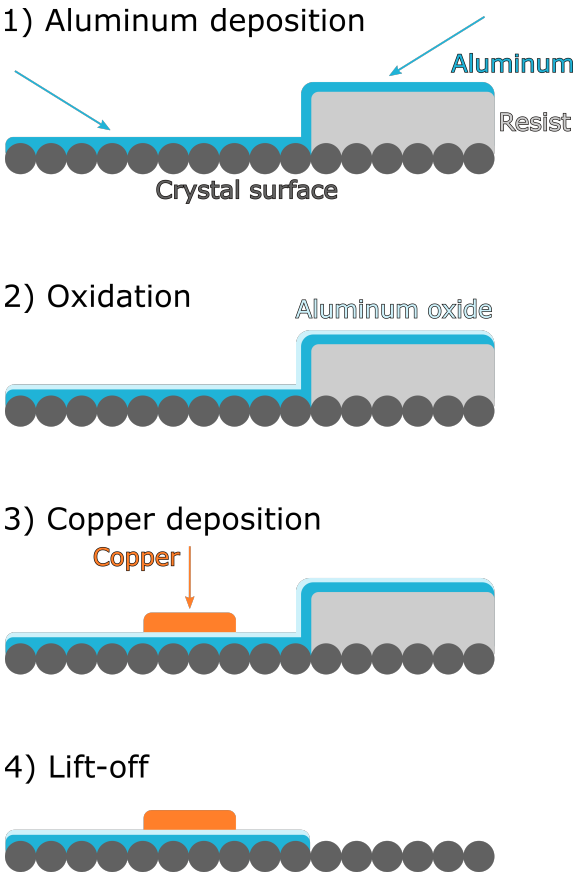


Figure 26. Steps in SINIS deposition. Sample is presented as a cross-section along the aluminum wire.

3.7.6 SINIS two-angle deposition

The evaporation scheme for the SINIS junctions is presented in Figure 26. First, aluminum is evaporated while the sample is tilted to high angles in such a way that the deposition is only made to the lines in one direction. Then the sample is moved to the loading chamber, where pressure is raised to 200 mbar with oxygen gas. The sample is kept there for 20 min to form an aluminum oxide on top of the aluminum wires. Then the sample is turned by 90° rotation in the sample plane, loaded into the main chamber and the deposition is repeated for copper, also from large angles. Figure 22b shows the sample stage, where the round part is rotatable, which is turned to achieve the 90° change in sample orientation.

The angles and thicknesses for the evaporation are presented in Table 1. The angles were always changed in such way that the normal of the sample surface was kept away from the evaporation source to make sure there was no unwanted deposition. The rate for both aluminum and copper was roughly 0.1 nm/s. The total layer thicknesses for both metals were quite thick to compensate for surface roughness. In total, along the surface normal, aluminum was around 40 nm thick and copper

Table 1. Evaporation parameters for SINIS junction. The angle of evaporation is measured from the surface normal which is at 0°. The thickness is given along the evaporation direction.

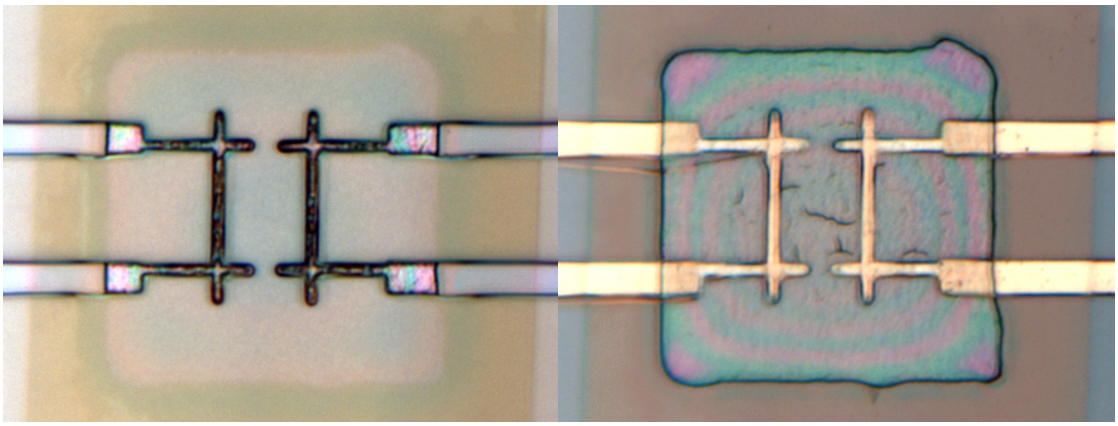
Material (surface orientation)	Angle	Thickness (nm)
Aluminum (0°)	±70°	10 + 10
	±66°	10 + 10
	±64°	10 + 10
	±60°	15 + 15
Copper (90°)	±70°	10 + 10
	±68°	10 + 10
	±65°	15 + 15
	±63°	15 + 15
	±60°	20 + 20

60 nm thick.

3.7.7 SINIS fabrication results

As with the test evaporation, SINIS fabrication directly on top of the crystal surface was successful. A typical example of a sample after the exposure and the development is shown in Figure 27a, and after evaporation and lift-off in Figure 27b. As it can be seen from the figures, the metal was deposited only to areas where there was no resist. The shape of the evaporated thin films follows closely the patterned geometry. In Figure 27b it is clear that the two-angle deposition of SINIS junctions had succeeded quite nicely as the two different metals, copper and aluminum, can be differentiated by their color in the optical microscope image. Copper in the middle of the junctions has reddish tint, while aluminum is closer to white. However, it is also possible to see some really thin extra wires on the left side of the figure. This is some extra deposition which might occasionally be left over from the lift-off, because some deposition is done also on to the resist walls, and it might stay attached to the sample.

Nevertheless, there were also some problems. Wires might occasionally end up with no contact. This was partially countered by making wires thicker at the crystal edges where there were the biggest steps. In addition, as the crystals did not fully fill the containers, the spin coated resist was not completely uniform. Adjustments were done in such a way that the pattern had multiple repeats along the z-axis directly on top of crystal, where there was the most delicate part of the pattern, and fewer elsewhere. This way it was more likely that the resist in the junction area was exposed the whole way through. 80 % or 70 % laser power seemed most reliable to produce continuous films to junctions, while with lower power values, there was



(a) Sample after exposure and development. **(b)** Sample after evaporation and lift-off.

Figure 27. Optical microscope images of fabrication steps of SINIS junctions. Size of crystal area is 50 µm × 50 µm.

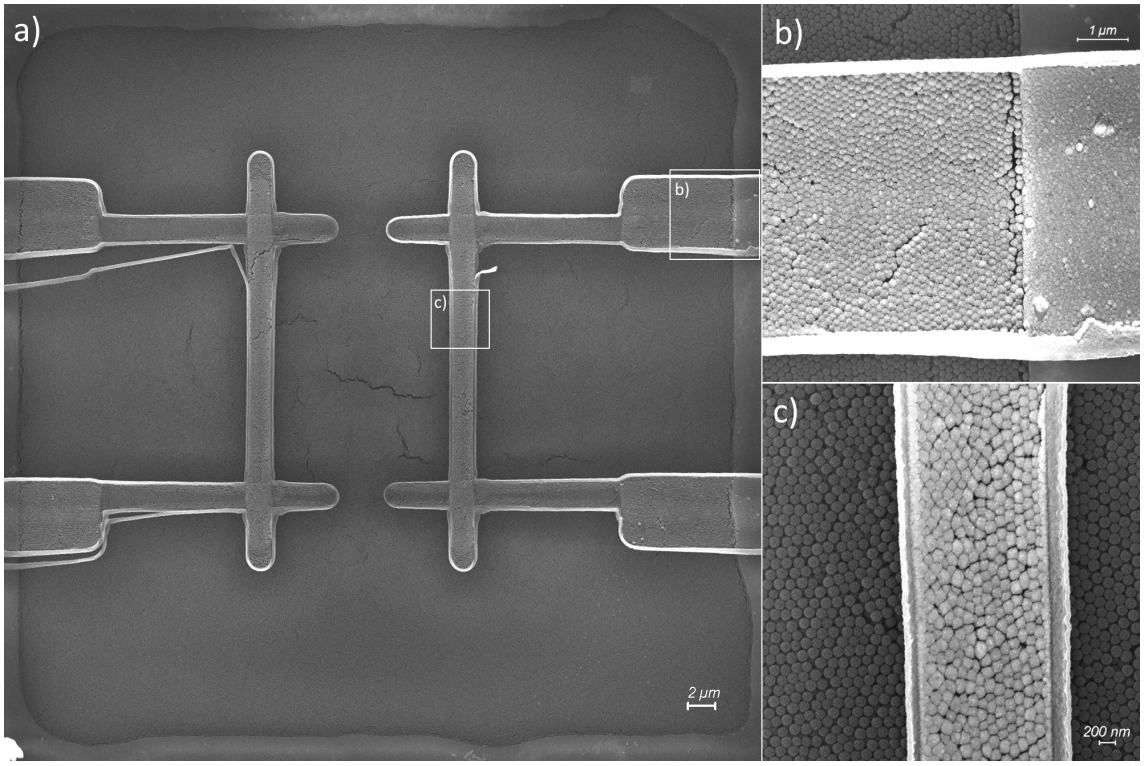


Figure 28. SEM images of SINIS junctions on top of a crystal. a) Overview of the whole crystal. Square areas show where the insets are from. b) Wire at the crystal edge. Some minor cracking is present. c) Copper wire on top of crystal.

usually no electrical contact.

SEM images of a fabricated sample are presented in Figure 28 which was first used in measurements reported later in section 4.3, before imaging. The optical images of the same sample presented in Figure 27 were taken before the measurements. SINIS junctions are so delicate in nature that they can be broken easily by imaging techniques other than optical microscopy, which is why measurements were carried out first. In addition, the sample was coated with a thin gold layer for SEM imaging which would have disturbed the measurements. In Figure 28a the whole crystal can be seen along with the wiring on top of it. Part of the normal metal wire is presented in Figure 28c. Copper and aluminum can be differentiated from each other similar to Figure 27b, but in the case of the SEM image copper is slightly lighter than aluminum. The junction parts where two metals cross each other can be clearly seen. In addition, the excess deposition at pattern edges can be seen even more clearly in the SEM images. Especially in Figures 28b and 28c the wires seem to have additional width that looks different from the middle parts of the wire. In Figure 28b some cracking can be seen at the crystal edge. However, the crack lengths are much thinner than the whole wire width. Also, the measurements have shown that the junctions were conducting, so such small cracks are not an issue. It still gives a hint that the crystal edge really needs wide wires. As the SEM imaging was carried out only after the measurements, it is possible that the cracks at the edge were formed during cooling. At least the bigger cracks in the middle of the crystal were present even before measurements, as those can be seen in the optical microscope image in Figure 27b, but the smaller cracks can not be resolved from it.

By measuring distances from the SEM images, it was found that the junction wires were 2 µm wide, and the wires at the crystal edge were 6 µm wide. The distance between the two parallel SINIS junctions was 13 µm when measured from the normal metal edges (and 15 µm when measured from wire centers), and the normal metal island was 17.5 µm long between the superconductors.

The fabricated junctions had room temperature resistances ranging from few hundred ohms to hundreds of thousands of ohms. Resistances below 1 kΩ most likely had a SNS contact instead of SINIS, as is known from previous studies [16]. The test wires made from gold in section 3.7.4 had resistances of the same order of magnitude. Resistances in the range of 1-10 kΩ seemed most typical for these junctions. Resistances over 100 kΩ were probably very damaged from too long a lift-off, or were highly noncontinuous from surface roughness, or there were some sort of other problems. Resistances so high were previously encountered [16] with thinner aluminum - aluminum oxide - copper junctions which had undergone additional lithography and etching steps. There, the increase in resistance was attributed to damaged copper.

3.8 Control sample

3.8.1 Materials and methods for polystyrene thin film

To really study the effects of PnC, it should be compared to a simple sample without the crystal structure, but which is otherwise as close to the PnC sample as possible. In the case of 2D PnCs, a continuous suspended thin film without a hole pattern can be used as a control sample [4], as shown in Figure 3. In our case of a 3D PnC, a continuous piece of polystyrene in place of the crystal with the same thickness would be an optimal solution. However, as seen in section 3.6.4, such sample can not be simply fabricated by destroying the crystal with solvents. First of all, immersing non-treated crystals to acetone caused huge cracks between the PS and the SU-8 container, which would make junction fabrication impossible. In addition, as deformed crystals become more dense, they also most likely get thinner. As a conclusion, some other method had to be found.

PS can be dissolved into various chemicals, as already noted. Solutions containing dissolved PS can be used in spin coating to produce thin films of various thicknesses. Toluene is common choice for this application. [41] Toluene is known not to break PS chains, which means that it does not deform the polymer structure much. PS has also good solubility to toluene even in room temperature. [42] A dried PS microsphere suspension was used so that the PS structure is as close to the PnC samples as possible. If some other PS source were to be used, there could be different molecular weights, lengths and branching. Toluene $\geq$99.5 % (AnalaR NORMAPUR ACS, Reag. Ph. Eur. analytical reagent, VWR Chemicals) was used as solvent. Toluene is flammable, so no high temperatures were used during dissolving. 0.35 g of dried PS microspheres were weighted to a container and subsequently dissolved into 4 ml of toluene. This resulted in approximately 10 % solution by weight. The concentration was chosen so it is known from literature to produce thin films with thickness close to 1 µm [41].

The solution was spin coated to both clean silicon chips (after steps presented in section 3.3) and samples with pre-patterned SU-8 layer (like at the end of section 3.4 right before crystallization). The spin coating was done with the same spin coater as in the SU-8 deposition. After the spin coating, the samples were always left to dry in vacuum overnight to make sure no toluene was left [41]. PS layer thicknesses were measured with the same profilometer as for SU-8.

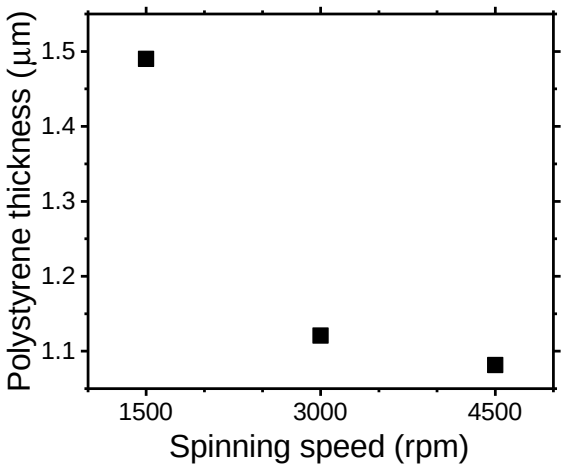


Figure 29. Polystyrene thickness as a function of spinning speed.

3.8.2 Spin coating results

Spin coating on plain silicon chips was done with spinning speeds of 1500, 3000 and 4500 rpm, and the results are presented in Figure 29. As it can be seen, the increase in spinning speed does not affect the thickness much after 3000 rpm. The decrease from 3000 rpm to 4500 rpm is only under 50 nm. 4500 rpm produced the thinnest film, and also closest to 1 µm, measured to be (1.08 ± 0.02) µm thick. This was chosen to be most suitable thickness for the reference sample.

The same solution and 4500 rpm spinning was then used in spin coating on top of the prepatterned SU-8. However, both the pits and the SU-8 surface were covered by the 1 µm thick layer of PS, which resulted in tall walls around the pit sites. The features were relatively smooth so the pits were hard to differentiate from the rest of the sample with the SEM. Due to this, the whole sample area would get some exposure while looking for the right place, and it was not possible to expose and cross-link only very specific places with this method. Good markers would be required to make sure not to expose unwanted places. The exposure was too much so the PS surrounding the pits was left in place even after immersion to acetone. Because of this, there would be big topographical changes near the places where SINIS junctions would be made. Metal deposition from large angles might not be possible.

Judging from these tests, it would be more straightforward for SINIS patterning and junction deposition to simply use a continuous PS film on top of a plain silicon chip. This would mean that the control sample would not have SU-8 like the actual samples. Nevertheless, SINIS junctions serve as a local thermometer and heater, so that surrounding areas that are relatively far away most likely do not cause too big of a change to measurements.

3.8.3 Control sample fabrication

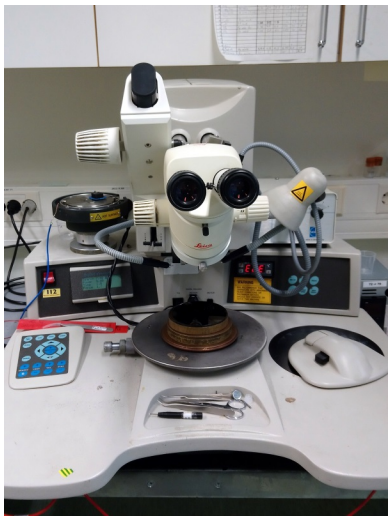
After making the continuous PS thin film, the rest of the fabrication steps should follow usual the sample fabrication as closely as possible. These are already covered in sections 3.6 and 3.7. However, because the control sample does not have SU-8 to surround it, the whole area, also for the pads, has to be hardened with electron beam irradiation. This was done in a similar way as before, except that the area was made larger. The center area where junctions would be positioned was hardened with the same dose as the crystals (> 20000 µC/cm^2) to make sure it would behave similar to hardened crystals. Elsewhere, slightly lower dose seemed good enough (> 2000 µC/cm^2). Otherwise the sample fabrication was carried out as usual.

4 Measurements

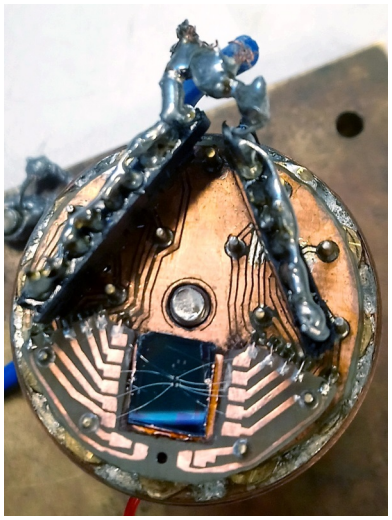
4.1 Attaching sample to the sample stage

The first step to make measurements possible is to attach the sample to a sample stage and form electrical contacts from the sample to the stage. The sample is glued to a cleaned stage with a varnish that has good thermal conductivity. Then thin aluminum wires are used to make contacts from the stage to the pads. Kulicke & Soffa 4523A wire bonder was used shown in Figure 30a. The bonder supplies wire from a tip of a needle, uses a force to move the needle to touch the sample and then bonds the wire with ultrasonic power. In these samples, the bonding pads were fabricated on top of SU-8, which is relatively soft material compared to usual bonding, where pads are on top of silicon or similar material. In a previous study [22], bonding was attempted directly on top of colloidal crystal consisting of SiO_2 microspheres. However, such material was too soft and easy to crumble, and bonding destroyed the sample. Also in this study it was noted that bonding directly on top of SU-8 was not very stable. This has been previously found with even much thinner SU-8 layers [43]. The needle could easily penetrate the surface, and the applied high power could destroy the pad, or metal could be ripped away by the aluminum wire. Especially, mesh style pads were easily broken and contact was lost. Wires could attach to the surface, but there would be no contact as the conducting lines were broken. Pads with continuous metal seemed to withstand the harsh process better, and those were used for the samples. The bigger the pads were, the easier the bonding. However, making large continuous structures with Nanoscribe is time consuming, so a pad size around couple of hundred micrometers was used. Examples of pads before and after bonding are presented in Figure 31. As it can be seen from the figure, thin film has been removed from the places where bonding was attempted. An example of a bonded sample is presented in Figure 30b.

The contacts made with the bonder seemed unstable. Some of them were lost, if multiple cool downs were attempted with the same sample. Because of this, alternatives were investigated. One idea was to use indium bonding. In indium bonding, gold wires are pre-cut into short pieces, and soldered indium is used to connect them to sample pads and to the stage. No machine is used in the process. Instead, the wire ends are pushed to contact with a sharp tool by hand. Because of this, four-point-measurements are not possible directly at the chip. The pads are too small to fit two wires to single pad with this method. However, instead, four-point-measurement can be made at sample stage by connecting two stage pads with each other. This is still much better compared to two- or three-point-measurement



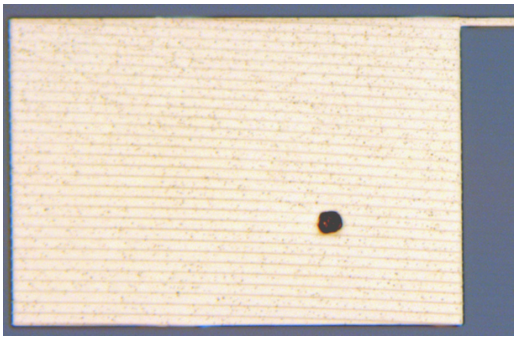
(a) Kulicke & Soffa 4523A wire bonder.



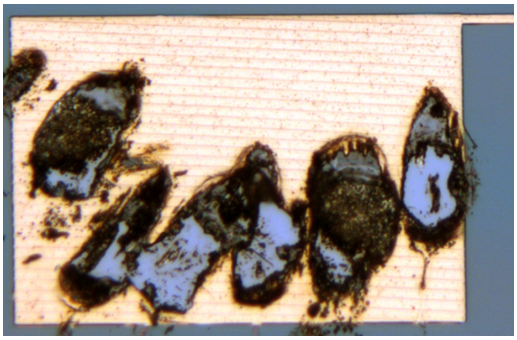
(b) Bonded sample. Grounding is still attached to sample stage.

Figure 30. Photographs of the bonding process.

at chip because the wiring inside the cryostat is canceled out. Indium bonding was carried out successfully even on top of SU-8, and all the made bonds survived cool down which is promising. However, no actual data has been collected with this type of bonding from these samples yet. The measurements reported in later sections had bonds made with the ultrasonic bonder.



(a) Pad before bonding.



(b) Damaged pad after bonding.

Figure 31. Optical microscope images of effects of bonding to a sample. Pad size is 300 µm × 200 µm, and it was made from a continuous thin film.

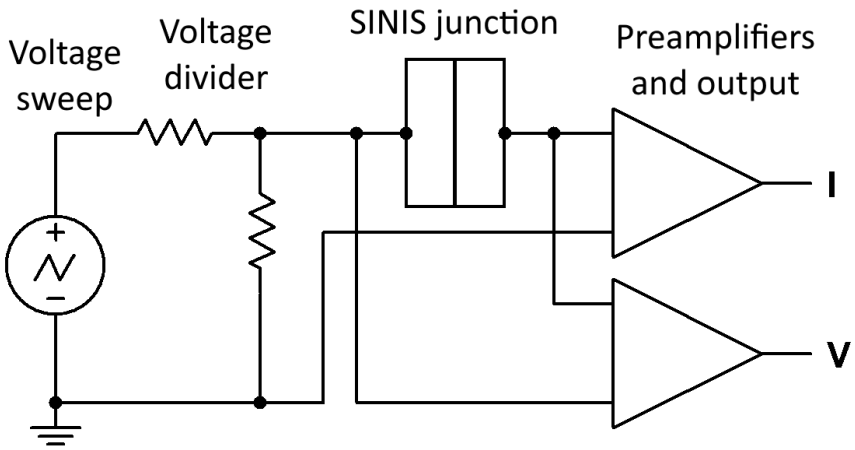


Figure 32. Circuit drawing of the current-voltage characteristic measurement scheme.

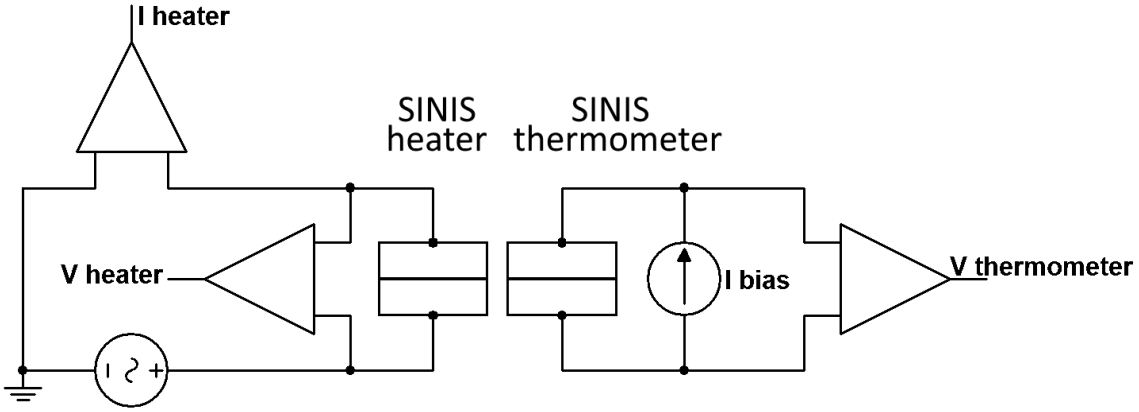


Figure 33. Circuit drawing of the thermal conductance measurement scheme. Only the right side circuit would be used during the thermometer calibration when bath temperature is slowly changed, and it is recorded along with the voltage reading.

4.2 Measurement set-up and scheme

Measurements were carried out in EM noise shielded measurement rooms. ^{3}He-^{4}He dilution refrigerator was used to reach the measurement temperatures. A four-point measurement directly on the chip is preferred to be used for all junctions. It would eliminate voltage drops in the lead wires and contacts, and only the junction and nanofabricated wires would be taken into account. However, because of the unstable bonding process discussed in previous section, contact was sometimes lost from some of the bonds. In such cases only three- or two-point measurement was carried out.

First, current-voltage characteristics of the SINIS junctions are measured by a slow voltage sweep. Circuit drawing of the set-up is presented in Figure 32. The measurement is repeated at different temperatures starting from the lowest. The

temperature is increased by heating the sample stage with a electrical heater. A voltage divider is chosen according to the superconducting gap size, so that the swept voltage has an appropriate amplitude. The divider can be changed between measurements to gain a wider range of data. From the current-voltage measurements, the junctions can be characterized and the data can be compared to the theory. The preamplifiers used were Ithaca model 1211 current preamplifier and Ithaca model 1201 voltage preamplifier.

For thermal conductance measurements, the plan would be to determine a suitable value for biasing current from the current-voltage data. The current would be chosen to cover the temperature range that is of interest. Next, the junction would be biased with a chosen constant current, and a voltage-temperature calibration would be carried out during slow cooling of the sample. After that, the junction could be used as a thermometer as the temperature of the junction is known from the voltage reading. So finally, heater-thermometer measurements could be carried out. One junction would be heated while measuring used power. The other junction, serving as thermometer, would have its voltage read while the biasing current stays constant. Circuit drawing of this is presented in Figure 33.

4.3 Characterization of single SINIS junction

As a first measurement, one junction on top of a crystal was cooled down and its characteristics were studied. Measurements were done as a two-probe measurement on the chip. 1:5000 divider was used for most of the measurements, as it was enough to bring the sweep amplitude close to the gap value. The results are presented in Figures 34-38. The voltage and current off-set are corrected in these plots to the best ability. Voltage was adjusted with the knowledge that the middle point of the superconductive gap should be positioned at zero voltage. Respectively, the current should be zero when voltage reaches zero. These considerations were used to advantage when adjusting the off-sets of the data.

In Figures 34 and 35, the current-voltage characteristics are presented in linear scale. As it can be seen, the current drops to zero between specific voltages at low temperatures. This is the gap area. At higher temperatures this effect is slowly lost. At 800 mK the curve almost resembles a straight line which would be Ohmic behavior. The junction behavior is a bit asymmetric. At higher voltages all curves are grouped together.

The current-voltage measurement at 50 mK with smaller 1:500 divider is presented in Figure 36 along with a linear fit. The total tunneling resistance across the junction can be determined from fitting parameter b by simply $R_T = 1/b \approx (7.124 \pm 0.003)$ kΩ.

Similar behavior as in the linear scale can also be seen in log-linear presentation of the data, shown in Figure 37. All curves merge together at high voltages. However, as the current approaches zero, the resolution of the digitizer start to have a large

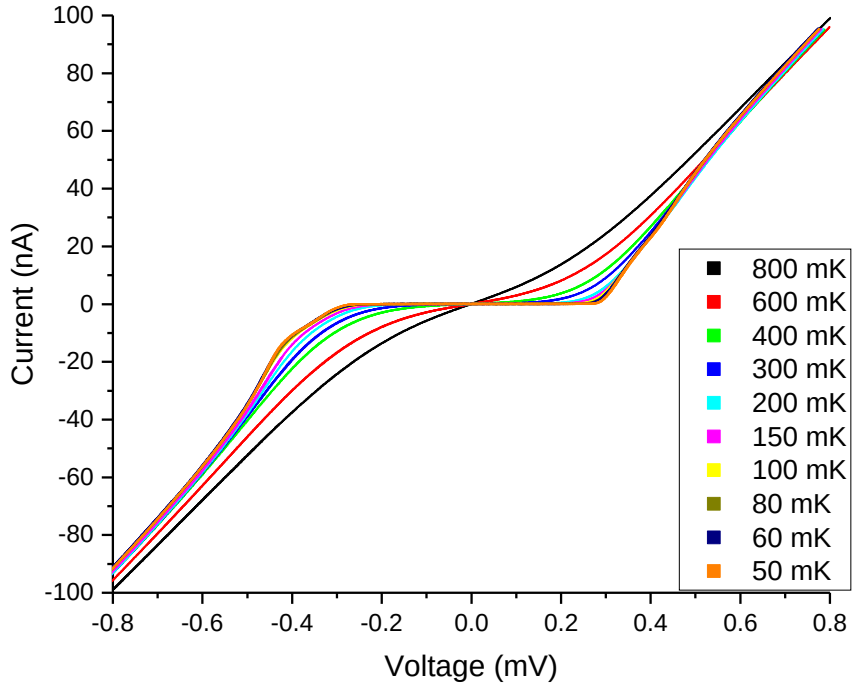


Figure 34. Current-voltage curves at different temperatures in linear scale, full measurement, SINIS junction.

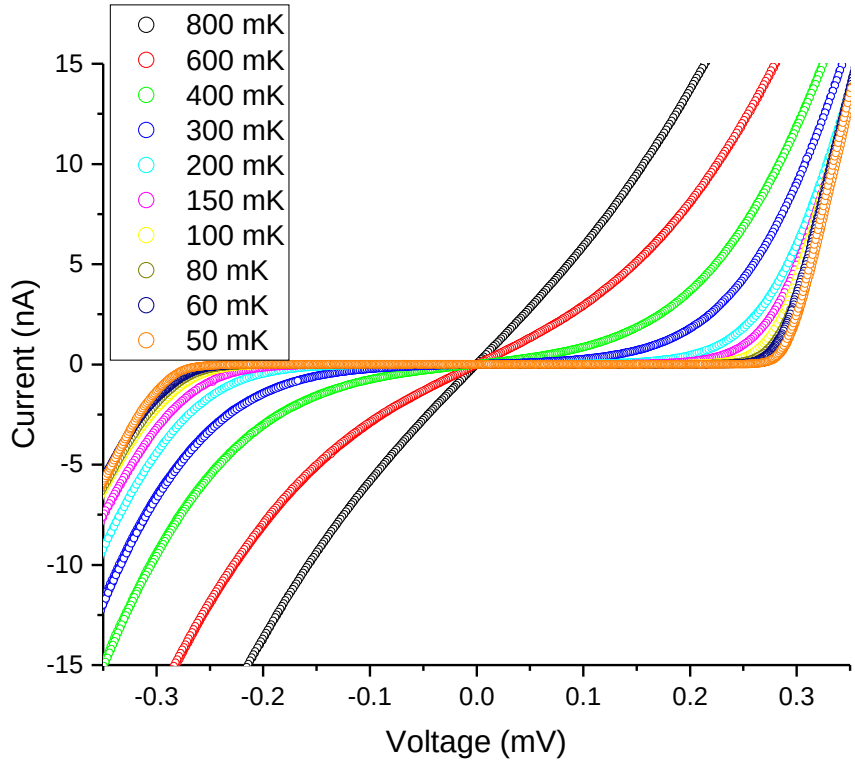


Figure 35. Close-up of gap-area from Figure 34, SINIS junction.

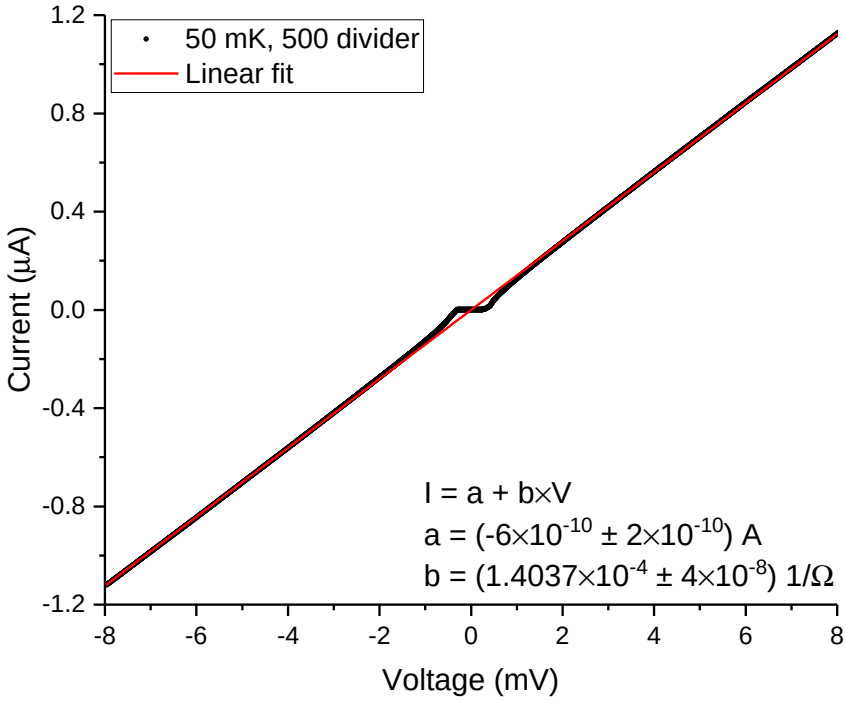


Figure 36. Current as a function of voltage at 50 mK with linear fit, SINIS junction.

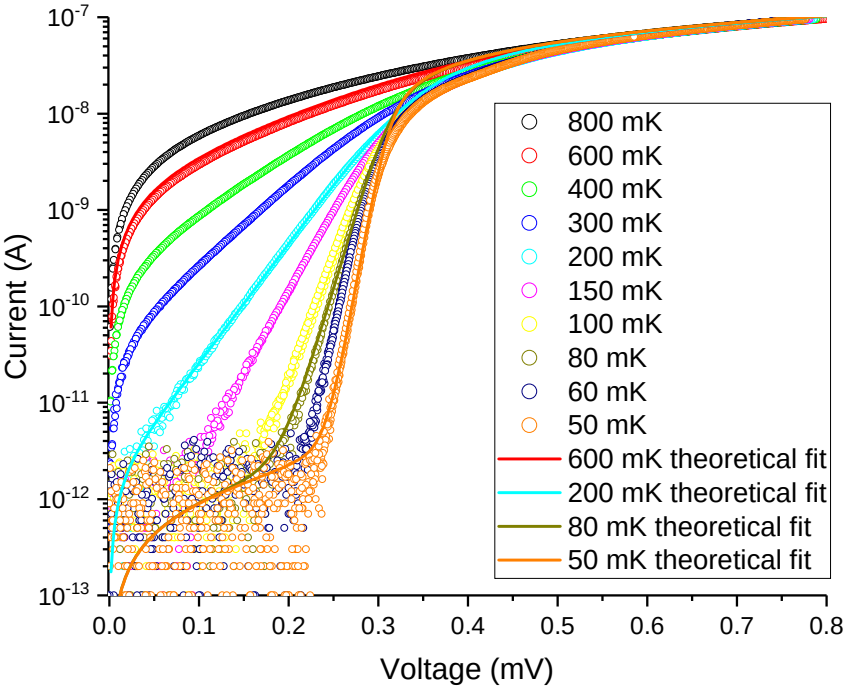


Figure 37. Current-voltage curves at different temperatures in log-linear scale, SINIS junction. Theoretical curves are calculated with the simple BCS theory of equation (4).

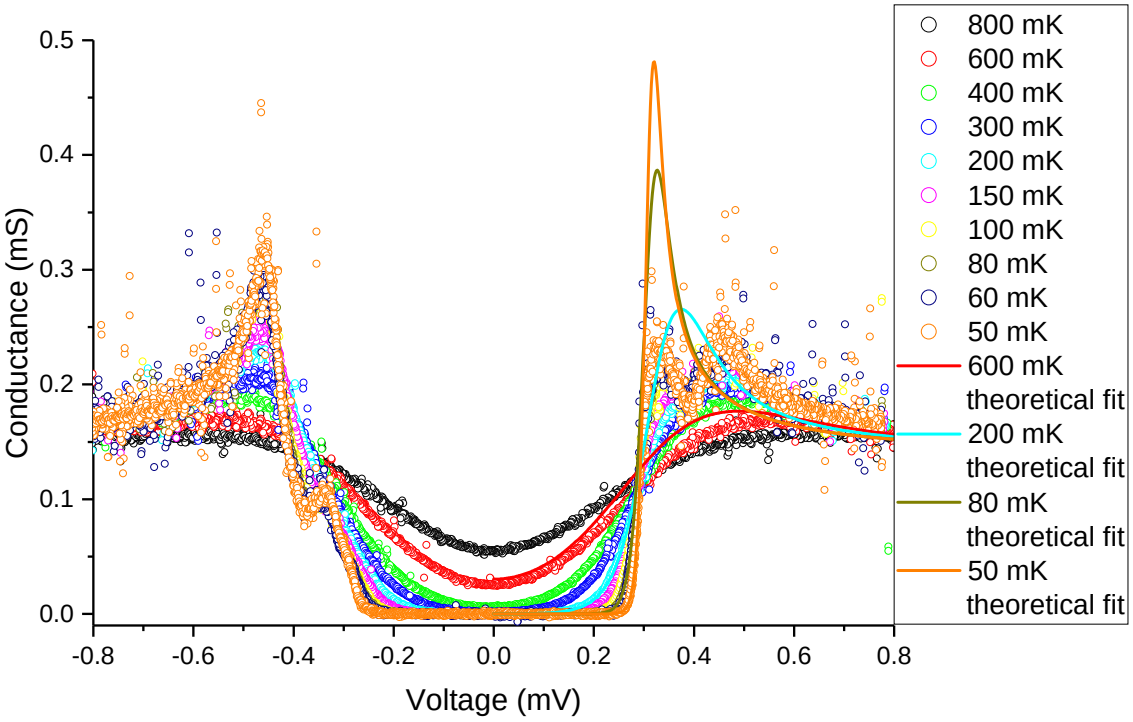


Figure 38. Conductance at different temperatures, SINIS junction. Theoretical curves are calculated with the simple BCS theory of equation (4). Only the right side was fitted due to asymmetry.

effect which shows in log-linear scale. That is unfortunate because due to this, the leakage current can not be determined directly from the data. By leakage current we mean the current that flows even inside gap area. Nevertheless, some simple theoretical fits were made to the data according to equation (4). Tunneling resistance was taken from fitting in Figure 36, and value $R_T = 7.124$ kΩ was used. The SINIS junction was assumed to be symmetrical. The critical temperature was not measured separately so a literature value was used, $T_c = 1.2$ K, and the temperature of both the superconductor and the normal metal was approximated to be close to bath temperature, $T_{bath} = T_N = T_S$. The gap size was estimated from the conductance graph (Figure 38) and varied slightly to find values which produced the best fit. Gap size of only 155 µV and 165 µV was used, the lower value for the two lower temperatures and the higher value for the two higher temperatures. Typically a value around 200 µV is observed for thin film Al [4, 16]. The Dynes parameter in the superconductor density of states, equation (6), which determines the leakage current, was chosen to match the order of magnitude in data. $\Gamma/\Delta(0) = 6 \cdot 10^{-5}$ was used. As it can be seen from Figure 37, the theoretical fits follow the data quite nicely at sub-gap voltages and also at high voltages. However, at gap-edge voltages the fitting gets higher values than actual data for lower temperatures. This, however, is a common effect in all SINIS junctions, even on Si substrates.

The differential conductance (dI/dV) as a function of voltage is presented in Fig-

ure 38, determined by numerical differentiation. Unexpectedly, the conductance has asymmetrical double peaks around the gap. In addition to peak heights, also slopes are asymmetric on different sides of the gap. The extra smaller peaks disappear by increasing the temperature. Theoretical fits are also presented along with the data. It can be seen here even more clearly how the fits deviate from the measurement data at gap edges. The fits present the ideal situation where there are only single peaks symmetrically at gap edges. The low value for gap size which was used in fitting is most likely connected to the double-peak behavior.

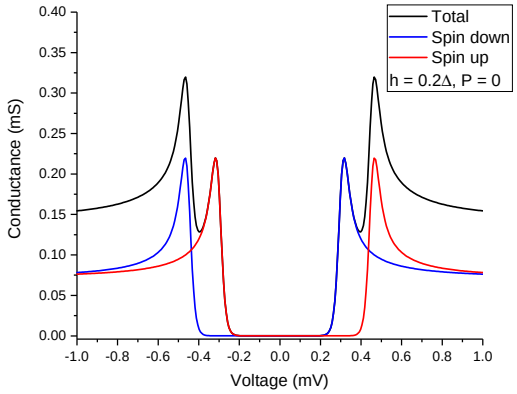
The gap size can be usually measured accurately directly from the conductance graph (Figure 38) but in this case, it was simply used as a fitting parameter when making theoretical curves. The double peaks also make it unclear which peak should be used for fitting. When measured from the two peaks furthest from each other, the resulting gap size would be around 225 µV, and when measured from peaks that are closest together result would be 160 µV. The later would be closest to values used in current-voltage fitting. However, when the distance is measured between an inner and an outer peak, the resulting gap size is for both pairs around 192 µV, which is more reasonable value for aluminum.

Despite the asymmetry of the current-voltage curves and the double peaks in conductance-voltage graph, the data clearly suggest a SINIS junction. Both current and conductance go to zero inside the gap, and the temperature dependency of the effect is present. Interestingly, even the two lowest temperatures, 50 mK and 60 mK, can be differentiated from each other. Quite often this is not the case due to environmental overheating effects. When put to use, the junction would be calibrated with a well known thermometer which can be used to eliminate the non-ideal effects. As a conclusion, this type of junction should still be suitable to be used as a thermometer.

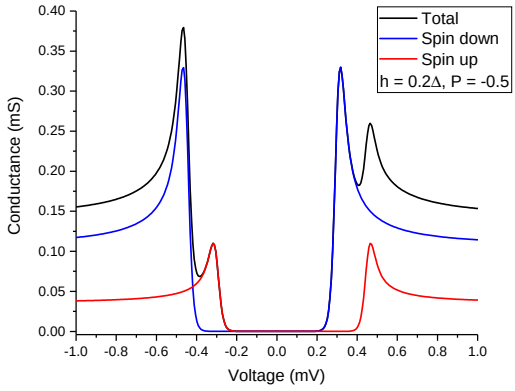
4.4 Analysis of SINIS junction measurement with spin-splitting and -polarization

It has been pointed out [44] that asymmetric SINIS junctions with unequal tunneling resistances can cause an extra hump to conductance curves. However, the effect should not be dependent on voltage polarization which means that the behavior should be symmetric in the data. That is not the case in Figure 38, in which there are asymmetric double peaks. In addition, a hump caused by junction asymmetry should not be as strong as the one in this data. Most likely, the asymmetric effect present in data in section 4.3 is not caused by asymmetricity of the junction. Asymmetric double peaks similar to this study have been encountered previously in our group [43], although the origin of this effect was not clear. Some non-equilibrium effects were suggested.

The peaks in Figure 38 look almost as if the junction behavior has been doubled unevenly and if this doubling is shifted. The doubling of the peaks could be caused



(a) Spin splitting without polarization ($P = 0$).



(b) Spin splitting and polarization ($P = -0.5$).

Figure 39. Simulated conductance behavior of SINIS junction with spin splitting effects. Used parameters are $T_N = T_S = 75$ mK, $T_c = 1.2$ K, $\Delta(0) = 188$ µV $\Gamma/\Delta(0) = 10^{-4}$, $h/\Delta(0) = 0.2$, $R_T = 14$ kΩ.

by some sort of splitting effect. For example, magnetic field can cause spin splitting due to Zeeman effect. This causes energy levels to split to different energies for spin up and spin down particles. This causes the peaks to double and the effective gap to get smaller. [45] The spin up energies at $-\Delta$ are shifted up by an amount h and the spin down energies at Δ are shifted down by h, which results in decreased effective gap size. The density of states presented in equation (6) can be modified to include the splitting resulting in:

$$n_{S,\uparrow\downarrow}(E, h, T_S) = \frac{1}{2}\left|\mathrm{Re}\left\{\frac{E \pm h + i\Gamma}{\sqrt{(E \pm h + i\Gamma)^2 - \Delta(h, T_S)^2}}\right\}\right| , \tag{7}$$

where $\uparrow\downarrow$ represent the spin and $h = \mu_B B$ is the shift caused to the energy levels. μ_B is Bohr magneton and B is the magnetic field. The function for Δ is also modified by h, but it can be noted that the effect is really small especially at low temperatures and with small values for h. However, this simple adjustment to the density of states causes double peaks and decrease in gap size, but not asymmetry. An equal amount of both spins travel through a junction, which results in peaks for both spins having equal height. [46] Plots of equation (7) are presented in Figure 39a, where it can be seen that the behavior is symmetric.

Asymmetry of the data could be due to some sort of polarization, which favors one spin species over the other. Polarization can be expressed with:

$$P = \frac{n_\uparrow - n_\downarrow}{n_\uparrow + n_\downarrow} , \tag{8}$$

where $n_\uparrow$ and $n_\downarrow$ represent the amount of spin up and spin down particles respectively. Spin polarization could be achieved for example by using ferromagnetic material as

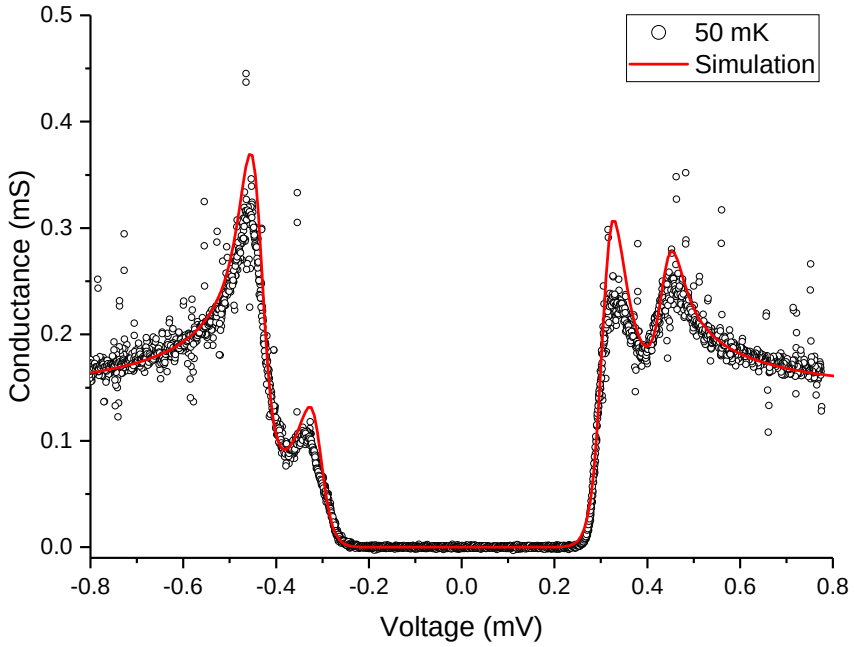


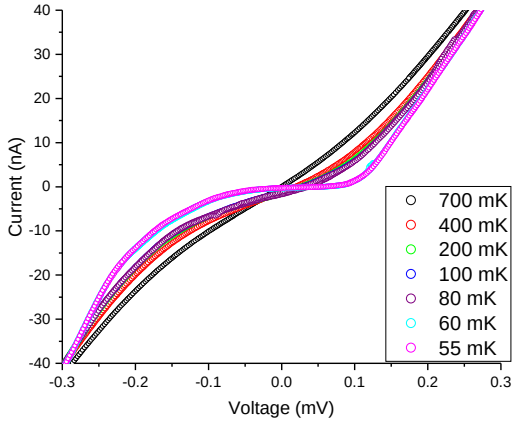
Figure 40. Conductance at 50 mK, first measurement, with spin splitting and polarization simulation. Used parameters are $T_N = T_S = 75$ mK, $T_c = 1.2$ K, $\Delta(0) = 188$ µV, $\Gamma/\Delta(0) = 10^{-4}$, $h/\Delta(0) = 0.17$, $P = -0.4$, $R_T = 14$ kΩ.

a spin filter. By taking into account both the spin splitting and the polarization, SINIS junction current from equation (4) can be modified to:

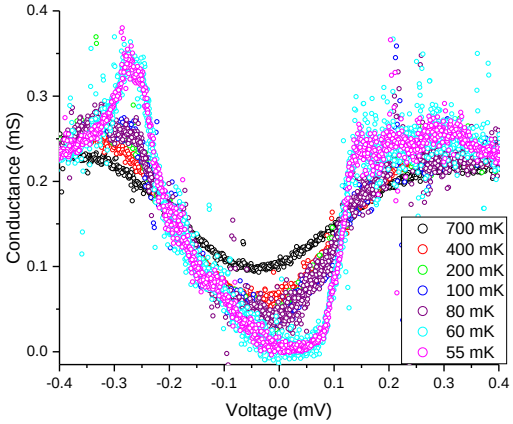
$$I(V) = \frac{1}{eR_T}\int_{-\infty}^{\infty} [[1+P]\, n_{S,\uparrow}(E,h,T_S) + [1-P]\, n_{S,\downarrow}(E,h,T_S)] \times [f_N(E-eV/2,T_N) - f_N(E+eV/2,T_N)]\, dE \ , \tag{9}$$

where V is again the voltage across the whole SINIS junction. [46]

By adding the polarization to the simulations, they show an asymmetric behavior, as presented in Figure 39b. The shape is really close to the data in Figure 38, which could suggest that this might be a possible explanation for the data. A best fit is presented in Figure 40 which follows the data surprisingly well, even though a higher temperature and tunneling resistance had to be used than in the simple model fitting. Nevertheless, it should be noted that even as small spin splitting as $h/\Delta(0) = 0.2$ for aluminum requires a magnetic field that is in the order of one Tesla. Such high magnetic fields are not present inside the cryostat. However, the required magnetic field could also come from an effective exchange field due to ferromagnetism. [45]



(a) Current-voltage curves at different temperatures.



(b) Conductance at different temperatures.

Figure 41. Second junction characterization measurements with excess noise coming from grounding. No off-set adjustment has been made.

4.5 Characterization of single NIS junction

A second measurement was carried out similar to one in section 4.3. Again, only one junction was measured but this time with a three-point connection on the chip. The contact to the other junction on the chip was lost before measurements could begin. First results are presented in Figure 41. As it can be seen, the data was really noisy and so no accurate off-set correction was possible. There is a clear asymmetry in current-voltage behavior. However, no double peaks can be seen from conductance graph in Figure 41b. Also the slopes are much less steep compared to the previous sample, in Figure 38. Because of this, it is hard to say if the behavior is similar to the previous experiment or not. It can also be suspected that the noise is also heating the sample, because the temperature behavior of the junction is very unclear. There seems to be at least some temperature dependence but many of measured lines overlap with each other. For example two lowest bath temperatures, 55 mK and 60 mK can not be differentiated from each other, but in addition temperatures $80 - 200$ mK overlap completely, and even 400 mK is really close to them. Based on this data, the junction in this setup would be not very suitable to be used as an accurate thermometer.

The source of this excess noise was investigated, and it was found out that it was coming from power line grounding of the current preamplifier. When removing the cable and using only the battery mode, the resulting data did not display such level of noise and heating anymore. This reduction was also achieved by adding an isolation transformer between the power socket and the preamplifier, instead of just a straight cable. The transformer was used, and the measurements were repeated with this set-up. 1:5000 divider was always used. The results are presented in Figures 42-44. The voltage and current off-set was now corrected as previously.

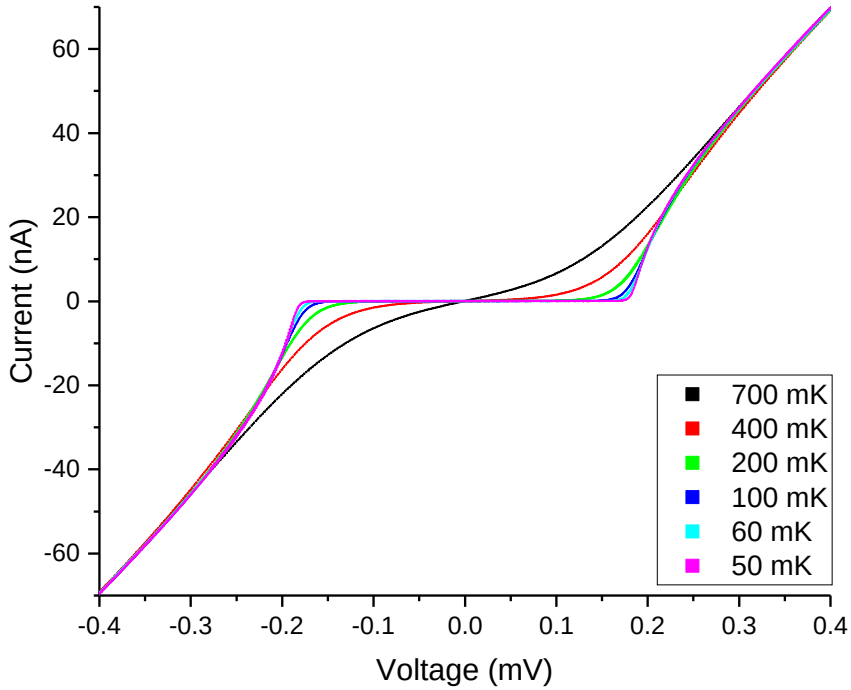


Figure 42. Current-voltage curves at different temperatures in linear scale, NIS junction.

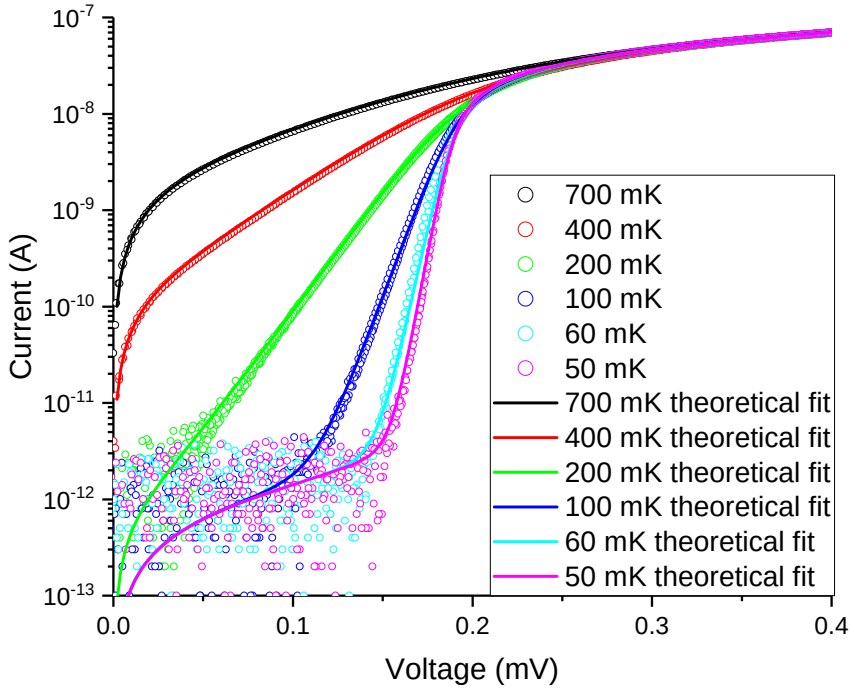


Figure 43. Current-voltage curves at different temperatures in log-linear scale, NIS junction. Theoretical curves are calculated with the simple BCS theory of equation (4).

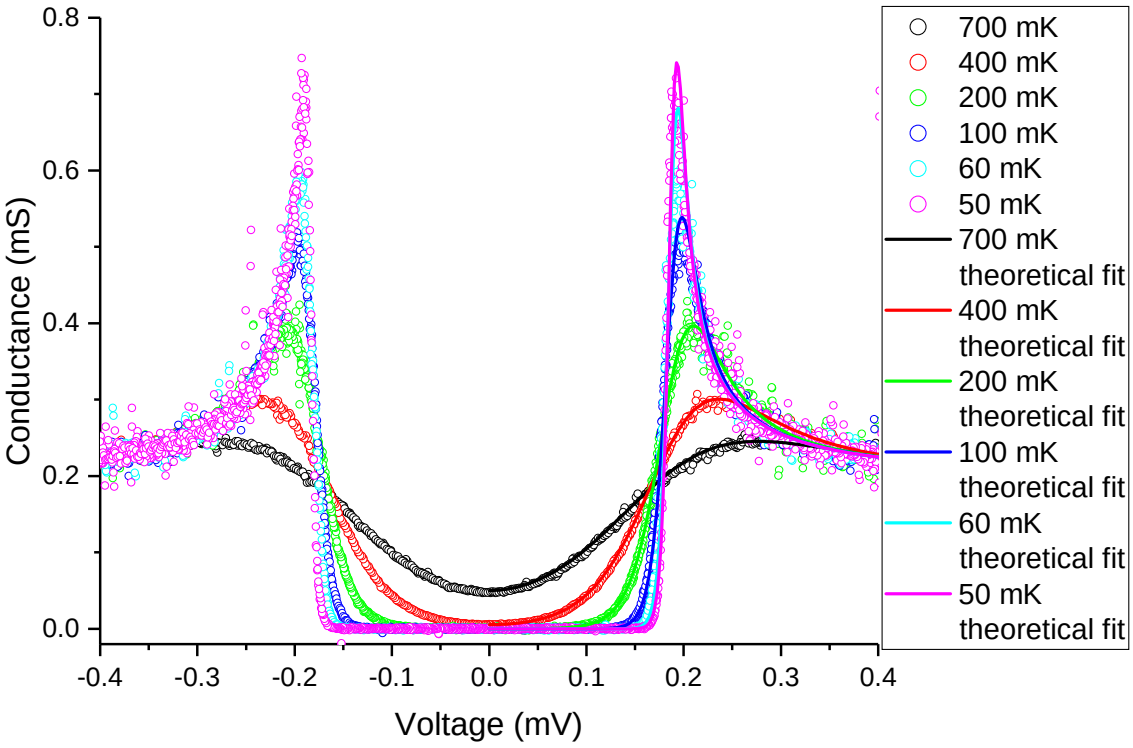


Figure 44. Conductance at different temperatures, NIS junction. Theoretical curves are calculated with the simple BCS theory of equation (4).

The current-voltage characteristics in linear scale are presented in Figure 42. Temperature dependence is clearly present also in this data. All measured temperatures can be easily differentiated from each other. At low temperatures, the changes at gap edges are very sharp. The noisiness and asymmetricity has completely disappeared when compared to Figure 41a. In comparison to the first measurement, Figure 34, the behavior looks much more symmetric on both sides. However, the voltage range also seems different.

The current-voltage characteristics along with theoretical curves in log-linear scale are presented in Figure 43. In this scale it is even easier to see the temperature dependence. Even the two lowest temperatures can be differentiated from each other, like previously. However, the noisiness at low currents is also repeated similar to Figure 37. Because of this, the Dynes parameter can not be determined exactly even for this sample. Nevertheless, it should not be an issue when using junction as a thermometer, as the biasing current is always chosen well above noisy level, in the 10 pA range in this case.

The conductance (dI/dV) along with theoretical curves is presented in Figure 44. From this it can be concluded that the asymmetric double peaks in previous measurement (in Figure 38) are not repeated in this sample. Instead, the conductance data looks really neat with strikingly steep edges at low temperatures. However, when the gap size is measured from this data, it can be seen that it is actually only

one junction, NIS instead of SINIS. In full SINIS junction the distance between peaks corresponds to $4 \times \Delta/e$, but in this case it would result in gap size that is smaller than 100 µV which is not very realistic. If treated as a single junction (NIS) the measured gap size is 188 µV. This is close to value that was obtained also from previous measurements when determined from the asymmetric peaks.

The theoretical curves in Figures 43 and 44 were generated in a similar way as previously in section 4.3. This time the junction was treated as asymmetric. In the symmetric case, tunneling resistance is attributed 1:1 to both junction sides, but with the asymmetric junction, only one side is taken into account. No measurements were done with a smaller divider so the tunneling resistance could not be determined from a linear fit. The tunneling resistance was instead used as a fitting parameter. $R_T = 5.040$ kΩ produced the best result. A critical temperature of $T_c = 1.2$ K was used, and again $T_{bath} = T_N = T_S$ was assumed. The gap size measured from Figure 44, 188 µV, was used. For Dynes parameter, the same value as before seemed to produce best result, so $\Gamma/\Delta(0) = 6 \cdot 10^{-5}$ was used.

As it can be seen from Figures 43 and 44, the theoretical curves follow the data quite nicely. Compared to the first measurement (Figures 37 and 38) the simple fits follow the data even close to gap edges. It can be concluded that the data is in excellent agreement with the theory.

5 Conclusions

As a conclusion from sample fabrication, SU-8 was a suitable material for the template structure, as the phononic crystal was found to form mostly inside the patterned pit areas. Especially with the smaller sphere size, diameter of 140 nm, there was almost no crystal formation on top of SU-8. This made clean sample surface possible and also made wiring deposition easier. Crystals also were found to be in good contact with the pattern edges like in previous experiments. This is probably due to the similarity of the materials, polystyrene and SU-8. This allowed wiring to be deposited from SU-8 to the crystal surface, as there was almost no cracks that would be in the way. SU-8 could also clearly withstand all following processing steps with ease, after early problems caused by bad adhesion were solved. However, as a downside, SU-8 proved to be a difficult material for wire bonding, as the metal on top of it could easily be ripped apart. Nevertheless, bonding was still possible, although contact was easily lost. If similar samples are attempted in the future, it could be beneficial to make experiments with indium bonding in hopes that it would be a more stable method.

The colloidal crystallization provided much better results with the smaller sphere size compared to the bigger one. This was most likely caused by contamination in the first suspension. The bigger sphere size was much more prone to cracking, including cracks at crystal edges. The smaller sphere size produced less cracks and, in addition, cracks were thinner. The highest concentration, 10 %, produced thickest crystals so it was used for the smaller sphere size. Judging from profilometer measurements, even the thickest crystals were not as thick as SU-8 resist layer, which means that there was most likely a small step between crystal and SU-8 surface.

Based on solubility tests, PS crystals were too easily destroyed. All chosen chemicals which were or could have been required for further processing, caused serious damage to the crystals. Electron beam irradiation was necessary to introduce additional cross-linking to PS. The exposure dose chosen from dose tests was suitable, as further confirmed with the finished samples, where crystal had retained its shape even after lithography and deposition of SINIS junctions. In addition, all of the hardened crystals stayed in template positions as they should. There were no problems of crystals detaching, as with plain substrates.

Continuous wires were repeatedly fabricated directly on top of the crystals which is an improvement to previous attempts. Previously, some sort of coating had been required. This was most likely made possible by the usage of smaller sphere size compared to before. The crystals had fewer and thinner cracks, in addition to smaller

sphere size, which should result in smaller surface roughness. However, the wires, both straight test wires and actual junctions, were quite large compared to nanoscale. Even the thinnest were 1 µm wide. Wide wires probably enabled the successful junction deposition in addition to further adjustments of the pattern. Thinner wires could be possible, but fabrication might be more unreliable.

The possibilities for control sample fabrication were investigated. A sample with continuous PS film was found to be the most straightforward option, and it could be fabricated simply by spin coating a silicon chip with polystyrene-toluene solution. However, it required that larger area is hardened with electron beam irradiation, because there is no SU-8 template. Otherwise, control sample fabrication should follow the usual recipe and junction deposition should be easier compared to the PnC sample.

Fabricated junctions were characterized with low-temperature measurements. Room temperature resistances were also measured, but those only give a hint if junctions are working or not. Especially with such a rough surface, a high resistance could come from noncontinuous wiring. Nevertheless, the measured junctions showed tunneling characteristics, which confirms that fabricated junctions had a SINIS structure. The shape of the current-voltage curves was clearly temperature dependent and even 50 mK and 60 mK could be differentiated from each other. The simulated curves based on theory followed data really nicely, and so the junctions should be suitable to be used as a thermometer with an appropriate calibration.

Despite the clear temperature dependence, there was some non-ideal behavior present in the first measurements. The conductance graph showed that there were double peaks around the gap area. Usually, the gap should have only one peak on each side. Double peaks can be caused by splitting of states such as spin or electron/hole asymmetry. In addition, such peaks should be symmetric in amplitude and position if no polarization effects are present. This behavior is not yet understood but it should not be in the way of using such junctions as a thermometer.

As a conclusion, tunnel junctions that were fabricated on top of 3D PnCs were found to have good temperature resolution even at temperatures close to 50 mK. Despite some unexplained behavior in one of the measurements, they should be usable after calibration with a well known thermometer. Unfortunately, the crystal thermal characteristics were not able to be measured yet due to unstable bonding and unexpected cooling problems. However, these advancements in sample fabrication and initial measurements will hopefully pave the way for future thermal conductance measurements.

References

[1] Junhu Zhang, Zhiqiang Sun, and Bai Yang. Self-assembly of photonic crystals from polymer colloids. *Current Opinion in Colloid & Interface Science*, 14(2):103--114, 2009.

[2] Wei Cheng, Jianjun Wang, Ulrich Jonas, George Fytas, and Nikolaos Stefanou. Observation and tuning of hypersonic bandgaps in colloidal crystals. *Nature Materials*, 5(10):830--836, 2006.

[3] Suxia Yang, J. H. Page, Zhengyou Liu, M. L. Cowan, C. T. Chan, and Ping Sheng. Focusing of sound in a 3D phononic crystal. *Physical Review Letters*, 93(2), 2004.

[4] Nobuyuki Zen, Tuomas A. Puurtinen, Tero J. Isotalo, Saumyadip Chaudhuri, and Ilari J. Maasilta. Engineering thermal conductance using a two-dimensional phononic crystal. *Nature Communications*, 5(1), 2014.

[5] T. A. Puurtinen and I. J. Maasilta. Low temperature heat capacity of phononic crystal membranes. *AIP Advances*, 6(12):121902, 2016.

[6] Yan Pennec, Jérôme O. Vasseur, Bahram Djafari-Rouhani, Leonard Dobrzyński, and Pierre A. Deymier. Two-dimensional phononic crystals: Examples and applications. *Surface Science Reports*, 65(8):229--291, 2010.

[7] Tero J. Isotalo, Yao-Lan Tian, Mikko P. Konttinen, and Ilari J. Maasilta. Statistical characterization of self-assembled colloidal crystals by single-step vertical deposition. *Colloids and Surfaces A: Physicochemical and Engineering Aspects*, 443:164--170, 2014.

[8] Yaolan Tian, Tero J Isotalo, Mikko P Konttinen, Jiawei Li, Samuli Heiskanen, Zhuoran Geng, and Ilari J Maasilta. Integrating metallic wiring with three-dimensional polystyrene colloidal crystals using electron-beam lithography and three-dimensional laser lithography. *Journal of Physics D: Applied Physics*, 50(5):055302, 2017.

[9] Frank Pobell. *Matter and Methods at Low Temperatures*. Springer: Berlin Heidelberg, 2007.

[10] Martin Maldovan. Phonon wave interference and thermal bandgap materials. *Nature Materials*, 14(7):667--674, 2015.

[11] Abdelkrim Khelif and Ali Adibi, editors. *Phononic Crystals*. Springer: New York, 2016.

[12] Martin Maldovan. Sound and heat revolutions in phononics. *Nature*, 503(7475):209--217, 2013.

[13] Martin Maldovan. Narrow low-frequency spectrum and heat management by thermocrystals. *Physical Review Letters*, 110(2), 2013.

[14] O. Weis. Thermal phonon radiation. *Zeitschrift für angewandte Physik*, 26:325--334, 1969.

[15] I. J. Maasilta, T. A. Puurtinen, Y. Tian, and Z. Geng. Phononic thermal conduction engineering for bolometers: From phononic crystals to radial casimir limit. *Journal of Low Temperature Physics*, 184(1-2):211--216, 2015.

[16] Yaolan Tian. *Studies of Two-Dimensional and Three-Dimensional Phononic Crystal Structures*. PhD thesis, University of Jyväskylä, Nanoscience Center, Department of Physics, Jyväskylä, 2016.

[17] Yaolan Tian, Tuomas A. Puurtinen, Zhuoran Geng, and Ilari J. Maasilta. Minimizing coherent thermal conductance by controlling the periodicity of two-dimensional phononic crystals. submitted, 2018.

[18] Roman Anufriev, Jeremie Maire, and Masahiro Nomura. Reduction of thermal conductivity by surface scattering of phonons in periodic silicon nanostructures. *Physical Review B*, 93(4), 2016.

[19] Jeremie Maire, Roman Anufriev, Ryoto Yanagisawa, Aymeric Ramiere, Sebastian Volz, and Masahiro Nomura. Heat conduction tuning by wave nature of phonons. *Science Advances*, 3(8):e1700027, 2017.

[20] Jaeho Lee, Woochul Lee, Geoff Wehmeyer, Scott Dhuey, Deirdre L. Olynick, Stefano Cabrini, Chris Dames, Jeffrey J. Urban, and Peidong Yang. Investigation of phonon coherence and backscattering using silicon nanomeshes. *Nature Communications*, 8:14054, 2017.

[21] T J Isotalo, Y L Tian, and I J Maasilta. Fabrication and modelling of three-dimensional sub-kelvin phononic crystals. *Journal of Physics: Conference Series*, 400(5):052007, 2012.

[22] Mykhailo Savytskyi. Fabrication of 3-D phononic crystals for thermal transport management. Master's thesis, University of Jyväskylä, Nanoscience Center, Department of Physics, Jyväskylä, 2016.

[23] M. Tinkham. *Introduction to Superconductivity*. Dover Books on Physics Series. Dover Publications, 2004.

[24] Ivar Giaever and Karl Megerle. Study of superconductors by electron tunneling. *Physical Review*, 122(4):1101--1111, 1961.

[25] R. C. Dynes, J. P. Garno, G. B. Hertel, and T. P. Orlando. Tunneling study of superconductivity near the metal-insulator transition. *Physical Review Letters*, 53(25):2437--2440, 1984.

[26] Y. Xia, B. Gates, Y. Yin, and Y. Lu. Monodispersed colloidal spheres: Old materials with new applications. *Advanced Materials*, 12(10):693--713, 2000.

[27] Maria Stepanova and Steven Dew, editors. *Nanofabrication*. Springer: Vienna, 2012.

[28] N. D. Denkov, O. D. Velev, P. A. Kralchevsky, I. B. Ivanov, H. Yoshimura, and K. Nagayama. Two-dimensional crystallization. *Nature*, 361(6407):26--26, 1993.

[29] Kuniaki Nagayama. Two-dimensional self-assembly of colloids in thin liquid films. *Colloids and Surfaces A: Physicochemical and Engineering Aspects*, 109:363--374, 1996.

[30] Charles-André Fustin, Gunnar Glasser, Hans W. Spiess, and Ulrich Jonas. Parameters influencing the templated growth of colloidal crystals on chemically patterned surfaces. *Langmuir*, 20(21):9114--9123, 2004.

[31] P. Jiang, J. F. Bertone, K. S. Hwang, and V. L. Colvin. Single-crystal colloidal multilayers of controlled thickness. *Chemistry of Materials*, 11(8):2132--2140, 1999.

[32] Zhong-Ze Gu, Akira Fujishima, and Osamu Sato. Fabrication of high-quality opal films with controllable thickness. *Chemistry of Materials*, 14(2):760--765, 2002.

[33] Robert G. Shimmin, Alexander J. DiMauro, and Paul V. Braun. Slow vertical deposition of colloidal crystals: a langmuir-blodgett process? *Langmuir*, 22(15):6507--6513, 2006.

[34] L.K. Teh, N.K. Tan, C.C. Wong, and S. Li. Growth imperfections in three-dimensional colloidal self-assembly. *Applied Physics A*, 81(7):1399--1404, 2005.

[35] Sang Hyuk Im, Mun Ho Kim, and O Ok Park. Thickness control of colloidal crystals with a substrate dipped at a tilted angle into a colloidal suspension. *Chemistry of Materials*, 15(9):1797--1802, 2003.

[36] P Ferrand, M J Minty, M Egen, J Ahopelto, R Zentel, S G Romanov, and C M Sotomayor Torres. Micromoulding of three-dimensional photonic crystals on silicon substrates. *Nanotechnology*, 14(2):323--326, 2003.

[37] M. A. McLachlan, N. P. Johnson, R. M. De La Rue, and D. W. McComb. Domain size and thickness control of thin film photonic crystals. *Journal of Materials Chemistry*, 15(3):369, 2005.

[38] R.L Clough. High-energy radiation and polymers: A review of commercial processes and emerging applications. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 185(1-4):8--33, 2001.

[39] MicroChem, Newton, Massachusetts. *SU-8 2000 Permanent Epoxy Negative Photoresist, PROCESSING GUIDELINES FOR: SU-8 2000.5, SU-8 2002, SU-8 2005, SU-8 2007, SU-8 2010 and SU-8 2015*, 2018.

[40] E. F. Reznikova, J. Mohr, and H. Hein. Deep photo-lithography characterization of SU-8 resist layers. *Microsystem Technologies*, 11(4-5):282--291, 2005.

[41] David B. Hall, Patrick Underhill, and John M. Torkelson. Spin coating of thin and ultrathin polymer films. *Polymer Engineering & Science*, 38(12):2039--2045, 1998.

[42] María Teresa García, Ignacio Gracia, Gema Duque, Antonio de Lucas, and Juan Francisco Rodríguez. Study of the solubility and stability of polystyrene wastes in a dissolution recycling process. *Waste Management*, 29(6):1814--1818, 2009.

[43] Andrii Torgovkin. High-frequency filtering for low-temperature thermal transport studies in nanostructures. Master's thesis, University of Jyväskylä, Nanoscience Center, Department of Physics, Jyväskylä, 2012.

[44] S. Chaudhuri and I. J. Maasilta. Cooling, conductance, and thermometric performance of nonideal normal metal-superconductor tunnel junction pairs. *Physical Review B*, 85(1), 2012.

[45] F. Sebastian Bergeret, Mikhail Silaev, Pauli Virtanen, and Tero T. Heikkilä. Colloquium : Nonequilibrium effects in superconductors with a spin-splitting field. *Reviews of Modern Physics*, 90(4), 2018.

[46] F. Giazotto, P. Solinas, A. Braggio, and F. S. Bergeret. Ferromagnetic-insulator-based superconducting junctions as sensitive electron thermometers. *Physical Review Applied*, 4(4), 2015.

A Appendix

A.1 Typical code for Nanoscribe

```
%Initial parameters%

PiezoScanMode
ContinuousMode
ConnectPointsOn

TimeStampOn
PerfectShapeOff
InvertZAxis 1

TiltCorrectionOn

LaserPower 20
Powerscaling 1
SettlingTime 200
UpdateRate 100
PointDistance 150

%SINIS junction%

XOffset 150
YOffset 150
ZOffset 0

LaserPower 70

include sinis.gwl
Write

%Wires closest to the junction%

LaserPower 80
AddZOffset 1

include lines.gwl
```

```
Write

%Rest of the wires and bonding pads%

LaserPower 100
XOffset 0
YOffset 0

MoveStageX 155
MoveStageY 45

Include wires_and_pads.gwl
Write
```