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Title: Single Event Transients and Pulse Quenching Effects in Bandgap Reference Topologies for Space Applications

Year: 2016

Version:

Single Event Transients and Pulse Quenching Effects in Bandgap Reference Topologies For Space Applications

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Abstract—An architectural performance comparison of bandgap voltage reference variants, designed in a 0.18 μm CMOS process, is performed with respect to single event transients. These are commonly induced in microelectronics in the space radiation environment. Heavy ion tests (Silicon, Krypton, Xenon) are used to explore the analog single-event transients and have revealed pulse quenching mechanisms in analogue circuits. The different topologies are compared, in terms of cross-section, pulse duration and pulse amplitude. The measured results, and the explanations behind the findings, reveal important guidelines for designing analog integrated circuits, which are intended for space applications. The paper includes an analysis on how pulse quenching occurs within the indispensable current mirror, which is used in every analog circuit.

Index Terms—Analog single-event transient (ASET), bandgap voltage reference (BGR), charge sharing, CMOS analog integrated circuits, heavy ion, ionization, pulse quenching, parasitic bipolar effect, radiation effects, radiation hardening by design (RHBD), reference circuits, single-event effects (SEE), single-event transient (SET), space electronics, voltage reference.

I. INTRODUCTION

ANALOG single-event transients (ASETs), which belong to the broader category of Single Event Effects (SEEs), are evanescent fluctuations of electrical charges in integrated circuits (ICs). They may be observed when high-energy particles (alpha, protons and heavy ions), such as those found in the space environment (trapped particles in the Van Allen belts, solar energetic particles and galactic cosmic rays) [1], collide with analog ICs. When a high-energy particle penetrates the silicon substrate it ionizes the target material along its path. The ionization can occur through coulombic interaction, i.e. through Linear Energy Transfer (LET) or via nuclear reactions e.g. a commonly occurring Boron-10 dopant isotope is struck by a low-energy (thermal) neutron to give a lithium ion and alpha particle. The ionized region is proximal to the ion path, generating a multitude of electron-hole pairs [2]–[6] in the vicinity around the ion track. Built in electric fields or fields created by normal biasing conditions separate the pairs, leaving excess charge after the event. The excess charge injected at a sensitive circuit node can potentially disrupt the reliable functionality of of the circuit, causing instantaneous or permanent failures.

The energy deposited by the impinging ion per unit mass can be expressed by LET. For a unit length of a material it can be expressed in terms of MeV$\times$cm^2/mg and characterizes the average energy that a charged ion loses as it traverses a unit length of the material (the amount of energy that the ionising particle transfers to the material per unit length per density) [7]–[10]. Observable transients are most likely to occur when the impinging particles are ions with higher LET and hence displace more charge. The effect of the ASETs induced on the desired signals, depend on the sensitivity of the particular analog circuit to the injected charge. The sensitivity is dependent on the circuit architecture, the devices' operating speed and the nominal operating voltage. Furthermore, as the technology nodes scale down, the decreased transistor geometries and thinner gate oxides, reduce the charge required to disrupt normal functionality, thus making the circuits more prone to ASETs. Thus in deep sub-micron technologies [11]–[13] ASETs are of major concern and impose critical issues for the microelectronics reliability, while much ongoing research deals with characterizing the optimum circuit topologies, technology processes, devices and design approaches in order to mitigate ASETs in space applications [14]–[40].

When designing microelectronics for space applications, the constituent circuits and systems have to meet the required specifications of the particular mission, with respect to signal

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quality and microelectronics survivability. One of the most essential building blocks in IC design is the voltage reference, which is required for a variety of analogue, mixed-signal and digital circuits [41]–[49] such as flash memories, temperature sensors, amplifiers, DACs, etc. The performance of the voltage reference has a significant impact on the performance of all the subsequent circuits, which depend on the accurate and stable reference voltage/current [50]–[52]. Considering that reference circuits have to be widely used and integrated in modern, deep sub-micron and low-power technologies, the investigation of space radiation induced ASETs, due to heavy ions, are of major importance when designing reference circuits for space electronics [53], [54].

In this work, three bandgap-based reference (BGR) circuit variants have been explored with respect to heavy-ion induced ASETs. The scope of this paper is to reveal important design strategies at the architectural level of these analog circuits, so as to mitigate ASETs. The circuit variants differ with respect to the topology, the use of cascode stages, the supply voltage and the oxide thickness of the utilized transistors. All topologies were implemented using regular radiation-hardening-by-design (RHBD) layout techniques, such as extended use of guard rings, substrate contacts, increased transistor sizes for hardening against ASETs, whilst edgeless NMOS devices were employed for hardening against total ionization dose (TID) [9], [55], [56]. The integrated circuits were exposed to heavy ions (Si, Kr and Xe) and the resulting ASETs were recorded at the output of each topology independently by using a high-speed oscilloscope. An interesting result was the observation, of pulse quenching phenomena in fabricated analog circuits. We propose useful guidelines for the mitigation of ASET's and enhancement of pulse quenching, that can be used as a mechanism for countering the effects at high LETs. These guidelines are applicable to all analogue and mixed-signal circuits.

II. CIRCUITS UNDER TEST

ASETs usually originate from particle strikes which traverse reverse-biased pn-junctions or areas with strong electric fields. This is particularly a problem at the transistor's drain terminal, especially with the newer submicron technologies, where the generated plasma of e-h pairs drifts apart because of the high electric fields across the depletion region. The strike-induced extra charge then alters the voltage level of the drain node, as well as subsequent nodes, sometimes even leading to a malfunction of the IC.

In order to extract the best design strategies for ASET mitigation at the circuit level, the BGR ICs of Fig. 1 and Fig. 2 [57]–[59] were designed and fabricated using TowerJazz Semiconductor's 0.18 μm CMOS technology. The circuit in Fig. 1 is based on simple current mirrors (SCM) and was designed in two variations, one with 1. 8V transistors for the corresponding supply voltage of 1.8V and a second one with 3.3 V transistors and its corresponding supply voltage of 3.3 V. The circuit of Fig. 2 is a further variant of the topology of Fig. 1, designed with cascode current mirrors (CCM) and utilizing 3.3 V transistors, targeting a 3.3 V power source. The present

analysis does not take into account radiation effects on the diodes, since these are identical in all circuit implementations that are compared. Standard matching and RHBD techniques such as guard rings and well-substrate contacts are used in all circuits at the layout level so as to improve the immunity to device latchup, radiation induced leakage and ASETs.
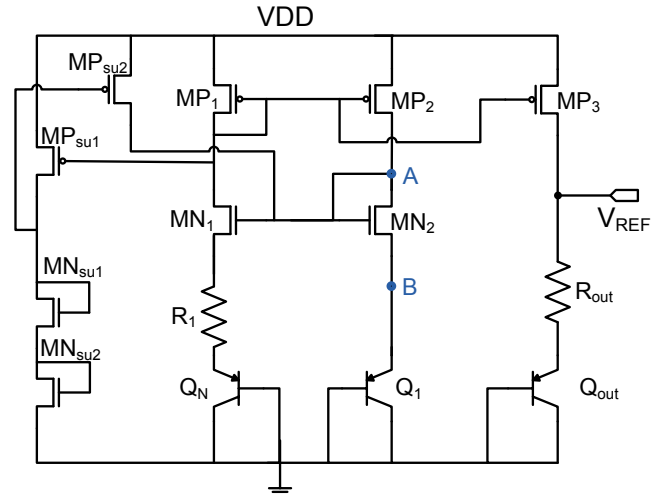

Fig. 1. Bandgap voltage reference reference circuit with Simple Current Mirrors (SCM) in two variants: one utilizing 1.8 V transistors and the other utilizing 3.3 V transistors.
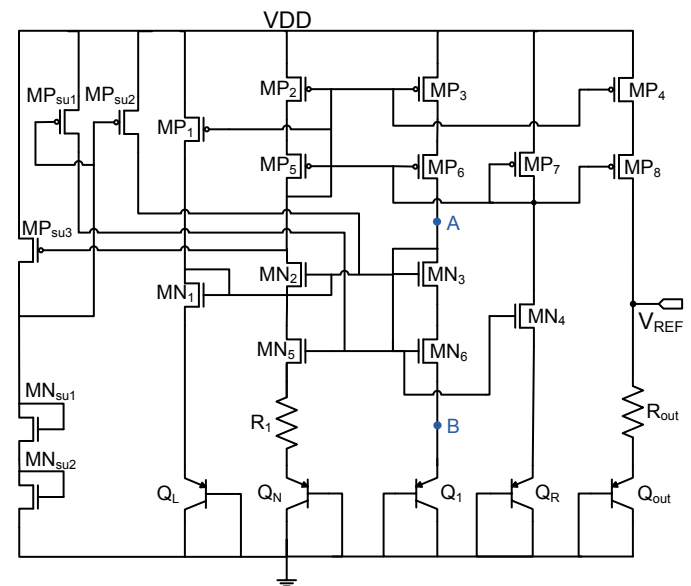

Fig. 2. BGR with Cascode Current mirrors (CCM) utilizing 3.3 V transistors.

The SCM and CCM BGR circuits of Fig. 1 and Fig. 2 are based on the principle of summing a PTAT (Proportional to Absolute Temperature) voltage and a CTAT (Complementary to Absolute Temperature) voltage in order to compensate the temperature effects and achieve a temperature independent voltage at the output. Therefore, the voltage across a forward biased pn-junction diode ($V_{BE(Q_1)}$) is used in order to provide a CTAT voltage. The base-emitter voltage difference ($\Delta V_{BE(Q_1, Q_N)}$) between two pn-junction diodes with non-equal current densities is used in order to provide a PTAT

voltage via the U_T (thermal voltage) which increases linearly with temperature. When the two voltages sum together they provide a temperature insensitive voltage. This principle is applied through the topologies of Fig. 1 and Fig. 2 where the current mirrors, that are composed by MP_1, MP_2, MN_1 and MN_2 in the case of SCM topology and MP_2, MP_3, MP_5, MP_6, MN_2, MN_3, MN_5, MN_6 in the case of CCM topology, forces the voltages at nodes B and C to be equal. This creates a $\Delta V_{BE(Q_1,Q_N)}$ voltage across resistor R_1 which is PTAT and is equal to:

$$\Delta V_{BE(Q_1,Q_N)} = \frac{kT}{q} \ln N \qquad (1)$$

where V_{BE} is the base-emitter voltage T is the absolute temperature, k is the Boltzmann constant (1.38×10^{-23} J/K) and q is the electron charge. The output of the reference circuit is the sum of $V_{BE(Qout)}$ and the voltage drop across the resistor R_{out} and can be expressed as:

$$V_{REF} = V_{BE(Qout)} + V_{Rout} \qquad (2)$$

where V_{Rout} can be expressed as:

$$V_{Rout} = I_{out} \times R_{out} = I_{R_1} \times R_{out} \implies$$
$$V_{Rout} = \frac{\Delta V_{BE(Q_1,Q_N)}}{R_1} \times R_{out} \qquad (3)$$

Therefore, combining (1), (2) and (3), the reference voltage at the output of the SCM and CCM topologies can be expressed as:

$$V_{REF} = V_{BE(Qout)} + \frac{R_{out}}{R_1} \frac{kT}{q} \ln N \qquad (4)$$

where the first term is a CTAT component and the second term is a PTAT component. A low temperature drift can be obtained by properly tuning the ratios of N, R_{out} and R_1 terms.

The layout of the SCM BGR topology of Fig. 1 with 1.8 V transistors is shown in Fig. 3 while the one with 3.3 V transistors is shown in Fig. 4. The layout of the CCM BGR topology with 3.3 V transistors of Fig. 2 is shown in Fig. 5. All the NMOS transistors are designed in edgeless shape while extensive guard rings where utilized to enclose all the matched devices groups.

Fig. 4. Bandgap voltage reference reference circuit with Simple Current Mirrors (SCM) utilizing 3.3 V transistors.

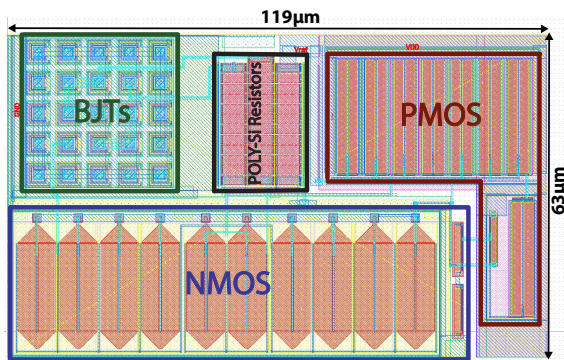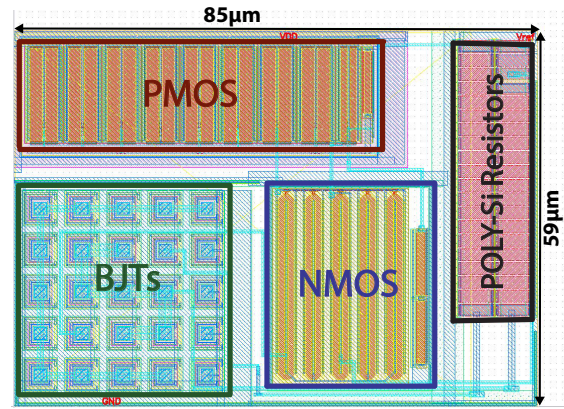Fig. 5. BGR with Cascode Current mirrors (CCM) utilizing 3.3 V transistors.

Fig. 3. Bandgap voltage reference reference circuit with Simple Current Mirrors (SCM) utilizing 1.8 V transistors.

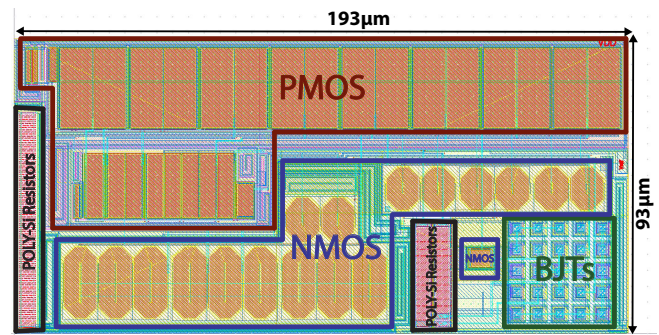The three BGR circuit variants were initially simulated at a schematic level against radiation induced ASETs. The simulation was performed with Cadence®, by injecting transient current pulses, in order to mimic the local disturbance effects of a heavy ion strike at particular nodes of the circuit, whilst monitoring the circuit output as the disturbance propagates through the whole circuit. The transient current pulses were modelled by utilizing the double exponential law and incorporated into the simulations using Verilog-A. The double exponential current pulse is expressed as [60]–[62]:

$$I(t) = I_0 \times (e^{-t/\tau_f} - e^{-t/\tau_r}) \qquad (5)$$

where I_0 is the maximum charge collection current and is equal to $Q/(\tau_f - \tau_r)$, τ_r) is the current pulse rising time constant and τ_f) is the current pulse falling time constant. For the purpose of the Cadence® Verilog-A simulations, I_0 was set at 30 μA, while τ_f and τ_r were set at 7 μs and 1 μs respectively. The double exponential current pulse was injected at node A and then at node B of the two BGR variants with simple current mirrors (1.8 V and 3.3 V) of Fig. 1 and the corresponding nodes of the BGR with cascode current mirrors of Fig. 2. These circuit nodes were selected since they are those that perturbed the most key elements of a BGR circuit; these are the V_{BE}, the ΔV_{BE} and the current mirror. In addition, Q_1 is approximately twenty times smaller than Q_N hence for the same charge and current, the perturbation is less due to lower inherent resistance between the collector and the emitter.

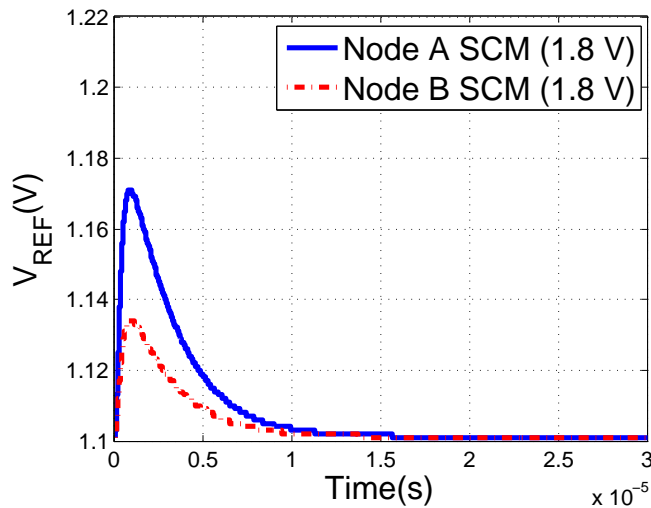The simulation results for strike-induced charge injection

Fig. 6. Spice simulations of the SCM (simple current mirrors) circuit with 1.8 V transistors by injecting a double exponential current pulse at circuit nodes A and B using a Verilog-A model at the schematic level.
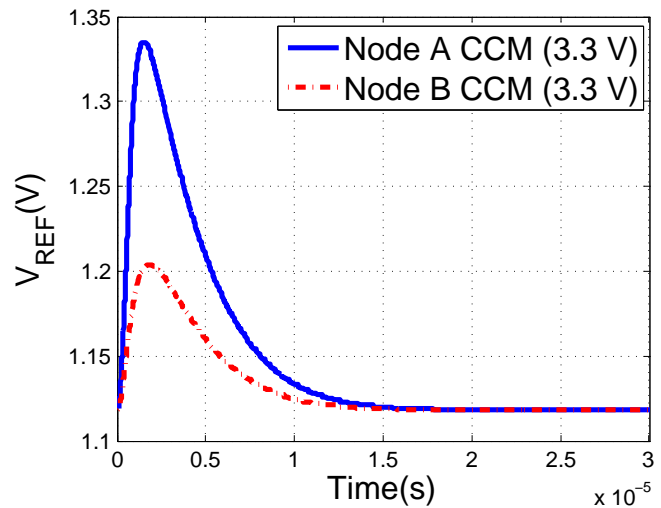

Fig. 8. Spice simulations of the CCM (cascode current mirrors) circuit with 3.3 V transistors by injecting a double exponential current pulse at circuit nodes A and B using a Verilog-A model at the schematic level.
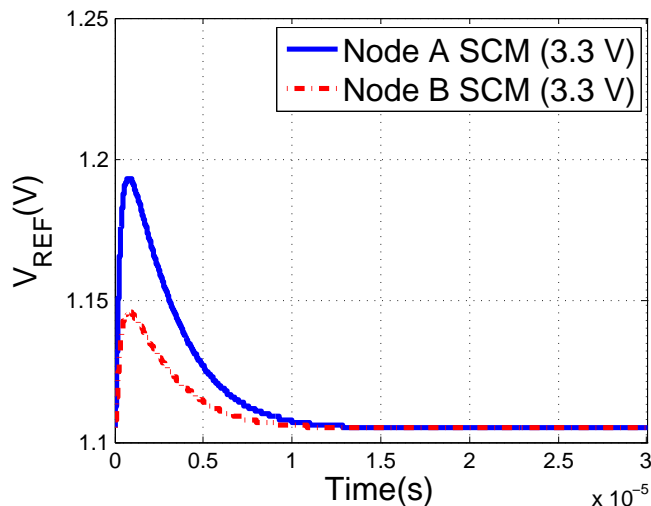

Fig. 7. Spice simulations of the SCM (simple current mirrors) circuit with 3.3 V transistors by injecting a double exponential current pulse at circuit nodes A and B using a Verilog-A model at the schematic level.

at nodes A and B are shown in Fig. 6 for the SCM-1.8V, in Fig. 7 for SCM-3.3V and in Fig. 8 for CCM-3.3V. For both nodes the circuits that show the most resilience, are the circuits with simple current mirrors, which have almost identical results. The circuits containing cascode current mirrors exhibit much stronger transients, both in terms of pulse duration and pulse amplitude. A possible explanation for this, is that the cascode stages increase the resistance to VDD or ground from intermediate nodes, thus impeding the transfer of the additional charge to the small-signal ground terminals and increasing the voltage gain associated with the injected current. Furthermore a slow return to the nominal bias point at a cascoded high-impedance terminal has the effect of allowing the transient to propagate to other nodes, which might have otherwise not have been affected. Thus the two circuit variants of Fig. 1 are more likely to dissipate and hence tolerate excess charge as

opposed to the circuit of Fig. 2.

III. EXPERIMENTAL MEASUREMENTS

The three variants of this circuit were fabricated in a regular CMOS 0.18 μm technology and were tested at RADEF (Radiation Effects Facility) at the University of Jyvaskyla, for ASETs. Heavy ions (Si, Kr and Xe) from RADEF's standard 9.3 MeV/μm cocktail were used in order to provide different LET characteristics, so as to extract the cross-section (σ) for each circuit design. The circuit irradiations were performed in air with a Kapton foil thickness of 25 μm and air thickness of 5 mm. During irradiation, the circuits were biased at nominal supply voltages and the ASETs were recorded using a high sampling-rate oscilloscope (Agilent Technologies DSO9104A 1GHz/20GS/s). The oscilloscope was set to record all the transient segments above a threshold trigger level (12 mV). This level is higher than the reference circuit noise floor and ensures that stray electromagnetic fields at the testing facilities do not trigger the oscilloscope. A typical ASET response with Xe ions, obtained from the circuit SCM - 1.8V of Fig. 1, is shown in Fig. 9. The ASET duration is approximately 10 μs and the amplitude is approximately 55mV.

The RADEF's heavy ions cocktail provided Si ions with a LET(Si) of $\sim$6.9 MeV·cm^2/mg, Kr ions with a LET(Si) of $\sim$36.1 MeV·cm^2/mg and Xe ions with a LET(Si) of $\sim$64.7 MeV·cm^2/mg. The charge that will be deposited in the projected material is greater at higher LET.

In order to get a quantitative approach of the charge that each particle can deposit we calculate the N_0 (electron-hole line density) as well as the $\frac{Q}{L}$ (charge transfer rate per unit length of material penetration) that corresponds to each of the heavy ions that were used in these experiments. The results are presented in Table I where higher LET induces more electron-hole pairs and hence deposits more charge in the material.

In order to evaluate the resilience of the tested circuits when exposed to heavy-ions one has to calculate the cross-section, σ, which is expressed as $\sigma = N_{ASET'S}/\phi$ (cm^2)

TABLE I
CALCULATED N_0 AND $\frac{Q}{L}$ FOR THE HEAVY IONS THAT ARE USED IN THESE EXPERIMENTS

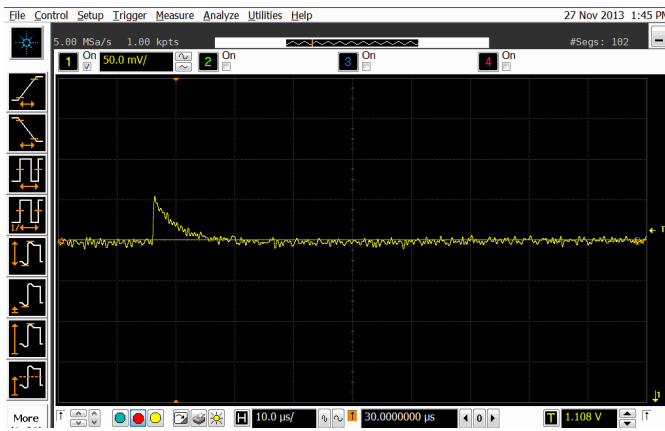| **Heavy Ion**	$N_0[Si]$ ($e\text{-}h\ pair/\mu m$)	$\frac{Q}{L}[Si]$ ($pC/\mu m$)	$N_0[SiO_2]$ ($e\text{-}h\ pair/\mu m$)	$\frac{Q}{L}[SiO_2]$ ($pC/\mu m$)
Si (LET∼6.9 MeV·cm^2/mg)	4.45×10^5	0.0712	1.075×10^5	0.0172
Kr (LET∼36.1 MeV·cm^2/mg)	2.33×10^6	0.3728	5.62×10^5	0.09
Xe (LET∼64.7 MeV·cm^2/mg)	4.17×10^6	0.67	1×10^6	0.16

Fig. 9. A measured typical ASET of BGR with Simple Current mirrors (1.8 V transistors), acquired with the oscilloscope during irradiation with Xe ions. The ASET duration is approximately $10\mu s$ and the ASET amplitude is 55 mV. The scale of the x-axis is is 10 μs for every grid time window (scale is shown at the bottom of the image) and of the y-axis is 50 mV for every grid voltage window (scale is shown at the top-left of the image).
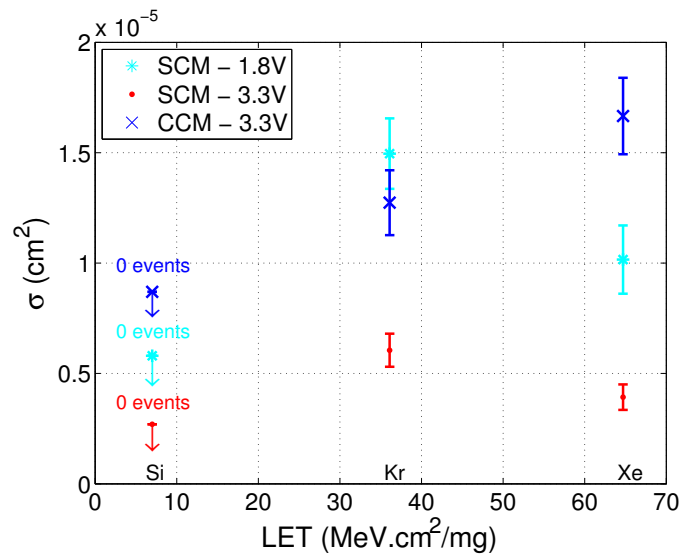

Fig. 10. Measured Cross-Section of all bandgap voltage reference circuits variants, including simple current mirrors with 1.8 V transistors (SCM-1.8V), simple current mirrors with 3.3 V transistors (SCM-3.3V) and cascode current mirrors with 3.3 V transistors (CCM-3.3V).

where $N_{ASET'S}$ is the observed number of ASET events and ϕ is the uniform particle fluence (particles/cm^2) and depends on the total dose. The time duration was obtained by running a Matlab script on the measured data acquired by the oscilloscope. The script detected the onset and the end of the ASET by using a threshold (1 mV). This was defined to be 10% of the minimum ASET amplitude (10 mV), which was defined to be well above the noise floor of the circuits and any external electrical interferers at the test facility.

The measured σ for all the BGR circuits variants, including the two versions with simple current mirrors of Fig. 1 with 1.8 V transistors (SCM-1.8V) and 3.3 V transistors (SCM-3.3V) as well as the circuit with cascode current mirrors of Fig. 2 with 3.3 V transistors (CCM-3.3V) are shown in Fig. 10. All the three tested topologies did not exhibit any significant sensitivity to Si ions, (LET∼6.9 MeV·cm^2/mg) since Si ions were not able to induce detectable transients to any of the circuits.

While using Kr ions (LET∼36.1 MeV·cm^2/mg), the SCM-1.8V- circuit exhibited a much higher σ , when compared to the SCM-3.3V circuit and slightly higher σ when compared to the CCM-3.3V circuit, as shown in Fig. 10. A possible explanation behind these results is the fact that the SCM-3.3V circuit, which exhibits the lowest σ, has a thicker gate oxide which in circuit terms translates to a lower transconductance per unit area, hence requiring more charge to alter a transistor's steady-state, when compared to the SCM-1.8V circuit. Fur-

thermore, the SCM-3.3V circuit utilizes fewer cascode stages, which leads to lower impedance to VDD or Ground (smaller time constant) when compared to the CCM-3.3V circuit. The smaller time constant of the ASET decreased the probability that it will propagate to the output of the circuit. In addition, the cascode stages increase the physical distance between the high impedance nodes (which are the most sensitive to charge injection) and the supply rails, hence weakening the electric field that could collect excess charge generated in the substrate. The fact that in Fig. 10, CCM-3.3V shows slightly less σ, when compared to the SCM-1.8V circuit, reveals that gate oxide thickness could be a dominating factor in terms of ASET resilience when compared to the cascode stages.

While using Xe ions (LET∼64.7 MeV·cm^2/mg) the SCM-3.3V circuit still exhibits the lowest σ, as shown in Fig. 10, for the reasons explained above, though a relatively minor decrease in cross-section, with respect to Kr, is observed. One would expect that the SCM-1.8V would be the worst performer or at least be comparable to the CCM-3.3V, following the trend given by the Kr ions σ result. Paradoxically the σ of the SCM-1.8V drops significantly both in comparison to the CCM-3.3V and in comparison to its Kr σ result, with almost half the LET. This anomaly can only be explained by the pulse quenching phenomenon, that has been observed in other circuits [63].
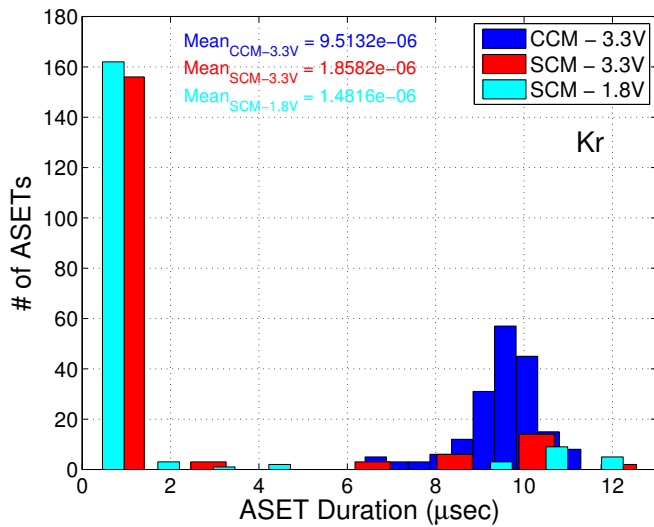
Fig. 11. Measured number of ASETs Versus ASETs duration for all BGR circuit variants, including simple current mirrors with 1.8 V transistors (SCM-1.8V), simple current mirrors with 3.3 V transistors (SCM-3.3V) and cascode current mirrors with 3.3 V transistors (CCM-3.3V).
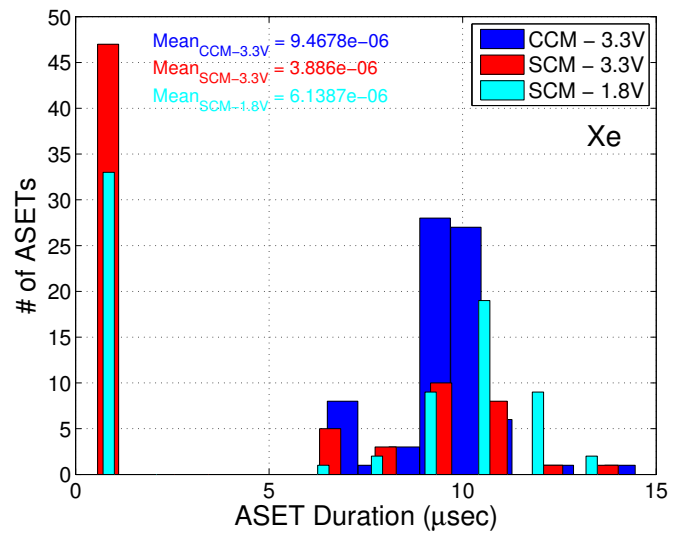

Fig. 12. Measured number of ASETs Versus ASETs duration for all BGR circuit variants, including simple current mirrors with 1.8 V transistors (SCM-1.8V), simple current mirrors with 3.3 V transistors (SCM-3.3V) and cascode current mirrors with 3.3 V transistors (CCM-3.3V).

This phenomenon will be explained in more detail in section IV.

Apart from σ, the duration and amplitude of the ASET is an important factor in RHBD. These results are shown in Figs. 11 and 13 where we analyze and present the first 185 segments recorded for each circuit, while exposed to Kr, and furthermore, in Figs. 12 and 14, where we analyze and present the first 85 segments, recorded for each circuit while exposed to Xe. The measured results of Fig. 11 with Kr ions, show that SCM circuits have smaller average ASET durations, when compared to the CCM circuits. As explained earlier the lower impedance at critical nodes enhances the escape speed of the surplus ionisation charge towards VDD or Ground. The measurements with Xe ions of Fig. 12 show that SCM circuits still exhibit smaller average ASET durations when compared to the CCM circuit. As expected, the average ASET duration of all circuits increases, when compared to the results of Fig. 11 with Kr ions, because of the higher LET of Xe compared to Kr ions.

The results of Fig. 13 show that, as with the results of ASET's duration, the SCM topologies exhibit smaller ASETs peak amplitudes when compared to the CCM topology when exposed to Kr ions, with the SCM-1.8V circuit exhibiting the smallest peak amplitudes. This can once again can be explained by the low impedance route to VDD or Ground seen by the excess charge. The measurements of the ASETs average peak amplitudes when the ICs are exposed to Xe ions are shown in Fig. 14. These results agree with the ones of Fig. 13, where the SCM topologies exhibit smaller peak amplitudes compared to the CCM topology. Overall, all circuits exhibit increased ASET amplitudes for Xe compared to Kr irradiation exposure due to increased LET which further perturbs the circuits charge state at particular nodes.

An overall evaluation of the three circuit architectures reveal that the best performance in terms of σ is achieved by the

Fig. 13. Measured number of ASETs Versus ASETs peak amplitude for all BGR circuit variants, including simple current mirrors with 1.8 V transistors (SCM-1.8V), simple current mirrors with 3.3 V transistors (SCM-3.3V) and cascode current mirrors with 3.3 V transistors (CCM-3.3V).

SCM-3.3V circuit, while the best performance in terms of average ASET duration and amplitude (smaller is better) is achieved by SCM-3.3V and SCM-1.8V which have very similar results. The key factors that affect their performance are the circuit topology, the device gate oxide thickness and the supply voltage. The circuit topology includes, the resistance to VDD/Ground and the sensitive nodes' connections, which in turn affect the time and rate that the generated charge needs to be absorbed, to return to the normal operating conditions. The gate oxide thickness (depends on the type of device that is selected) and the supply voltage, both affect the amount of energy needed in order to alter the transistor's normal operating conditions. In addition, a thinner gate oxide leads to
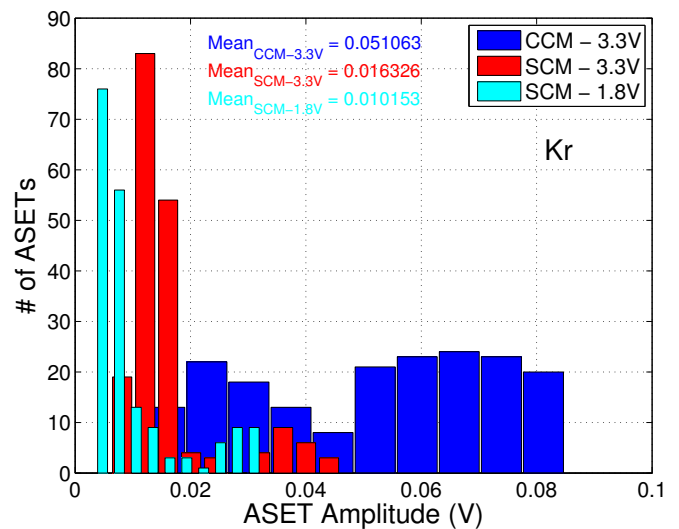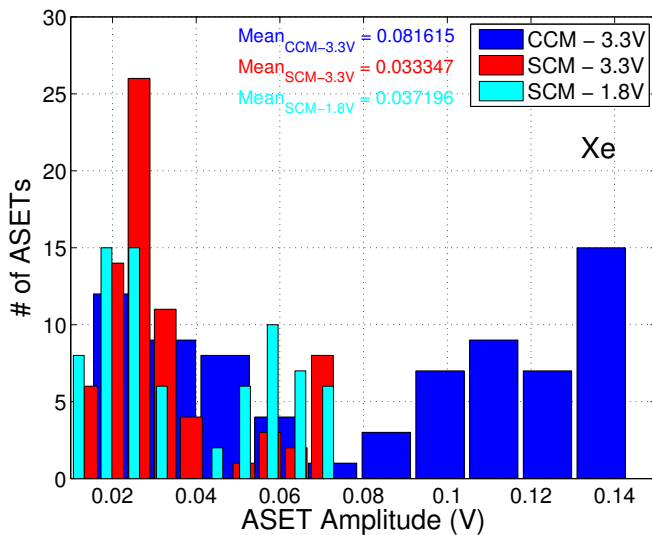
Fig. 14. Measured number of ASETs Versus ASET's peak amplitude for all BGR circuit variants, including simple current mirrors with 1.8 V transistors (SCM-1.8V), simple current mirrors with 3.3 V transistors (SCM-3.3V) and cascode current mirrors with 3.3 V transistors (CCM-3.3V).

a greater transconductance for a fixed device area, since the channel charge is better controlled. Thus the charge released by an ion at sensitive nodes is amplified and propagated to other adjacent nodes more efficiently in 1.8 V based topologies when compared to 3.3 V topologies, thus affecting the total circuit performance.

Among the designed and tested circuit architectures, the optimal circuit is the SCM-3.3V circuit, because of smaller path resistance to VDD/Ground as opposed to the CCM-3.3V, while it utilizes the 3.3 V transistors which have thicker oxide and higher supply voltage compared to the 1.8 V transistors that are utilized by the SCM-1.8V circuit. The worst circuit in terms of σ, ASET duration and ASET amplitude would marginally be the SCM-1.8V due to the fact that the gate oxide thickness and supply voltage are slightly dominating the ASETs time constant parameters. This is be supported from the results of the Kr ion irradiation. However, it actually turns out that the worst circuit in terms of σ and ASETs duration and amplitude is the CCM-3.3V. This very interesting and important outcome that is revealed from the experimental measurements is originating from pulse quenching that occurs in both the SCM architectures, as opposed to the CCM one.

As BGR circuits' performance is highly dependent on architectural design, such as the topology and the devices parameters, most of the guidelines that are extracted from these experimental results may be used in other analog and mixed signal circuits, intended for the space environment.

IV. PULSE QUENCHING PHENOMENA IN MEASURED RESULTS

The cross-section of the two variants (SCM-1.8V and SCM-3.3V) of Fig. 1, which utilize simple current mirrors give a seemingly paradoxical response, as is shown in the measured results of Fig. 10. Although Xe ions have a higher LET than Kr ions, the cross-section for Xe-ion-induced ASETs is lower

than the cross-section of Kr-ion-induced ASETs. This paradox can be explained through the pulse quenching phenomenon [2], [64]–[66], which has been previously observed or used to mitigate SETs in other analog or digital circuits such as digital inverters, current sources, switched capacitor amplifiers, continuous time amplifiers, folded cascode amplifiers and differential circuits design [6], [23], [63], [67]–[74]. In the next section we justify the measured results by focussing on the key topological difference between the two circuit classes, i.e. the simple/cascode current mirror.

The quenching effect depends heavily on radiation-induced charge sharing. This is the charge interaction of several adjacent circuit nodes *via the substrate* (outside the active channel), instead of *through the the transistors' active channel or via the wiring*. Charge sharing through the substrate induces parasitic currents, which alter the electrical signals that propagate through the intended circuit architecture. Transport outside the active channel consists of two mechanisms: diffusion of the radiation-induced charge within the bulk and charge transport via a parasitic bipolar effect. These two charge sharing mechanisms are explained thoroughly by using Fig. 15, within the context of the current mirror part of the SCM BGR circuits of Fig. 1 and pulse quenching.

The current mirror of this circuit is shown in Fig. 15(a). The most sensitive areas for charge separation of electron-hole pairs are: (a) the depletion region of the reverse biased pn junction of the drain terminal, and (b) the substrate in the close vicinity; thus we analyse the case of energetic ion strikes at node D (drain of MP_1). However the principles of charge sharing would still apply to strikes in other less sensitive regions.

A. Funneling

The physical cross-section of the mirror is shown in Fig. 15(b), including the above mentioned ion strike location and trajectory. Upon impact it transfers enough energy to create a multitude of electron-hole pairs in the region. The high electric fields separate the charges via the drift mechanism and decrease the probability of electron-hole pair recombination. The electric field forces holes to drift towards the drain (funneling mechanism), whilst the electrons are likely to drift towards the n-well substrate bias contacts as illustrated in Fig. 15(c). Due to the difference in mobility, after initial charge separation, a higher concentration of holes remain around the drain terminal therefore extending the collection region relatively far from the drain terminal via funneling drift collection mechanism. Funneling mechanism (based on drift) is much faster compared to the diffusion based mechanism.

B. Diffusion Based Equalization Mechanism

The other well-know transport mechanism that affects the charge redistribution is that of diffusion. In Fig. 15(d), the high hole concentration, that is left behind after the electric field has separated the electron-hole pairs, initially increases the voltage at node D, which in turn increases the gate voltage of MP_1, and therefore the gate voltage of MP_2 and MP_3. The decreased gate-source voltage (V_{GS}) of these devices reduces
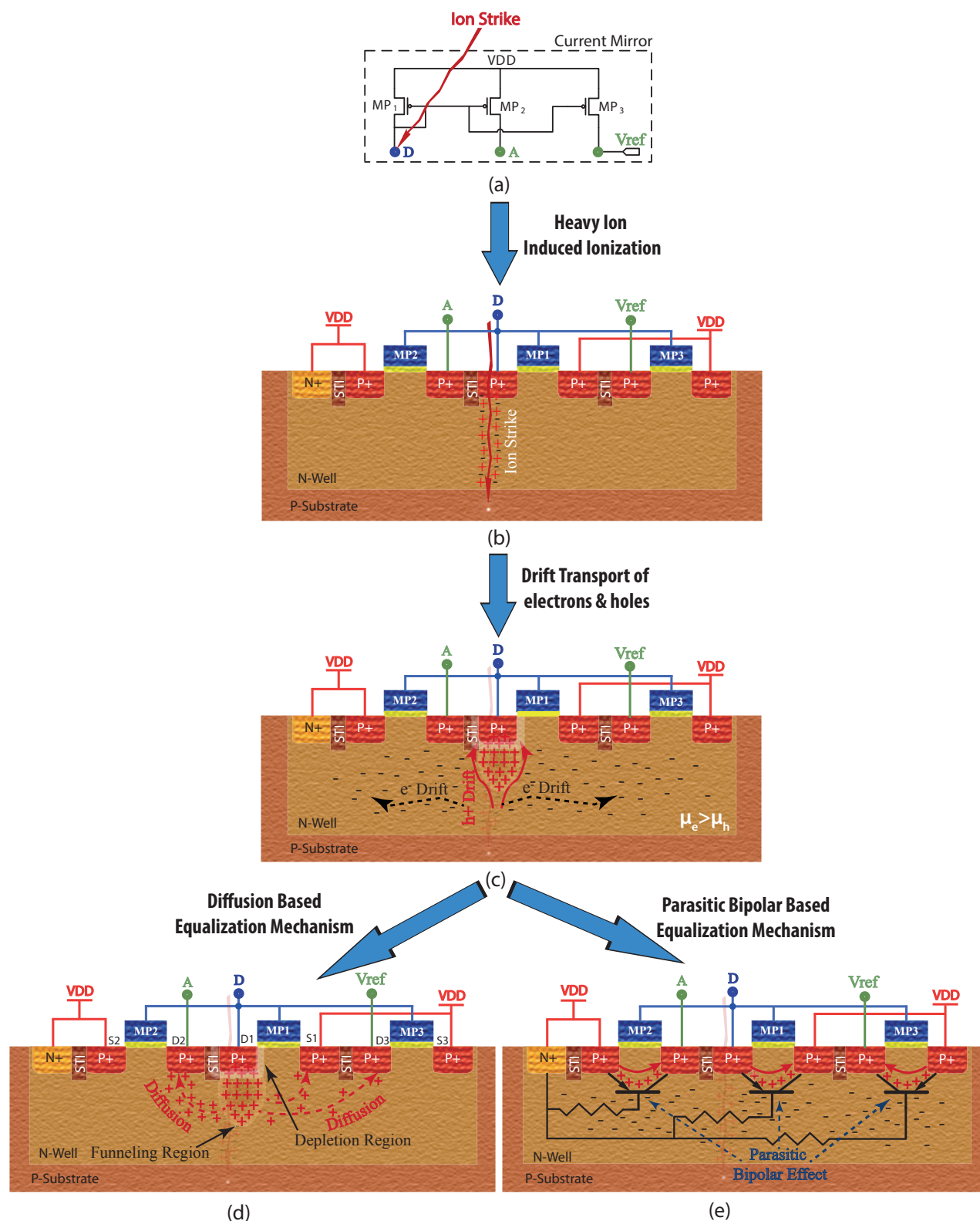
Fig. 15. Illustration of the PMOS Current Mirrors' ASETs Pulse Quenching due to charge sharing from heavy ions induced ionization that was observed in the measured results of Fig. 10 and corresponds to the BGR circuit architectures of Fig. 1. (a) Schematic with the current mirror of the Fig. 1 circuit shown in a dotted lines box, (b) Ion Strike at node D where it generates an excess of e-h pairs due to ionization along its path (c) The generated e-h pairs start to drift under the electric field (note that mobility of the e$^-$ is greater than that of holes). Holes drift towards the transistor's drain which is at a lower potential than the N-Well substrate and electrons drift within the N-Well. (d) Charge sharing due to diffusion of holes from the high charge concentration of node A towards the low charge concentration of nodes D(D1), $V_{ref}(D3)$ and VDD(S1) (diffusion towards this node occurs only if the charge of the excess holes increases beyond that of VDD), (e) Charge sharing due to parasitic bipolar effect (the current direction at MP_1 depends if the radiation-induced charge at node D will be lesser or greater than the charge at VDD).

the current flowing through MP_1, MP_2 and MP_3, and therefore the voltage at nodes A and V_{ref} will drop. The fact that the substrate under node D has now significantly more charge in comparison to nodes A and V_{ref}, will trigger a diffusion process of holes from node D towards the adjacent nodes A and V_{ref} as illustrated in Fig. 15(d). Once the diffused holes are within the vicinity of the reverse biased pn junction of nodes A and V_{ref}, they are swept across the depletion region, thus increasing the node voltages, and 'quenching' the initial effect of the transient. Hence, the end result of the diffusion of the positive charge through the substrate will be to partially or totally restore the charge disturbance that was induced from the ion strike at nodes A, D and V_{ref} through this charge redistribution. This effect is highly dependent on the transistor spacing/concentration gradients, and thus was first observed in a 0.13μm [63]. The diffusion rate is a function of the charge concentration gradient, therefore with increasing LET the diffusion rate increases, draining via D1 (see Fig.15(d)). If only this phenomenon was at play, the Cross-Section σ would be monotonic i.e. first derivative is positive, but decreasing in value. In order to explain the non-monotonic function of σ Vs LET, Fig. 10, something else is happening. It is either due to the fact that once the hole "cloud" passes the STI barrier a second pn junction D2 assists in the charge draining process, hence enabling a non-monotonic Cross-Section σ, since the drainage capacity doubles. Even though junction S1 is at the same potential as the bulk, it will also assist in draining excess positive charge since the concentration of free holes at the depletion region interface is lower, due to the built in potential, that sweeps the holes from the n-region to the p-region. Furthermore the non-monotonic function of σ Vs LET, could be assisted by the Parasitic Bipolar Based Equalization Mechanism.

C. Parasitic Bipolar Based Equalization Mechanism

The parasitic bipolar effect is an additional effect that involves charge draining after a charged ion strike [12], [65], [66], [71], [74], [75]. Parasitic bipolar effect is the process where a PMOS transistor's junction between the P+ source and the N-well is forward biased, resulting in a P-N-P parasitic bipolar junction transistor through the PMOS substrate to be turned on. Thus, through this parasitic BJT, the PMOS source will inject holes to the PMOS drain through the N-well. This effect, involves charge sharing, not between multiple transistors' terminals like the diffusion process, but between the terminals within a single transistor. The electrons that drift in the bulk due to ionization are confined within the N-Well, thus they will temporarily cause the N-Well potential to drop. This may force the junction between the P+ source and the N-Well to be forward biased, resulting in a P-N-P parasitic bipolar junction transistor through the PMOS N-Well to be turned on as shown in Fig. 15(e). The PMOS source, drain and N-Well bulk will act as a P-N-P bipolar transistor's emitter, collector and base respectively, allowing a flow of holes from source (emitter) to the drain (collector) via the N-Well (base). As a consequence, node D will collect more charge through holes injection from the supply aggravating its charge state,

while nodes A and V_{ref} will collect charge through holes from the supply thus partially recovering their charge state.

The parasitic bipolar transistors at nodes A and V_{ref} have a certain threshold where the voltage at the base is greater than that of the emitter and smaller than that of the collector ($V_E > V_B > V_C$). This will occur in relatively high LETs where the BJT base voltage will drop below the emitter one (due to ionized e^- drift in the N-Well) while concurrently the BJT base voltage will get higher than that of the collector one (due to the decrease charge at nodes A and V_{ref} caused by the reduction of V_{GS} of the current mirror). When this threshold is valid then the parasitic BJT enters the active region where the parasitic transistor acts as an amplifier. Therefore the effect of radiation induced e^- in the N-Well is restoring the radiation induced charge disturbance with an amplification. This amplification can also explain the non-monotonic function of σ versus LET in the measured results of Fig. 10. Therefore, above a certain LET threshold (ionized electrons-holes pairs is proportional to LET) the σ begin to decline albeit of the higher charge release in the sensitive node.

D. The Effect of Pulse Quenching on Simple and Cascode Current Mirrors

In Section III the effect of the cascode mirrors on the SETs was explained in terms of a higher impedance path for the excess charge to be routed to the supply rails. Quenching is also affected by the cascode devices, since even if a second pn junction, like the example of S1, assists in the charge draining process, the extra charge will have to pass through a second transistor, via the normal operating path, and be limited by the saturation current. In order to verify the hypothesis that the decrease in output disturbance at larger LETs can be attributed to Pulse Quenching, a SPICE simulation in Cadence was utilized. Without pulse quenching, a double exponential pulse charge was injected in both the simple current mirror and the cascode current mirror at the key node being node D of Fig. 15(a). For examining the effect of Quenching, a second, smaller double exponential pulse was applied to the second key node, being node A of Fig. 15(a), emulating the charge sharing effect from node D towards node A. The results are shown in of Fig. 16 where both implementations improved in terms of duration and amplitude due to charge sharing enhancement. The simple current mirror is more robust in terms of both cases, with or without pulse quenching. The results show that the simple current mirror circuit's ASET amplitude and duration are reduced to half of the non-quenched. However the cascode current mirror circuit has a minor amplitude reduction which is far larger compare to the simple current mirror one. This suggests that pulse quenching is more advantageous in non-cascode circuit nodes for diminishing or completely eliminating the ASETs.

Pulse quenching in current mirrors can occur under a number of conditions that have to concurrently be valid. These conditions involve the small spacing between the transistors that facilitate charge sharing, the absence of guard ring between those transistors, the LET, the layout design and the circuit architecture. The layouts of the current mirrors that are utilized
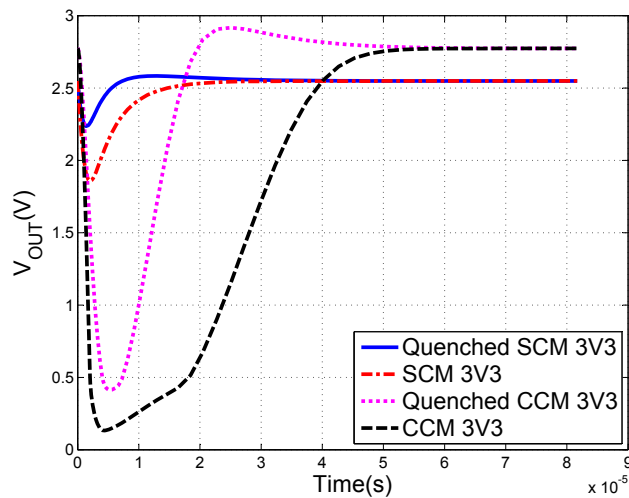
Fig. 16. Comparison of a simple current mirror and a cascode current mirror output through SPICE simulations, with and without pulse quenching phenomena.

in the circuits that are reported in this paper were designed in common centroid configurations with multiple fingers for improved transistor matching. In addition to matching issues that are of critical importance in the performance of current mirrors, the matching techniques and common centroid layout will facilitate the charge sharing [76] between the current mirrors during ion strikes in space. This is justified by the fact that in common-centroid layout the mirroring transistors are designed in pairs with minimum distance from each other and they have a common guard ring around them, without any guard ring in between them. The observations revealed from these designs and experimental tests are applicable for current mirrors in all analog and mixed signal integrated circuits.

V. CONCLUSION

Radiation sensitivity for high performance deep-submicron IC technologies is expected to be mainly determined by radiation induced ASETs due to continuous shrinking of the devices' feature size and reduced supply voltage. Thus, lower required ion energies will have higher probability to induce ASETs in a circuit node that will propagate to a circuit's output and corrupt the performance of the subsequent circuits, deteriorating the performance of whole system. In order to extract guidelines for mitigating ASETs radiation effects, three BGR circuit variants were designed in 0.18 μm CMOS technology, fabricated and characterised against heavy-ion induced ASETs. After thorough data processing of the measured results, some useful practices were extracted that can be used by designers in order to mitigate SEEs when designing for space electronics. These practices indicate that a better ASET performance can be achieved whilst using devices with thicker oxides, higher supply voltage and fewer cascode stages. Finally, a very important finding suggest that the indispensable current mirrors designed in modern technologies, that are widely used in all analog and mixed signal circuits, can be designed such that they will assist charge sharing that will

subsequently trigger pulse quenching. Thus charge sharing, which in many cases is undesirable, in current mirrors is shown to be extremely beneficial for ASETs mitigation or complete compensation as demonstrated in this paper and could be extended in other analog circuit blocks depending on the circuit architecture and the nature of the electrical coupling between proximal circuit nodes. Based on the measured as well as the simulated results, charge sharing can be utilized as a RHBD technique [56], [67]–[69] for one of the most fundamental analog building blocks, the current mirror.

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