Fabrication of 3-D phononic crystals for thermal transport management

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Abstract

Since the technological revolution and invention of computers, overwhelming changes in human life happened. Every day we develop smarter and more powerful electrical devices, which can process information faster and store more and more of it based on semiconductor elements. Such dramatic increase in power leads us to the problem of efficient cooling of logical elements. On the other hand, the enormous number of electrical devices in our lives requires a lot of energy production, which is costly and limited. So, for that reason the question about energy conservation arises. Moreover, thermal noise is usually an unavoidable source of errors for ultrasensitive detectors even at low temperatures. One of the possible solutions to these problems is the development of artificial materials, which can demonstrate high thermal conductivity for efficient cooling purposes, and extremely low thermal conductivity for proper thermal shielding aims.

In this work, we demonstrate the possibility to fabricate artificial 3-D phononic crystals, which, based on theoretical predictions, should reveal a significant decrease in thermal conductivity at low temperatures. Initial thermal transport measurements were performed by applying Normal metal – Insulator – Superconductor (NIS) tunnel junction thermometers, which have been diligently studied since 1976.

Contents

Introduction

Thermal transport is an important physical phenomenon, and it has recently become even more relevant for the reduction of energy losses and the increase of efficiency in novel devices based on thermoelectricity [1]. Significant reduction of thermal conduction was recently achieved by coherent modification of phonon modes [2], with the help of periodic phononic crystal structures. However, currently the experimental studies have only been performed for two-dimensional (2-D) nanostructures. Theoretically, the magnitude of control of thermal transport should be even stronger in three-dimensional (3-D) phononic crystal structures. For that reason, the question arises how to fabricate the desired 3-D phononic crystal nanostructures.

The first attempts to fabricate 3-D phononic crystals were already performed [3], however, Tero Isotalo, Yaolan Tian and others did not succeed in fabrication of the thermal transport measurement setup for these nanostructures, mainly because they used polystyrene colloidal particles, which are not stable enough under harsh chemical compounds required in electron beam lithography. For that reason, here we introduce a non-organic material, silicon dioxide (SiO_2), in the form of spherical 170 nm sized colloidal particles. The most challenging step in fabrication 3-D phononic crystal nanostructures for thermal transport management is to make superconducting tunnel junctions on top of this rough nanosphere surface. They will serve as low temperature thermometers. Here various methods were initially utilized, including physical vapor deposition (PVD) and plasma enhanced chemical vapor deposition (PECVD) coating of thin layers of SiO_2 and Al_2O_3, but they did not give any positive results. The coating with the material initially in liquid phase might be the proper solution to this problem. That is why negative photoresist (SU-8) was found to be the most promising material to make the rough nanosphere surface smooth, giving us the possibility to fabricate tunnel junctions on top of it and to conduct thermal transport measurements.

Chapter 1

Theory and Background

1.1 Phononic crystals

1.1.1 Phonons in continuous media

Crystalline, nonmagnetic insulators do not have free electrons, which usually carry most of the energy in metals and other conductive materials. As a result, in most cases the only possible mechanism for heat transfer in this kind of insulators are vibrations of atoms, which are called phonons [4]. The number of excited vibrational states of atoms strongly depends on the temperature of the material, and at high temperatures all possible vibrational states of lattice atoms are excited.

At first, by considering each atom as a classical harmonic oscillator, the Dulong – Petit law was applied for description of heat capacity of insulators. Unfortunately, later it was revealed that this law works well only for high temperatures, because it assumes that all vibrational states of atoms are excited independently. When thermal energy k_BT is small enough, not all vibrations of lattice are excited, with the limiting temperature around 100 K [5]. So, after the development of quantum theory, Einstein proposed to treat each atom as an independent quantum harmonic oscillator with the same frequency. It was shown that the average number of phonons (excited lattice vibrations) can be described by the Bose-Einstein distribution function:

$$\langle n_{ph} \rangle = \frac{1}{e^{\hbar\omega/k_BT} - 1} \ , \tag{1.1}$$

where ω is a phonon angular frequency, and T is its temperature. At low temperatures Debye showed that actually the phonon density of states can be described by the following expression [5]:

$$g_{ph}(\omega) = \begin{cases} \left(\dfrac{3V_m}{2\pi^2\vartheta_s^3}\right)\omega^2, & \omega \le \omega_D, \\ 0, & \omega > \omega_D, \end{cases} \tag{1.2}$$

where V_m is the molar volume, and the average acoustic velocity with linear dispersion relation is defined by:

$$\frac{1}{\vartheta_s^3} = \frac{1}{3}\left(\frac{1}{\vartheta_{long}^3} + \frac{2}{\vartheta_{trans}^3}\right), \tag{1.3}$$

where $\vartheta_{long}, \vartheta_{trans}$ are the longitudinal and transverse acoustic velocities of vibrational modes of atoms [5]. This expression arises from the linear dispersions $\omega = \vartheta \cdot k$ for the lowest energy phonon modes. He also defined the limit for the maximum allowed vibrational frequency, called Debye frequency ω_D when all 3N vibrational degrees of freedom are excited in a crystal with N atoms:

$$\omega_D = \left(\frac{6\pi^2 N}{V_m}\right)^{1/3} \vartheta_s \tag{1.4}$$

This frequency corresponds to specific thermal energy $k_B T_D$, which is different for different materials. If the temperature is lower than the Debye temperature T_D, the number of excited modes starts to decrease. As a result, the total thermal energy of 3-D crystalline insulator at temperatures lower than Debye temperature can be expressed by the following equation:

$$E_{tot} = \int g_{ph}(\omega) \cdot \left(\langle n_{ph}\rangle + \frac{1}{2}\right) \cdot \hbar\omega_{ph} \cdot d\omega \tag{1.5}$$

The heat capacity is traditionally defined by:

$$C_V = \left(\frac{\partial E_{tot}}{\partial T}\right)_V \tag{1.6}$$

And by applying Equation 1.5, the heat capacity for temperatures $T < T_D/10$ yields [5]:

$$C_{ph}(T) = \frac{12}{5}\pi^4 N k_B \left(\frac{T}{T_D}\right)^3 \tag{1.7}$$

Our main focus in this thesis is phononic thermal conductivity, which in continuous media is expressed through heat capacity as follows [6]:

$$k_{ph} = \frac{1}{3}\frac{C_{ph}}{V_m}\vartheta_s\lambda_{ph} \sim T^3\lambda_{ph}(T), \qquad at\ T \leq T_D/10 \qquad (1.8)$$

where λ_{ph} is the mean free path of phonons in material. It worth to notice, that the same expression is obtained by using either quantum mechanical or classical treatment. The value of the mean free path of the heat carriers is defined by scattering processes in the material. In the case of insulators, the dominant scattering mechanisms are due to boundaries, defects, and phonon-phonon scattering [6]. The significance of the latter mechanism is strongly reduced with decreasing temperature due to the reducing number of phonons at low temperatures [5, 6].

1.1.2 Phonons in artificial crystals

Phononic crystal is the equivalent structure to the well-known photonic crystal, but designed for acoustic waves, instead of electromagnetic. It can be obtained by creating the structure with periodically changing density of material and sound velocity, instead of a periodic dielectric constant. In analogy to photonic crystals, Michael Sigalas and Eleftherious Economou in 1992 [7] theoretically proved that a periodic 3-D lattice of identical hard spheres surrounded by low-density media has a phononic band gap. The origin of this band gap in dispersion relation is explained by Bragg`s interference [7, 8], and can be observed in 1-D, 2-D, and 3-D phononic crystals (see Figure 1.1.1). One of the first experimental evidence of existence of a phononic band gap was presented in 1995 by Francisco Meseguer [9] when he and his group studied the acoustic properties of a kinematic sculpture by Eusebio Sempere, which is depicted in Figure 1.1.2.
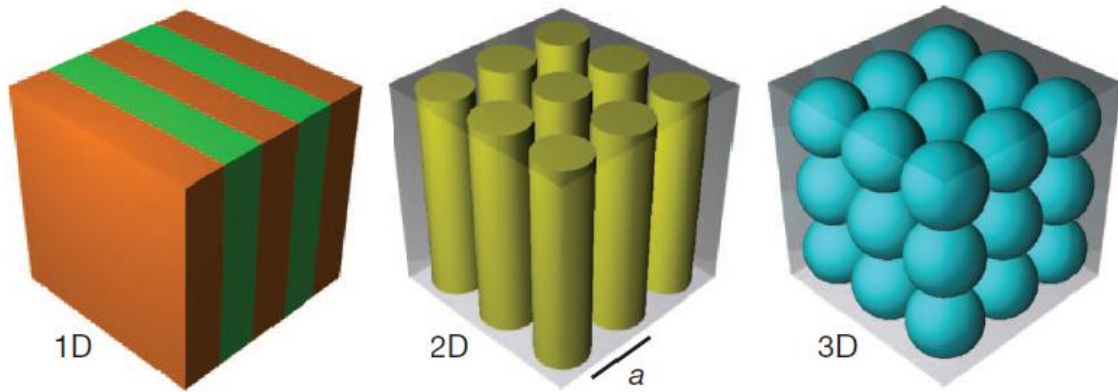
Figure 1.1.1. Schematic representation of phononic crystals made of two different elastic materials (depicted by different colors) arranged periodically [10].

These experiments revealed that at a specific direction the sound wave at a frequency of 1670 Hz is strongly attenuated, which is a first solid proof of the existence of a phononic band gap. The band gap in that structure existed only in specific direction and for a small range of frequencies, because in order to get constructive interference, the difference in acoustic wave path should be equal to the integer number of wavelength. The constructive interference of the incident and reflected acoustic waves will not allow the wave to propagate inside the lattice, which results in band gap for this wavelength. Of course, the path difference depends on the direction of wave propagation. However, the existence of so-called complete band gaps in properly designed phononic crystals were reported independently [11, 12] in 2-D and 3-D periodic structures. The complete band gap means that a wave with specific frequency cannot propagate in such phononic crystal, and it does not matter what is the direction of propagation inside the crystal [10].

Figure 1.1.2. Kinematic sculpture by Eusebio Sempere consists of a periodic array of hollow stainless-steel cylinders, each 2.9 cm in diameter [9].

The interest in phononic crystals rose significantly through the last decade because of the recent progress in nanofabrication, which allows us to fabricate nanometer scale periodic structures. Those might be useful for the control of the propagation of thermal phonons. At room temperatures, heat in insulators is transferred by phonons at a frequency of around THz, which corresponds to angstrom scale wavelengths. However, at sub-kelvin temperatures, this frequency is reduced to around GHz, which corresponds to nanometer - micrometer size of the lattice constant. This gives us the possibility to fabricate materials with phononic band gaps that will reduce the flow of thermal phonons, and, consequently reduce the thermal conductivity [2, 9]. There are a vast number of applications, especially thermoelectric devices, where this might be useful.

Moreover, it was proven that the width of the band gap strongly depends on materials properties such as the sound velocity and the density; the shape of the periodic inclusions; and the dimensions of the structure [9, 11]. There is still a lot of research to do in order to study properly which parameters yield the widest band gap. For instance, colloidal shape of periodic inclusions produces a wider band gap than cubic ones [11]. Moreover, the calculations reveal that the band gap should be wider in case of 3-D phononic crystal than for 2-D or 1-D crystals [2, 9, 10].

1.1.3 2-D phononic crystals

In 2014 the successful control of heat transport was reported, which was achieved by utilizing 2-D phononic crystals [2]. The authors fabricated two samples with different sizes of periodic inclusions, which formed 2-D phononic crystals. In practice it was realized by perforating suspended silicon nitride membranes into square arrays of circular holes. The smaller lattice constant of 970 nm was designed to have a complete band gap within region of phonons` thermal excitation energy at 0.1 K. The bigger lattice constant was 2425 nm, and it was designed without any band gap. In addition, the thermal conductivity of the sample with continuous silicon nitride membrane was measured. All the rest of the parameters of the last sample were exactly the same as for the first two.

The results of their measurements are presented in Figure 1.1.3. The noticeable reduction of thermal conductivity was observed for the perforated structures comparing to the sample with full membrane. The value of thermal conductivity was found to be strongly dependent on the bath temperature. It worth to notice, that thermal conductivity of the sample with bigger inclusions was lower than thermal conductivity of the sample with smaller inclusions, which was designed to have band gaps. It means that the maximization of the phononic band gap does not necessarily lead to the minimum of thermal conductance [2].
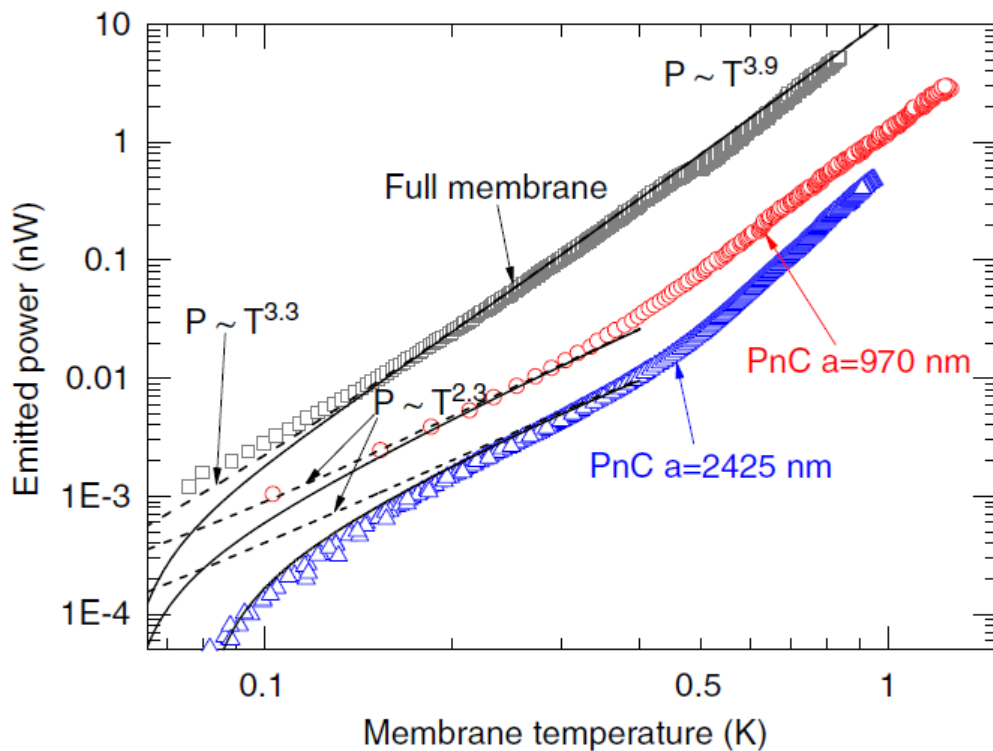

Figure 1.1.3. Measured emitted phonon power versus temperature in 2-D phononic crystals versus unperforated membrane [2].

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1.1.4 3-D phononic crystals

All calculations for 3-D phononic crystals are based on the constitutive equations for macroscopically isotropic media. Hooke`s law for linear elastic media, where the strain-stress relation is obtained reads [13, 14]:

$$\sigma_{ij} = C_{ijkl}\epsilon_{kl}, \qquad with\ i,j,k,l = 1,2,3 \tag{1.9}$$

where σ_{ij} represents the stress tensor, ϵ_{kl} is the strain tensor, and C_{ijkl} corresponds to the elasticity tensor.

By using the specific materials parameters of the media, a theorist from our group, Dr. Tuomas Puurtinen, has solved the vibrational eigenvalue phonon spectrum for a SiO₂ 3-D phononic crystal with the help of finite element method (FEM). It is depicted as a dispersion relation within the first FCC Brillouin zone in Figure 1.1.4.
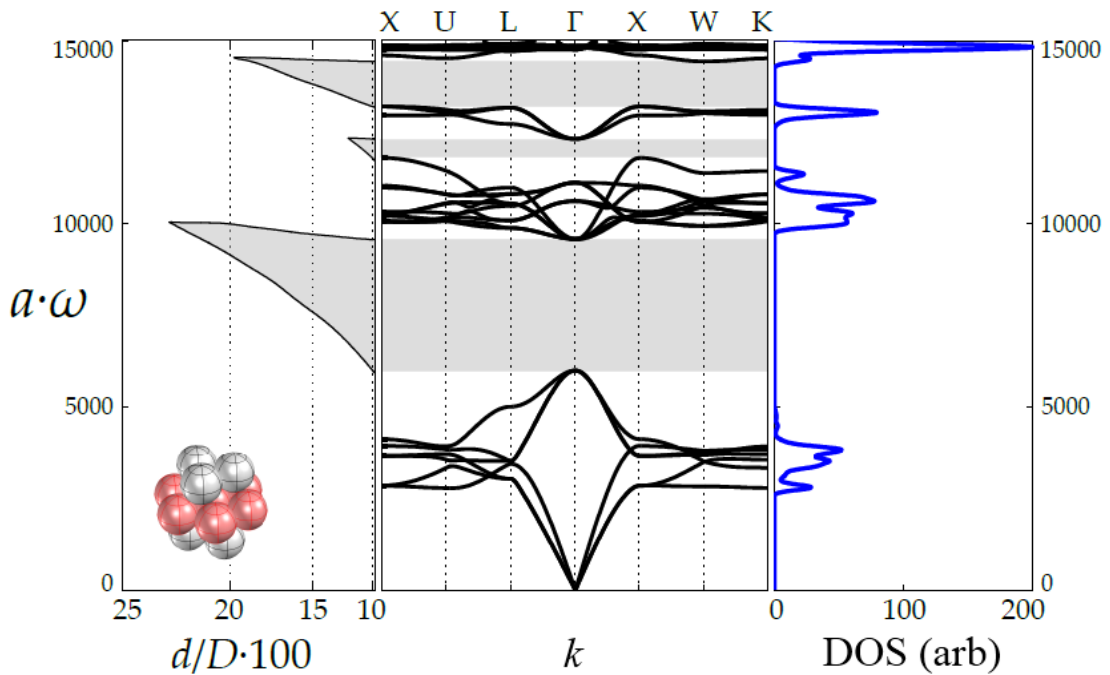

Figure 1.1.4. FEM based calculation of a dispersion relation of a 3-D phononic crystal structure for d/D =1/10. The shaded areas represent band gaps.

However, it is quite difficult to design and to fabricate 3-D phononic crystals. In this figure, all presented units are within System International (SI). Parameters a, ω, k, d, and D correspond to the lattice constant, angular frequency of phonons, the wavevector, the diameter of contact

area between neighboring spheres, and the diameter of spheres, respectively. Silicon oxide spheres were treated as periodic inclusions within a vacuum media in this model. The density of states (DOS) are depicted in arbitrary units, conserving real proportions.

As a result of these theoretical calculations, a few complete band gaps are found to exist, indicating that a noticeable decrease in thermal conductivity should be observed. For a temperature of 100 mK, the thermal phonon wavelength is approximately few hundreds nanometers. Therefore, in order to detect the reduction of thermal conductivity, we should fabricate 3-D phononic crystal nanostructure with lattice constant of the same order of magnitude.

1.2   SINIS Thermometry

In this thesis, in order to measure thermal conductivity of 3-D phononic crystals, normal metal-insulator-superconductor (NIS) tunnel junctions were utilized [15, 16]. In practice, two symmetric NIS junctions were fabricated connected in series, and the resulting structure formed a SINIS structure. The density of states diagram of a NIS junction is depicted in Figure 1.2.1. The functional properties of NIS junctions are observed in consequence of appearance of a gap in the superconductors' excitation spectrum below a critical temperature, and the quantum mechanical tunneling phenomenon. The nature of the superconducting band gap was explained by Barden, Cooper and Schrieffer (BCS) in 1957 [17]. They suggested the creation of so-called Cooper pairs, coupled electrons, which can interact attractively and move through the lattice without dissipation [18].
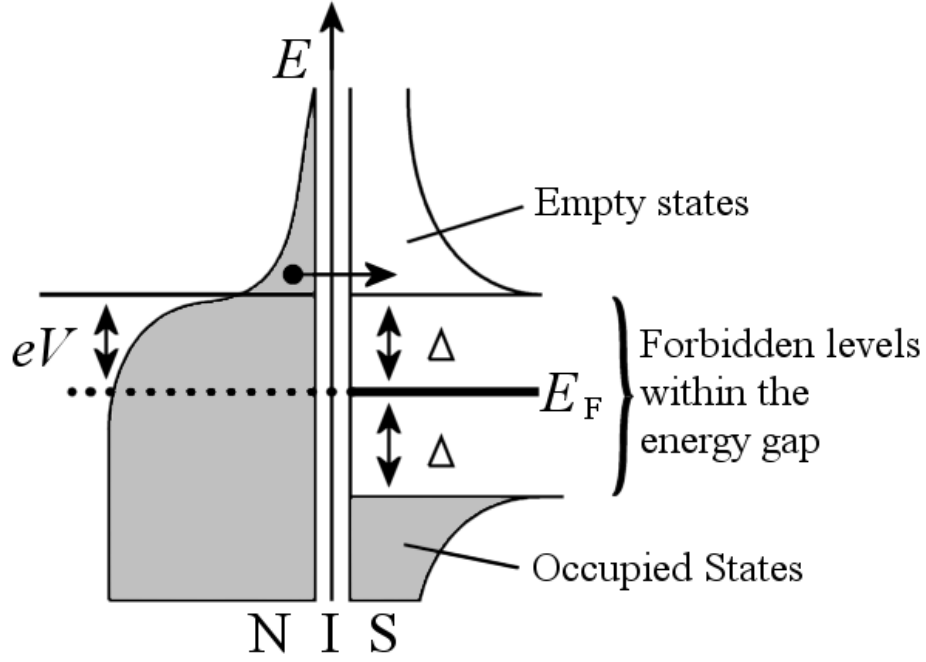
Figure 1.2.1. Density of states diagram (DOS) for normal metal-insulator-superconductor (NIS) tunnel junction with its tunneling mechanism [19].

The density of states of superconductor above and below the gap can be expressed as follows:

$$N_S(E) = N_F \frac{|E|}{\sqrt{E^2 - \Delta^2}},$$ (1.10)

where E is electrons` energy measured from Fermi energy E_F, Δ is the superconductor gap, and N_F is the density of states at the Fermi level, when the sample is in the normal state [20].

Electrons from the tale of Fermi-Dirac DOS distribution can readily tunnel through a thin insulating material in the case where high enough voltage is applied across the junction (V $\geqslant$ Δ/e), in order to have empty states above the energy band gap at the second electrode. However, at non-zero temperatures some "hot" electrons can also tunnel at lower voltages [21]. The tunneling current through a NIS junction, if the constant DOS of normal metal is assumed, can be written as [20]:

$$I_{NIS}(V,T) = \frac{1}{2eR_T} \int_{-\infty}^{+\infty} \frac{|E|}{\sqrt{E^2 - |\Delta|^2}} \cdot [f(E - eV, T_N) - f(E + eV, T_S)] \cdot dE,$$ (1.11)

where $f(E - eV, T_N)$ and $f(E + eV, T_S)$ correspond to the distribution functions for the normal metal and the superconductor, respectively. Here the tunneling resistance can be written in the following form:

$$R_T = \frac{\hbar}{4\pi A e^2 T_N^2 N_F^2},$$ (1.12)

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where A denotes the area of NIS contact. In the case of an ideal symmetric SINIS junction, we have a twice bigger tunneling resistance, which leads to smaller tunneling current:

$$I_{SINIS}(V_{tot}, T) = \frac{1}{2eR_{T,tot}} \int\limits_{-\infty}^{+\infty} \frac{|E|}{\sqrt{E^2 - |\Delta|^2}} \cdot \left[f\left(E - \frac{eV_{tot}}{2}, T_N \right) - f(E + \frac{eV_{tot}}{2}, T_S) \right] \cdot dE \, , (1.13)$$

The traditional view of current – voltage characteristics for NIS tunnel junction is presented in Figure 1.2.2a. It worth noticing, that the tunneling current depends strongly on temperature of electrons in the normal metal, and it does not depend on temperature of the superconductor at all [21]. Based on the I-V characteristics published in literature [2, 19, 20], we can observe the rapid decrease of current at lower temperatures while decreasing the voltage applied to SINIS junctions. Moreover, in the ideal case, at zero temperature the current at bias voltages lower than band gap should be zero; however it is not true in practice. There are few reasons for this behavior. Firstly, because of finite quasiparticle lifetime, the DOS of superconductor is broadened [21, 22]. The broadening parameter severely depends on the purity of the superconductor film. Also, the existence of pinholes in insulating layer, and thermal radiation may affect the broadening of superconducting DOS.

In practice, in order to use SINIS junctions as a thermometer, the dependency of voltage of current biased SINIS versus bath temperature is used (Figure 1.2.2b).
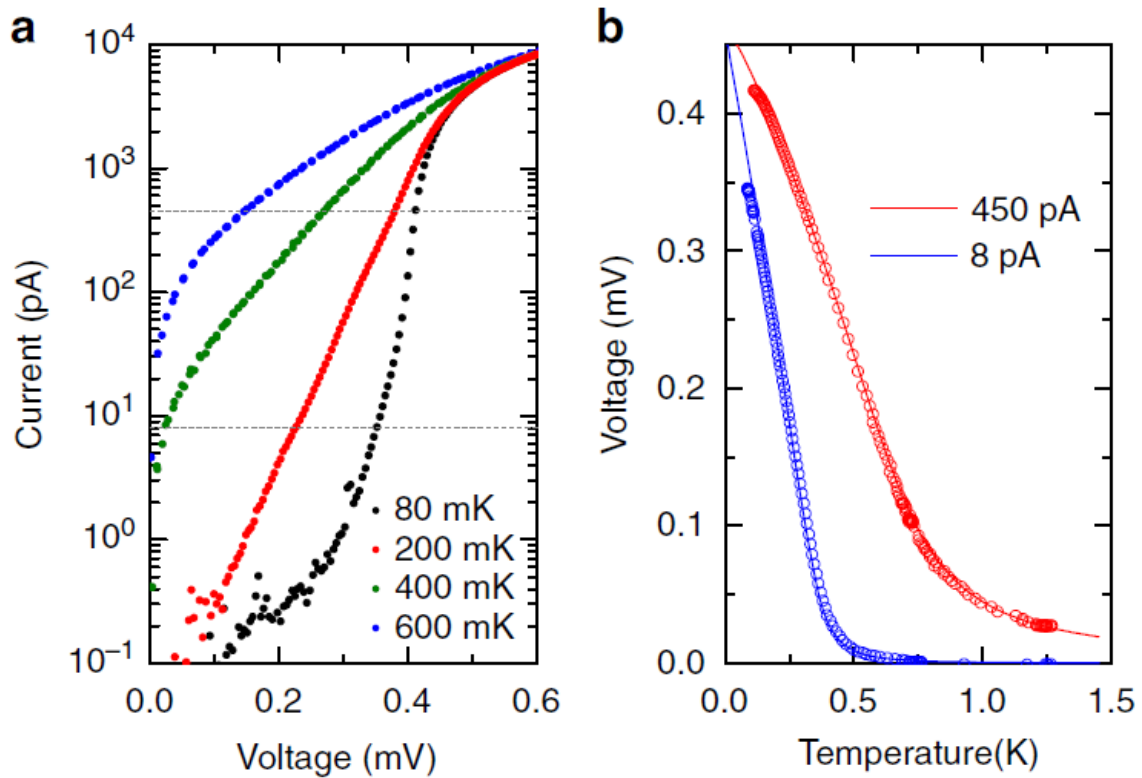
Figure 1.2.2. *(a)* Measured I-V characteristics of SINIS tunnel junctions ($2R_T$ = 43 kΩ) at different bath temperatures, where dashed lines correspond to bias currents applied for *(b)* SINIS voltage – bath temperature response. Solids lines represent the theoretical fit based on BCS theory [2].

We can observe the strong correlation between voltage and bath temperature in Figure 1.2.2b at low temperatures. The working range of this thermometer is limited from above by critical temperature of superconducting material, and by noise heating of the tunnel junctions from below. The latter phenomenon makes the voltage-temperature dependency non-linear and not sensitive to temperature changes anymore.

Based on the I-V characteristics of SINIS tunnel junctions, we can choose the bias current, which should be applied to SINIS junctions for voltage- temperature measurement in order to achieve the biggest voltage response with small changes in temperature. Unfortunately, we cannot cover a wide temperature range with high sensitivity, so, consequently, we should measure the temperature with different bias currents depending on the specific problem.

Chapter 2

Fabrication

In this chapter the detailed fabrication process will be described. All the fabrication was done by using clean room facilities provided by Nanoscience Center, University of Jyväskylä in the years 2015-2016.

The successful fabrication of the sample with 3-D phononic crystals can be divided into four main steps: substrate preparation, deposition of silicon dioxide colloidal nanoparticles, coating its surface with negative photoresist (SU-8), and SINIS tunnel junction deposition. The schematic illustration of the above mentioned fabrication steps is presented in Figure 2.1.
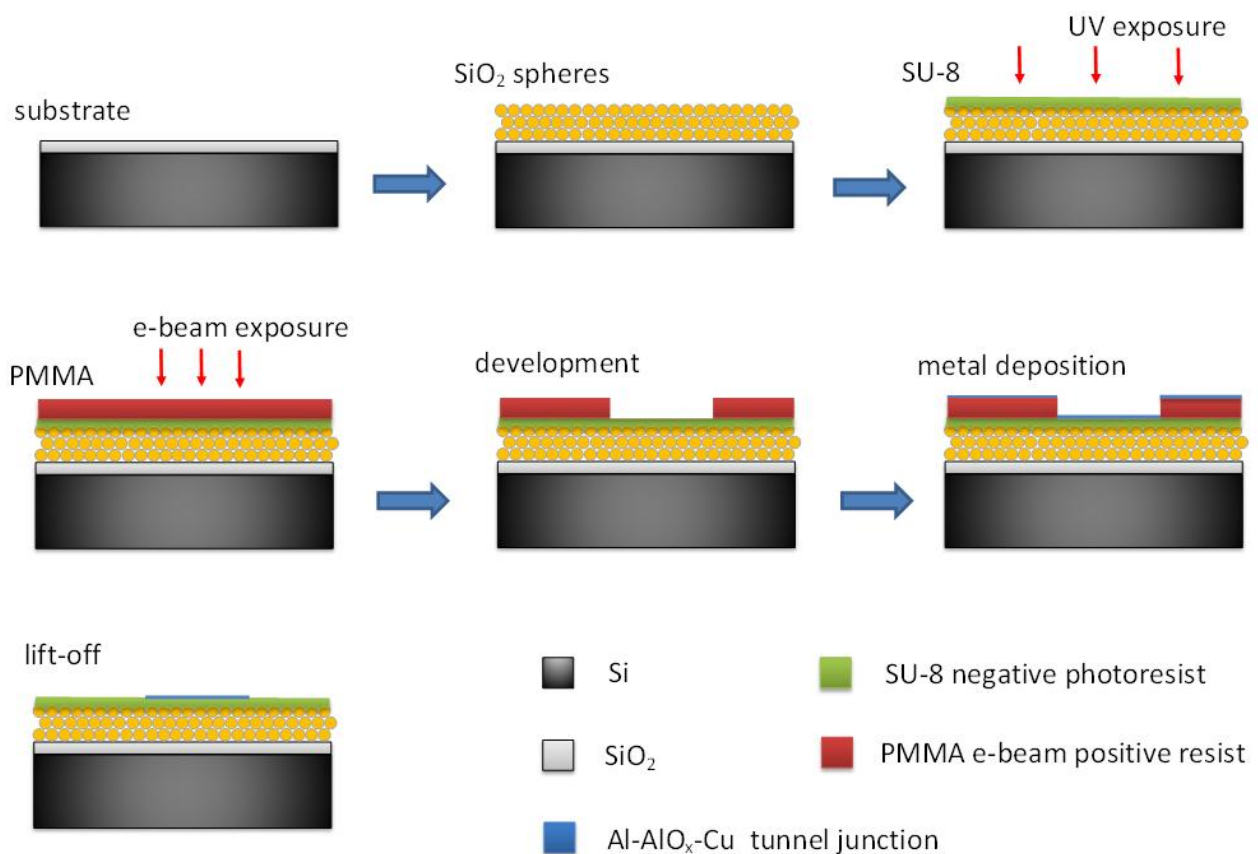

Figure 2.1. Schematic representation of fabrication process of 3-D phononic crystals sample including coating with SU-8, its hardening with UV light, and e-beam lithography on top of this structure.

2.1 Sample preparation

2.1.1 Cutting and cleaning

The fabrication of the sample with 3-D phononic crystals starts with cutting a 500 μm thick naturally oxidized p-doped (with boron) silicon wafer. The initial sizes of silicon pieces are approximately 16 mm in length and 8 mm width. Afterwards, these rectangular pieces are scratched in the middle with the special silicon scribe; however, it is not broken into smaller pieces at this point. Consequently, we have a silicon chip with dimensions 16 mm by 8 mm with a scratch in the middle of the longer side and perpendicularly oriented to that longer side of silicon chip (see Figure 2.1.1). Later we can easily break the chip into two halves exactly along this scratch.
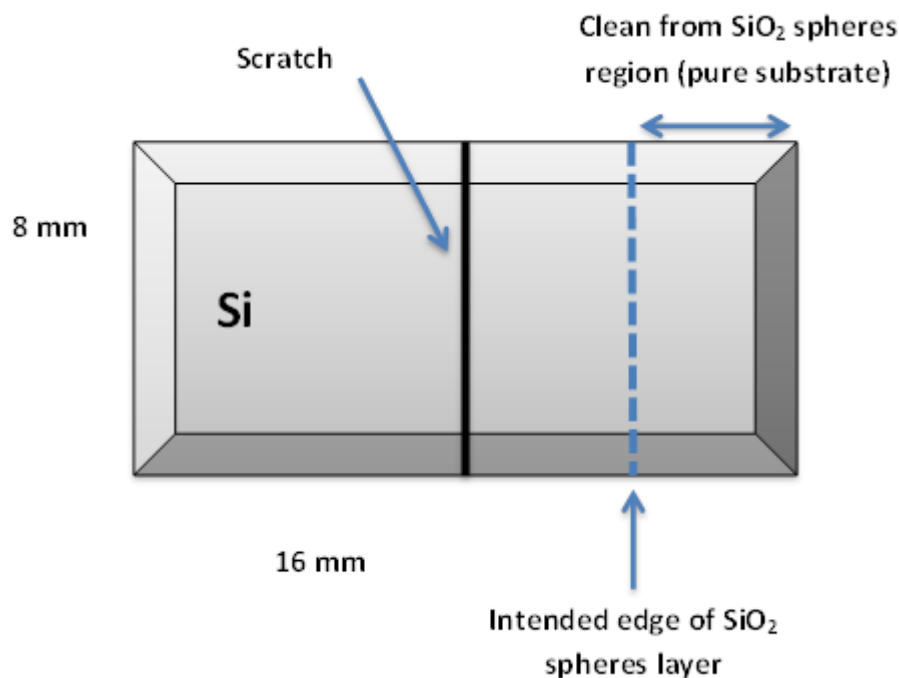

Figure 2.1.1. Schematic representation of the prepared substrate used for 3-D phononic crystals sample fabrication.

This step is usually the dirtiest fabrication step in cleanroom, because it produces lots of silicon dust, which can be easily observed in optical microscope (Figure 2.1.2a). Consequently, the proper cleaning is required. The conventional cleaning during the nanofabrication was utilized, which includes cleaning the substrate at first in hot acetone with additional fiber swiping from both sides of the wafer, in order to remove all soluble organic contamination. Then the substrate was placed into isopropyl alcohol (2-propanol, IPA), and placed into the ultrasonic bath for 10 minutes. This ultrasonic device has a water bath with temperature

control made by FinnSonic. Afterwards, the substrate was dried out by N_2 gas flow. In parallel, the sample stage was cleaned too by swiping it with deionized (DI) water and IPA solution, and then dried too in the same manner as the substrate. The result of the cleaning is presented in Figure 2.1.2b. It worth to mention that it is impossible to conduct a perfect cleaning, and, as a result, there are always some residual impurities on the chip surface, which can later form pinholes. The residual contamination will not necessarily allow the oxide layer to grow on top of the silicon surface, what makes it electrically conductive at these places, and might cause current leakages during measurements.
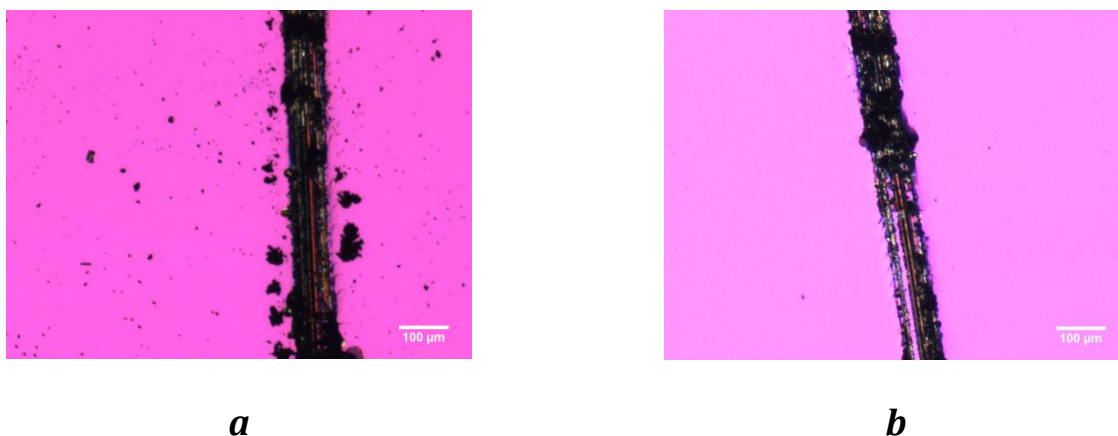

a   *b*

Figure 2.1.2. Silicon based substrate before cleaning *(a)* and right after *(b)*.

2.1.2 RIE oxidation

In order to reduce the electrical conductivity of the naturally oxidized silicon substrate and make it more hydrophilic, oxygen plasma treatment was applied. By using Oxford Instruments Plasmalab 80 system the substrate was bombarded by excited oxygen ions, which penetrated into the substrate`s surface and formed silicon oxide layer. It was proven by measuring the electrical resistance between two different areas on the substrate surface. It revealed that after the oxygen ion bombardment, the substrate`s surface became non-conductive at all. The substrate was treated by oxygen plasma for 120 seconds by applying 200 W of RF power at 40 mTorr.

2.2   SiO₂ nanospheres deposition

As it was mentioned in the previous chapter the SiO_2 nanospheres formed a close-packing FCC crystal structure, therefore becoming a 3-D phononic crystal nanostructure. In this paragraph, the deposition method, which is based on self-assembly is presented.

2.2.1 Self-assembly background

The second law of thermodynamics states that the entropy of an isolated system or in any cyclic process will increase over time or will stay the same. Often entropy is understood as a synonym to disorder or chaos. However, the spontaneous crystallization of hard spheres has been observed in early computer simulations done by [23] in 1960s. The system initially in liquid state with suspended hard spheres formed a crystal structure. It is possible only in the case where the entropy of the ordered system is higher than the entropy of the disordered system? The answer is yes.
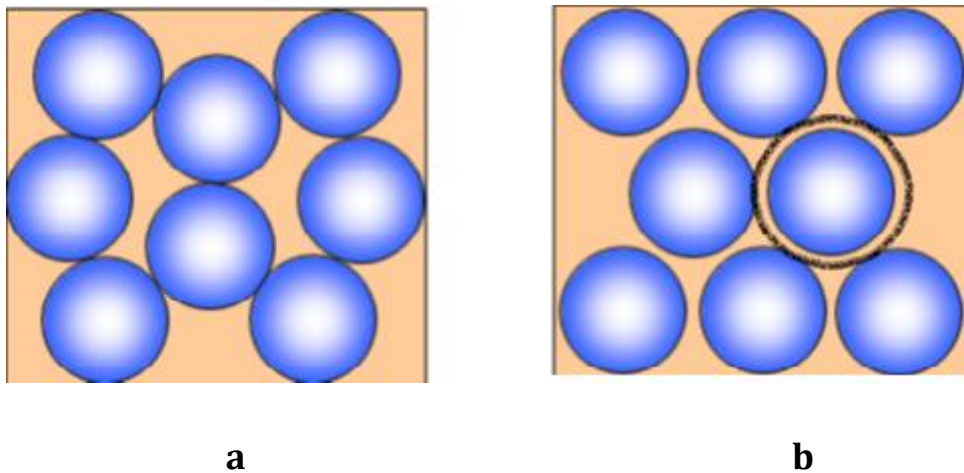

a   **b**

Figure 2.2.1. *(a)* Disordered close-packed structure with "locked" particles and *(b)* ordered structure with space for particles to move around their equilibrium positions [24].

Let us distinguish firstly the configurational entropy S_{cf}, which is defined by the number of possible arrangements of the particles inside certain volume, and the thermal entropy S_{th}, which is defined by the accessible free volume around the particle. For a close-packed structure, which consists of hard spheres, the thermal entropy is practically zero because all particles are locked within certain volume; however, the configurational entropy is large (see Figure 2.2.1a). On the other hand, the thermal entropy of the ordered structure can be non-zero because particles can move around their equilibrium positions [25], but the

configurational entropy is definitely smaller (Figure 2.2.1b). It was proven that for systems where the packing ratio is above $\phi = 49\%$,

$$S_{tot} = S_{cf} + S_{th} \qquad (2.1)$$

the total entropy is larger for crystalline structures, which yields spontaneous crystallization [24, 25].

The above-mentioned hard sphere systems can be created experimentally by utilizing colloidal particles suspended in some liquid. For that reason, we used SiO_2 colloidal particles surrounded by deionized water medium. Moreover, it is important to notice that the self-assembling can happen only for low-concentration suspensions [26] in order to have enough space for particles to relocate and created the crystalline structure. On the other hand, the rate and strength of the formation of the ordered structures is directly proportional to the density of small spheres in this suspension due to Gibbs free energy lowering [24]:

$$\Delta F \approx -\frac{N}{V} \cdot k_B T \cdot \Delta V, \qquad (2.2)$$

where N stands for the number of colloidal particles, V is the accessible volume, T stands for the temperature of suspension, and ΔV is the increase of accessible volume while arranging into close-packing structure by creating, as a result, a crystal lattice structure. To sum it up, the entropic forces are the driving force towards creating the self-assembled crystalline nanostructures.

2.2.2 Single-step vertical deposition

In order to fabricate 3-D phononic crystals, we used SiO_2 colloidal particles suspended in deionized water prepared by Microparticles GmbH. The diameter of these spheres was approximately 177 nm. Suspensions with different particle sizes are also available. The concentration of these nanospheres was 5% by mass. We used a single-step vertical deposition method [27] (Figure 2.2.2) to create a close-packing crystalline structure from these colloidal nanoparticles by utilizing the phenomenon of self-assembly.
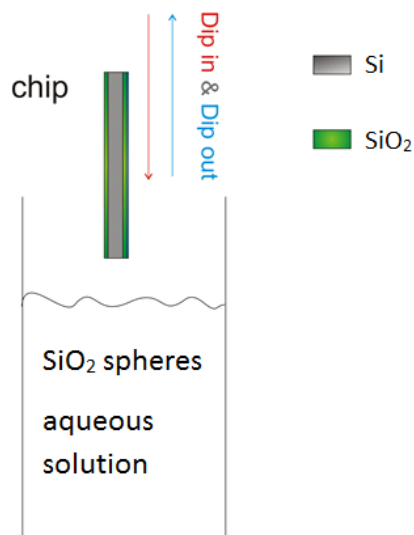
Figure 2.2.2. Dipping setup schematic representation.

Silicon substrate after RIE oxidation was attached to the clamp right above the vessel with the nanosphere suspension and dipped in with the rate of 1 mm/min. After reaching the lowest point, which was set by computer software, the dipping out started immediately. Usually the dipping out rate was set to 0.015 mm/min. However, it was discovered that by changing the dipping out rate, we can control the thickness of the SiO_2 colloidal nanoparticle film. Photograph of the dipping setup is presented in Figure 2.2.3.

Furthermore, it is extremely important to have a hydrophilic surface of the substrate in order to deposit the nanoparticles, due to the suspension in DI water. It was discovered that we were not able to deposit SiO_2 nanosheres as a crystal structure on top of an untreated silicon nitride surface as it is not hydrophilic.

As a result of the dipping, nanospheres are attached to the substrate surface, and form a close-packed crystalline structure during the slow dipping out and drying process. Consequently, by controlling the humidity inside the dipping chamber, we can control the water evaporation rate, which yields different thicknesses of the structure. By setting a high humidity inside the chamber, low evaporation rate is achieved, which leads to thin, well-ordered crystalline structures built by the nanospheres. We set the humidity inside dipping chamber as high as possible, close to 100%, and the suspension concentration was kept constant close to 5% by mass in all experiments in order to control the thickness of the structure only by changing the dipping out rate.
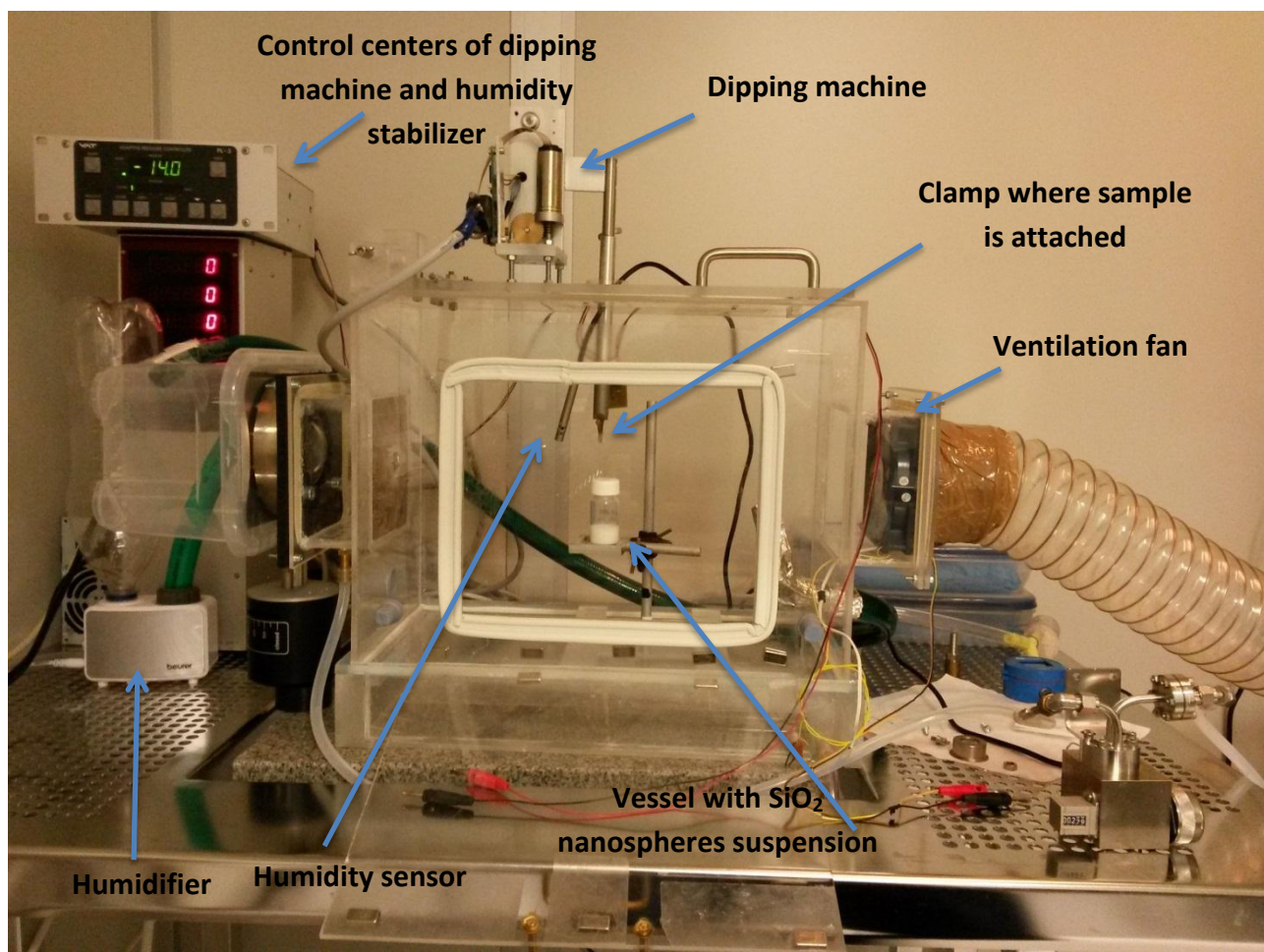
Figure 2.2.3. Home-built humidity controllable dipping setup for self-assembled nanoparticles deposition.

2.2.3 Dipping results

After the dipping process was finished the sample was taken out of the dipping chamber and gently broken along the scratch, fabricated during the first step of the fabrication. As a result, we obtained an approximately 8 mm by 8 mm silicon oxide chip, half of which is covered with deposited SiO_2 colloidal nanoparticles. The first reason for using this approach is due to the limitations in size of the sample stage, which can be mounted to a ^{3}He-^{4}He dilution refrigerator, providing us with the possibility to conduct thermal conductivity measurements. Secondly, we were not able to contact wires between the contact pads located on the sample area with SiO_2 nanospheres, and the sample stage by utilizing the ultrasonic wedge bonder F&K Delvotec 5432. The bonding device uses a thin aluminum wire as a conductor, and the bonding process for the wire requires applying some force and ultrasonic power to melt it.

Consequently, the needle, from which the aluminum wire is supplied, penetrates the deposited SiO₂ colloidal nanoparticle structure readily and breaks it. In order to prevent the sample from this damage, we designed the sample in such a way to leave part of the chip clean and smooth, just a clean silicon oxide substrate, where we can easily bond the aluminum wires.

The deposited silicon oxide nanospheres were imaged by applying a scanning electron microscope (SEM), in particular, the Raith e-Line system. The top view of a structure is presented in Figure2.2.4a. Moreover, the roughness of nanospheres surface was checked by utilizing atomic force microscope (AFM), in particular, the Dimension 3100 AFM. The image obtained by AFM is depicted in Figure 2.2.4b.
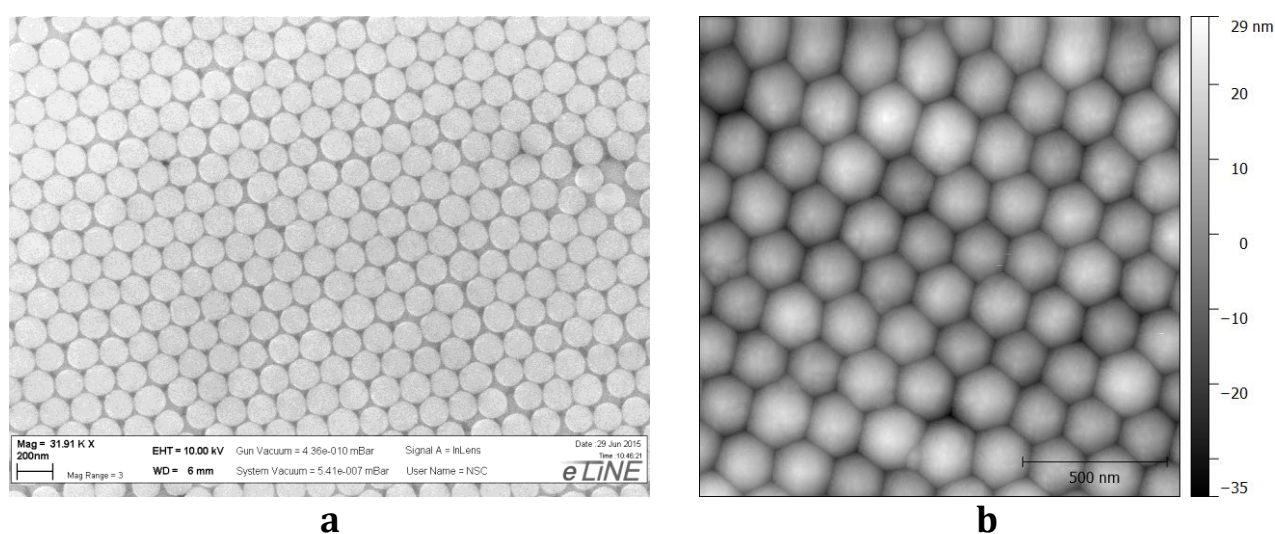

a

b

Figure 2.2.4. Top view SEM *(a)* and AFM *(b)* images of self-assembled SiO₂ colloidal nanoparticles structure.

It is easy to notice the creation of the self-assembled crystalline structure, which is close to FCC lattice structure as it was predicted. However, defects can be also observed. The main cause for these defects is probably the presence of contaminations (small dust particles), which destroys the perfect crystalline lattice. During the theoretical simulation of a 3-D phononic crystal, we assumed touching spheres, but in Figure 2.2.4a there are some regions where the particles are barely touching each other, or even not at all. Here it worth to mention that the nanospheres are made from silicon dioxide, which is non-conductive material, as well as the substrate underneath. All this causes charging effects due to scanning electron microscope, which utilizes electrons for imaging. They charge the nanospheres negatively, and, as a result, the elecrostatic repulsion force between the spheres appears. Even during the imaging it was possible to observe movement of nanoparticles in opposite directions from each other in the region where the electron beam was focused.

On the other hand, there are no charging effects in AFM imaging (Figure 2.2.4b). We can observe an almost perfect crystalline structure built by SiO_2 colloidal nanoparticles. By having AFM images, we can make conclusions about the roughness of the surface. The average roughness of close-packed nanospheres surface is approximately 40÷50 nm, which is expected from the known particle size. This level of roughness makes it difficult to fabricate tunnel junctions on top of this structure for thermal conductivity measurements. However, we will discuss this issue in the following paragraphs.
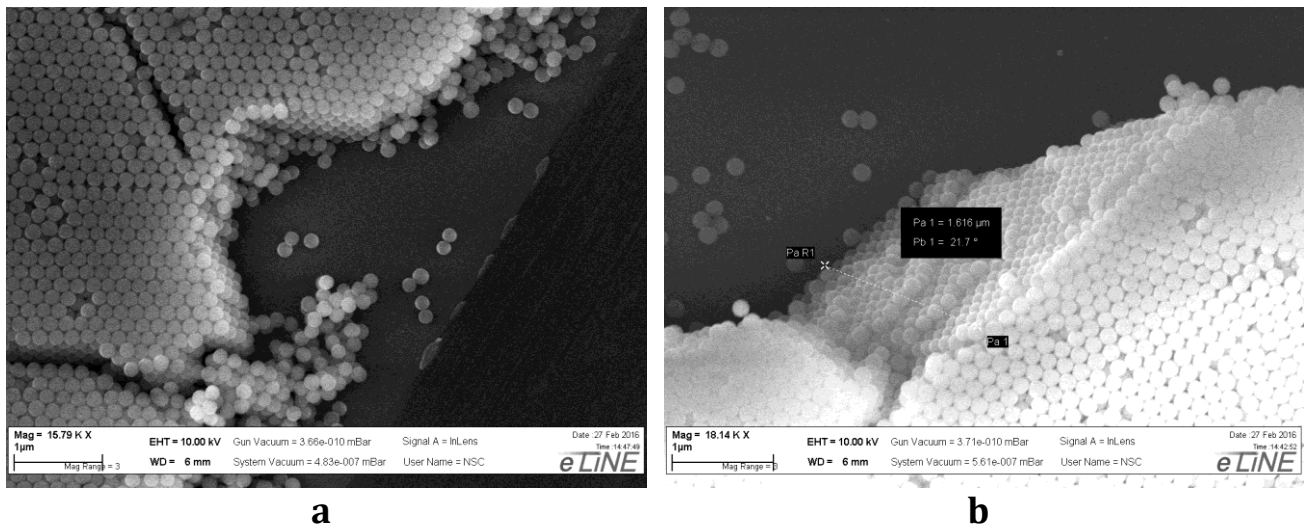

a   **b**

Figure 2.2.5. Cross section SEM images of self-assembled SiO_2 colloidal nanoparticles structure.

In order to check the thickness of the fabricated structures a small delicate scratch was made with the help of a scalpel. Afterwards SEM imaging near the scratch was done. Structures with different thicknesses are depicted in Figure 2.2.5. They were obtained by using the same silicon substrate after oxygen plasma treatment and keeping the suspension concentration near 5% by mass and humidity level at almost 100% constant. The only parameter, which was changed, was the dipping out speed. In order to obtain the thickness around 10 layers of SiO_2 colloidal nanoparticles, the dipping rate was 0.015 mm/min (see Figure 2.2.5a). A crystal with thickness around 20 layers of SiO_2 nanospheres was obtained when the dipping rate was set to 0.01 mm/min. In addition, the thickness of these structures are not necessary the same everywhere on the chip, it might be thicker on one edge and thinner on another. However, this diversity is not huge, at most up to a few layers, so it should not affect the band structure of phononic crystal.

We have tried various dipping out rates keeping all the rest of the parameters constant and measuring the thickness of the deposited structure. The plot, which represents the dipping

speed – thickness correlation is presented in Figure 2.2.6. This dependency was fitted by the following formula:

$$y = ax^b, \tag{2.3}$$

with parameters $a = 3.80758 \cdot 10^{-4}$ and $b = -2.36786$. The fitting was done by taking into account the approximate dispersion of the thickness of the SiO_2 nanospheres film fabricated at the same conditions, which was observed in numerous samples.
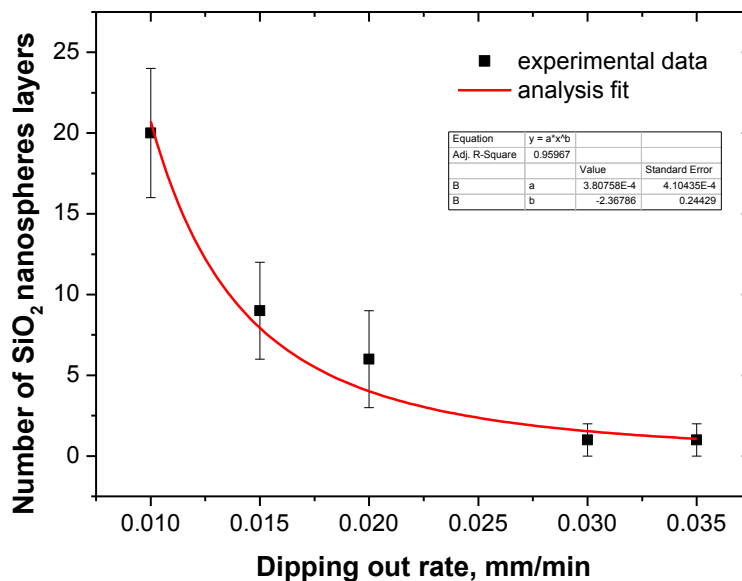

Figure 2.2.6. Thickness of the deposited SiO_2 colloidal nanoparticles structure depending on the dipping rate.

2.3 Coating of SiO_2 nanosphere surface

At this point in fabrication process, we have successfully fabricated 3-D phononic crystals, from SiO_2 colloidal nanoparticles, located on silicon dioxide substrate. The next step is to conduct thermal transport measurements. For that reason we need to fabricate a heater and a thermometer on top of the phononic crystals, which are suitable for low temperature measurements. We decided to use NIS (normal metal-insulator-superconductor) tunnel junctions for this purpose. These tunnel junctions are created by a thin superconducting metal separated by few nanometers thick insulator from a thin layer of normal metal. Conventional

NIS tunnel junctions are somewhat fragile, and they cannot be fabricated on top of a rough, bare nanosphere surface.

2.3.1 PVD, CVD, ALD coating

We realized the necessity to coat the silicon dioxide nanoparticles surface with thin layer of smoothening material, which allow us to fabricate the working tunnel junctions on top of it.

First, we tried to utilize a physical vapor deposition (PVD) method, e-beam evaporation, by coating the sample surface with thin layer of Al_2O_3 and, afterwards we also tried another material - SiO_2. In order to make the surface smoother we put the sample onto a rotating platform.
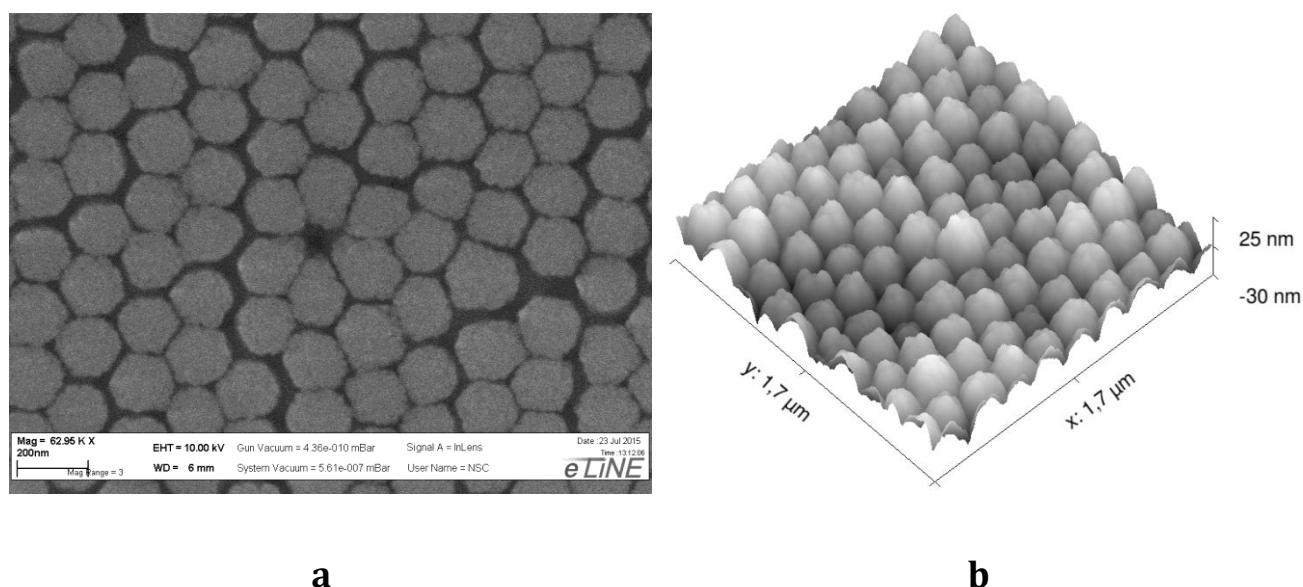
a

b

Figure 2.3.1. SEM *(a)* and AFM *(b)* images of SiO_2 colloidal nanoparticles coated with 60 nm of SiO_2 deposited on rotated sample tilted at 60° to the incident molecular beam by PVD.

This platform was set at different angles to the stream of evaporated molecules from the crucible filled with a specific material. For PVD coating, we used the electron beam evaporator "Balzers". In Figure 2.3.1a the scanning electron microscopy image of the sample surface coated with 60 nm of SiO_2 is presented. We can observe the appearance of grainy structure on the sphere surfaces, and small changes in their dimensions. The nanoparticles are also separated a little from each other due to the charging effect. In Figure 2.3.1b, the AFM image of the same surface is depicted. It was revealed that the roughness of this surface was reduced in two times, to roughly 20÷25 nm. Following coatings with thicker layers (up to 200 nm) did

not affect the roughness anymore. The smallest value of average roughness, which was achieved by changing angles and thicknesses of the evaporated material, reached 14 nm. This result seemed to be reasonable to start the fabrication of tunnel junctions on top of the coated sample.

In Figure 2.3.2 the SEM images of the NIS tunnel junctions fabricated on top of coated surface are presented. The final step of the electron beam lithography, which was used to fabricate NIS junctions, is lift-off, when the residual resists and metals on top of them are removed by acetone. After this step some random parts of the structure with its coating layer were easily detached from the substrate. This happened for coatings using PVD or CVD (chemical vapor deposition) methods, no matter which material was used as the coating.
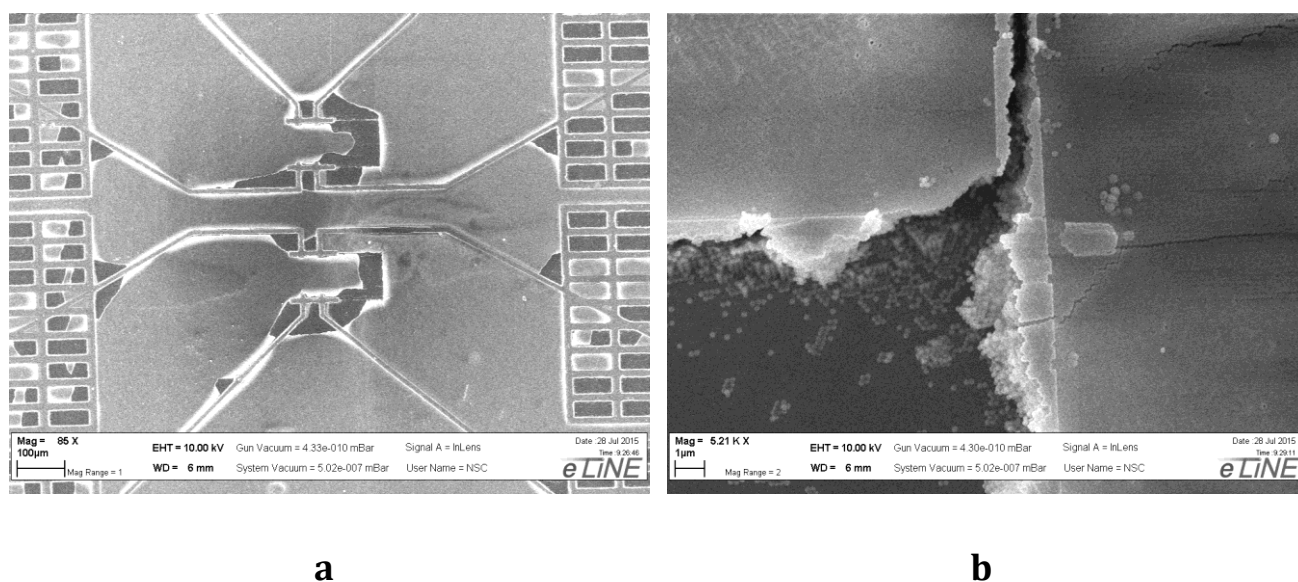

a   **b**

Figure 2.3.2. SEM images of the sample coated with 60 nm of SiO_2 by using PVD after lift-off.

We believe that the reason of such behavior is due to the high deposition temperature of the coating materials. The usual deposition temperature for silicon dioxide coated by chemical vapor deposition method (CVD) is 300 ℃. The deposition temperature by PVD method can be even higher due to necessity to melt and evaporate the material. As a result, high temperatures deposited films will induce stresses on the surface of the structure, because of thermal contraction. Thus, this phenomenon yields detachment of self-assembled nanospheres from the substrate surface as they are not "glued" to it very strongly.

Moreover, we tried the atomic layer deposition method (ALD) to coat the SiO_2 colloidal nanospheres surface with thin layer of Al_2O_3 (up to 120 nm). The lowest possible deposition temperature for this method was 50 ℃. In this case, the final structure was not detached so

readily. On the hand, due to equal coverage of all spheres, the roughness by applying ALD coating method did not change a lot comparing to clean nanopheres surface, which still did not allow us to succeed in fabrication of the working tunnel junctions on top of this structure.

2.3.2 SU-8 negative photoresist

For the above reasons, we started looking for other methods, which can solve this issue. We decided to use SU-8 negative photoresist, which initially in liquid state can be used for coating the rough surface, and after an UV exposure becomes hard and stable to harsh chemicals required for lift-off process. By diluting it with cyclopentanone, different thicknesses of the coating layer can be obtained. It was found that 800 μl of negative photoresist SU-8 resin from Microchem diluted with 2 ml of cyclopentanone yields in 28.6% concentrated by volume SU-8 photoresist (the row Microchem SU-8 photoresist solution was considered to be 100% concentrated), which can smoothen the colloidal nanoparticles surface almost perfectly.

After preparation of the solution with correct concentration, the sample chip, half of which was covered with SiO_2 nanospheres, was spin-coated with this 28.6% concentrated negative photoresist at 4500 rpm for 60 s. Afterwards it was dried for 3 minutes at temperature close to 100 ℃. The next fabrication step is depicted in Figure 2.3.3. By exposing negative photoresist to UV light we harden it, and, consequently, the exposed regions will be impossible to remove by casual chemicals, which are available for simple UV and e-beam lithography, including acetone. However, we should leave the area without nanospheres clean from the photoresist layer, because photoresist is also too soft material for the bonding of connection aluminum wires to the sample stage.
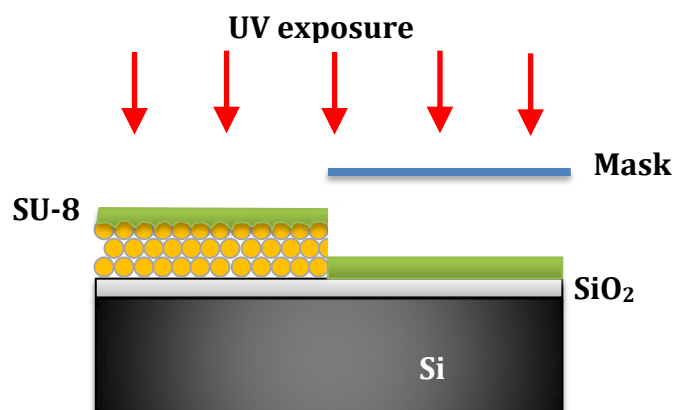
Figure 2.3.3. Coated with negative photoresist SU-8, the sample is exposed by UV light. Region without SiO_2 colloidal nanoparticles is shadowed by the mask.

For that purpose, a contact UV mask was designed to cover half of the sample and not allow the UV light to expose the area underneath. In practice it was a copper foil with an opening window with dimensions close to 8 mm by 4 mm. This window was adjusted by eye to be positioned roughly above the area with SiO_2 colloidal nanoparticles, and the rest of the sample was covered with approximately 0.5 mm copper foil. After that, by using the home-built UV lamp, the sample was exposed to UV light for 7 minutes. Then, it is important to hard bake the sample with the exposed SU-8 photoresist at temperature close to 100 ℃ for 4 minutes. Afterwards, the non-exposed negative photoresist was removed by dipping the sample into a crucible with boiling acetone for 5 minutes. Then, it was washed with the help of isopropyl alcohol (2-propanol, IPA), and gently dried out with light stream of gaseous nitrogen.

As a result, the most suitable thickness of negative photoresist SU-8, which corresponds to 28.6% concentrated SU-8 solution, was approximately 250 nm. Coating with thinner SU-8 photoresist layers were tried as well, however the roughness was still too high eventually. Inspection was done with the help of AFM. The AFM image of such a structure is presented in Figure 2.3.5. Most of the sample is smoothly coated with the photoresist layer; however, a separation line between neighboring nanosphere areas is still present. These cracks appear always during self-assembly where drying processes are involved, and they are unavoidable [3]. In Figure 2.3.4 the AFM image with its roughness plot of another sample before SU-8 coating are presented.

During the self-assembly, nanoparticles form a domain structure separated by cracks (see Figure 2.3.6). Recently, the size distribution of these domains created by single-step vertical deposition of multi-layer polystyrene colloidal crystals was studied [3]. They revealed that this size distribution follows a log-normal distribution by counts. Moreover, the size of the

domains is bigger for smaller dipping out rates (see Figure 2.3.7). It means that for smaller dipping rates, the number of cracks should be lower. That is why we kept the humidity inside the dipping chamber as high as possible, which gave us possibility to use the lowest possible dipping rate in order to achieve the same thickness of the structure with smaller number of cracks.
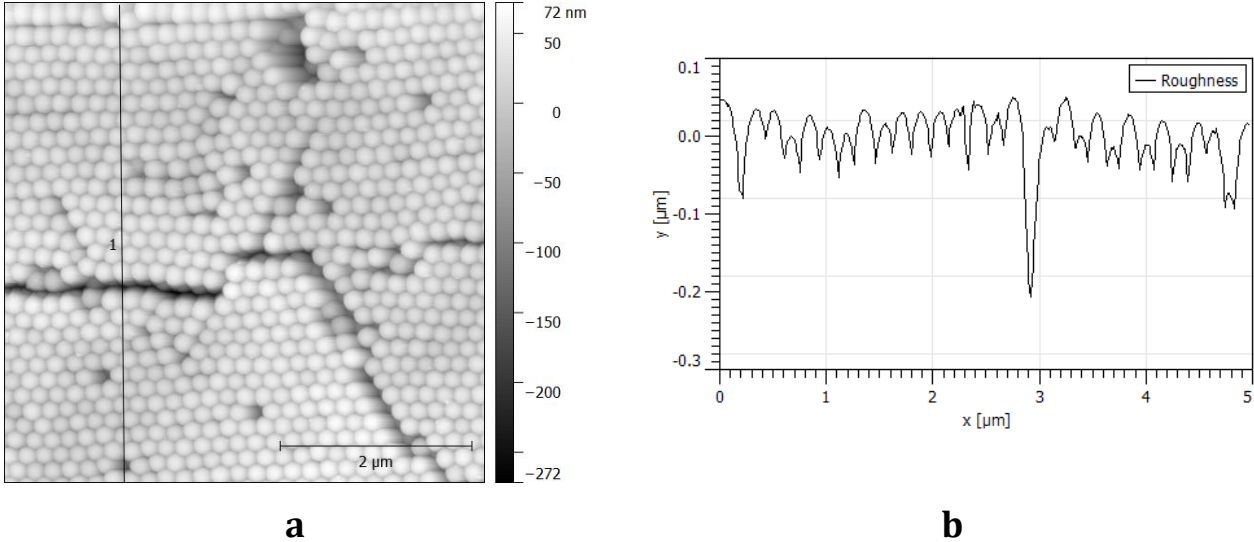

a   **b**

Figure 2.3.4. *(a)* AFM image of SiO_2 colloidal particles structure`s surface before coating with negative photoresist SU-8 and *(b)* its roughness plot along the black line depicted on the AFM image.
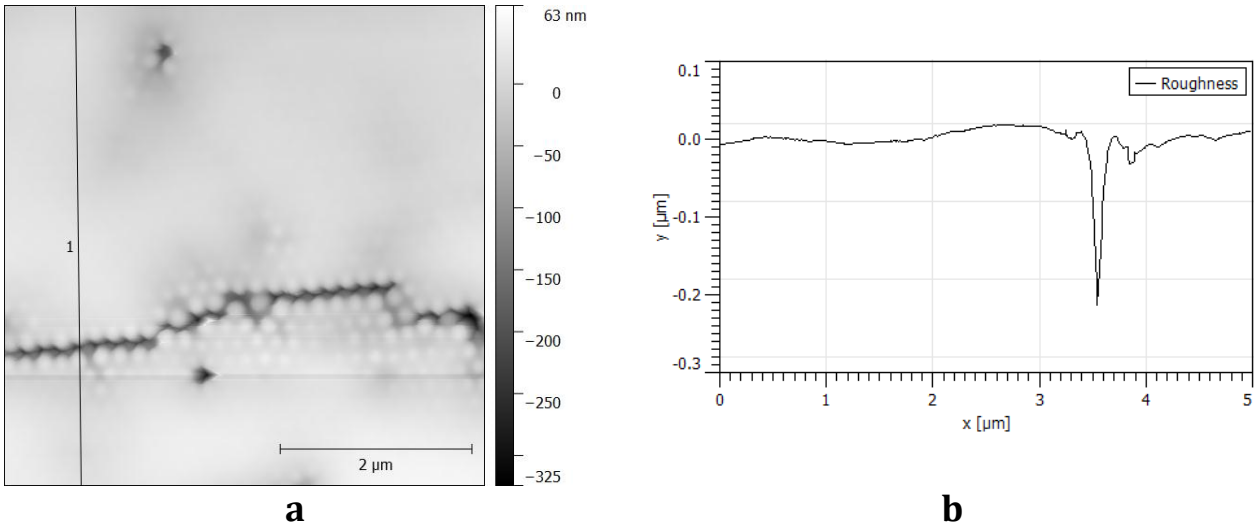

a   **b**

Figure 2.3.5. *(a)* AFM image of SiO_2 colloidal particles structure`s surface after coating with approximately 250 nm of negative photoresist SU-8 and *(b)* its roughness plot along the black line depicted in the AFM image.

During our research it was found that the number of cracks also depends on the thickness of the silicon dioxide nanospheres structure. By fabricating thinner structures, the number of cracks was reduced drastically. As a result, we were successful in fabrication of 3-D phononic crystals by coating the surface with 250 nm thick layer of negative photoresist, with working NIS tunnel junctions on top of this structure. These 3-D phononic crystals are formed by "thin-medium", up to 10 layers thick SiO_2 colloidal nanoparticle structure. In order to achieve this thickness, the dipping out rate was set to 0.015 mm/min at almost 100% humidity in the chamber and by using 5% concentrated suspension of silicon dioxide spheres in DI water.
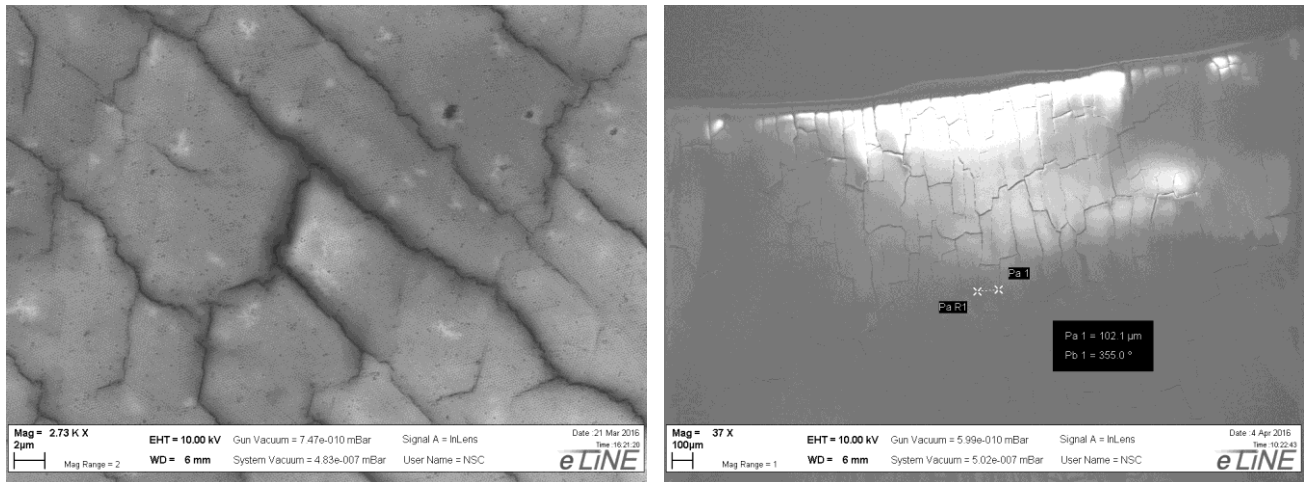
a   **b**

Figure 2.3.6. SEM images of SiO_2 colloidal particles domain structure before coating obtained by setting 0.023 mm/min dipping rate. Typical domain size is 100 μm by 30 μm.

In addition, it is worth to notice that initially in the liquid phase, the negative photoresist SU-8 can penetrate through the holes between silicon dioxide nanospheres, and fill out the medium between the two first layers of self-assembled structure, at most. This might decrease the size of band gap, which was calculated initially for vacuum media between SiO_2 nanospheres. However, the reduction of thermal conductivity should be possible to observe at low temperatures for these structures.
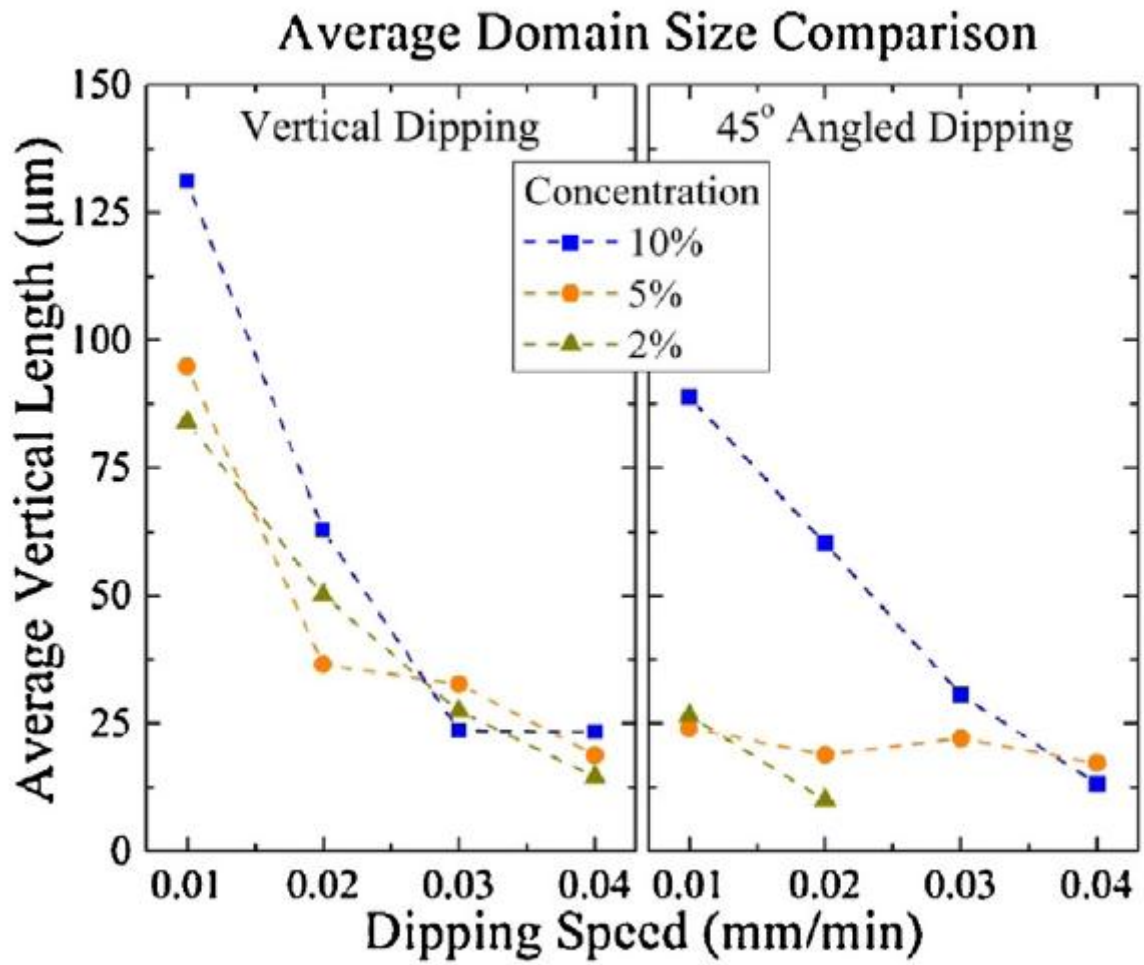
Figure 2.3.7. Average vertical length of domains depending on the dipping speed for vertical and angled single step deposition [3].

2.4   NIS tunnel junctions fabrication

For thermal transport measurements there is a need to have thermometer and a heater. Normal metal-insulator-superconductor (NIS) tunnel junctions can be used as a thermometer at low temperatures and also as a heater due to their unique current-voltage characteristics. Nowadays, they are fabricated in clean room facilities by applying electron beam lithography (EBL), which consists of the following steps: pattern design, photoresists deposition, electron beam exposure, resists development, metal deposition, and lift-off. In this paragraph we will describe all these steps in detail.

2.4.1 Fabrication design

In practice, we fabricated two NIS junctions, which formed a superconducting-insulator-normal metal-insulator-superconductor (SINIS) tunnel junction structure. The pattern, which was used for electron beam lithography is presented in Figure 2.4.1. The size of one NIS junction was designed to be 500 nm by 500 nm (see Figure 2.4.2). One SINIS can serve as a thermometer, and another as a heater. In order to measure the thermal conductivity of the sample as accurate as possible, there should be no contacting wires between the two SINIS, and they should be located as close as possible. In addition, relatively big contact pads should be present to make the eventual bonding to the sample stage possible.
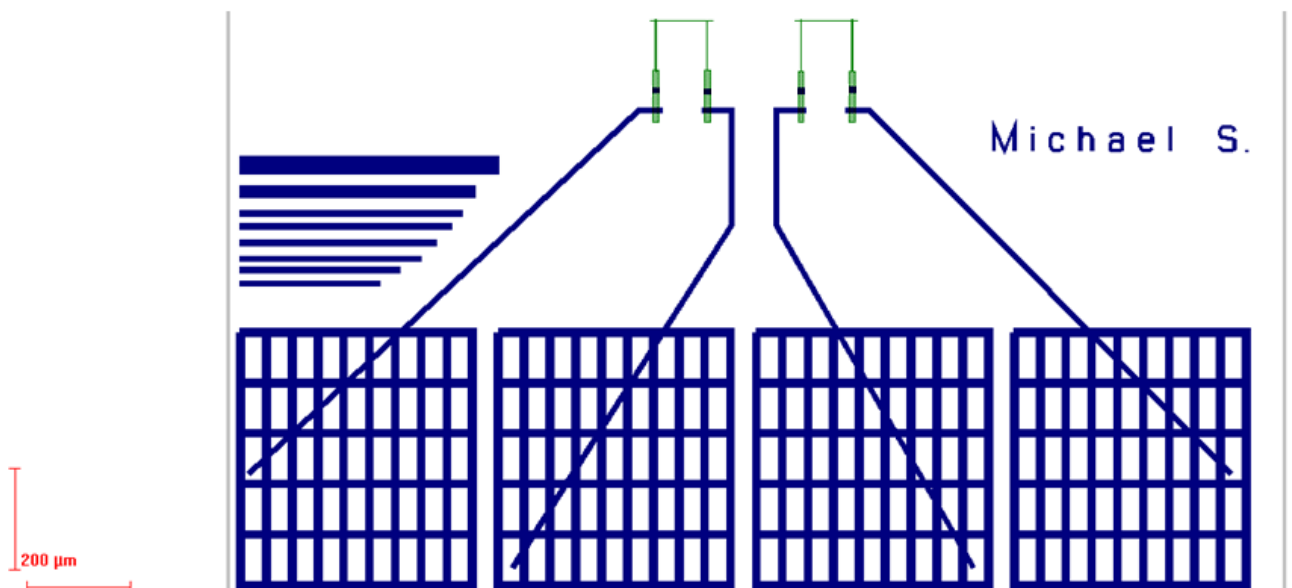

Figure 2.4.1. Pattern of two SINIS tunnel junctions for electron beam lithography.
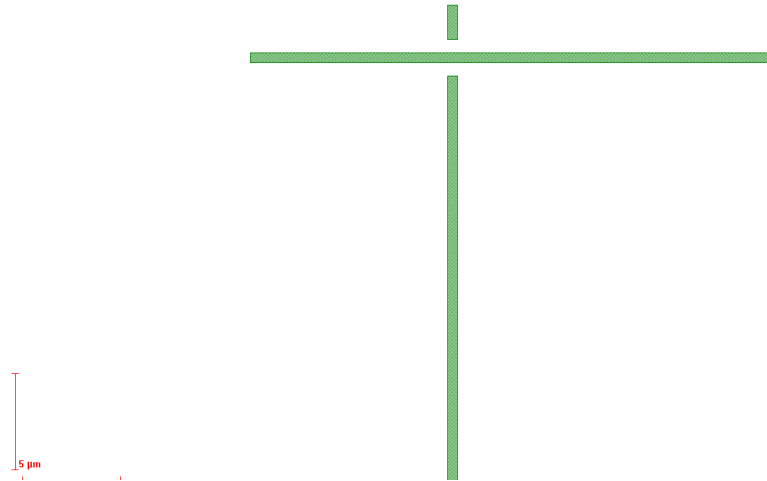
Figure 2.4.2. Pattern of one NIS tunnel junction for electron beam lithography.

Moreover, in the EBL pattern we notice some separate rectangles, which served as the exposure current adjustments at the beginning of electron beam exposure by starting the exposure from these rectangles.

The pattern depicted in Figure 2.4.1 was designed for the angle evaporation method of material deposition. The NIS tunnel junction, which we fabricated, was made of the layer of aluminum, its native oxide, and copper. The aluminum bulk superconducting transition temperature is 1.2 K, and copper stays as normal metal at low temperatures. By depositing two layers of different positive electron beam resists on top of the previously coated and hardened SU-8 sample surface, we can use the shadow metal deposition technique. At the bottom we deposited the copolymer EBL resist, which formed the undercuts after the resist development, due to its higher sensitivity to electron beam exposure than the upper layer electron beam resist. As a result, on the top resist layer shadow bridges were formed, which are the essential part of NIS tunnel junction fabrication.

First, a thin layer of aluminum was deposited at an angle along the vertical green stripe showed in Figure 2.4.1 and Figure 2.4.2. Then, the natural oxide on top of this aluminum layer was formed, which is electrically non-conductive. Afterwards, copper was deposited perpendicularly to the plane of the pattern images. The schematic representation of metal deposition and EBL pattern designing criteria are presented in Figure 2.4.3.

2.4.2 Electron beam lithography

After the design of the pattern for electron beam lithography, the practical implementation fabrication the tunnel junctions can start. First of all we spin-coated the sample`s surface with the EL9 methylmetacrylate copolymer (9% solution of MMA in ethyl lactate) for 45 s at 2500 rpm, what yields in 400 nm thick layer. Afterwards it was baked for 2 minutes at approximately 160 °C. Then, the second layer of resist was spin-coated. For that purpose we used A7 PMMA (7% solution of PMMA in anisole). It was deposited by utilizing the same spinner as it was used as the first resist layer; however the spinning speed was set to 2000 rpm for 45 s, what yields in 600 nm thick resist layer. Eventually the sample was baked for 2 minutes at 160 °C again. With the help of the spinner, the resists were spread uniformly on the surface and baked to allow the resists, which are polymers, to become solid.

The next step of EBL is the actual electron beam exposure. In order to be able to focus the electron beam and to achieve high exposure currents, the corner of the sample was intentionally contaminated with electrically conductive silver nanoparticles.

The EBL was done with the Raith LEO 1430 scanning electron microscope. The beam was focused with zooming in to the impurity particle. It is extremely important to adjust all exposure settings somewhere at the edge of the sample, where the pattern will be absent, because the electron beam exposes resist all the time, even during imaging. By changing the aperture size, the beam current is controlled. The latter one dictates mainly the exposure intensity. Then the program corrections of the sample`s left lower corner coordinates were done to know the position of the chip more precisely, so that it was possible to make an exposure of the pattern exactly where it was needed. After these adjustments, the e-beam was off and set to the destination of exposition. The sample chip had a square shape with length of 8 mm approximately. It means that the structure was exposed near the center of the specimen, where the resist layer is more uniform and cleaner. Then beam was on for a short time to check focus and aperture settings. Formation of the latent image during exposure is a photochemical process, which causes the chain breaking in case of positive resist or crosslinking in case of negative resist.

Due to the fact that the required structure was divided into "smaller" - SINIS tunnel junctions structure (green color lines in Figure 2.4.1 and Figure 2.4.2) and "bigger" – contact wires and pads (depicted by blue color in Figure 2.4.1); it was exposed also by two steps, because the system needs to be reset for different scales. The first one was the "smaller" structure. It was

exposed with magnification of 370, and working area of 512 μm. The beam current was set to 150 pA with area step size of 72 nm. The "bigger" structure was exposed with magnification of 90 and working area of 2048 μm. The beam current was set to 6.8 nA with area step size of 312 nm. It can easily be noticed that for smaller structures the smaller beam current and step size are used, because of higher required resolution. The resist sensitivity, which is defined by the dose factor, was set to 110%. The acceleration voltage for electrons was set to 25 kV and the system vacuum was less than 10^{-5} mbar.

Also, it worth to mention that the additional contact lines with pads (1.8 mm long) were exposed to make the contact pads on the pure silicon oxide surface without negative photoresist SU-8 on top of it. Therefore, two SINIS tunnels junctions were exposed in the middle of the region with coated silicon oxide nanospheres layer by having long contact wires, which ended on the pure SiO_2 surface.

Afterwards, the development of e-beam resists was done. During this process, the exposed parts of the resist are taken away from the structure by dissolving them in a developer. The rest of the resist (unexposed) stays because it has worse solubility properties, which are changed during the exposure process. Firstly, the sample was dipped into a cup with the solution of methyl isobutyl ketone (MIBK) dissolved in IPA with ratio 1 to 3 for 50 s. And then it was washed with a stopper – IPA. The stopper is needed to stop the development reaction and to take out the rest of the developer, because the unexposed resist can be also developed if the time of reaction is long enough. After this step, all the exposed areas were removed, and sharp vertical lines etched through the first resist were left on the sample.

Eventually, the sample was dipped into the second developer, which consists of methoxyethanol dissolved in methanol, for 5 s. And immediately after that it was put into the vessel with the stopper solution (IPA) for 30 s. Then, the specimen was dried by blowing with gentle nitrogen gas stream. The second developer does not affect the top layer of e-beam resist (PMMA). It was done to create the cavities underneath by an isotropic etch of the copolymer resist layer, which was the only sensitive material to the second developer present on the sample. It is extremely important to dip the specimen into the second developer for a short time as it is quite strong etchant for the bottom resist layer.

Before the actual metal deposition, the sample was cleaned by oxygen plasma (RIE) to take off all the residual parts of resist and organic impurities on the sample surface. The name of the chosen program on the control computer was "ELE O_2 Extra soft PMMA", that means low

plasma energy and soft cleaning regime to avoid any damage of the sample with unexposed resist. The specimen was treated by oxygen plasma for 15 s at 30 mTorr and the temperature inside the chamber was 27 ˚C. The RF power was set to 20 W.
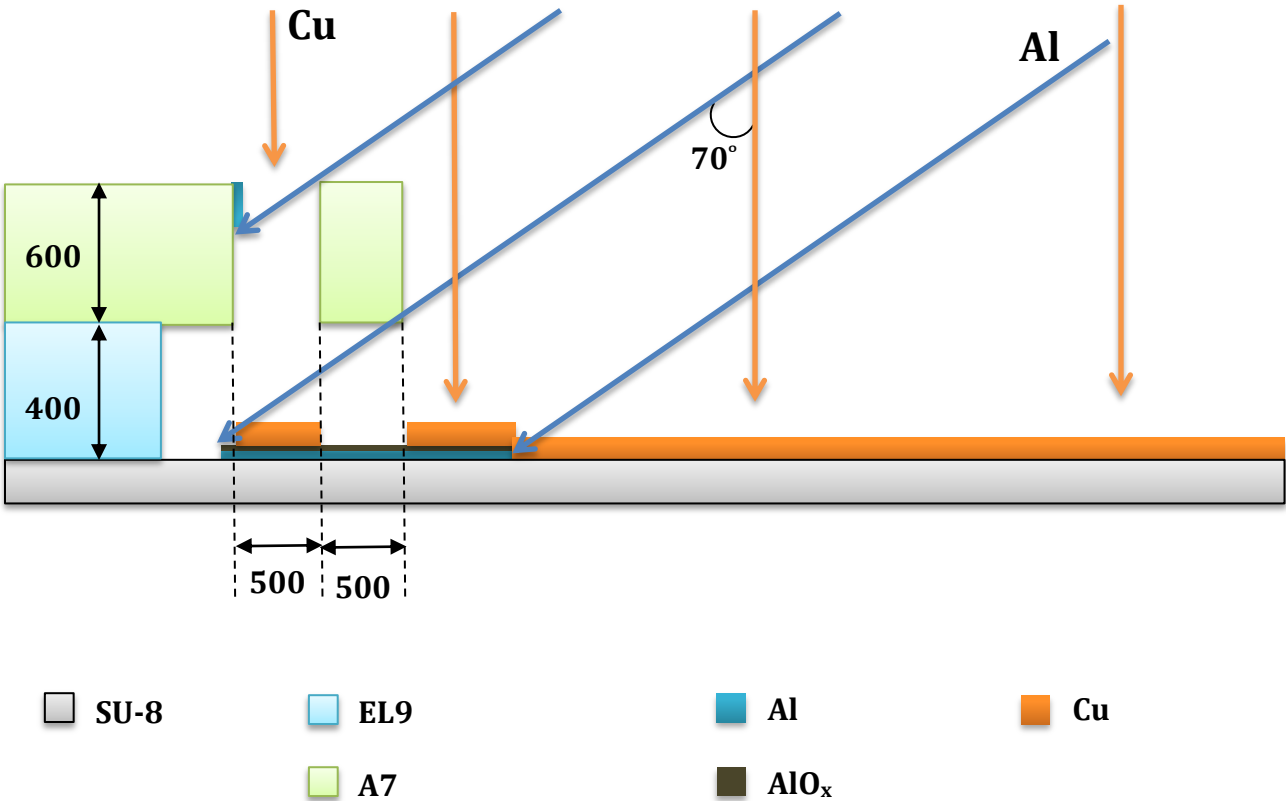
2.4.3 Metal deposition and results

Figure 2.4.3. Schematic representation of metal depositions after the electron beam exposure and resists development.

While designing the pattern for electron beam lithography, few things should be considered carefully. First of all, the chosen thickness of the copolymer resist (bottom resist layer) will affect the aluminum deposition angle. It should be high enough to deposit aluminum under the horizontal green line depicted in Figure 2.4.2. The actual NIS tunnel junction was formed right under this opening after the resist development. In our particular case, by designing the size of tunnel junction to be 500 nm by 500 nm, and the width of the top layer e-beam resist to be also 500 nm, aluminum should be deposited for a distance of more than 1000 nm counting from the beginning of the PMMA resist bridge layer (see Figure 2.4.3). In Figure 2.4.3 the

cross-section along the vertical green line depicted in Figure 2.4.2 is presented with e-beam resists after development.

Secondly, the top e-beam resist layer should be thick enough in order to prevent the formation of aluminum layer on the sample surface from the tunnel junction opening by considering the calculated previously aluminum deposition angle. The aluminum layer, which was formed on the PMMA resist wall, because of the angle evaporation, is depicted in Figure 2.4.3.

Thirdly, the copper layer should be thick enough to cover smoothly without any breaks the step, where pure surface ends and the aluminum layer is already deposited. For that reason the thickness of copper layer should be by approximately 30% thicker than the aluminum layer.

The metal deposition was done with the help of Ultra High Vacuum (UHV) Metal Evaporator (see Figure 2.4.4). It consists of main chamber and loading chamber. The main chamber is quite large (tens of liters) and in an UHV, as a result, it takes many hours to pump it to the required vacuum from atmospheric pressure. It is unpractical to vent and re-pump the main chamber every time when it is needed to change the metal or the sample. The main chamber is used to deposit a thin layer of chosen metal to the sample surface. Firstly, electron beam heats the crucible with metal and, therefore, the atoms are evaporated in UHV chamber due to thermoemission. Then these atoms stick to the sample surface. To make a thin metal layer uniformly spread, the electron beam oscillates near the center of metal source. To make the film deposition clean, uniform and controlled by thickness, there is a need to have ultrahigh vacuum inside the chamber, where particles stick to the surfaces. Also, one of the walls of the main chamber is filled with liquid nitrogen at temperature of 77 K. This all improves the vacuum and cleanness of metal depositions. The latter one is achieved by preventing desorption of metals from chamber walls after previous depositions. The first one is based on the same principle as for cryopumps. The UHV conditions are achieved with the help of a cryopump operated at 20 K.
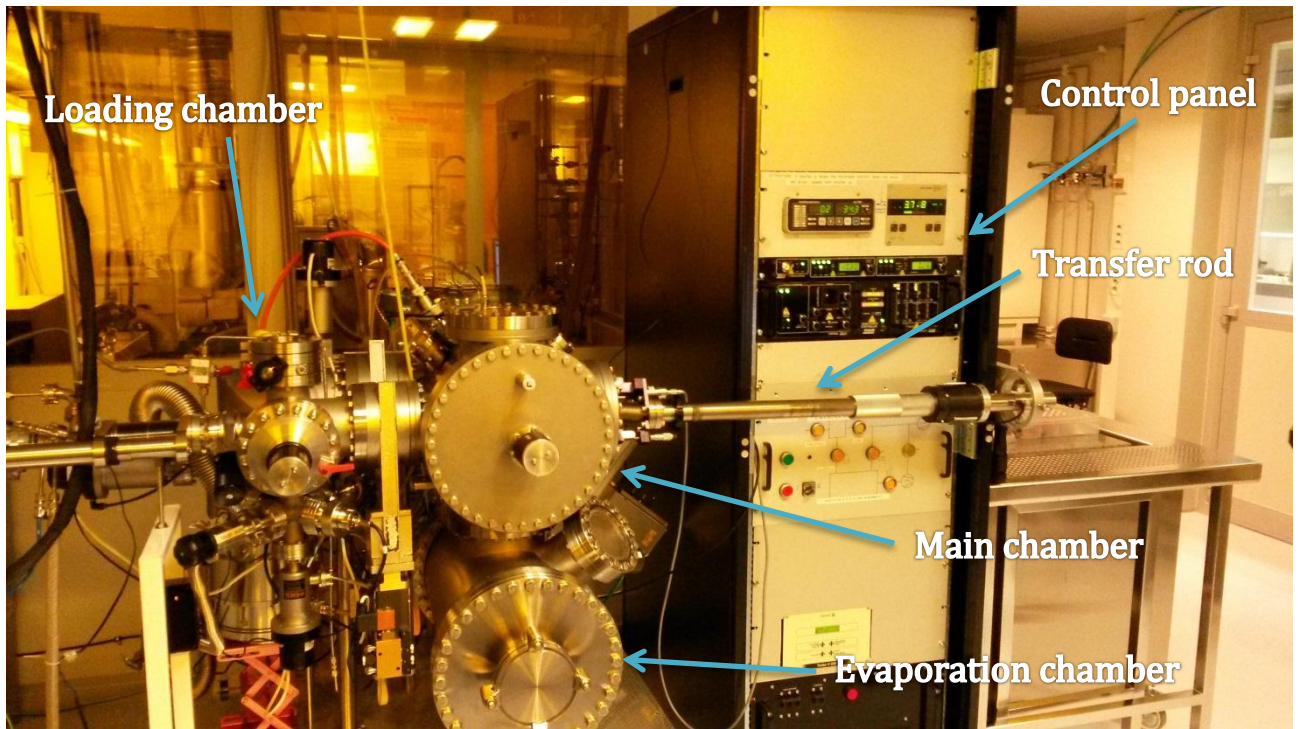
Figure 2.4.4. UHV metal evaporator utilized for NIS tunnel junctions fabrication located in the cleanroom facilities.

The loading chamber is a small chamber connected to the main chamber for loading and unloading samples to the main chamber without lowering the vacuum level in it. It can be disconnected from the main chamber by a gate valve for sample exchange. After the sample is loaded, the loading chamber can be quickly pumped to a pressure lower than 10^{-4} mbar and then connected to the main chamber without decreasing the main chamber vacuum. The gate valve has a safety mechanism that it cannot be opened when the pressure in the loading chamber is higher than certain value to protect the vacuum in the main chamber.

First, 70 nm thick aluminum layer was deposited at the angle of 70°. The rate of deposition was kept to be 0.1 nm/s, because at this rate we have the most uniform smooth aluminum deposition of the sample (atomic evaporation without bulk metal drops). Then, the sample was taken to loading chamber, where by creating a pure oxygen atmosphere for 4 minutes with pressure of $2 \cdot 10^2$ mbar, the aluminum oxide layer was formed. The thickness of this layer is small enough (few nanometers) in order to observe later the electrons` tunneling phenomenon. Lastly, 100 nm thick copper layer was deposited normally to the sample plane also by keeping the deposition rate quite small, around 0.1-0.2 nm/s. During the deposition, pressure in the main chamber was approximately $1 \cdot 10^{-8} \div 8 \cdot 10^{-8}$ mbar.

Finally, the last step of the electron beam lithography is lift-off. During this process the residual resist is taken off and consequently the metals deposited on these parts. It was done with hot acetone that can dissolve the unexposed resist. To make this process faster, usually a mechanical impact is added: with the help of syringe rinsing. However, considering the existence of the SiO₂ colloidal nanoparticles layer on top of silicon chip, we did not use this approach. Thus, the sample was left in hot acetone for 15 minutes, then the acetone bath was changed, and also left for some additional time. Then the specimen with deposited structure was cleaned with IPA and dried with a gentle stream of nitrogen gas.

After all the above-mentioned steps, the sample with the required tunnel junctions was ready. The imaging of the fabricated structures, presented in Figure 2.4.5, was done with the help of Raith eLine Scanning Electron Microscope (SEM) and Atomic Force Microscope (AFM). The acceleration voltage of electrons was set to 6 kV, the aperture size was 30 μm, and working distance was set to 6 mm. To obtain a better image, the scanning speed was lowered and the pixels` information was averaged. It is important to notice that after imaging, the fragile tunnel junctions usually do not work anymore, they become shortened or broken. As a result, the sample, which was used eventually for thermal transport measurements, was not imaged neither with SEM nor AFM.
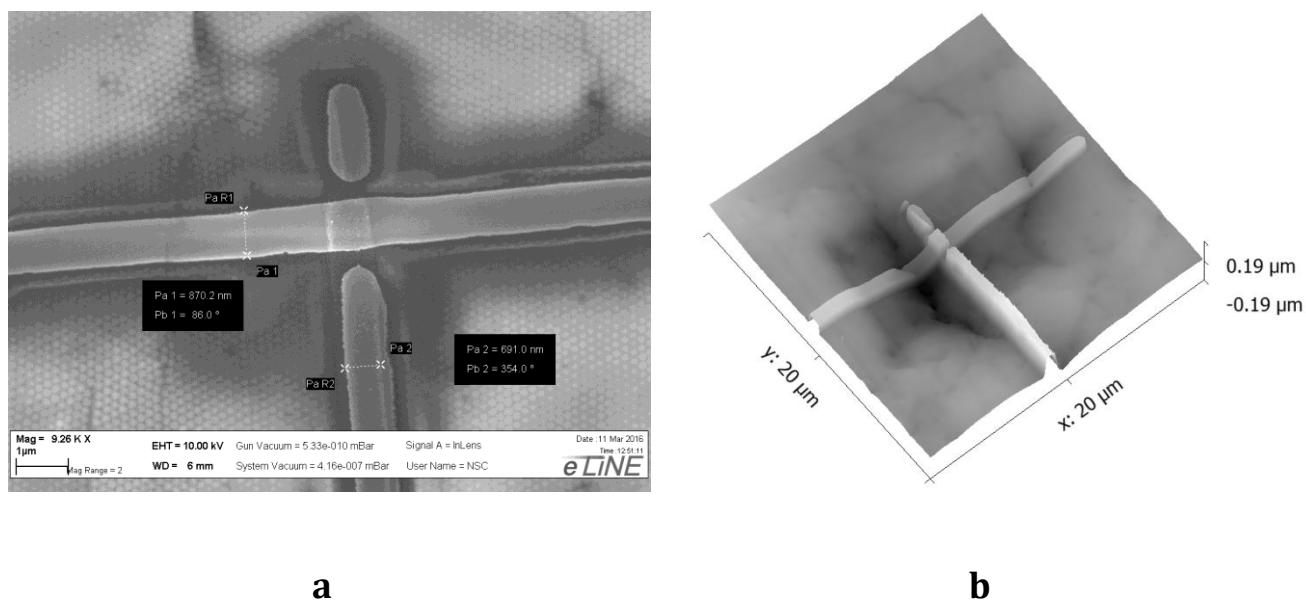

a   **b**

Figure 2.4.5. SEM *(a)* and AFM *(b)* images of the successfully fabricated two different NIS tunnel junctions on top of SiO₂ colloidal nanoparticles layer surface coated with negative photoresist SU-8.
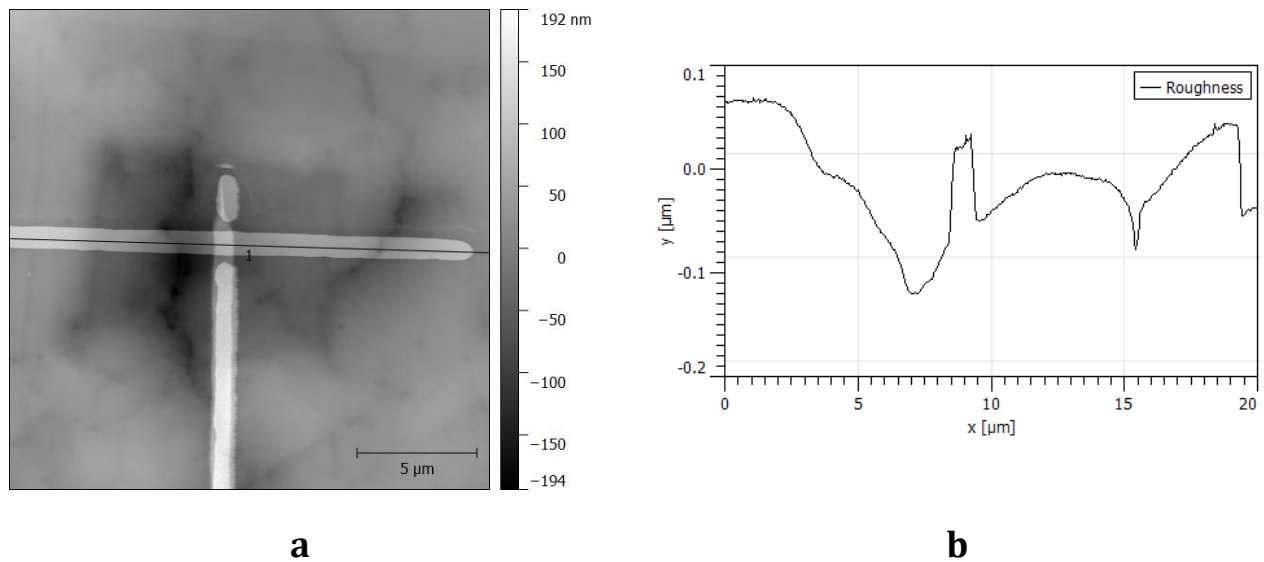
Figure 2.4.6. *(a)* AFM image of the successfully fabricated NIS tunnel junction on top of SiO_2 colloidal nanoparticles layer surface coated with negative photoresist SU-8 and *(b)* its roughness plot along the black line depicted in the AFM image.

In Figure 2.4.5a near the successfully fabricated NIS tunnel junction, an area near the metal lines looks different. This effect is present in some samples due to topography of the sample after the electron beam lithography. The thickness of the negative photoresist SU-8 has thinned nearby the metal wires by approximately 10 nm. We believe that this effect can perhaps be explained by the additional electron beam exposure of the negative SU-8 photoresist, which causes severe over exposure. Another reason might be due to the high temperature of metal atoms during the deposition in the electron beam evaporator. In Figure 2.4.5b and Figure 2.4.6, the roughness of the sample`s surface, on which NIS tunnel junctions were successfully deposited, is explicitly presented. Few cracks can also be seen (darker areas), however they did not cause the damage to the tunnel junctions, which were designed to be thick. Conventional NIS tunnel junctions have the height of approximately 30 nm of Al and 45 nm of Cu, but we fabricated them almost more than two times thicker.

Chapter 3

Preliminary Measurements

After the successful fabrication of a sample with 3-D phononic crystals and two SINIS junctions on top of SU-8 coating, we were able to start preliminary measurements of thermal conductivity. In order to cool down the sample to sub-kelvin temperatures, a ^{3}He-^{4}He dilution refrigerator was used. All the measurements were performed in a shielded room (Faraday cage) to minimize the influence of the environmental electromagnetic noise. First, current-voltage characteristics of the SINIS tunnel junctions were measured at different temperatures. Second, the SINIS voltage response to the bath temperature changes at different bias currents were measured, in order to be able to use later these SINIS tunnel junctions as a thermometer. And, finally, the preliminary thermal conductivity measurements were conducted. However, as a result of our fabrication, we obtained only one SINIS working properly, and another did not show any tunneling effects – it was shorted. So, as a heater we used the shorted SINIS, which showed Ohmic behavior.

3.1 SINIS tunnel junctions measurements with DC bias

After the fabrication of the sample it was taken out to the measurement laboratory. First, the sample was glued to the copper sample stage, which can be mounted to the cryostat, with the help of GE-IMI 7031 varnish diluted with methanol. Then, by utilizing the ultrasonic wedge bonder F&K Delvotec 5432, the sample was electrically connected to the sample stage. Thin aluminum wires were bonded to the regions on the chip`s surface, where contact pads were deposited after electron beam lithography, which were located on the pure silicon dioxide substrate. The second ending of these thin aluminum wires were connected to the copper sample stage.

Afterwards, the sample stage with the bonded sample was mounted on a ^{3}He-^{4}He plastic dilution refrigerator. The cool down was done gradually. First the cryostat was cooled by liquid nitrogen to 77 K. Then it was dipped into vessel with liquid helium at 4.2 K. The helium was pumped from the pot, and it was cooled to 1.5 K. Finally, the circulation of the ^{3}He-^{4}He

mixture was started, and the cooling down to about 40 mK began. The detailed description of the working principle of ^{3}He-^{4}He dilution refrigerator can be found in numerous publications [5, 28, 29, 30, 31].

After the cool down was successfully performed, the current-voltage characteristics of the working SINIS junction were measured by utilizing the four-probe electrical scheme represented in Figure 3.1.1.
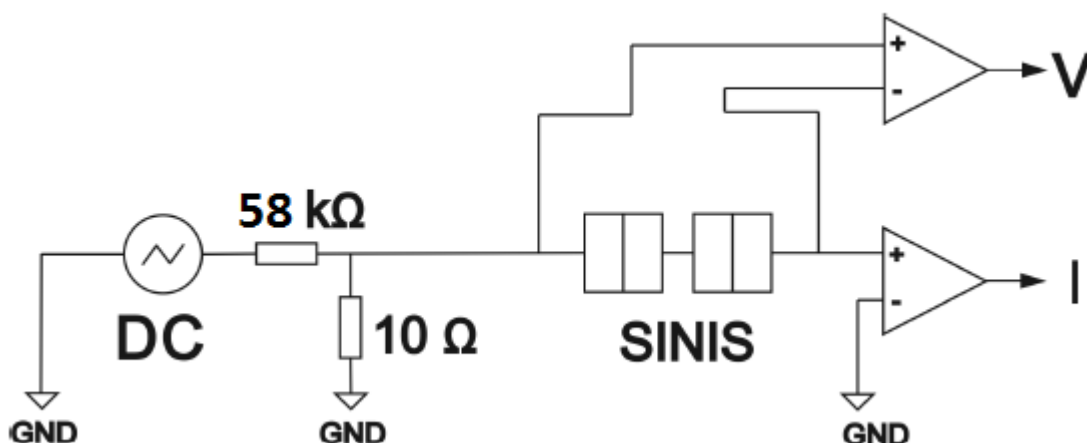

Figure 3.1.1. Measurement scheme for I-V characteristics of SINIS tunnel junctions.

In order to measure the I-V characteristics of SINIS tunnel junctions, we used the home-built DC voltage source with linearly sweeping output from -4 V to 4 V. The sweep time was set to the maximum of 1770 s to achieve the highest possible voltage resolution. Moreover, by using the 1/5800 voltage divider we were able to shrink the range of the voltage bias, but still with the same sweep time, closer to the gap voltages. The voltage divider was formed by two ohmic resistors: 58 kΩ and 10 Ω. The voltage applied to the SINIS was equal to the 10 Ω resistor voltage. By utilizing the voltage pre-amplifier ITHACO Model 1201 with low pass filter at 3 Hz, we were able to measure the voltage across the SINIS tunnel junctions. For measuring the current response through the SINIS, the current pre-amplifier ITHACO Model 1211 with integration time of 300 ms was used. The previously calibrated RuO resistor served as a bath thermometer.

All the readings from voltage pre-amplifier, current pre-amplifier and the bath thermometer resistance bridge went through the ADC converter, and were recorded by a home-built LabView program.

The first current-voltage SINIS tunnel junctions characteristics were measured at 300 mK bath temperature, by using a lower voltage divider in order to measure the ohmic resistance of the SINIS tunnel junctions at voltages far from superconducting gap. The measured I-V characteristic at 300 mK with its linear fit are depicted in Figure 3.1.2.
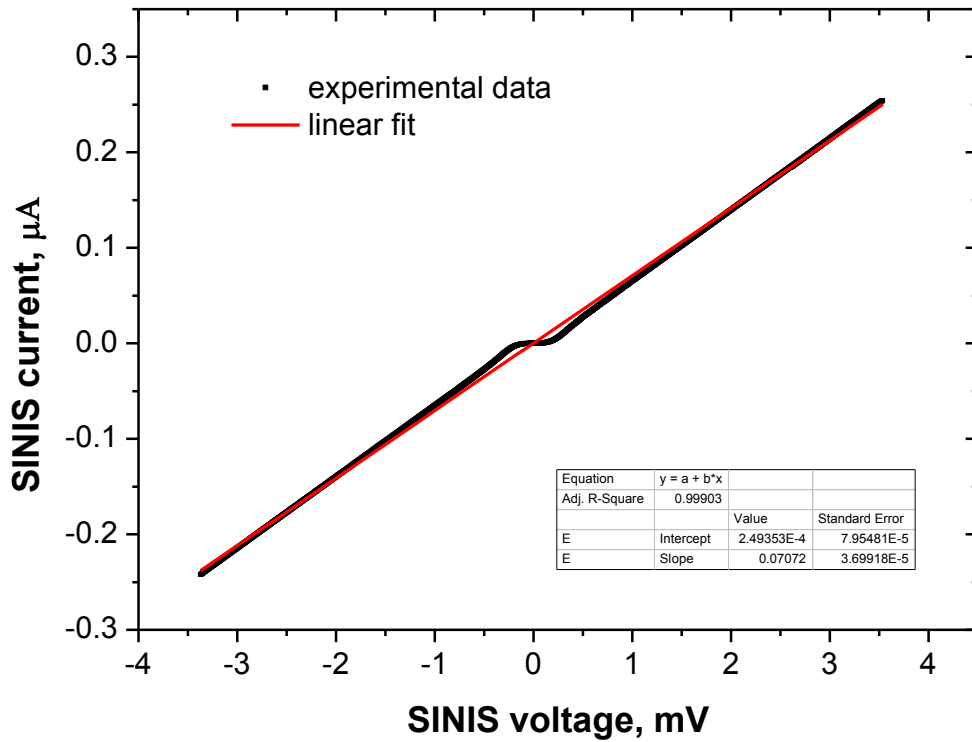

Equation	y = a + b*x		
Adj. R-Square	0.99903		
		Value	Standard Error
E	Intercept	2.49353E-4	7.95481E-5
E	Slope	0.07072	3.69918E-5

Figure 3.1.2. I-V characteristic of SINIS tunnel junctions at 300 mK with its linear fit.

It is not hard to notice that at high voltage values the SINIS I-V characteristic has a simple Ohmic behavior, which provides us with the value of the tunneling resistance. At voltages lower than 0.5 mV superconductivity starts to contribute. In order to evaluate the size of the superconducting gap, more precise the I-V characteristics with a higher voltage divider were measured, and their numerical derivatives were taken (see Figure 3.1.3). However, the I-V characteristic presented in Figure 3.1.2 is useful to obtain the tunneling conductance value, and, therefore, the tunneling resistance value, which appeared to be $R_T = {}^1/_{G_T} \approx 14140\ \Omega$ for the fabricated SINIS tunnel junctions on top of SiO_2 colloidal nanoparticles surface.

From Figure 3.1.3, where differential conductance of the tunnel junctions is depicted against its voltage measured at 50 mK, the size of the superconducting band gap was found to be equal to $\Delta = 0.185$ mV. For a SINIS device, a peak in the conductance band appears at $2\Delta \approx 0.37$ mV Based on the known tunneling resistance and the size of the gap, the calculation of

BCS theory curve was made (red solid line in Figure 3.1.3). A home-built program was utilized for the simulations of symmetric SINIS tunnel junctions.
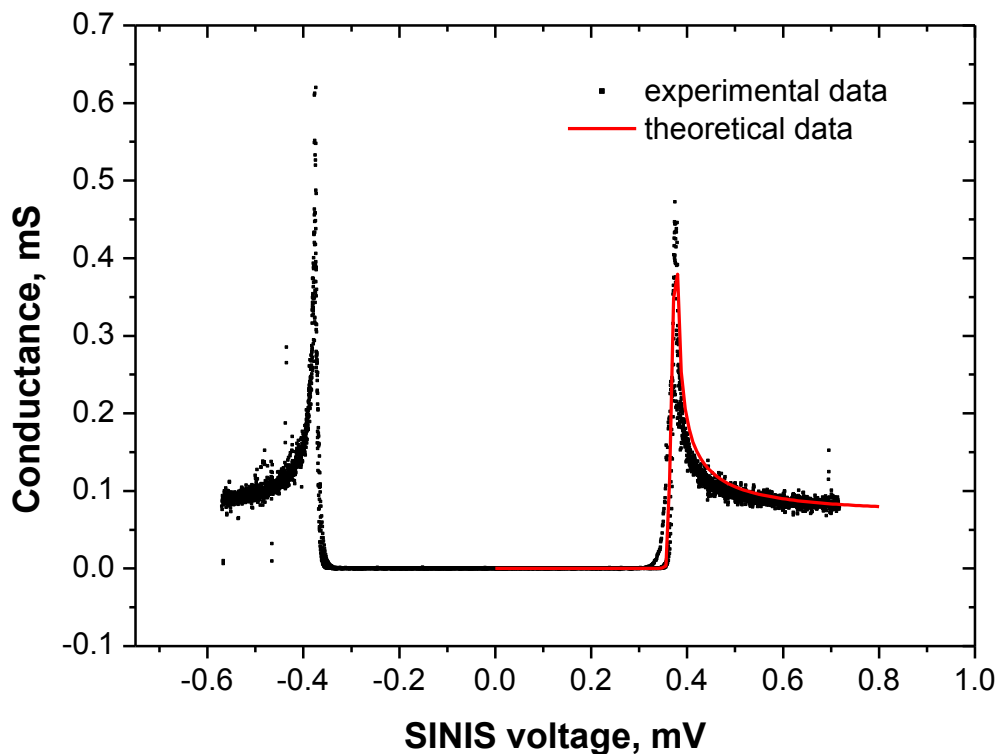

Figure 3.1.3. SINIS tunnel junction conductance characteristic for DC measurement at 50 mK and the theoretical fit by BCS superconducting theory.

The experimental data and the theoretical fit based on BCS superconducting theory are in a good agreement in general, as it is possible to notice in Figure 3.1.3. However, the temperature, which was used to fit this experimental data, was set to 10 mK. It implies that the actual temperature of the SINIS tunnel junctions was lower than the bath temperature.

Later, the I-V characteristics at different temperatures were also measured. They are presented in Figure 3.1.4 and Figure 3.1.5 by using linear and logarithmic scale correspondingly. In Figure 3.1.5 the theoretical curve for I-V characteristic measured at bath temperature around 50 mK (according RuO thermometer) is depicted by red line. The fitting temperature was set to 10 mK and the broadening parameter to $3 \cdot 10^{-4}$ dynes. It is worth to notice that they behave similarly to the classical SINIS tunnel junctions fabricated on smooth silicon substrates [29, 30]. As it was mentioned in the first chapter, at higher temperatures we can observe the existence of "hot" electrons, which tunnel even while the lower than the band gap size voltages are applied. Moreover, the I-V characteristic measured at 50 mK explicitly

shows a knee structure at sub-gap voltages, effect of the superconducting DOS broadening [32].
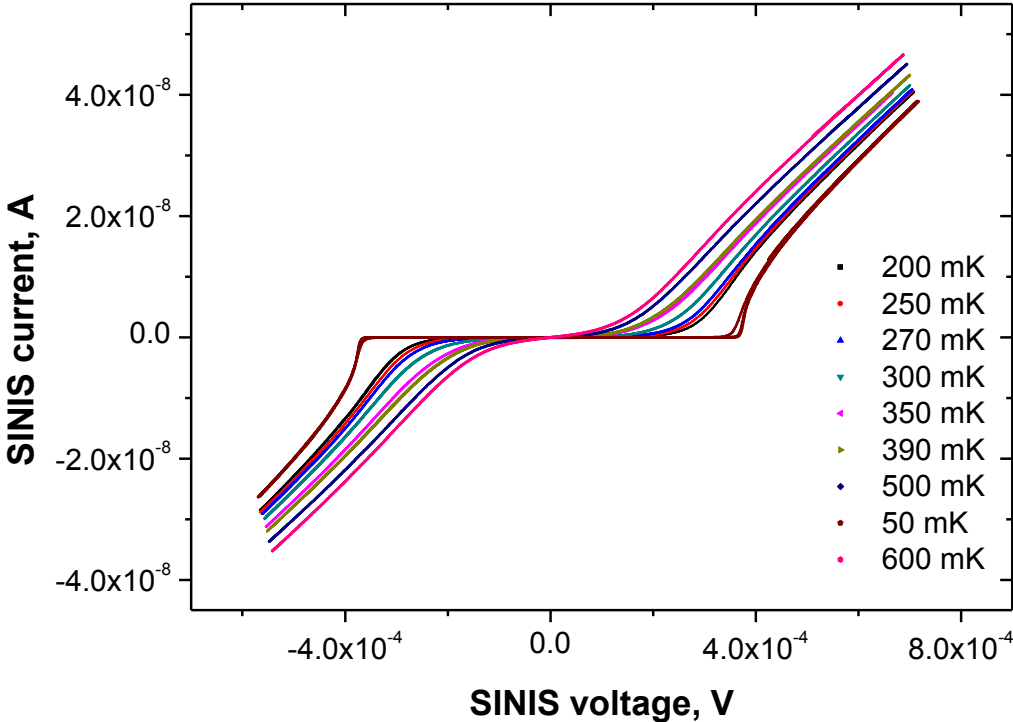

Figure 3.1.4. SINIS I-V characteristics measured at different bath temperatures presented in linear scale.
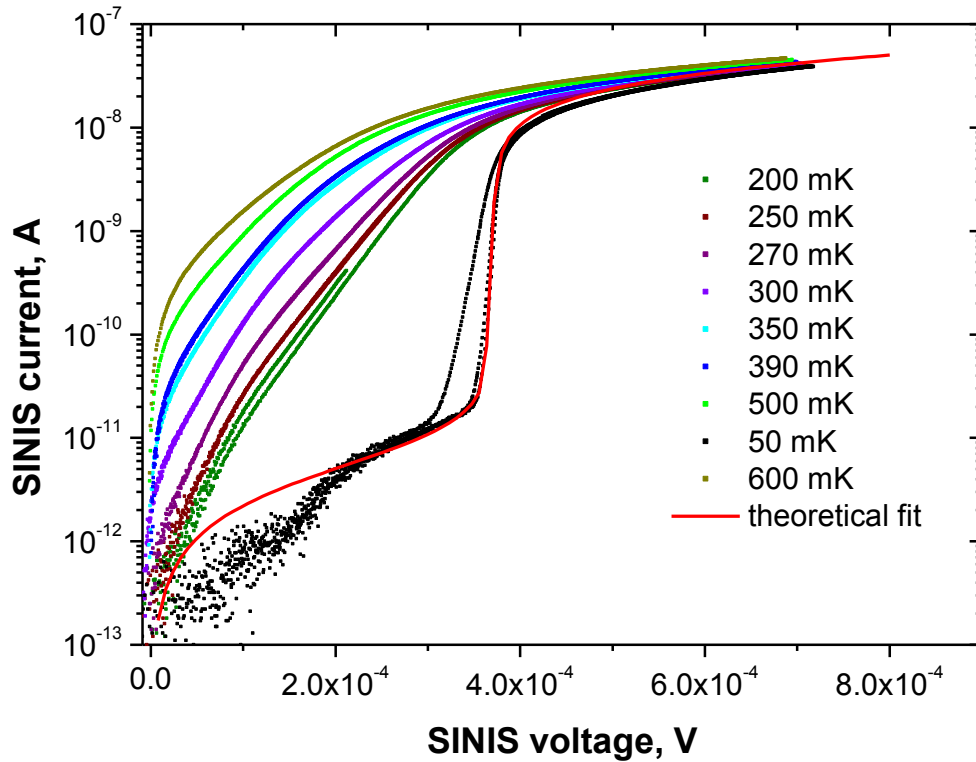
Figure 3.1.5. SINIS I-V characteristics measured at different bath temperatures presented in logarithmic scale.

Afterwards, the sample was heated to approximately 1.2 K, and the slow cooling started again. While this cooling a constant bias current was applied to SINIS tunnel junctions, and the dependency of SINIS voltage from the bath temperature was measured. It is important to measure this V-T characteristic during the cool down, because the cooling process usually is slow and smooth, what we cannot always claim about in heating. The V-T characteristics were measured at two different bias currents: 0.051 nA (see Figure 3.1.6) and 0.97 nA (see Figure 3.1.7).
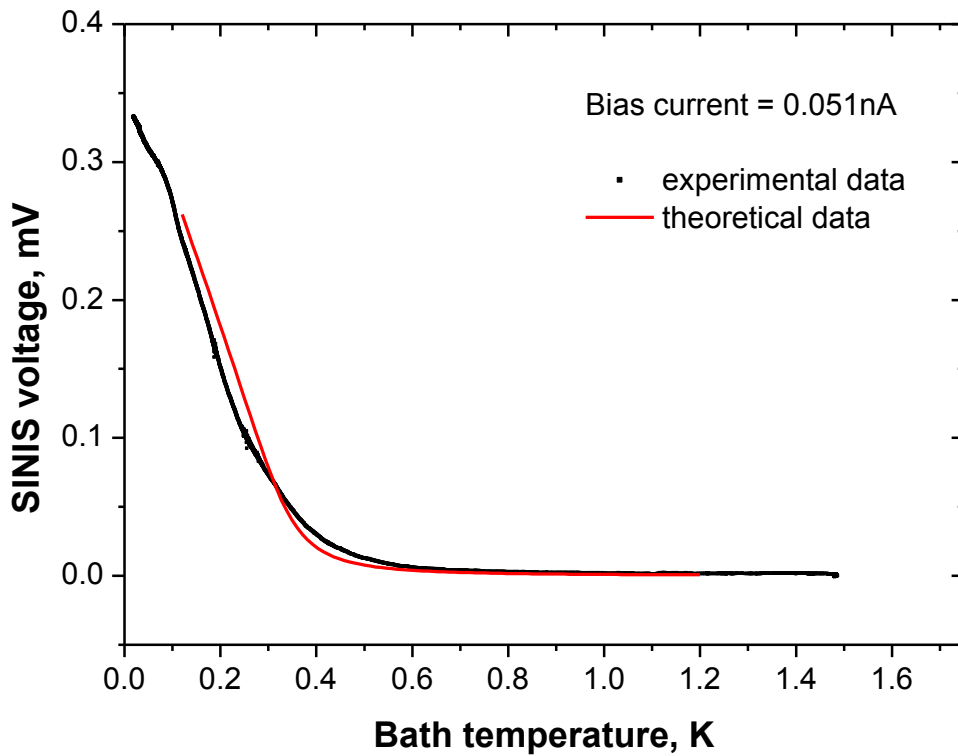
Figure 3.1.6. Voltage across the SINIS versus bath temperature at 0.051 nA bias current.

All the measured voltage-temperature dependencies were fitted theoretically by performing calculations based on the BCS theory of superconductivity. The same values of tunneling resistance and gap size were used as in the calculations of the current-voltage characteristics. The broadening parameter was set in all simulations to $3 \cdot 10^{-4}$ dynes [32]. It is not hard to notice that the theoretical curve for lower bias current is closer to the corresponding experimental data, than what is obtained for the higher bias current curve. The discrepancy between the theory and experiment is not fully understood yet, it might have to do with asymmetry of the junction resistances, for example.

The measured V-T characteristics served as calibrations for SINIS thermometer during the thermal transport measurements.
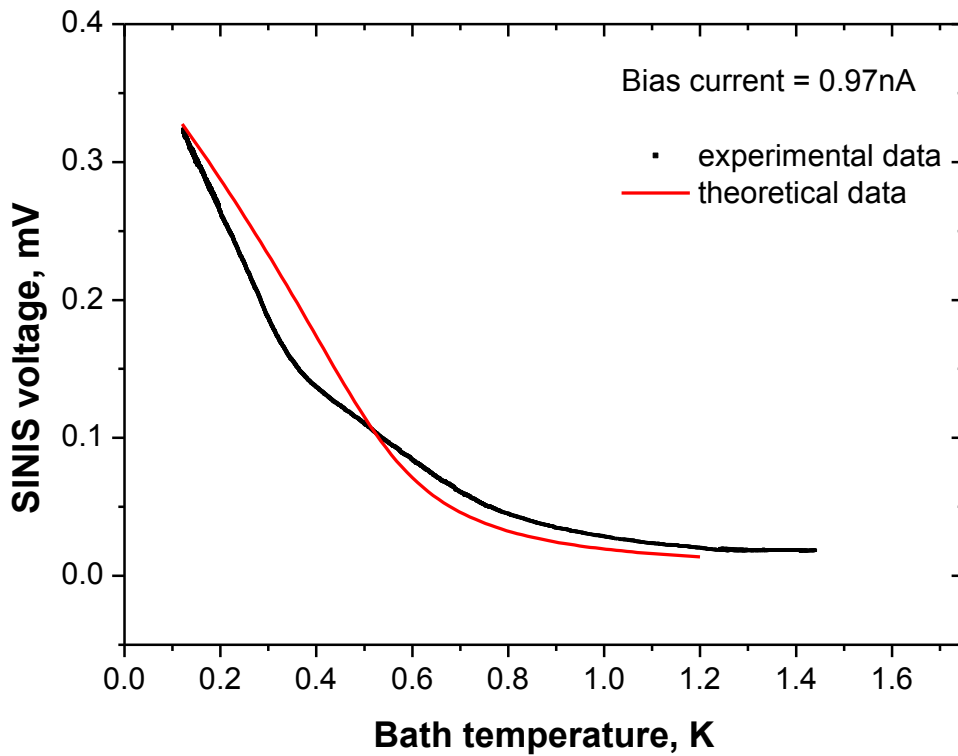
Figure 3.1.7. Voltage across the SINIS versus bath temperature at 0.97 nA bias current.

3.2 Thermal conductance measurements

Finally, the preliminary thermal transport measurements were conducted. As it was mentioned before, one SINIS (which had tunneling behavior) served as a thermometer. The current-voltage characteristic of the second fabricated "SINIS" was also measured. It showed fully linear I-V dependency, which is appropriate to a simple ohmic contact (see Figure 3.2.1). Nevertheless, we can use this shorted SINIS as a heater easily. By applying a bias voltage to the shorted SINIS, we measured the voltage response of the SINIS, which was biased with 0.97 nA current. The measured SINIS voltage response values were later transformed to the temperature values by using the appropriate V-T characteristics. For that reason, a special Java SE 1.8 program was created, which finds the closest voltage value from the experimental V-T dependency to the measured one during thermal transport experiment, and provides us with the temperature value.
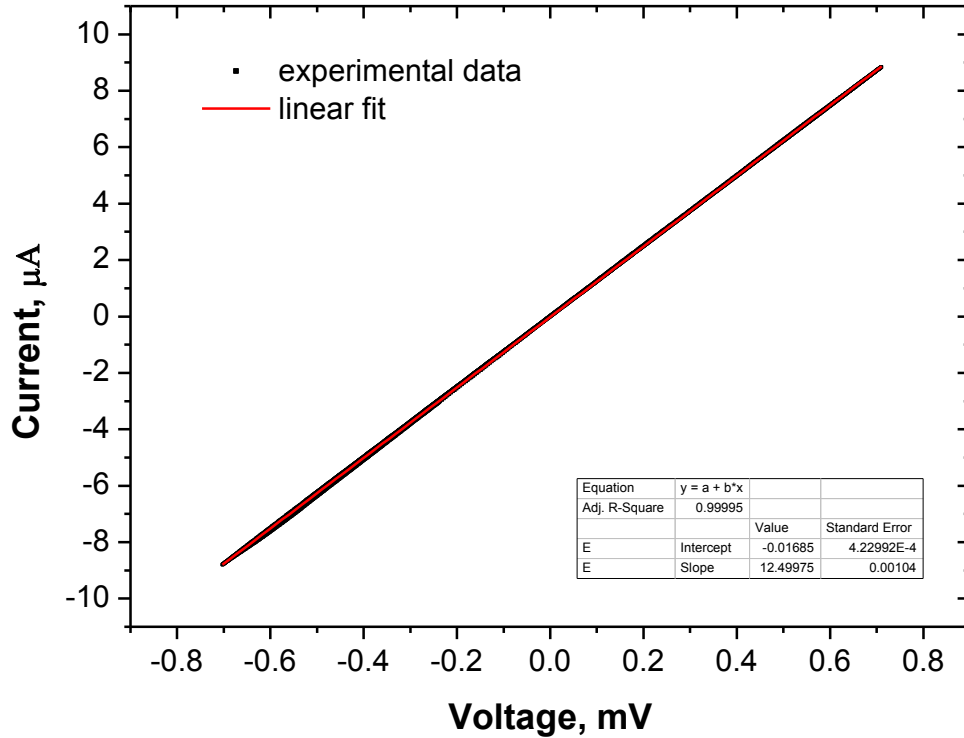
Figure 3.2.1. Current-voltage characteristic of shortened SINIS measured at 1 K bath temperature. The measured resistance was around 80 Ω.

The geometry of the heater and thermometer, which were utilized for thermal transport measurements is presented in Figure 3.2.2. The distance between them was around 58 µm. And the length of the normal metal of one SINIS was approximately 44 µm. The SEM image presented in Figure 3.2.2 refers to the sample with the exact geometry, which was used for the actual measurements.

However, it is extremely hard to predict the actual heat flow directions by utilizing this heater-thermometer geometry. The thickness of the SiO_2 colloidal nanoparticles layer is roughly a few microns, which provides the possibility for the heat to flow down to the substrate quite readily. Moreover, the heat reflections from the silicon surface chip are also possible. Consequently, we were able to measure a heat-temperature response, which is presented in Figure 3.2.3, but we cannot calculate the actual value of thermal conductivity based on these measurements yet, due to the absence of a theoretical heat flow model for this geometry and the sample in general.
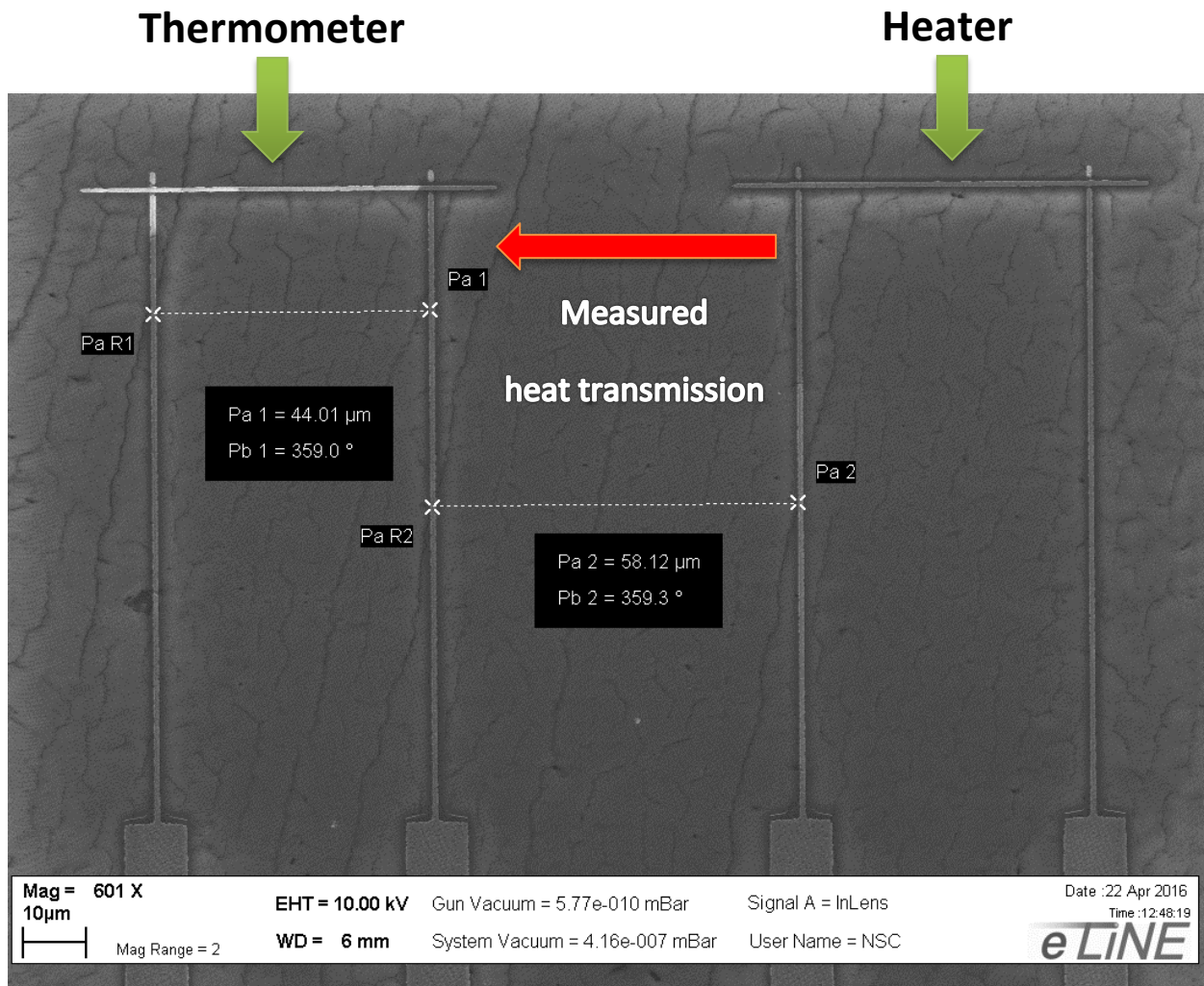
Figure 3.2.2. Geometry of the sample, which was utilized for thermal transport measurements.

In Figure 3.2.3 the power emitted by heater and the corresponding temperature rise of the neighboring SINIS tunnel junctions relation is shown. By presenting this dependence in logarithmic scale, the curve becomes linear at higher temperatures. Therefore, we can fit this dependence by the power equation $P = a \cdot T^b$. With the help of Origin software, the values of a and b parameters were obtained. We cannot claim about physical meaning of parameter a at this point, because as it was already mentioned we do not know exactly how the emitted heat spread in the sample. On the other hand, the value of parameter b is equal to 4.15. Based on the Debye theory for 3-D materials, where regular phonons are the dominant heat carriers, the power emitted by the heater is proportional to the temperature to the power of four.
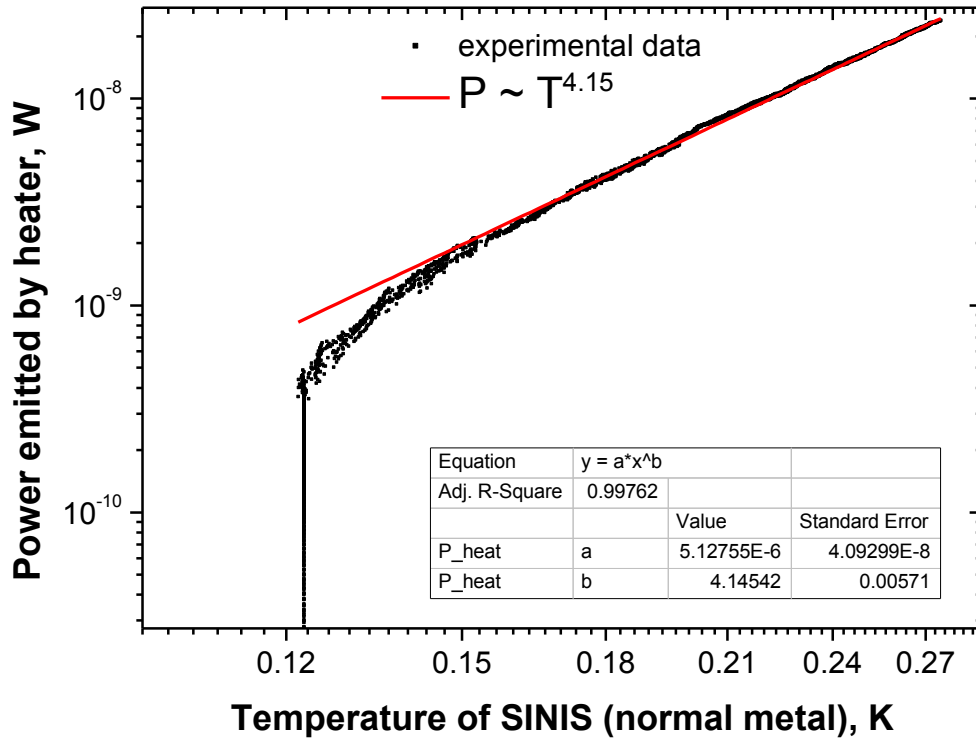
Figure 3.2.3. Power emitted by heater and neighboring SINIS temperature response in a logarithmic scale.

Conclusions

As a result of the research work presented in this thesis, the first SINIS tunnel junctions with contact pads were successfully fabricated on top of a medium thickness SiO_2 self-assembled colloidal nanoparticles structure, which formed the desired 3-D phononic crystals. It was achieved by coating the rough nanospheres surface with thin layer of negative photoresist SU-8. In addition, the thickness of SiO_2 self-assembled colloidal nanoparticles structure was studied depending on dipping out speed, humidity in the dipping chamber, hydrophobicity of the substrate, and the concentration of the colloidal suspension.

Two SINIS tunnel junctions deposited on top of 3-D phononic crystals were designed to serve as a thermometer and a heater to make the eventual thermal transport measurements possible. In practice only one SINIS was working properly, proved by measuring its current-voltage characteristics. The second SINIS appeared to be shorted, so we were able to use it as a heater with Ohmic resistance. The voltage-temperature dependences of working SINIS tunnel junctions biased by different currents were measured. These V-T curves had the utmost importance for the following thermal conductance measurements, because they served as calibration dependences for SINIS thermometer.

Finally, we were able to perform the preliminary thermal conductivity measurement. The obtained results expose quite close behavior to the typical phonons as the main thermal transport carriers, what is undoubtedly a positive sign. However we still cannot claim whether the reduction of thermal conductivity was observed or not. For that purpose, thermal conductivity measurements should be performed for the sample with the same heater-thermometer geometry but without phononic crystals. Afterwards, the comparison of thermal conductivity values can be done.

Moreover, improvements of the fabrication techniques can be done. For example, the fabrication methods of thicker 3-D phononic structures can be invented. The yield of successfully fabricated samples can be increased by trying new techniques, which can reduce the charging effects during EBL, and by using the more precise EBL equipment in general.

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