Fabrication of carbon nanotube field-effect transistors

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Bachelor's thesis

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Preface

Reported sample fabrication was done in summers 2011 and 2012 in Nanoscience Center, Department of Physics in the University of Jyväskylä.

I would like to thank my supervisor, Prof. Markus Ahlskog for interesting topic and for the opportunity to work with nanotechnology during my studies. In addition I want to thank the group members, especially Dr. Peerapong Yotprayoonsak and Mr. Konsta Hannula who taught me the use of the various instruments of Nanoscience Center. I'm also grateful for the staff of Nanoscience Center for their advices and for the discussions.

Jyväskylä, Finland, July 2014
Ville Saunajoki

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1 Introduction

Todays technology strongly bases on transistors. The integrated circuits construct of transistors which handle the information. The focus has been on decreasing the transistor size and fitting them more dense.

In 1965 Gordon Moore proposed that transistor density would double approximately every two year.[1] This prediction is known as Moore's law and has applied reasonably well for decades. How ever the transistor sizes are getting so small that the existing techniques are facing new challenges. The semiconductor industry uses mostly silicon as bulk and builds the circuits on one crystalline surfaces. As the scale decreases quantum mechanics starts to play more significant role and old manufacturing techniques may come to end of their road. As solution, to keep the trend going on transistor development, different transistor materials have been researched for one molecule transistors.

First carbon nanotube (CNT) field-effect transistor (FET) was reported in 1998.[2] CNT FETs seem potential technology but there are limitations for big productions. The research continues on basic properties and on possible applications while production is developed simultaneously. This thesis focuses on fabrication of individual CNT FETs for research use.

2 Theory

2.1 Carbon nanotube

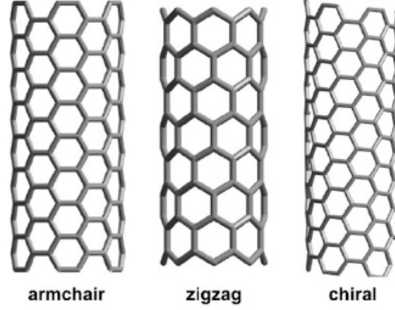


Figure 1: CNTs with different chiralities.

Carbon nanotube (CNT) is an allotrope of carbon where carbon atoms arrange as walls of a tube. CNTs can be considered as 1D material as the diameter of the tube can be ~1 nm but the length can be tens of micrometers meaning dimension difference in several orders of magnitude. The atoms connect to each others with sp^2 bonds forming a hexagonal pattern as in graphene. Closer observation of lattice shows that it varies as is shown in figure 1.

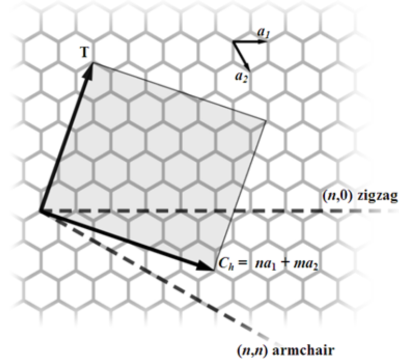
The lattice of CNT can be described with chirality vector $\vec{C_h}$. Base vectors $\vec{a_1}$ and $\vec{a_2}$ of CNT are shown on graphene lattice in figure2 and they denote the chirality vector

$$\vec{C_h} = n\vec{a_1} + m\vec{a_2} \qquad \text{,where}\, n,m \in \mathbb{N}.$$

The integers n and m are used to descibe the tube as (n,m). On tube the chirality vector points the circumference – ends in the same point as where it begins. Other vector which is sometimes used is the translation vector $\vec{T}$ which is perpendicular to $\vec{C_h}$. On tube $\vec{T}$ is parallel to the axis of tube and goes from lattice point to next similar point. Length of the vector $\vec{T}$ gives the unit cell length of a tube.

Different lattice means different electron transport. Depending on the lattice, CNT can be metallic or semiconducting with either narrow or moderate

Figure 2: Base vectors $\vec{a_1}$ and $\vec{a_2}$ shown on graphene lattice.*Base vectors are used to define the chirality vector $\vec{C_h}$ and the perpendicular translation vector $\vec{T}$.



band gap.[3] In the end roughly two thirds of the CNTs are semiconducting.[4]

CNTs may also have several layers of walls. Tubes with one layer are called single walled CNTs (SWCNT) and others can be called multi-walled CNTs (MWCNT) although names as 'dual-walled CNT' are used. Structure of MWCNT is shown in figure 3. The MWCNTs have layers with different chiralities but they do not suit that well to transistor use as MWCNTs usually show metallic behaviour unless there are some structural defects.[5]

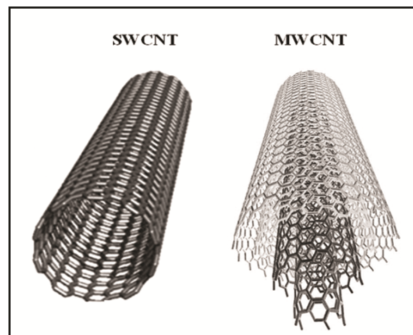


Figure 3: Comparison of SWCNT and MWCNT.

2.2 *Field-effect transistor*

Transistor is an electronic component which works as electric current switch. Usually a transistor has three contacts. Two of them are connected together

*The selection of base vectors may vary between publications. Selection of base vectors should be checked before comparing calculations.

through semiconductor and the third contact is used to control the conduction between the two others. Depending on the transistor type either voltage or current is applied on third electrode.

Field-effect transistor (FET) is one type of transistor. The contacts are called source, drain and gate (fig. 4). Source and drain are connected through semiconducting material and the gate lays close to this channel. Voltage on gate electrode effects the charge carriers on semiconductor, either by repulsing the or by attracting them. This changes the conduction of the semiconductor.

In semiconductors conduction is based on charge carriers which can be induced to material by process called doping. Semiconductors, with electrons as majority charge carries, are called n-type semiconductors. In lattice that means excessive electrons and their movement through the lattice creates current. In practice with FETs, source and drain are connected to the semiconductive area and the gate lays close to the channel (fig. 4). If negative potential is applied close to the n-type semiconductor, it repels the excessive, negative electrons on the semiconductor meaning weaker conduction. Positive voltage on the other hand attracts more charge carriers and improves the conduction. This way the channel between drain and source can be opened and closed.

In p-type semiconductors the lattice lacks electrons at some points. Charge carries in p-type are called holes as the structure can be considered as electron chain with hole at the point of missing electron. With p-type semiconductor positive potential on gate electrode attracts more electrons which fill the holes and the conduction decreases – negative gate voltage helps to keep the electron holes in lattice empty. The charge carriers of p-type are considered

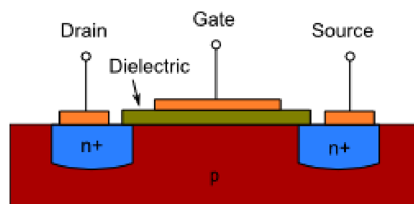


Figure 4: Structure of n-type MOSFET.

also as positive. Negative gate voltage in these means can be thought to attract positive charge carriers which increases the carrier density.

Typical transistors construct of combination of p- and n-doped areas.Device of figure 4 does not actually operate based on the two previous paragraphs although that is the general principle in semiconductors. For example with positive gate voltage the n-type MOSFET (fig 4) attracts the electrons from highly doped terminals (n+) to the interface of dielectric and p-doped part. On default electrons are the minor charge carriers in p-type but with the positive voltage they become major charge carriers on limited area and form a conducting channel between the terminals – the switch is open. Advantage of differently doped areas in this case is that p-n interface does not conduct which is also the principle used in diodes.

2.3 Carbon nanotube transistors

As the transistors are made smaller, at some point there will be a limit where the size of transistor approaches the scale of molecules. CNTs are a good candidate for single molecule transistors for their semiconducting properties.

In traditional silicon based transistor the conduction channel between drain and source is made on silicon by doping. The channel size can be decreased when it is created from a semiconducting molecule. CNT FETs have been made from individual tubes [2,5] and the most common structure can be seen in figure 5.

The CNT FETs are usually p-type [6] but it is possible to change them to n-type or ambipolar. [7,8] The metal-semiconductor interface seems to play

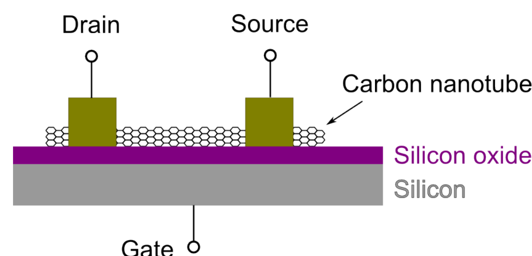


Figure 5: Commonly used structure of CNT FET.

the major role as it comes to charge carriers.[8,9] The behaviour of device may also change due to environment which has inspired CNT sensor research.[10,11]

2.4 Lithography

Word lithography originally meant printing technique but it is nowadays used also in microfabrication in which it is a common fabrication technique. The mainline in photolithography is to coat a surface with a film of light-sensitive chemical (photoresist) on which a desired pattern is exposed. Development of film transfers the pattern to the resist layer. The patterning enables the focusing of some surface treatments to specific areas as the other areas are protected simultaneously.

The resists are divided to two groups based on the effect of exposure. Positive resists become soluble to developer solution when exposed as negative resists lose their solubility to developer after exposure. As resist are different chemicals each of them has specific developers and exposure method.

The light used in exposure of photolithography depends on the resist. Chemical reaction occurs in resist molecules as required activation energy is reached. The energy of photon must exceed this activation energy for the reaction to occur. Photon's energy is related to the wavelength of the light and often light of UV region is used.

The patterns in photolithography are commonly exposed using a mask. Light is shined through a mask and mask will leave shadows (fig. 6 upper path). In microfabrication the size of the pattern starts to play a role as the transparent parts of the mask become slits when the scale is decreased enough. As the slit size approaches the wavelength of the light diffraction becomes significant and it affects the accuracy of the exposure pattern. As smaller patterns are reached for diffraction needs to be overcome. Decreasing the wavelength is one option but it brings also new difficulties such as resists, lenses and light sources. In electromagnetic spectra for example extreme ultra violet has been tested but these techniques have not been used big productions.[12,13]

Also electron beam (e-beam) or ion beam can be used in exposure. The

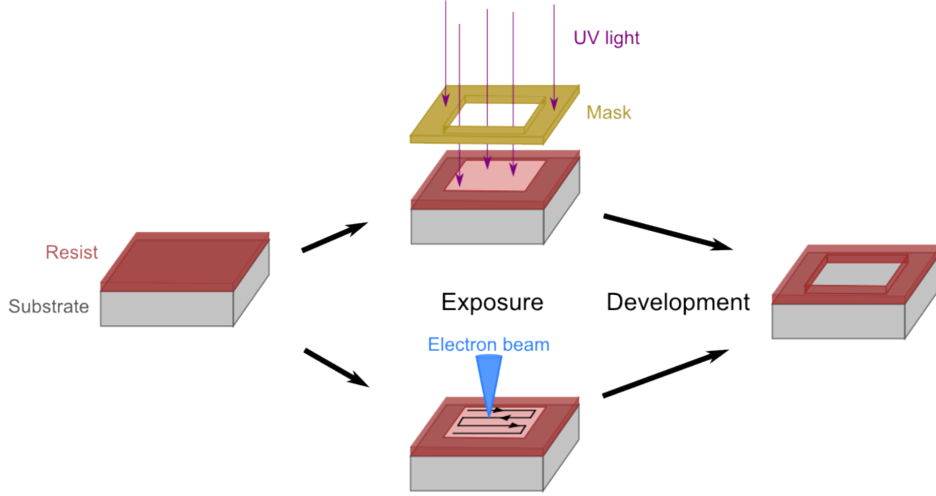


Figure 6: Lithography process using negative resist. The substrate has a resist film on top. Square shaped area is exposed to the middle by using UV light and mask (upper path) or by scanning electron beam (lower path). Development removes the exposed area of the resist film.

beam has similar effect to certain resists so that the chemical structure of the resist changes. Accelerated electrons behave like waves due to wave-particle duality and their energy is proportional to acceleration voltage U. Wavelength λ can be calculated using de Broglie equation

$$\lambda = \frac{h}{p} = \frac{h}{m_e v}$$

in which the momentum p comes directly from the kinetic energy E_K of an electron, gained during acceleration.

$$eU = E_K = \frac{1}{2} m_e v^2 \quad \Leftrightarrow \quad v = \sqrt{\frac{2eU}{m_e}}$$

$$\lambda = \frac{h}{\sqrt{2 m_e e U}} \tag{1}$$

The constants h, m_e and e are Planck's constant, mass of an electron and elementary charge, respectively and v is velocity of electron. E-beam can

reach shorter wavelengths than what is mainly used in photolithography and the diffraction limit can be pushed forward.

Masks are rarely used in beam lithography. The beam can be focused extremely well with magnets and the focused beam can be then used directly to expose the pattern by scanning. E-beam can be focused to area of less than 1 nm diameter.[14,15] This yields higher resolution than the masks of photolithography although the exposure time increases significantly as the beam has to scan through the pattern pixel by pixel (fig. 6 lower path).

In e-beam lithography scattering limits the resolution instead of diffraction.[14] The electrons mainly penetrate the resist layer without problems. Some forward scattering occurs in the vacuum-resist interface and the beam spreads a bit in film. The substrate causes some of the electrons to back scatter in random direction inside the film. These scatterings widen the exposed area and the limiting factor will be the resolution of the used resist.

Usually after the development some kind of surface treatment is done to the areas that are not covered by resist. Such treatments can be depositions of new layers or etching of the revealed area. The treatment can be limited to certain areas as the left over resist covers and protects the other areas. When a process is planned the resist and the thickness of the layer are decided. For example in etching the resist layer must protect the areas which it covers. The chemicals of etching may be so strong that they damage also the resist and in such cases the resist layer should be thick enough so that it endures the chemicals a bit longer than what it takes to etch the focused areas to required depth. The thickness of resist layer then again effects to exposure dose.

As it comes to deposition of new layers and lithography the needed properties of resist differ when compared to etching. For example PVD (physical vapour deposition) does not damage the resist layer and the purpose of the resist is to limit the treated areas. A new layer is created all over the substrate surface but the part covering the resist may be removed by dissolving the resist. As the supporting resist layer is lost on some areas they can be easily swept or washed clean.

2.5 Electron beam physical vapor deposition

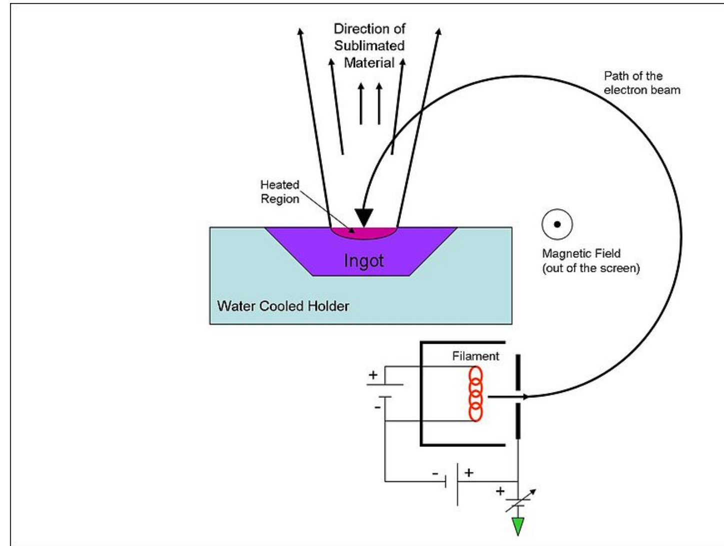


Figure 7: A common e-beam PVD setup.

E-beam PVD is one method of physical vapor depositions (PVD). PVD in general is a vacuum deposition of thin films by condensating material vapor on substrate. In e-beam PVD the target material is evaporated by e-beam. This causes a flux of material to flow away from the target growing a film on surfaces it faces.

A common build of e-beam PVD setup is shown in figure 7. The whole system is in vacuum where filament emits electrons. Electrons are gathered through an aperture for a parallel electron flow. The beam is turned with magnets to hit the evaporated material ingot. The substrate is positioned over the ingot so that the treated surface is facing the ingot.

The thickness of the film is adjusted with shutter that is between the substrate and the ingot. The flow is let on substrate only certain amount of time. The material flow can be measured with vibrating crystals. As material layers grow on the crystal, it's resonance frequency changes which is proportional to the evaporation rate.

The substrate is roughly 30–80 centimeters above the ingot and the heated region of ingot is about 1 cm by diameter. Due to this the flow on the

substrate can be considered uniform and the film will not grow on surfaces parallel to the flow. This can be used as an advantage in several cases but on the other hand it means poor film uniformity on complex surfaces.

2.6 Marker structure

The fabrication process of this thesis has many aspects that have to be considered. One essential part is locating the carbon nanotubes (CNTs). The deposition is coarse and the tubes will lay randomly on the surface. For exact navigation on the chip marker structure is made before the CNT deposition. The marker structure has also electrodes that help to connect the microscopic devices to macroscopic setups.

The marker structure is represented in figure 8. The figure on lower left is with the smallest magnification. Width of that structure is 5.5 mm as the chip is about 6 mm. Square shaped connection pads circulate on the edges and are meant for further connections from the chip. From each connection pad goes an electrode to the middle. The lower left image of figure 8 has also crosses in three corners and an arrow in the last corner. The arrow points which way the chip is handled – we use it to mark the lower right.

The crosses are for alignment. As the tubes are found, electrodes are planned and made using lithography which means that a new pattern will be exposed. The exposure pattern has to be aligned with the existing pattern. Scanning electron microscope (SEM) is used for the e-beam exposure and as the sample is inserted to the machine, its positioning is not known. SEM navigates on its own coordination system and the chip has its own. The crosses are taken as exact points to get their coordinate in both systems and then the transformation between the coordination systems is defined. Three points is enough to define the shift, rotation and scale differences between the systems. When looked more carefully at figure 8 one can notice that there is crosses on the red layer corners but also in green layer in the middle. The outer crosses of green layer are in line with the arrow heads and the inner ones are rotating the center close to the lower right arrow (lower right of fig. 8), just barely left out from the last magnification area (top part of fig. 8). There

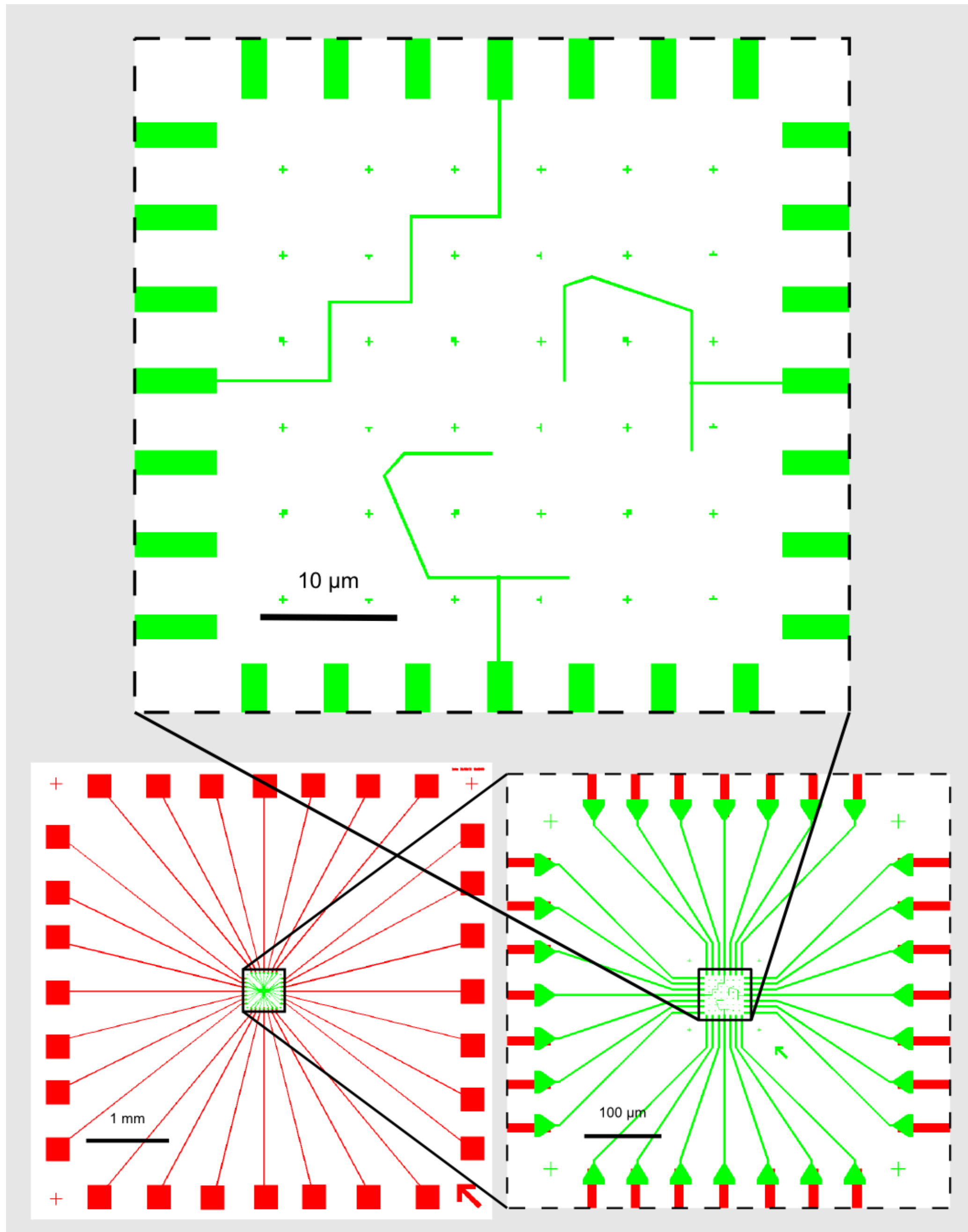


Figure 8: Marker structure in different magnifications. Red and green parts are exposed areas.

is three sets of these alignment crosses as the outer ones are meant for rough alignment and the inner one for the last, most exact alignment.

The crosses on the upper part of figure 8 are not for alignment of exposure pattern but for the alignment and navigation of AFM images. The middle can be considered to construct from 25 (5×5) square shaped areas where each cross represents a corner of an area. The areas are imaged on AFM on such magnification that the crosses of each corner are visible on image. The distance between crosses is 7 µm and the size of the AFM image is usually 10×10 µm. On such magnification the tubes are visible and the accuracy of AMF's piezo elements is good enough. If the imaged area on AFM is too big the piezo element needs to move longer distance which might cause distortion to image. The AFM images are fixed by rotating, scaling and tilting to correspond the markings and then the positions of tubes are defined. The corner crosses are modified slightly so that when crosses of an area are visible, the area can be recognized. Some lines from a cross can be left out or an area between the lines can be filled to make each area recognizable.

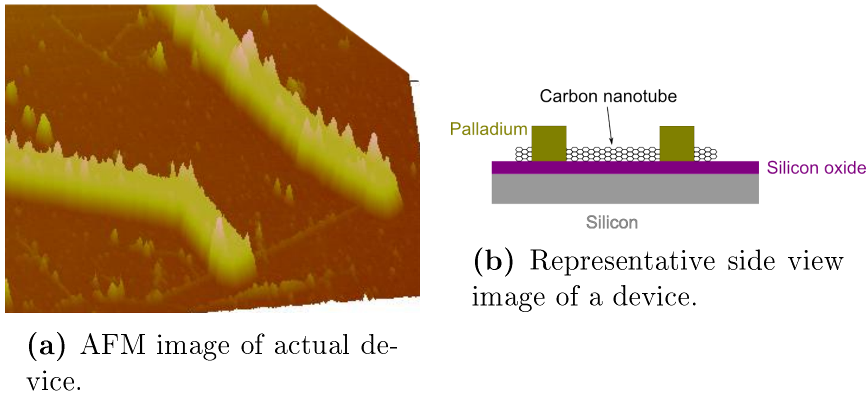
The electrode's width decreases as the center is approached from the patches (10 µm → 2 µm). The wider the electrode, the smaller the voltage loss along it is but also wider electrodes are more durable as it comes to impurities and scratches. The exposure of marker structure is done in two steps with different apertures of SEM. The bigger the aperture the more it lets electrons through but the accuracy decreases as wider range of travelling directions is included to the beam. The bigger aperture speeds up the exposure as the electron dosage increases. The biggest aperture is used for wider lines as accuracy can be decreased.

The pattern of marker structure has to be divided to smaller pieces for SEM because the movement range of the beam is limited. The smaller partitions are called write fields and together they form working area. This means that the lines of pattern may not be exposed at once and there is a chance that there is a minor mismatch between working areas. To ensure proper connections on area interfaces the electrode may be modified a little. For example in lower right part of figure 8 red and green represent differ-

ent exposure layers and to ensure the electrical connection, oversized arrow heads are made to overlap the connection. These arrow heads allow a minor mismatch between the layers and the connection will still work. There is also layer of patches to ensure the interfaces between write fields but it has been left out from the figure 8.

The thinnest electrodes in the middle of marker structure are made for direct CNT connections. There is a chance that some tubes fall partly on these electrodes. Often CNT connections are made on the tube but these electrodes enable connections where only the beneath of tube touches the electrode. Otherwise electrode lays on the tube and partly surrounds it. Connection where electrode goes over the CNT is called symmetric and the other case is asymmetric. There is a chance to compare different connections if there is a device where one end of a long tube lays on electrode and two more connections are made to the other end. This case there would be s-s-a connections on the tube ('s' for symmetric and 'a' for asymmetric). The tubes usually don't have defects and the effect of connection can be shown when s-s connection is compared to a-s connection of the same tube.

3 Fabrication



(a) AFM image of actual device.

(b) Representative side view image of a device.

Figure 9: Carbon nanotube transistor.

In figure 9a is an AFM image of a fabricated device. At least two contact electrodes are made on carbon nanotube laying on silicon oxide surface. Figure 9b shows the structure of a device.

The fabrication goes from bottom to top, layer by layer. At first the silicon surface of a chip needs to be oxidized for insulating layer. Marker structure is made using litography to enable navigation on a chip. The marker structure also helps to connect the microscopic devices to macroscopic measurement setup. CNT's are deposited on the chip and located. As the usable tubes have been found they need to be connected to electrodes of marker structure so a new layer of electrodes is made. Finally the silicon chip is attached to chip carrier for quick connections to measurement setup.

The following sections go through the process more detailed.

3.1 Preparation of silicon wafer

Silicon is often used for its semiconducting properties. In these transistors the silicon wafer is used as a substrate on which the transistor is build. Few properties of silicon make it great substrate for these purposes. The manufacturing process of silicon produces one crystalline silicon and by selecting the cutting angle correctly surfaces of one lattice can be made. The smooth-

ness of the surface eases the search of carbon nanotubes a lot as the tubes diameter is in nanometers and could be lost on coarse surfaces.

Silicon is ordered in round wafers with diameter of 7 inches and thickness of 1 mm. Other chosen properties are doping and surface treatment. We have ordered highly doped silicon for its good conductivity and if possible with 500 nm oxide layer. The silicon needs to be highly conducting as it is used as gate electrode.

As the devices are build on the substrate for electrical measurements the surface needs to be insulating. Silicon forms a native oxide layer of about 10 nm in normal room air. Biases applied in measurements over silicon oxide are 5–30 V and such can not be held by the native oxide. The oxide layer is thickened in furnace where the temperature rises to 1100 °C and a oxide flow is led through. Oxide layers used in these samples are 300–500 nm thick. The growth of the oxide layer effects the surface smoothness but just so little that it will not make the search of CNT's more difficult. Silicon wafers with grown oxide layer can be also be bought from manufacturers and we have preferred that over self-made.

We have used square shaped silicon chips, which are 5.8 millimeters by side, for samples. The cutting is done with silicon saw. The saw cuts to defined depth in silicon and leaves pre-cut lines. After this the chips can be broken from the wafer like chocolate bar. The pre-cut wafer pieces are a bit easier to handle than the smaller fragments so the fragmenting is usually withheld after the pre-cut. The cutting leaves silicon dust on the chip which is cleaned using acetone and cotton sticks or cleanroom sheets. One should be careful with mechanical cleaning as the surface may scratch. The acetone is just to wash dust away as it does not dissolve the dust. After acetone wash the wafer is rinsed with isopropanol and dried with nitrogen gun.

3.2 Marker structure

The marker structures were made using electron beam litography. Resist layer of 100 nm was made on the chip from MicroChem's PMMA 950 A2 resist according to manufacturers instructions. Just a single layer of one

resist was used as it had been noticed to work in lift-off. The exposure used different apertures for different line widths to speed up the process (30 and 120 µm).

The metal used was palladium as it creates good connections with CNT's.[16] The electrodes of the marker structure had an additional sticking layer under the palladium. The purpose of sticking layer is simply to improve the attachment between silicon oxide and palladium. The sticking layer was 5 nm of titanium. As there is no current going through the palladium-titanium interface titanium, it will not effect in measurements. The final electrodes, of only palladium, are evaporated partly on the marker structure so there is a palladium-palladium interface and no voltage drop should appear.

Several marker structures are usually exposed at a time. The resist layer is made on bigger pre-cut piece of wafer. The alignment of the chip is made on SEM and exposure is programmed to repeat the pattern several times around the pre-cut wafer. After development of the pattern wafer is checked and electrodes are evaporated. First 5 nm of titanium and then 20 nm of palladium . The lift-off is done in acetone which dissolves the remains of resist layer. All metal evaporated on the resist will lose contact to wafer and can be washed away with ease.

The quality of marker structure is checked again with optical microscope. It is possible that the acetone bath does not dissolve all the resist at the first time or some leftover metal is stuck between the electrodes of the pattern. Some methods may be used to finish the lift-off. For example injection needle can be used to squirt acetone to focused area. If the injection needle is above the acetone surface air bubbles will mix to the acetone flow. The air bubbles seem to increase the effectiveness of the washing maybe due to the turbulence of the flow. If more power is needed to finish the lift off cotton stick can be used. Surface can be gently swept with the cotton stick as the sticking layer improves the attachment of the electrodes. Without the sticking layer electrodes come off easily. Such mechanical cleaning should be avoided as it may also scratch the surface and the electrodes but also it may round up the edges of the created pattern.

As the marker structure is finished, individual chips can be broken from

the wafer for sample preparation. In some cases, if individual marker structure from a wafer needs to be improved, it is safer to brake it to separate chip and continue the processing with just the one chip. This way, if some rougher methods are needed, the other chips will not be damaged.

3.3 Carbon nanotube deposition

We have used SWCNT's from Nanocyl for these devices. They are dissolved in solution for easier deposition. Their dissolvement is more difficult when compared to MWCNT. The tubes are dissolved in dichloroethane, which is toxic and carsinogenic. User needs to be protected and it is highly recommended to handle this solution in fume hood. Small amount of SWCNT's (< 1 mg) is added to vial with about 10 ml of dichloroethane.

The tubes do not dissolve perfectly to the solvent and some sonication is needed. We have used Hielscher's UPS400 fingertip sonicator at 50 % power, 0.5 cycle and for 10-20 minutes. The sonication may brake the tubes which sets limits to power and time of sonication. The transistor devices are easiest to build on long CNT's so the shortening the tubes should be avoided but still the solution needs to be sonicated before each use as the tubes tend to bundle.

The deposition on chip is done in cleanroom. The surface is washed with acetone, rinsed with isopropanol and dried with nitrogen gun. Sometimes gentle oxygen recipes of reactive ion etching system (RIE) may be used for stubborn organic impurities. Cleaned chip is put on spinner and spun 1500 rpm. CNT solution is deposited with pipette drop by drop. The deposition amount is tested experimentaly as the solutions do not have precisely defined concentrations. When the droplet hits the spinning chip it spreads on the surface and soon the dichloroethane solvent evaporates. The wetting and drying can be seen as color changes of the spinning surface. After the droplet has dried the next droplet is deposited.

Usually 8–12 drops are deposited. The process this far happens in cleanroom where the surface has a smaller risk of contamination. The AFM is outside of the clean room and the risk of impurities increases as the chip pro-

cessing is continued in normal room air. If enough usable tubes cannot be found in AFM imaging, deposition can be made again on existing tubes but the amount has to be estimated based on the used solution and the previous deposition tries. Too high concentration of CNT's makes the planning of final electrodes challenging as they may create additional connections between electrodes. The aim is to measure properties of individual tubes and there should not be several tubes in parallel connection. Also extra tubes between electrodes may create current leakages in measurements. If the tubes have a risk to make these extra connections the whole chip can be cleaned in RIE with oxygen recipes that will burn the carbon of the tubes and clean the surface. That is a back up plan to reuse the chip with marker structure but all the previous tubes are lost and deposition starts from the beginning.

3.4 AFM imaging of the tubes

After the CNT deposition chip is taken out from the cleanroom for AFM imaging. The risk of airborne and other impurities increases but rarely has significant effect for the final use. The chip centre is imaged for CNT's. The center has patterning for locating the tubes (section 2.6) from which 10×10

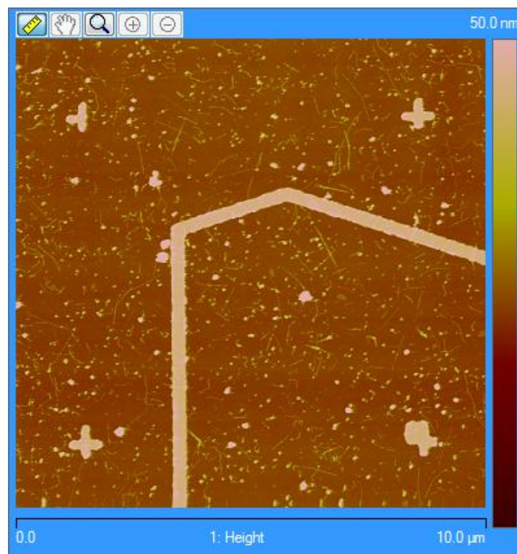


Figure 10: AFM image of CNT's on sample.

µm images are taken area by area (fig. 10).

Tapping mode is used in imaging. The resolution should be high enough so the scanning AFM tip would not jump over any tube and each tube would be drawn in image. It is required to recognize the tube diameter, ends and possible bundles or structural faults but also bigger impurities.

3.5 *Final electrode design*

Final electrodes to tubes are made using lithography as with the marker structure. The images from AFM are uploaded to the design software of SEM to get the locations of the tubes. The AFM images are slightly manipulated before uploading as the AFM tends to sheer the images a bit and the taken image is usually slightly rotated. This manipulation has been done on Gimp by using the navigation crosses of the areas. The manipulated image is uploaded to design software which can scale the image and position it correctly. The AFM image is shown on one layer through which the outline of marker structure can be seen. The location is found by comparing the navigation crosses in different layers. The AFM image is moved and scaled until the location and corresponding magnification is found. If the image needs to be rotated or sheered again it is further manipulated on Gimp (as the SEM software does not have these abilities) and tried to fit again on the SEM software.

A map is created from the AFM images to show the tube locations. The best tubes are selected for devices and drawn on a new layer of SEM software. The selected tubes have to be separated from other tubes and long enough to overcome the practical limitations of electrode designing. From the images the diameter of the tube is measures to ensure that there is just one SWCNT. The diameter should be $\lesssim 2.5$ nm and the tube should not be connected to such CNT network so that there is a risk of connecting to other electrodes.

There is a huge risk to burn CNT's during back gate sweeps. The voltage may be risen to 30 V on some measurements which would create a huge current density to a CNT and destroy it if the tube is biased too. The back gate lays under the oxide layer which should endure such voltages but the

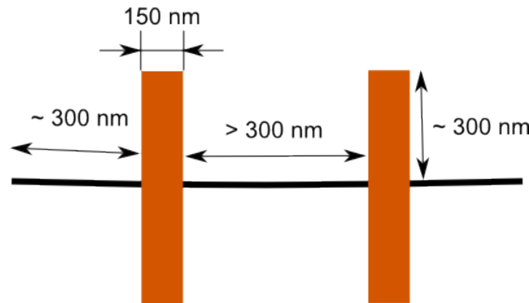


Figure 11: Some extra is left on the electrodes and to tube when a device is planned.

manufacturing process of the oxide may leave small pin holes in the layer through which a current leakage is possible. If these pin holes are under an electrode the electrode will be almost at the same potential as the back gate and the high bias will be applied also on the surface on which the devices lay on. Often a few electrodes per sample leak to back gate. The leaking electrodes disables the back gate measurement of each device to which it is connected to. In pattern design this is taken to account so that device connections with common electrodes are avoided.

The electrodes connecting to CNT have usually been 150 nm wide and almost perpendicular to tube close by the connection. Approximately 300 nm has been left for extra on both ends of the tube but also for the electrodes to cover minor misalignment of the pattern. The gap between electrodes has been over 300 nm (fig. 11). These measures have shown to be good rules of thumb for successful exposure and lift-off for us. Too small distance between the electrodes may leave metal flakes between the electrodes even though they have formed on the resist layer. The e-beam PVD tends to leave minor layers also on vertical resist walls which may connect the electrode weakly to the metal layer on top of the resist layer. When the distance between electrodes is long enough stronger acetone flow can rip the excessive metal layer away. Electrode width is compromise between minimal width and high enough durability.

As described the tube for use should be over 1.2 µm long. Good way to fit electrodes on tube is to plan contacts to the very ends of the tube and

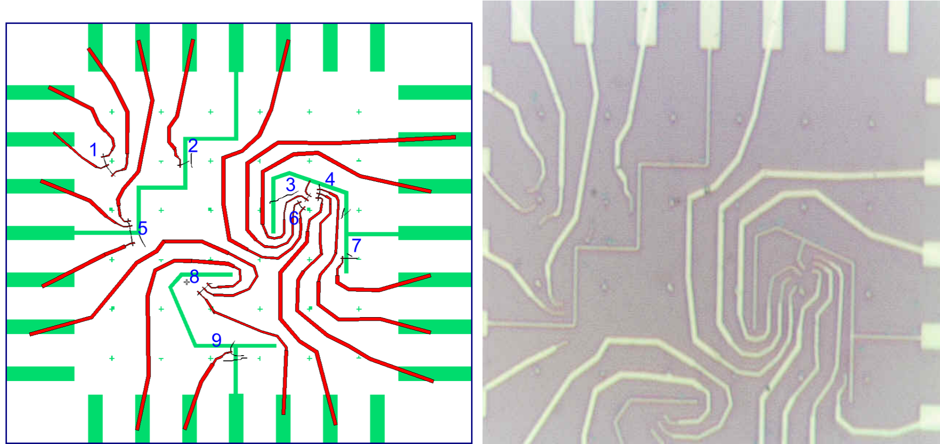
to check how much is left in between. Devices with various gap lengths are recommended and it is possible to make several electrodes per device. This way the effect of gap length can be shown.

Asymmetric connections are a specific case. The AFM imaging shows if the tube lays on an electrode of the marker structure. The tube should go over an electrode or the end should clearly lay on one. For the other electrodes of the asymmetric device the same rules apply as they did in symmetric case. Some extra should be left to electrodes and to the ends of the tube for possible alignment errors and electrode distance should be 300 nm or more. The tubes of asymmetric devices rarely are perpendicular to the electrode of marker structure. The additional contacts should be almost parallel to the asymmetric one when the distance is set. If the angle between electrodes is big, the distance between should be set according to the shortest path for the lift-off to succeed.

The final electrodes naturally connect to CNT's on the other end but the connection has to be made also to the electrodes of marker structure. As mentioned the electrode width is usually 150 nm on a tube. The wider the electrode, the more durable it is and better the contact but the size of the nanotubes prefers narrow electrodes. Solution to this is to widen the electrodes as they get further from the tube (150 nm $\rightarrow$ 500 nm). The electrodes spread apart as they approach the marker contact (fig. 12a). The spreading allows widening of the electrodes which increases the durability. The connection to marker structure is not made precisely to the end of the electrode due to the risk of misalignment of lithography. The final electrode can be pulled further on the marker structure and possible sideways mismatch can be avoided by tilting the contact angle (fig. 12a) or by making a perpendicular patch over the contact of electrodes. This allows minor alignment errors also on the marker contacts.

3.6 Exposure of the final electrode pattern

E-beam lithography is used again for the electrode patterning. Compared to marker structure manufacturing the alignment has to be made with greater



(a) Planned exposure pattern of final electrodes on red. Black lines are the usable CNTs and green pattern is the already existing marker structure.

(b) Optical image.

Figure 12: Final electrodes planned for a sample and optical image after the process is done.

accuracy. The chip is again coated with PMMA 950 A2 resist according to manufacturers instructions. The pattern laying under the resist can be seen through the resist layer on SEM although it absorbs the electrons slightly. 30 µm aperture is used in the patterning of final electrodes as high accuracy is needed. Acceleration voltage on exposure is 10 kV as it gives good enough image from the sample and is enough for the resist but also it does not harm the CNTs on the surface. The beam of SEM is focused on the level of resist surface by using nano-spherical polyester on the resist film. The spheres are deposited on the edge of the sample chip on such area where the resist thickness is about the same as in the middle but where over exposure will not be a problem.

Once the sample is inside of SEM it is searched and aligned. Rough rotational alignment is made by using the edges of the chip. Focusing of the beam is recommended to be done in the beginning as then all the alignments can be done at once without refocusing of the beam. The nanospheres are located and the beam focus is set first to bigger particles. Then the particle

is changed to smaller one and so on until particles with diameter of tens of nanometers can be seen. As the focus is found the stigmation of the beam will be adjusted. Stigmation in practice adjust the beam perpendicular to the sample surface and the SEM image becomes clearer as the shadows from objects are decreased to minimum. As the stigmation starts to look good, focus is fixed again and then the stigmation can be further adjusted. This should be done as many times as needed for the best image quality. The image quality of SEM is proportional to beam focus. When the best values are found the settings are saved.

The SEM we have used has an in-build aligning software which compares chosen points on sample to the points of existing pattern's design. In the end the machine will know the exact alignment of the sample and high accuracy exposure can be made. The alignment is done by using three same sized alignment crosses from the marker structure at the time. The centers of crosses are defined in the coordinate system of the chip/SEM and in the coordinates of pattern design. The system calculates and approximate coordinate transformation which can be checked and fixed by adjusting the cross locations on the chip one by one. The fixing goes through the three crosses by showing a crosshair where system suggests the cross to lay and the user can adjust the point. Once the patterns start to fit, alignment precision is increased by moving to one step smaller alignment crosses where the same procedure is done again.

The alignment software shows points on the sample on chosen magnification. Each time the e-beam sweeps the resist surface it becomes slightly exposed. Exposure of the close surrounding of alignment crosses does not matter but the worst case scenario is to expose some area between electrodes so that the electrodes would connect after evaporation of metal layer. It is important to keep track on the imaged location. As the alignment accuracy increases, crosses become smaller and the SEM magnification should be adjusted accordingly. On roughest alignment the crosses are easiest to see if their size is about fourth or half of the image size but the same magnification would cause dangerously big area to be exposed closer to center. Usually image magnification is estimated by comparing distances to electrode design.

The magnification should be big enough to see the cross properly despite some alignment errors but of course small enough to clearly recognize the center of the cross.

The chip alignment and beam focusing are the most important things to take care of before the exposure. After that the desired exposure layers are selected and some exposure parameters are set. To ensure proper exposure exposure dosage has to be defined according to the used resist and it's thickness. The beam current is measured from which the system will calculate the proper scanning speed in exposure. We have had some self-defined limits for the speed which seems to do continuous line but with the maximal speed. The steps size of exposure can be adjusted to reach certain speed range.

The exposure of final electrodes takes usually 40-60 sec depending on the area of the pattern. The adjustment of the exposure setting takes the most of the exposure. After exposure the pattern is developed according to the resist manufacturers instructions. The pattern is checked afterwards on optical microscope. If the exposure has not gone as planned, the resist layer can be dissolved by using acetone without harming the tubes. Then new resist layer would be made and the exposure would be done again. If the pattern looks about right, the last palladium layer is evaporated.

3.7 Evaporation of final electrodes

The final electrodes are evaporated as the marker structure was but there is no sticking layer. 25 nm palladium layer is evaporated on the exposed resist layer followed by lift-off. After lift-off the sample is checked thoroughly on the optical microscope (fig. 12b, p. 22). All the electrodes are checked for cracks and possible extra connections. If some metal flakes is left from lift-off one can try to wash them away in acetone with injection needle. Any mechanical cleaning should be avoided because the final electrodes would not endure it as they lack the sticking layer.

The damaged electrodes are taken into consideration for the steps to come. Often the devices are also imaged on AFM too, to ensure the proper connections on tubes (fig. 13). After quality check the chip is attached to

chip carrier.

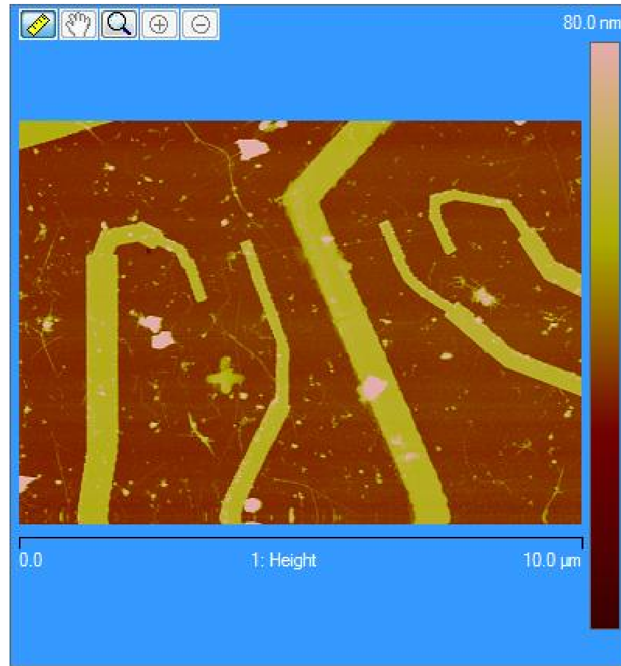
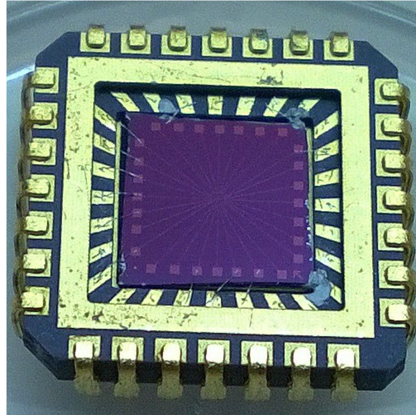


Figure 13: AFM image of fabricated device. There is one long tube with s-s-a-s-s contacts.

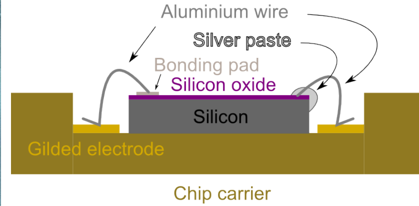
3.8 Attachment to chip carrier

Silicon chip of roughly 6 × 6 mm is difficult to handle or connect to any setup by hand. The chip is attached to chip carrier for which the measurement setup's connections are designed. The carrier is shown in figure 14a. The chip is glued in the middle using vernissa glue and electrode connections are bonded using aluminium wire. Used electrodes on the chip are bonded from the connection pads to electrodes of the carrier (fig. 14b).

Bonder has a needle and an aluminium wire going around its tip (fig. 15). The needle presses the wire against the bonding point and is vibrated with a soft ultrasonic pulse, which bonds the wire to the point. Adjustable parameters are the pressing force of the needle, power and the length of the pulse. Too high values may brake the wire but also damage the chip. Values have to be adjusted according to the bonding surface.



(a) Photograph of chip on carrier.



(b) Glued chip on chip carrier. The left bond is done on the bonding pad of the chip and the right one is done on silicon oxide and connected to the back gate using silver paste.

Figure 14: Chip carrier

The bonding point at chip carrier is the gilded end of an electrode (fig. 14b). The requirements are just to get the wire attached and there is no risk to damage the electrode of the carrier so the upper limit to parameter is just not to break the wire.

The connection to chip is trickier. The values for the bond have to be set for the bond to attach but there is a risk of braking the oxide layer between the bonding pad and silicon if too high values are used. If the oxide is broken anywhere underneath the bonding pad there will be leakage from the back gate to anything where the electrode connects to. Usually the force and power of the bond are decreased and pulse length increased when compared to bond on the carrier. The figure 14b shows this type of bond on the left.

The back gate needs to be connected also to the electrodes of carrier. The idea is shown in figure 14b on the right. The bond to the chip is made on

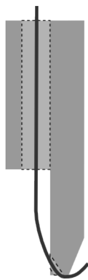


Figure 15: Cut image from the side of bonder tip. The aluminium wire comes trough the needle and around the tip. The tip has a small hole to keep the wire at right position.

the silicon oxide. The bonder needs smooth and horizontal surface so the bond can not be made directly to side of the chip. A droplet of silver paste is deposited on the bond so that it also goes around the edge and connects to silicon layer. Deposition of the droplet is done with sharpened wooden stick by hand with the help of the microscope of the bonder. Two back gate connections are made so back gate connection can be checked with resistance measurement – almost 0 Ω resistance means proper connection.

4 Discussion and conclusions

The yield of devices was low. In many cases a sample was imaged optically but also on the AFM before attaching it to the chip carrier. The alignment of the final electrodes was usually perfect, the final lift-off went well and broken electrodes were rare.

After bonding each device had resistance measurement so that the connection to CNT was ensured. The connections to tubes usually worked but in many cases too many electrodes leaked to back gate when resistance between back gate and an electrode was measured. This was done in room temperature and it was hoped that the leakage would decrease as the sample would be cooled down to about 5 K. Even in low temperatures the leakages through the oxide were too common. This would suggest that there is something wrong with the oxide layer.

At some point we started to order already oxidized silicon. The oxide layer thicknesses that we managed to fabricate were usually too thin and not uniform around the wafer. The ordered wafers did not change the situation much so we started to think if there was something that could damage the oxide.

Most likely the leakages trough the oxide layer are formed during the bonding. The used bonder was old and it had some problems with the needle control. Sometimes the needle could jump up and down during a bond as the gears and belts had gathered dust. This uncontrollable sharp movement could easily break the oxide. Other thing is that bonding needs clean surroundings including the surfaces, needle and wire. If the wire does not attach, one starts to doubt the parameters of bond and too much force can be used.

The whole fabrication process is long and there is plenty of room for errors. Each step of fabrication counts on the success of the previous steps. Functional samples can be made but it needs concentration and caution.

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