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High-frequency filtering for low-temperature thermal transport studies in nanostructures

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Abstract

Filtering of external unwanted RF-noise and thermal noise generated at the high-temperature parts of the measuring circuit is essential for successful measurements of thermal transport of nanostructures at low temperatures. This is because of thermal decoupling of the systems, i.e. the extreme weakness of thermal conduction at sub-Kelvin temperatures, leading easily to overheating even with excess power in sub pW range. We have started to improve the noise filtering in our cryogenic dilution refrigerators, which can reach a base temperature of ~ 50 mK. The miniature low-pass filters were made from special RF sealing compound Eccosorb CR124, stainless steel powder of grain size 50 μm and a typical low-temperature epoxy (Stycast). Measured cut-off frequency is at 1 MHz, low enough to cut most of the radiated RF power.

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1. Introduction

1.1 Problem statement

Since superconductivity was discovered by Kamerlingh Onnes in 1911, very many devices, of both practical and scientific interest, had been utilizing this phenomenon. Superconducting devices usually require extreme cooling, in many cases below boiling point of helium. It is also evident that the refrigeration ability of the cooling device decreases with the decrease of temperature. For example, ^{3}He-^{4}He dilution refrigerators used in this work have cooling power only several microwatts at temperatures below 0.1K and several tens of nanowatts below 0.050K. As one wants to maintain reasonably short cooling times, experimental setups are usually done with small samples.

Many cryogenic experiments need precise temperature measurements of micro- and nano-scale objects. There are variety of thermometers available to physicists working in the sub-K region. But already long ago the scientific community has turned its sight to the small-scale devices, in particular to nanoscale circuits, and to devices with reduced dimensions which have a large thermal response. The superconducting tunneling junction is one example of this kind of device. In this work, normal metal-insulator-superconductor tunnel junctions (NIS) are considered.

NIS junctions have been intensely studied since 1960s [1, 2]. Both fundamental [3, 4] and applied research has been carried out [5, 6]. Nowadays two main properties of NIS junctions are utilized in research projects of nano- and mesoscopic electronic devices. The first one is the strong dependence of NIS current-voltage characteristic on its electron temperature. It facilitates the development of electron temperature sensors for microbolometers [9] and nanodimensional structures [8]. The second property is cooling of metallic structures by means of electron tunneling. Both electrons and phonons cooling with NIS junctions have been demonstrated [9]. The physical mechanism of the cooling is based on a selective tunneling of hot electrons through the insulating barrier. When the junction is biased at voltages $V \leq \Delta / e$ (Δ stands for superconductor energy gap), only the particles with energies $E > \Delta$ can tunnel from the normal metal into the superconductor, since the states within the superconducting gap are forbidden. The on-chip cooling is essential for development of ultra-sensitive radiation sensors [9], qubits, etc.

In practice, NIS junctions are used in series to make the device symmetrical. NIS junctions are very miniature devices themselves, usually with dimensions of 100 to 500nm and several microns of supporting wires with typical thicknesses of several tens of nanometers. This yields in a very small mass of the device and thus a very small heat capacity. Assuming a junction size of 500nm by 500nm made of aluminium, aluminium oxide and copper, the mass of SINIS junction (which is simply a doubled NIS junction) can be estimated as 1.5 picograms, including 10 micrometers long supply leads. At room temperature the specific heat of copper is 0.385 J/(g·K), and thus the heat capacity of considered junction elements is about $0.57 \cdot 10^{-12}$ J/K. At low temperatures the specific heat of copper is reduced almost in 4000 times [10] and so does the heat capacity of SINIS. Thus, even an amount of energy as small as 10 picojoules accidentally applied to the cooled setup may completely ruin the experiment by increasing the temperture by 100mK.

1.2 Noise heating.

In low temperature experiments SINIS junctions are usually biased with currents up to several nanoamperes, and with a typical tunneling resistances of 10kΩ, this leads to a very small ohmic heating of the junctions. However, in real laboratory the measurement process is not ideal and biasing signal may

also carry noise of different components, which may deliver undesired power to the junction, heating it up.

The most significant contributors to the noise picture of the typical low-temperature experiment are : externally generated noise, flicker noise, shot noise and thermal (Johnson) noise [11].

External noise may consist of : 50Hz component together with its higher harmonics, or noise coming from digital electronic circuits involved in the experiment. External interference, such as communication radio frequency signals or an electromagnetic field of the power lines are usually avoided by placing the experimental setup inside an electromagnetically shielded room, and electrically decoupling it from the computers.

Flicker noise, which is also called 1/f noise, shows mostly at lower frequencies, as its power spectral density is inversely dependent on the frequency. It originates from different phenomena related to direct current. This type of noise, if coming from external circuit, together with external interference, can be eliminated by using proper low pass filters, installed in cryostat. The 1/f noise intrinsic to the tunnel junction, cannot be eliminated.

Shot noise is a type of electronic noise that may be dominant when the finite number of electrons in an electronic circuit is sufficiently small so that uncertainties due to the Poisson distribution, which describes the occurrence of independent random events, are of significance. In tunnel junctions, the magnitude of shot noise increases according to the square root of the expected number of electrons, passing through circuit. However, in ordinary metallic wires shot noise is almost completely cancelled due to anti-correlation between the motion of individual electrons, acting on each other through the coulomb force.

1.3 Johnson noise

Johnson–Nyquist noise (thermal noise) is the electronic noise generated by statistical fluctuations of electric charge carriers (usually electrons) inside an electrical conductor at equilibrium, which happens regardless of any applied voltage.

The mean-square potential fluctuation over the conductor is proportional to the electrical resistance and the absolute temperature of the conductor [12, 13]. It is independent of the size, shape or material of the conductor. It is independent of the electrical circuitry as well. Its apparent magnitude depends on the electrical characteristics of the measuring system as well as on those of the conductor itself [12].

The magnitude of the electrical noise is usually defined by the spectral density *S(ν)*. Nyqist showed [13] using equipartition law of thermodynamics that the spectral density of the voltage-noise $S(\nu)$ across the resistor R in the general case is

$$S_V(\nu) = 4R\left(\frac{h\nu}{\exp(\frac{h\nu}{k_B T}) - 1} + \frac{1}{2}h\nu\right), \quad (1.1)$$

here h is Plank's constant, k_B – Boltzman constant and T is temperature. This model takes into account the fundamental quantum nature of the noise, and the zero-point oscillations term $h\nu/2$. However, the quantum zero-point term does not carry any power. It can be explained by the fact that the opposite power is transferred from the termination resistor, even at T=0. Thus, quantum zero-point term only sets the increase of fluctuations if high enough bandwidth is considered. In this work we consider the noise power, which may influence the behavior of the tunnel junction, and not the fluctuations of the voltage readings during the measurement process. The voltage spectral density for the radiated power is then given by:

$$S(\nu) = 4R\left(\frac{h\nu}{\exp(\frac{h\nu}{k_B T}) - 1}\right). \quad (1.2)$$

When frequency is low ($\nu << \frac{k_B T}{h}$) the spectral density becomes

$$S(\nu) \approx 4Rk_B T . \quad (1.3)$$

The noise power W delivered by a conductor through a transmission line to a resistive termination R_0 is

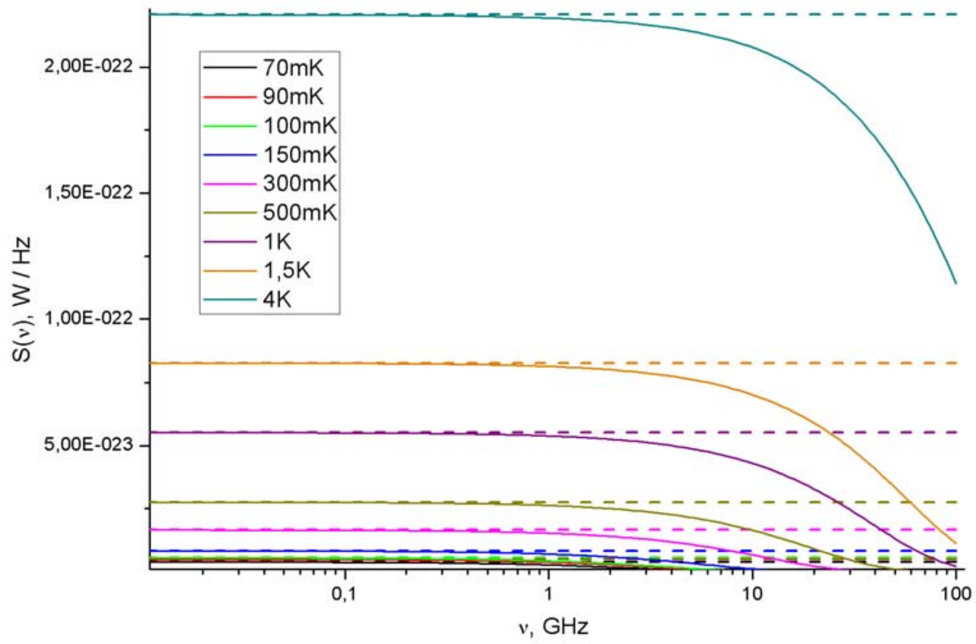
$$W = \frac{\left\langle \delta V^2 \right\rangle}{R_0}, \quad (1.4)$$

here $\left\langle \delta V^2 \right\rangle$ is squared averaged voltage deviation generated by charge thermal agitations. It can be calculated using the voltage spectral density:

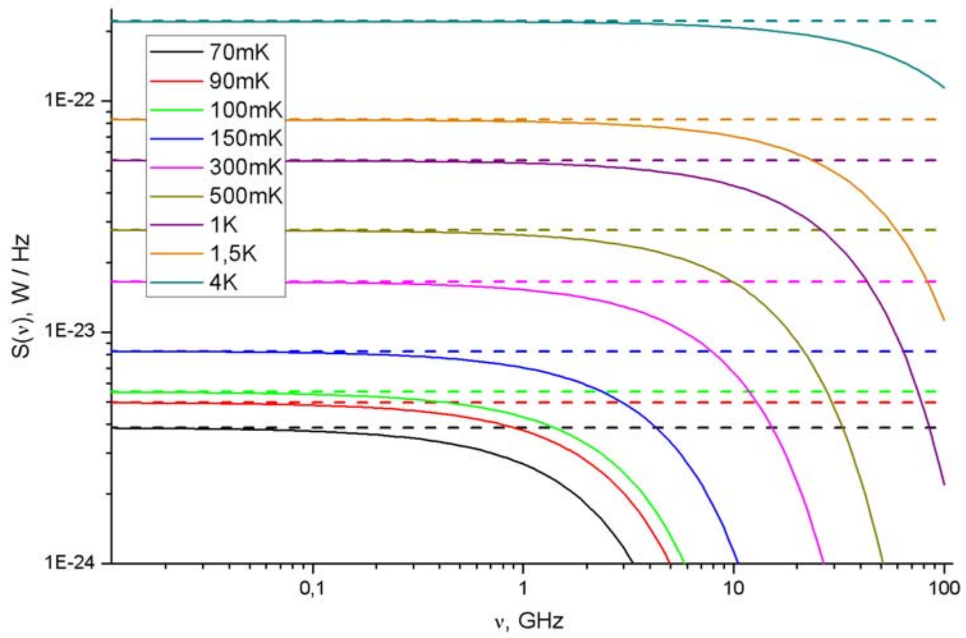
$$\left\langle \delta V^2 \right\rangle = \int_0^\infty S_V(\nu) d\nu . \quad (1.5)$$

Taking into account that the main task of this work is to construct low-pass filtering, we can consider finite bandwidth of noise power while integrating (1.5).

Fig 1.1 represents calculated power spectral density of the Johnson-Nyquist noise at several temperatures as a function of noise bandwidth. Dashed lines give the low frequency limit (1.3), solid lines represents the full formula (1.2). At the low frequency limit, the curves for the noise spectral density are flat. Therefore, the Johnson noise is typically considered to be white noise, as most measurement bandwidths are less than the crossover to quantum noise.



a)



b)

Figure 1.1. Power spectral density of the Johnson noise at several temperatures. a) Linear scale b) Log scale

In the most general case, the circuit is characterized by a complex impedance $Z(\nu)$ that has to be accounted properly instead of R_0 in equation (1.4) [12, 14].

For the low frequency limit ($\nu << \frac{k_B T}{h}$) the resistor dissipated power is

$$W = 4k_B T\Delta\nu \ . \ (1.6)$$

In general case the equation (1.2) sets the power. Fig 1.2 shows the noise power, delivered to a matched load as function of frequency bandwidth $\Delta\nu$ at different temperatures. Here, the power is measured in dBm units, which can be converted to SI (watts) using following expression:

$$W = 10^{(x-30)/10}, \ (1.7)$$

where W is expressed in watts and x is, expressed in dBm.

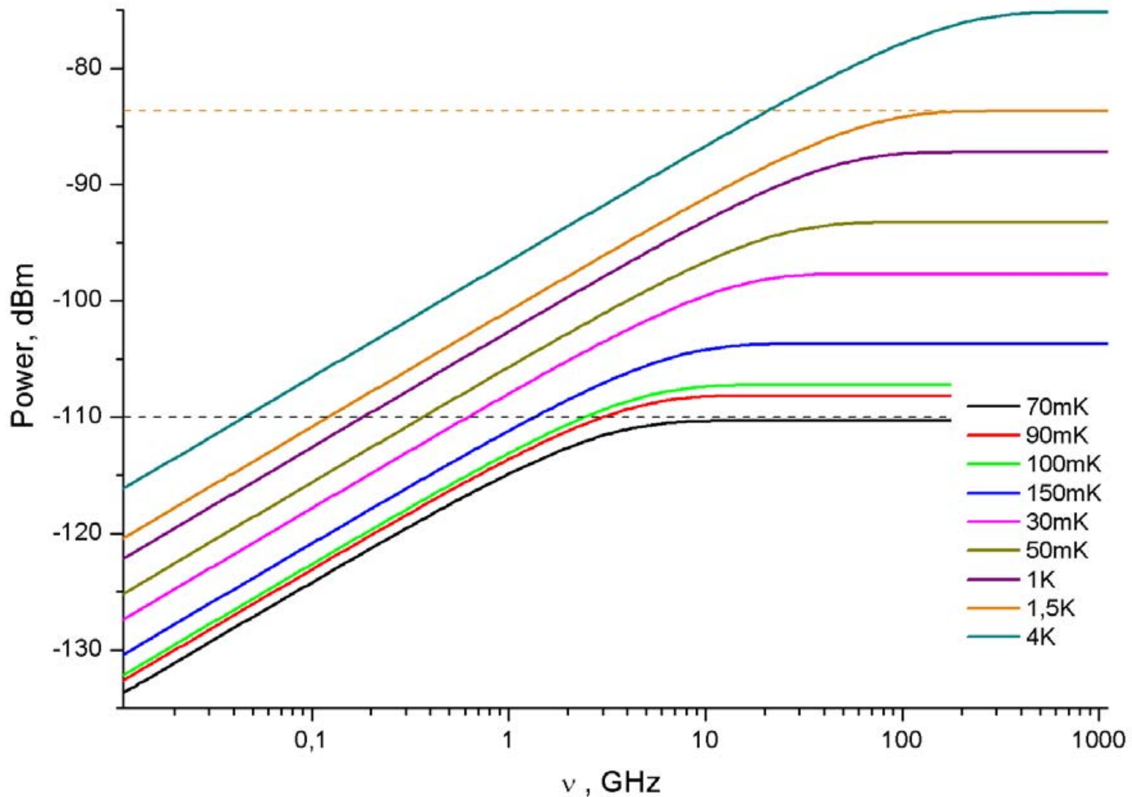


Figure 1.2. The Johnson noise power as function of frequency bandwidth.

Taking into account the fundamental thermodynamical nature of Johnson noise, one should realize that it is impossible to eliminate this noise at given temperature. When the low temperature experiment is considered, there are sources of thermal noise of different temperatures from different stages of the cryostat. It can be seen from Fig 1.2 that a matched resistor at 4K generates more than 30pW (-75 dBm) of noise power and 4pW (-84 dBm) at 1.5K. This power can be transferred further to the circuit elements and make the electron gas in metals to reach possibly the same temperature as the noise has. When a tunnel junction is a part of the circuit, this power can cause an extra increase of its

electron temperature that is often undesirable. This heating leads to changes in tunnel junction electrical behavior, making it impossible to use as a thermometer at the lowest temperatures. Other possible consequence of the noise heating may be seen as the so called leakage current in the sub-gap region of the superconductor of tunnel junction. The broadening of the density of states is often introduced in tunnel junction phenomenological model because of that (see section 3.3).

One possible solution to this problem is to install filtering directly at the lowest temperature stage of the cryostat. According to Figures 1 and 2 one can see that the noise power increases if high frequencies can be transmitted. Filtering at frequencies over several tens of GHz is challenging, as regular filtering elements, constructed with passive electrical components (resistors, capacitors and inductors), offer only very limited attenuation at high frequencies. Very special filtering techniques have to be involved. Miniature cryogenic metal powder filters are considered in this work.

Another way of filtering is suggested in references [15] , [16] and in particular in ref. [17]. There authors used RC filters with capacitive and resistive elements fabricated directly on the chip surface. This useful approach is also implemented in the present work.

2. Cryogenic setup.

2.1 Refrigeration

2.1.1 Equipment

Low-temperature experiments mentioned in this thesis were performed with a home-made plastic dilution refrigerator (model PDR-50) [6, 18, 19]. First, the sample was mounted on the sample stage, which was attached to the refrigerator. After placing the vacuum can, sealing it and checking the vacuum leaks the cryostat was precooled with liquid nitrogen to 77K, maintaining coarse vacuum inside the jacket. At 77K the 0.5mbar of ^{3}He were introduced to the environment inside the vacuum jacket. Next precooling with liquid Helium to 4.2K was done. As ^{3}He has lower boiling point than ^{4}He, at 4.2K it stays in gaseous form and is easily pumped away before further cooling. After this the dilution refrigerator was driven to achieve base temperature of 70mK.

The dilution refrigerator is a closed-cycle unit, allowing continuous cooling operation. The principals of dilution refrigeration can be found in many low-temperature physics books such as [11, 20, 21]. The unusual phase separation between ^{3}He and ^{4}He at low temperatures is the quantum physical effect that allows performance of dilution cooling (Fig 2.1) [20].

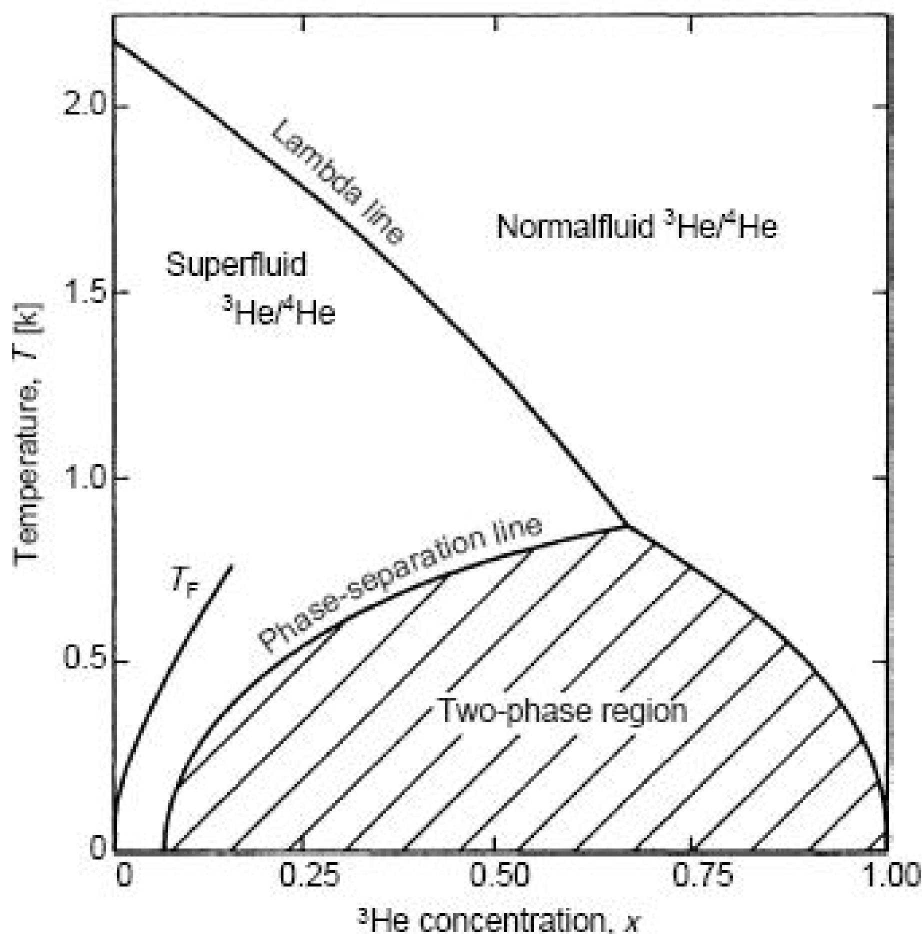


Figure 2.1. Phase diagram of liquid -^{3}He–^{4}He mixtures at saturated vapor pressure. The figure is taken from [20].

The schematic picture of the dilution refrigerator used in this work is shown in Fig 2.2. The dilution refrigerator has two thermally decoupled chambers, which are connected by means of input/output tubes. The upper chamber is called still and the lower one is called mixing chamber. The sample stage is thermally anchored within the mixing chamber. Another key component of the dilution refrigerator is the heat exchanger. The heat exchange occurs between the liquid helium that passes along the input tube and the liquid passing along output tube. The still, mixing chamber and heat exchanger can be made of metal as well as being plastic. Plastic heat exchanger, for example, has lower thermal boundary resistance than metallic one [20]. So less heat is reflected from the walls and lower temperatures can be reached. The tubular heat exchanger comprises a rod having one spiral groove from one end to the other. The groove accommodates plastic capillary (input channel). The output tube of the heat exchanger, which is used for the transportation of diluted ^{3}He away from mixing chamber, is located exterior to the input tube. The diluted ^{3}He is absorbing heat from ^{3}He-rich phase and prevents heat flow from the higher temperature stages. More information about plastic heat exchanger can be found in [22].

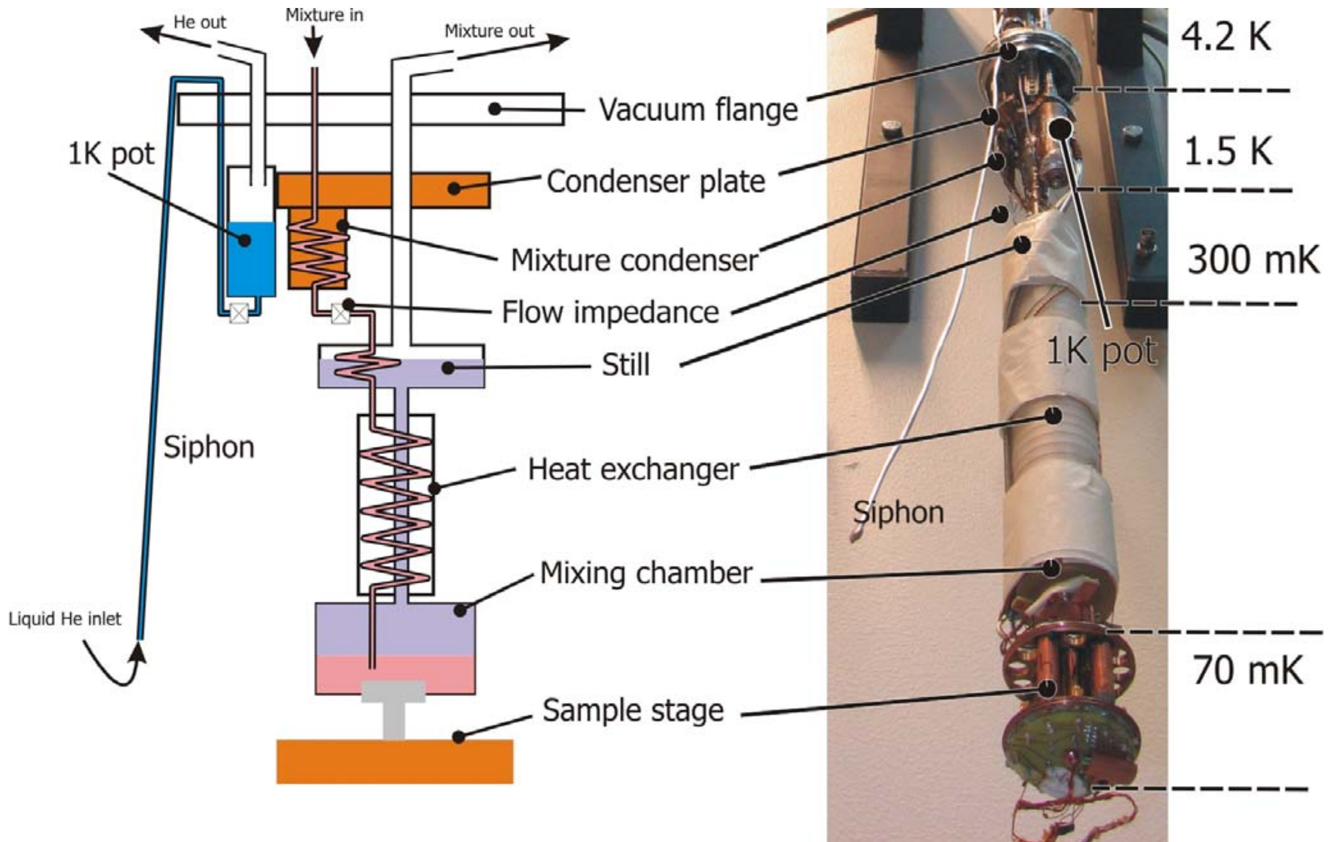


Figure 2.2. The schematic picture of the plastic dilution refrigerator Nanoway PDR50.

Circulation of ^{3}He is achieved by pumping the system at room temperature. Room temperature ^{3}He gas is precooled by the 4.2 K ^{4}He bath. Then the gas goes towards a ^{4}He evaporator called the pot. It is condensed there at 1.5K by forced pumping of ^{4}He from the bath. After that it has to go through main flow impedance, where sufficient pressure is achieved, so that liquefied ^{3}He must enter a heat exchanger, which is in the thermal contact with the still at 0.7K. After that, the liquid enters secondary flow impedance and passes to the next heat exchanger, where it is cooled by means of dilute phase that goes away from mixing chamber, as it was discussed already above. After being cooled there, the liquid ^{3}He enters finally the mixing chamber.

Initially the dilution refrigerator contains homogeneous mixture of ^{3}He and ^{4}He at 1.5-2K. At these temperatures, the mixture is homogeneous regardless of the ^{3}He/^{4}He concentration ratio. The liquid fills the input tube, the mixing chamber, the output tube and part of the still. The low pressure gas is pumped from the still, in equilibrium with the free surface of the liquid, and is compressed at the room temperature pump. A low impedance pumping line extends from the still to an external pumping system and further to the output line to form the closed-cycle pumping circuit. As soon as gas circulation starts, the temperature of the liquid drops. Below temperatures of 0.87 K the two liquid phases finally separate spontaneously to a normal fluid phase rich in ^{3}He on top of a superfluid phase rich in ^{4}He. The phase richer in ^{3}He has smaller density and floats on the top of the ^{3}He dilute phase and is pumped out and recondensed, filling the output tube and still. Since the vapor pressure of ^{4}He is lower than vapor pressure of ^{3}He, soon only ^{3}He is circulating and the temperature of the still drops to ~0.3K. But at this temperature the pressure of ^{3}He becomes very small and circulation nearly stops (being activated only by the heat leak from exterior to the refrigerator) and to cool further , external heat must be applied to the still to maintain the circulation.

The equilibrium concentration of ^{4}He diluted in ^{3}He is essentially zero while ^{3}He diluted in ^{4}He reaches 6.5% even at zero temperature [20]. In the mixing chamber the concentrated ^{3}He is in the equilibrium with diluted ^{3}He. Now if one tries to decrease the limiting concentration of ^{3}He in ^{4}He at fixed temperature by pumping the chamber, pure ^{3}He will cross the boundary and reestablish the equilibrium concentration. This process requires energy so heat will be absorbed and the temperature of the chamber together with its content will be lowered. To maximize the evaporation rate of ^{3}He, a resistive heater of the still is used. The largest cooling power is achieved when the mixing chamber temperature is very close to the temperature of concentrated phase entering the mixing chamber. For this purpose sometimes very large area heat exchangers are used, namely sintered silver plates.

2.1.2 Wiring of the refrigerator.

The refrigerator used in this thesis has eight measurement lines and seven technological ones. Measurement lines are filtered at several stages. Starting from room temperature to 4.2K all lines are made of manganin wires. Prior to entering the vacuum jacket they are connected to LC-filters (cut-off frequency of 250 kHz). From 4.2K to the 1K pot measurement lines enter a solder joint in the vacuum jacket flange as Thermocoax cables, which additionally filter the high frequencies. Technological lines are coming to the 1K pot as manganin wires through an epoxy feed through. At the 1K pot, the measurement lines enter a microstrip filtering box, where signals are passed through conducting meander on a thin film, surrounded by metal powder - epoxy compound. From 1K pot all lines continue as twisted pairs of high resistance manganin wires to the sample stage, where special high-frequency filters are installed (see section 2.3). Manganin wires are used because of low electrical and thus low thermal conductivity. However, the use of superconducting wires may be also considered. Twisted pairs of manganin wires are wound around the plastic heat exchanger to cool efficiently, assuring that at the lowest temperature end of the cryostat all lines do not introduce unnecessary heat load to the refrigerator.

Temperature of the sample stage is measured with a Ge resistance thermometer GR-200A-3 from Lake Shore Cryotronics, whose resistance is read by a Picowatt AVS-47 resistance bridge. The temperature of the sample stage could be set to required value with the use of resistive heating at the low-temperature end of the cryostat. One 1 kΩ resistor was installed at the sample stage. The power supplied to the resistor to maintain the constant temperature was controlled by PID controller, implemented in the measurement software.

During the measurements, the refrigerator and measurement electronics were placed inside of the electromagnetically shielded room. Measured signals were amplified by room temperature Ithaco Low Noise (1201/1211) voltage and current preamplifiers, and their output was read by an analog to digital converter and transferred to the computer by an optical fiber, to avoid electrical contact between the computer and the measurement electronics. The data acquisition electronic board was read through the GPIB interface by specially developed program in LabView software environment.

2.2 Filters.

2.2.1 Problem definition.

The properly designed cryogenic experiment has to employ several kinds of filtering units. The reason for that is the fact that there is no filter that can achieve suitable attenuation over wide range of frequencies.

Although anchoring the lines to heat sinks reduces the noise they generate, the lines themselves are the things that should be always remembered while designing low temperature filtering. The noise coming from parts at higher temperature can be handled in principle with reflective-type filters. However, reflective-type filters are not adequate, because their performance is very sensitive to impedance

mismatches in the rest of the line, which causes spurious transmission resonances. Therefore, one must typically choose dissipative type filters [23].

It is necessary to filter out the most of the Johnson noise that comes from the hot parts of the cryostat in the form of voltage noise through the measurement lines.

The last filtering stage must be installed at the lowest temperature stage, directly before the sample mounting. This is needed to ensure that the sample will not be exposed to the voltage noise of the filter itself, whose effective electron temperature is mostly higher than phonon temperature of the sample.

In this work in our dilution refrigeration setup the last stage, where the wiring is thermally anchored is the 1.5K stage. Thus, an estimation for the unwanted noise power coming to the sample is 4pW (-83dBm) with the full noise spectrum (see Fig 1.2). The cumulative power spectrum depicted in Fig 1.2 also indicates that the most of the noise power comes in a frequency band starting at ~ 100MHz . Frequencies lower than 100MHz are not important because the thermal noise of sample stage wiring itself at the lowest temperature (for instance, 70mK) is producing the same power in the full frequency range as the 1.5K wire noise low-pass filtered at 100MHz (-110dBm). The estimation of the highest noise power that may reach the sample is difficult, and thus we often use 4K thermal noise as an upper limit.

Thus, in order to fulfill good conditions for lowering the electron temperature one has to manufacture high-frequency filters with very high attenuation for the desired frequency range (tens of Gigahertz).

Another function of filters is to conduct away the heat generated from dissipated microwaves. Filters have to be connected to the thermal bath with low enough thermal impedance. This may be achieved with increasing amount of thermo-conducting material. Also one should take into account the finite cooling power of the cryogenic refrigerator, as well as space and mass limits for the lowest temperature stage of the assembly. Thus, a compromise must be found between high thermal conductance and space limitations.

Summarizing, our first task was to manufacture a set of cryogenic low pass filters, effective above 100MHz, having attenuation of at least 60dB and being compact and simple.

There are various ways to solve this problem. Several common solutions are discussed below.

2.2.2 Filters overview.

One obvious way to construct filters is to use RC , RL or RLC – filters. However, these designs do not have satisfactory attenuation over several GHz. Below we review and compare different types of filters.

RC filter.

Each measurement line can be equipped with a resistor and a capacitor (see Fig 2.3 a). This installation is very compact. A properly chosen resistor can change its resistance only a few percent upon cooldown. However, the capacitance can decrease significantly due to the temperature dependence of the dielectric constant in the capacitors [23, 24].

RLC filter.

An inductance can be added to the previous filter in series with the resistor to get more attenuation. This filter has the same advantages and disadvantages as the RC-filter.

On-chip version of RLC filter fabricated by means of optical lithography was presented in [23]. The filtering element is a distributed RLC meander line. The goal of this element was ~ -80dB at tenths of GHz measured at room temperature [23]. However, these filters are difficult to handle and may not withstand thermal cycling.

LC filter.

Since there are no resistive components, attenuation is almost zero up to the filter cutoff frequency. This approach includes also Pi-filters, which have two capacitors (see Fig. 2.3 b) and offers at least 30dB per decade attenuation [23].

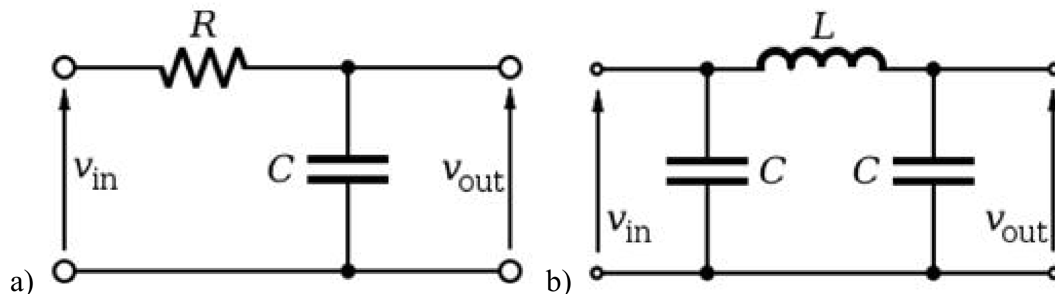


Figure 2.3. Schematis of the simple electronic filters. a)RC low-pass filter b) LC Pi-filter The figure is taken from [16].

THERMOCOAX.

The Thermocoax® was originally developed as a vacuum compatible heater cable but was found to be highly suitable for filtering in cryogenic applications [25]. It shows the typical square-root dependence skin effect without sharp cut-off regions [24, 25].

The center conductor is made from nickel/chrome and the outer conductor is stainless steel. The difficulty of soldering NiCr and stainless steel connectors as well as hygroscopic core of the cable make the usage of Thermocoax less attractive.

The cable with 0.5mm outer diameter measured at room temperature showed 200dB/m attenuation at 20GHz as reported in [25]. At 4.2K similar cable showed ~100dB/m attenuation at 8GHz, while achieving ~20dB/m at 300MHz [24].

However, in order to get reasonable attenuation one has to use the length of the Thermocoax cable of at least 1m. In terms of the present task, this long cable has to be situated at the lowest temperature end of the cryostat for each of the 16 lines. This construction would be too bulky to fit the space limitations and meet the cooling thermal mass requirements.

Twisted pair filter.

This filter consists of a twisted pair of resistive wires wrapped tightly in copper tape. The copper tape acts both as a shield and as a ground to which the lines are capacitively coupled. The copper tape is pressed around the wires very closely so that the distance between the wires and the shield is that of the insulator thickness on the wires, about 10 microns. Thus there is a certain capacitance from the wires to ground as well as between the two wires in any given pair. This capacitance to ground combined with the high resistivity of the wires makes the cable a continuous RC line. In [26] 1.87m long copper filter with capacitance 210pF/m achieved less than -80dB attenuation at 20GHz being measured at room temperature [26].

This kind of filtering could be made with zero DC resistance if superconducting materials were used [27].

Again, the space limitations in current task make this design impossible to implement.

Metal powder filter

Another common method is to use metal powder filters. In general, the low-pass metal powder filter is an insulated wire surrounded by fine metal grains. The attenuation of a signal occurs due to the dissipation of high frequency current induced in the grains. The large surface area of a metal powder

results in significant skin-effect damping. Attenuation depends on several parameters, such as the powder material, the size of the grains, and the diameter and length of the wire. Stainless steel powder is often used. Also available on the market Eccosorb line of microwave absorbing materials. They are often chosen because of the possibility to get different magnetic-loading and dielectric embedding.

In ref. [24], the stainless steel powder filter in a cylindrical geometry with an SMA connector was discussed. The goal of this filter performance was more than 50dB attenuation at 1GHz measured at 4.2K. It was fabricated by drilling a 45mm long hole, 5.3 mm in diameter, through a copper block. 1.4 m of the copper wire was wound into a spiral around a tube with diameter 3.5 mm. Half of the spiral was counterwound to reduce the magnetic field pick up. One end of the copper wire was then soldered to the center pin of one connector. For proper performance of the filter, it was important that the coil had a constant pitch over its entire length in the powder and that it was not deformed. The center conductor was thereafter sealed with epoxy. After soldering and sealing the other connector, stainless steel powder was filled into the filter. The empty space over the powder was filled with epoxy and the remaining connector was pressed into place. Due to this fabrication process, these filters were inherently strongly asymmetric with respect to their reflection properties [28]. In the final filter most of the powder was loose inside, since the epoxy could not penetrate the densely packed powder. This might help to reduce stresses in the filter during cooldown. However, if the epoxy cracked, the fine grain metal powder would be spread over the sample stage area, making fatal contamination of the cryostat.

The stripline geometry simplifies the filter fabrication. It supports a TEM mode at low frequency, with higher order modes appearing when the enclosure begins to act as a waveguide. The study on stripe-like filters made of different Eccosorb materials is done in ref. [29]. Authors used the FGM-40, GDS, and MCS materials, which are magnetically-loaded silicone sheets, as well as the Eccosorb CR-124 material, which is a powder-loaded epoxy. There, the magnetic loading material is carbonyl iron or ferrite powder, or a combination of the two. Authors used rectangular enclosure, machined in a block of copper, had length 32mm, width 12-13mm, height 1.5-4.6mmm. It was filled with absorbing material. SMA receptacles with an extended dielectric and pin contact were mounted on each end of the copper block such that the pins extended into the center of the enclosure. The 0.15mm copper foil strip connected the pins. The examination presented in [29] showed that the epoxy-based CR-124 material has ~ -80dB attenuation at 4GHz measured at 4.2K. Analyzing thermal and filtering properties of the considered materials, the authors suggested that CR-124 is the most suitable material for sub-Kelvin measurements.

Bronze powder low-pass pi-section filters are used in low frequency current bias lines in qubit experiments [30]. They are essentially easy to heat sink. 0.105 in. diameter bronze powder/epoxy rod that is 6 in. long was made using a simple straw as a form and injecting it with a bronze powder/epoxy mixture. After hardening, Cu-clad 0.005 in. diameter NbTi wire was space-wound around the rod and glued with varnish. The total length of NbTi wire was roughly 20 ft. Then, 0.031 in. diameter cotton string wound spacer was glued in a coarse helix on top of the NbTi wire to center the rod when it is pushed inside the brass tube. The thickness of the string was chosen to give a tight fit. The brass tube was 0.218 in. o.d. x 0.015 in. wall x 6 in. long. These filters were made using SSMC "nanohex" connectors and 0.01μF surface mount capacitors with an NPO dielectric, and therefore the capacitance did not change much with temperature. Two housings at the two ends of the filter partially filled with Stycast 2850 epoxy provided the thermal contact to the metal powder/epoxy rod and protected the electrical connections inside the housings. At 4.2K, the bronze pi-filter showed ~ -40dB attenuation at 3MHz.

Pi-filters with powder core

Taking into account the strong and weak points of the already developed cryogenic filters, the decision was made here to manufacture miniature LC Pi-filters with metal powder core. Main concept of the filter design is described very well in Ref. [31].

There are two main ways to surround a central wire with a metal powder: to use a pure powder or to mix it with epoxy. Since the metallic powder filter placed at low temperatures are used not only for the noise elimination, but also to thermalize the electric leads coming from the high temperature parts of a cryostat, the epoxy Stycast 2850FT mixture with the metal powder could be used. In this case the attenuation is a little less, but the thermalization of the central wire is much better.

One simple approach to make metal powder filters is the following. First, one usually prepares a coil using a thin insulated wire. To do this, one can take a rod, wind a wire around it, and after that remove the rod from the coil. Then it is necessary to place the coil into a metal box and fill its volume, both inside and outside the coil, with a mixture of metal powder and epoxy. Finally, it is essential to solder and mechanically fix the connectors and to close the jacket. As the epoxy may have relatively high viscosity, there is a risk of obtaining a nonhomogeneous spatial distribution of the powder due to the appearance of air bubbles. Together with a nonideal coil shape, this can result in additional unwanted resonances on the transmission characteristics of the filter. Moreover, due to the high viscosity of the epoxy it is difficult to fill the coil with a mixture with high enough powder content. Even if the powder-epoxy mixture is carefully degassed under vacuum, air bubbles are trapped during the process of pouring and casting.

Taking the above issues into account, a different approach was chosen.

2.2.3 Filter fabrication

Eccosorb rod

First, a set of rods of powder-containing material was prepared. It was not evident that use of Stycast-2850FT in mixture with stainless steel powder would result in the best filtering properties. As a result, two sets of rods were prepared. One set was made out of the mixture of Stycast 2850-FT and metal powder and another set was based on the commercially available material Eccosorb CR-124, made by Emerson & Cuming.

Eccosorb CR-124 is an epoxy resin loaded with iron powder. It has very good absorption properties for electromagnetic radiation at high frequencies. Among other series, CR-124 is intended for use in lowest frequency range from 5GHz and higher. This series has also the highest mixing ratio for epoxy base and curing agent, which results in hardly pourable product, as the epoxy base has high viscosity itself. The recommended curing schedule requires heating of the epoxy to 75°C during 12 hours. The experimental analysis in Ref. [32] shows for this epoxy that “the cooling capacity required to cool Eccosorb CR-124 from 4.2 (1.6) K to 50 mK is approximately 6.2 (5.4) times smaller than the cooling capacity required to cool an equal mass of copper from 4.2 (1.6) K to 50 mK “. The authors also estimate that the mass fraction of the iron filler in Eccosorb CR-124 could be as high as 60%.

Eccosorb epoxy base was warmed up to 70°C using water heat bath on thermostabilized magnetic stirring device. A PVC cup containing 20g of epoxy base was immersed into 30ml of hot water in wide and low-height chemical glass. The heating process was done inside a fume hood to prevent excess water vapor condensation on the epoxy, and was controlled manually with the help of remote electronic thermometer. The epoxy base slightly lowered its viscosity in the hot state. Next, 0.4g of hardener was added to the cup and manually mixed with the help of clean plastic rod. Mixing was done for 2 minutes after which the mixture was taken out of the hot water bath and put under vacuum conditions (5-7 torr) to eliminate trapped air bubbles. The vacuum treatment lasted for 120seconds, during which the material cooled down and substantially increased its viscosity, making further bubble flow difficult. After degassing, the epoxy was heated and poured into a preheated mold of cylindrical shape. The epoxy was cured at 75°C for 12 hours.

Pi-filter

During the second step, the internal parts of the filters were made.

After curing, the resulted rod was machined into small bobbins, 4mm in diameter and 15mm long with 5mm diameter flanges. One layer of copper wire was used to make a coil (see Fig. 2.4) The coil consisted of 114 turns of 0.05mm insulated copper wire, with no separation between turns. Direct calculation gives a number of 300 turns to be made, but one must take into account the thickness of insulation and the necessity to leave a gap between the coil and the flange of the bobbin. The wire escaped the bobbin through a 0.5mm notch purposely made in each flange and was glued to the ends of the bobbin with GE IMI 7031 varnish.

Pi-filters require capacitors to be installed on both sides of the coil (see Fig. 2.3 b). Regular SMD components could not be used, as the targeted frequencies to be filtered are in the range of 10 GHz and higher. At such a high frequencies significant power can pass through the circuit element and hit the sample. As filters were designed to have axial symmetry, the decision was made to use discoidal capacitors, as they could improve noise confinement inside the filtering volume. Also components of this type are made of ceramics and have low thermal expansion coefficients, and are thus suitable for applications at cryogenic temperatures. Miniature discoidal feed-through capacitors were purchased from Pacific Aerospace & Electronics (PA&E) company, part number FC200N472M500-050-050-C. The capacitance value is 4.7nF. These capacitors with dimensions of 5mm in diameter and 1mm in height could be glued with varnish to the coil ends.

The copper wire wound onto the spool was pre-tinned and soldered to the inner electrode of the capacitor on one side of the filter core. At the other side, a miniature MCX connector was soldered to the capacitor first. Prior to soldering the connector, all the pins were cut down to make the soldering side flat and round, except for the central pin, which was left 1mm long. Finally, the central pin was soldered to the capacitor center electrode and the shell was soldered to the outer, ground electrode. The signal is carried through the central electrode of the capacitor to the central pin of the connector.

Figure 2.4. Filter core with copper coil, two capacitors and one MCX connector. The schematic picture of the discoidal capacitor is also shown (capacitor image is taken from the PA&E official catalog).

Packaging

Finally, the filter was packaged into a copper shield, consisting of a 26mm long tube with outer diameter of 6mm and inner diameter of 5.5mm. Copper was chosen, as it is a material with high electrical and thermal conductivities, is non-magnetic and non-superconductive, as magnetic fields trapped inside superconductor could significantly influence experimental results. The softness of copper makes it very difficult to machine cut the tube with such thin 0.25mm walls, and special attention has to be paid to the inner surface quality and roundness of the tube.

The filter core was inserted into the copper tube so that the end with the capacitor without the connector was immersed into the tube by half of the capacitor's height. The filter core end with the MCX connector was carefully filed free of solder leftovers, in order to fit the 5.5mm diameter hole tightly. However, an air gap of 0.65mm would be left between the copper tube and the wire winding, which could serve as a waveguide for high-frequency radiation. One straightforward way to block this radiation is to supply Eccosorb into the gap. But extreme viscosity of the hardened Eccosorb leads to formation of air pockets and uneven filling of the tubular airgap. Thus, the decision was made not to use Eccosorb but use epoxy loaded with stainless steel powder (SSP) instead. Stycast 2850FT with Catalyst 24LV was loaded by fine 50 micron stainless steel powder 50% by weight. After mixing the epoxy primer with

catalyst and powder, it was kept under vacuum in order to remove air bubbles trapped into the viscous mixture during mixing.

Degassing of the epoxy mixture should be done in pulsed way. When a highly viscous mixture is first exposed to vacuum conditions with pressure lower than 100mbar it may raise a foam rapidly and evenly in the mixture volume, and contaminate the vacuum chamber with epoxy. Pressure should be lowered in a slow, controlled manner to keep the foam inside the cup container. After the first foam formation, one should leave the chamber at constant pressure for a short while, so that larger air bubbles have time to float to the mixture's surface. If one fills the vacuum chamber with atmospheric pressure at this point, the foam inside the mixture volume will fall but the floated bubbles will decrease in size and rest on the sidewalls of the cup, inside a thin layer of mixture. During the next vacuum exposure, these sidewall bubbles are more likely to burst efficiently before the main volume foam rises for next time. Epoxy degassing should not be done continuously for a long time, as it increases its viscosity over time both by hardening, which is normal process, and by evaporation of the hardener, which may lead to poor quality product.

Powder-epoxy mixture was finally applied into the air gap by a narrow syringe with a short needle. The filter core was moved inside the copper tube simultaneously while applying the epoxy mixture. The epoxy was left to dry for 24 hours at room temperature. Filter was left in a vertical position with the MCX connector pointing down, as the solder leftovers at this end were serving as stopper, preventing epoxy release.

2.3 Sample stage.

In order to incorporate new microwave high-frequency (HF) radiation filters into an existing dilution refrigerator, a new sample stage was designed. The machine drawings of the sample stage are shown in Appendix A.

The design objectives that had to be reached for the sample stage included placing of 16 HF filters into a limited space. The vacuum jacket of the cryostat restricts the size of the sample stage to a cylinder with diameter 40mm and height 55mm with sample cover attached. This space has to accommodate not only the filters but also the necessary supporting structures and mounting hardware, as well as provide sufficiently easy access for repairing.

In the sample stage design most elements have cylindrical symmetry with their axes aligned along the cryostat main axis. A photograph of the assembled sample stage half-filled with filters is presented in Fig 2.5.

The sample stage consists of two plates with holes to accommodate filters. Both upper (marked in Fig 2.5 as 1) and lower (2) plates have sixteen holes (3) for filters (4) and connectors (5) and one central 4mm hole for central rod (6). The bottom plate has M4 thread in the central hole, so that the threaded central rod can be twisted in there. The bottom plate is filled with complementary ("male"-type) MCX connectors (5) that have their center pins soldered to the PCB (7) containing thermally anchored place and electric contact pads for the samples.

Due to the fact that even single MCX connector is engaged very tightly, handling of 16 of them must be done very carefully. Central rod serves to this purpose. It is restricted from movement along its axis in the upper plate, and when it is screwed in to the bottom plate MCX connectors are engaged. The central rod also serves as an additional thermal link between upper and lower plates.

Holes for the filters are placed symmetrically in order not to unbalance the sample stage. Upper plate is equipped with a perpendicular support element (8), which is tightly fitted to the mounting silver screw, which is attached to the mixing chamber sintered plate of the cryostat. As the mixing chamber is constructed from plastic inside heat exchanger, there is a plastic-to-metal interface at the point where the silver mounting screw enters the plastic part. Any off-axis load applied to this interface may create a leak

that can lead to ^{3}He-^{4}He mixture loss from the mixing chamber. Also any uncompensated strain of the plastic heat exchanger can induce its permanent bending and make the sample stage to touch the walls of the vacuum jacket.

All supporting structural elements were made of copper to ensure good thermal conductivity. Filters were tightly fitted to the holes of the top copper plate and glued with the Stycast 2850FT from one side, and with silver-containing conductive epoxy at the discoidal capacitors end. Both copper plates have an outside thread, designed for sample cover cap that can be attached. Covering the sample area below lower copper plate makes the volume shielded from thermal radiation and unnecessary electric signals. Thus, the only way for the measurement signals to enter the sample stage is through the metal powder filters. Measurement lines as well as technological lines that are wrapped around the plastic heat exchanger are soldered to an intermediate cross-like PCB (9) for ease of repair, as high resistance manganin wires are very brittle and should not be bent many times. Starting from the PCB down to the filters, copper wires are used. There is no reason to restrict heat conduction by wires at this segment, as the cross-like PCB is already anchored to the lowest temperature end of the cryostat.

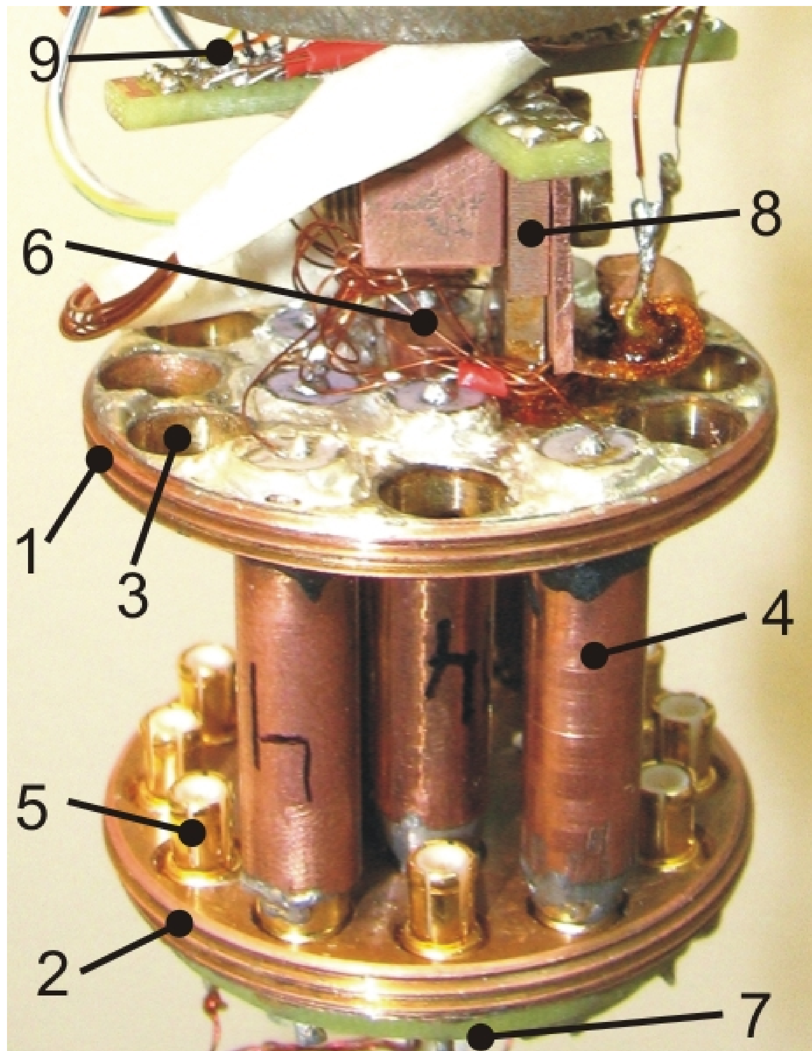


Figure 2.5. The scheme of the sample stage. 1 – upper plate; 2 – lower plate; 3 – hole 6mm in diameter; 4 – metal powder filter in a shield; 5 – MCX connector; 6 – central rod; 7 – PCB with contact pads; 8 – support element; 9 – intermediate cross-like PCB.

2.4 Evaluation of high frequency filters.

All filters were measured independently for their frequency response using a vector network analyzer ANRITSU 37369D, which is capable of measurements from 40MHz up to 40GHz. In terms of S-parameters, S_{21} characteristics of each filter were measured.

Measurements were done at room temperature and at 77K, however the lower temperature results were not qualitatively different from the room temperature ones. The resulting frequency response curves are shown in Figs 2.6 – Fig 2.11 . During the measurement the input power level was set to –6dBm (0.25mW). Due to the fact that each filter does not have connector at one end by design, the MCX connector was soldered to that end purposely for measurements and desoldered before installation to the sample stage. Measurement lines of the network analyzer were equipped with SMA connectors by default, and SMA-to-MCX interface connectors were used.

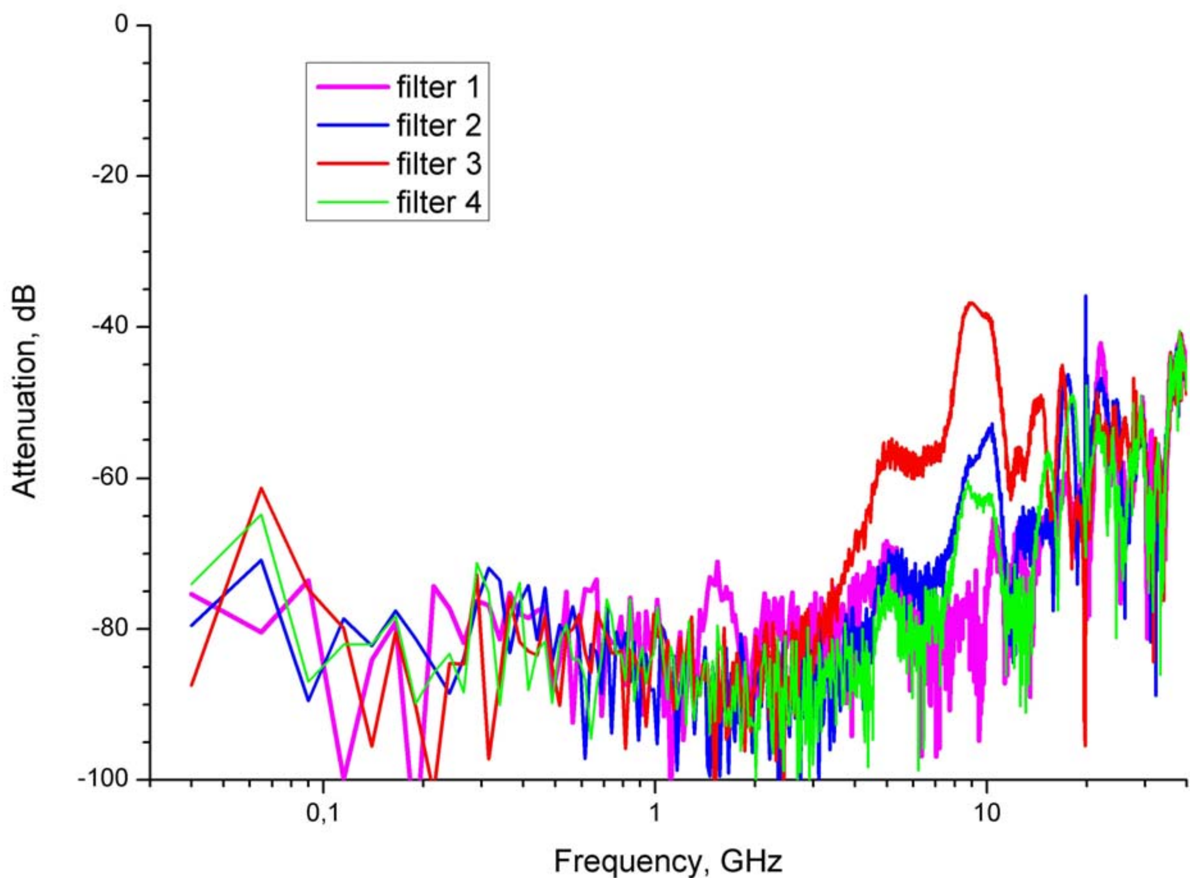


Figure 2.6. The frequency response of the filters marked 1, 2, 3 and 4.

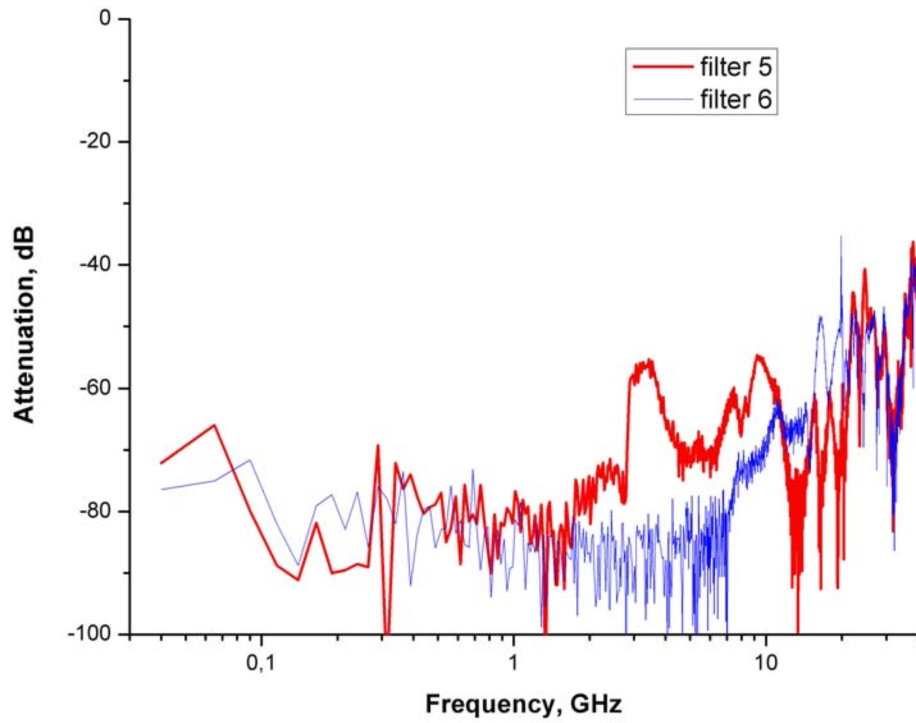


Figure 2.7. The frequency response of the filters marked 5 and 6.

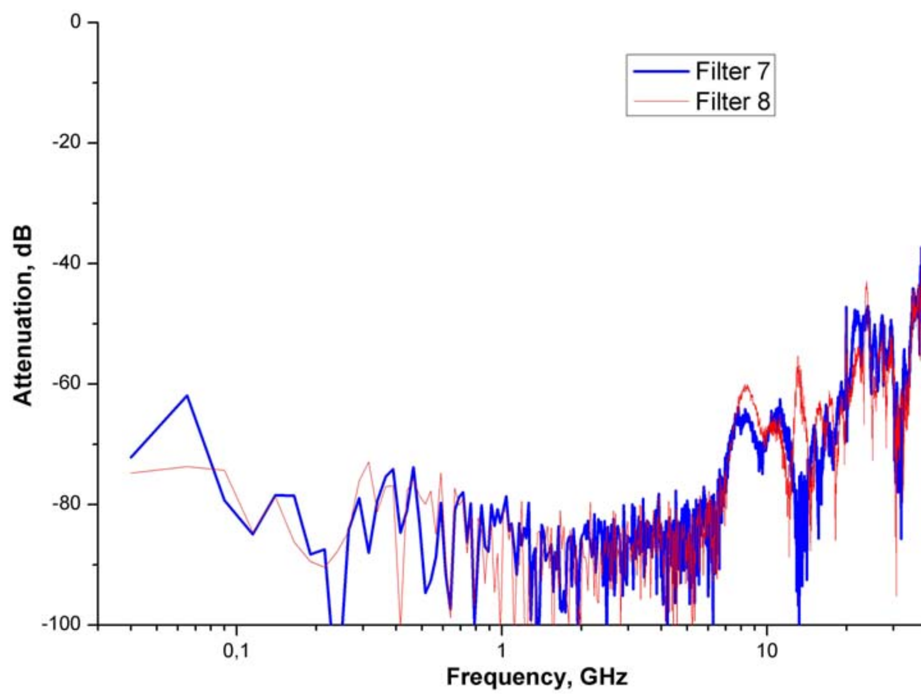


Figure 2.8. The frequency response of the filters marked 7 and 8.

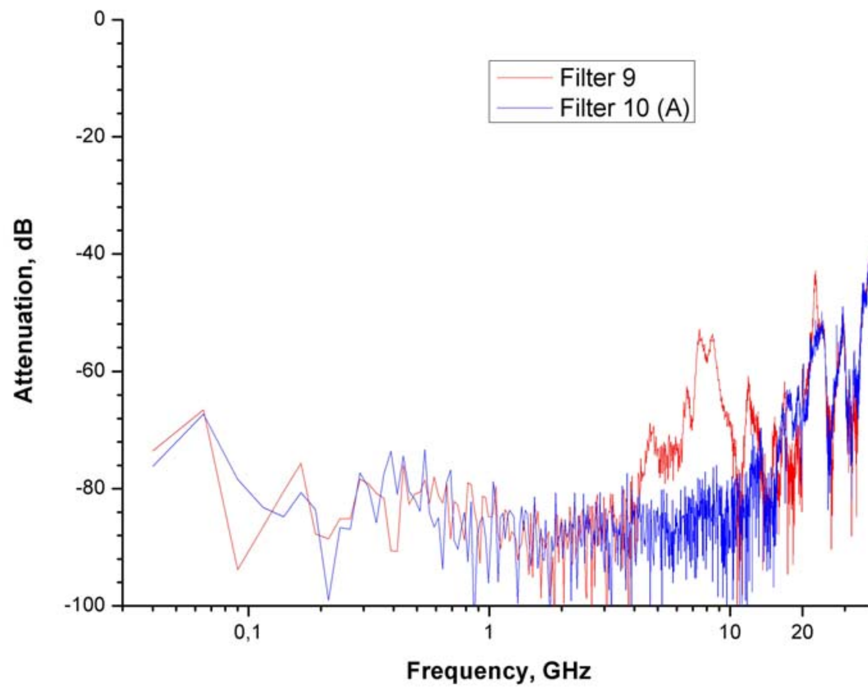


Figure 2.9. The frequency response of the filters marked 9 and 10.

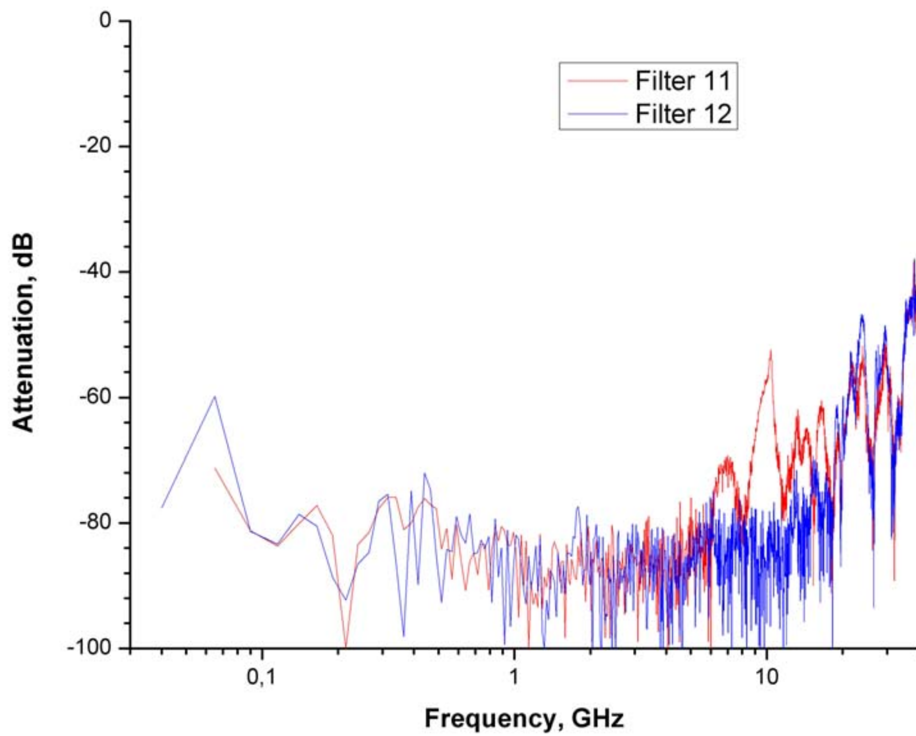


Figure 2.10. The frequency response of the filters marked 11 and 12.

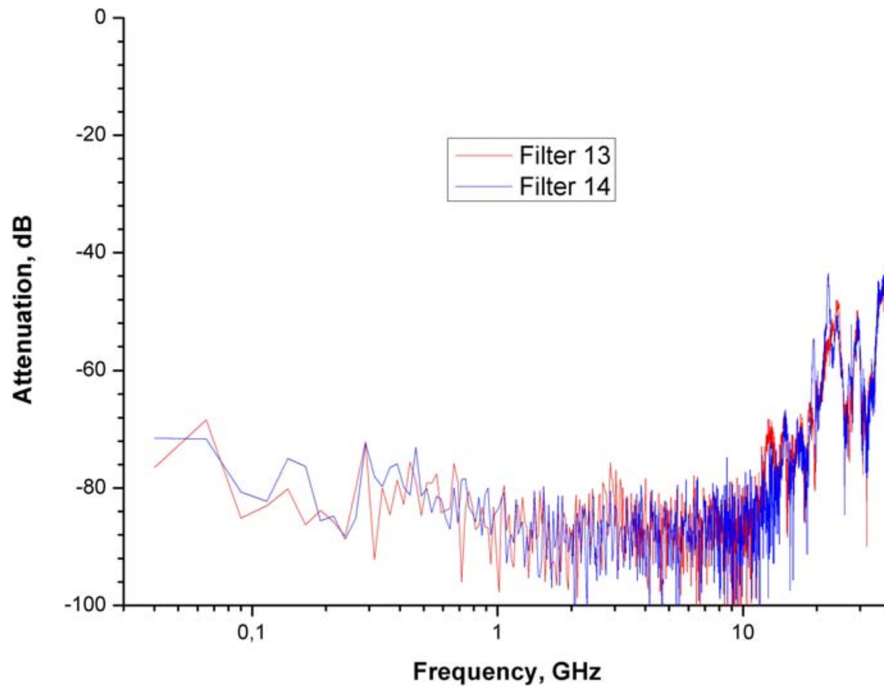


Figure 2.11. The frequency response of the filters marked 13 and 14.

The filters marked 1, 2, 3, 4, 5 and 6 were fabricated with the coil core made out of metal powder – epoxy mixture. The rest of filters used Eccosorb CR 124 as the core material. The measured characteristics did not show systematic differences in high-frequency behavior between these two sets.

After the filters were installed to the cryostat, high-frequency measurements became impossible, as the measurement lines in the cryostat were not shielded. The excitation RF signal from the network analyzer in the input line would be picked up by the return line without being passed through and attenuated by the filters at the sample stage.

The overall cryostat filtering frequency response at low frequencies up to 10MHz is shown in Fig 2.12. The measurement was done with the sample stage temperature of 100mK through two measurement lines, containing the low temperature Pi-filter, a microstrip filter at 1K and one LC filter at 4.2K each. The frequency spectrum was measured with an Agilent 89410A network analyzer, capable of measurements from DC to 10MHz. The excitation signal was preset to several different values during this measurement, in order to get a full picture of the transmission characteristics.

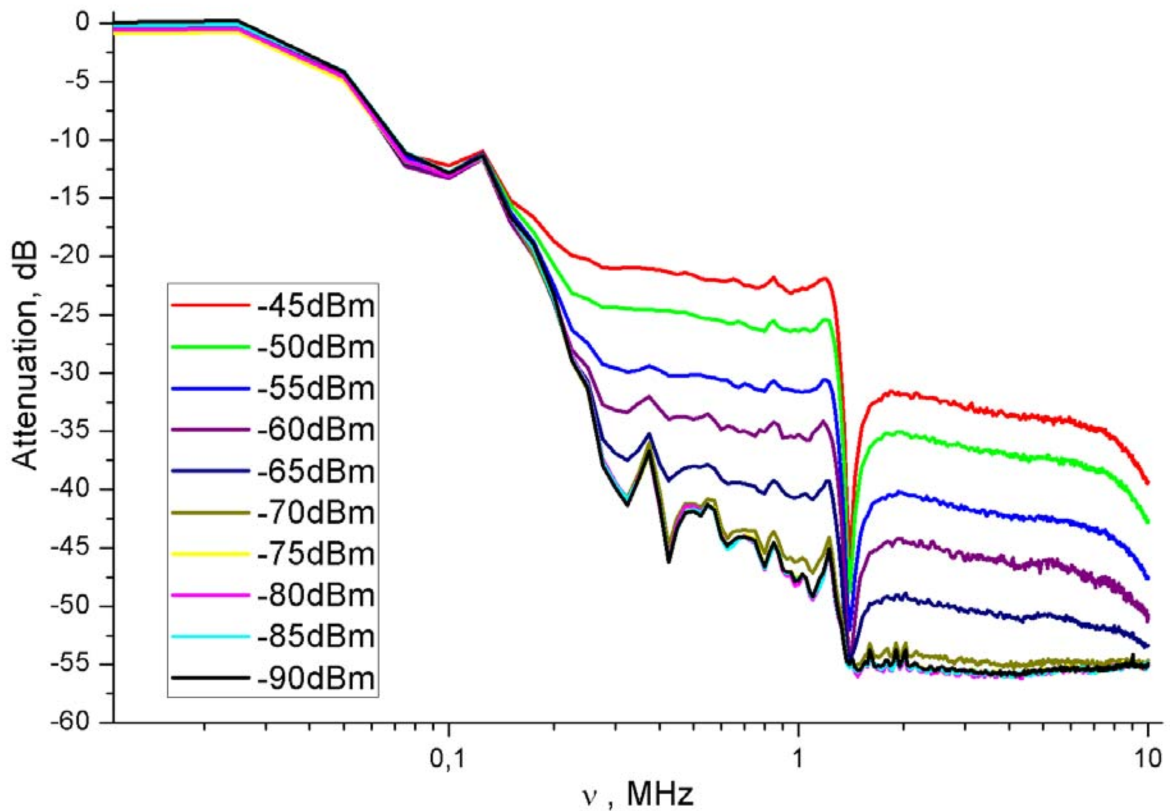


Figure 2.12. Frequency response of the cryostat measured at different excitation power values.

2.5 Discussion about filter characteristics

As it can be seen from the Fig **2.6** – Fig **2.11**, each filter has an attenuation ~ 80dB in the frequency range 40MHz – 2GHz. This fact allows proper filtering out of the thermal noise from the sample stage.

In the band 2GHz- 10GHz several filters showed non-systematically appearing broad resonance peaks. These peaks might appear due to non-homogeneous distribution of the SSP-epoxy mixture inside the gap between the filter core and the copper shield. Another possible reason for seeing resonance peaks is a low quality joint of the MCX connector that had to be soldered to one of the filter's ends to conduct measurements with the network analyzer. This MCX connector was not soldered permanently, possibly leaving an air gap between the grounding shell of the connector and the copper shield of the filter. An air gap could provide another pathway for the excitation signal of the network analyzer. In that case, the measured data does not represent actual attenuation of the filter in the frequency region of the resonance meaning that the real attenuation could be higher

At frequencies higher than 10GHz the noise floor of the measurement setup increased gradually with the increase in frequency. This might have happened because of poor soldering of the second MCX connector to the filter.

The data presented in Fig **2.12** were measured in order to test the actual filtering cut-off frequency of the cryostat in the frequency range below 10 MHz. This figure clearly shows the fact that during the measurement of the frequency response of the cryostat the excitation signal from the network analyzer was picked up by the return line without passing through filtering at high enough frequencies. In

the frequency region starting from 150kHz, one can clearly see that attenuation curves are equidistantly separated in magnitude, and this separation matches the 5dBm steps for input power until the input power drops to –70dBm (0.1nW). At power levels lower than 0.1nW the curves coincide.

There is also a resonance feature located at the frequency of 1.4MHz. This is in a good agreement with the simulation results of the simple circuit model presented in Fig 2.13. In the simulation, only two Pi-filters are included in order to get the frequency response of the sample stage without the subsequent filtering located at the 4.2K stage. The inductance value is taken as 5.1 μH, which was measured on a sample of a coil of copper wire on Eccosorb core with the same dimensions as in the actual filters.

The result of the circuit simulation is presented in Fig 2.14. One can see that the simulated curve has strong cut-off at 1.4MHz, following after a small resonance peak. Similar behavior is seen in Fig 2.12 on every curve which is above –70 dBm of input power. The strong attenuation peak at 1.4MHz originates from the parallel resonance nature of the double Pi-filter circuit.

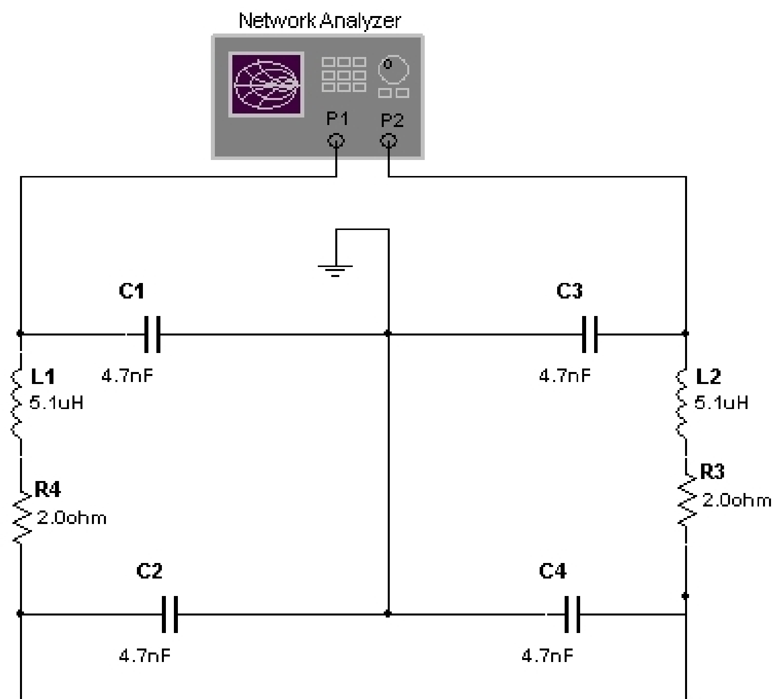


Figure 2.13. The equivalent circuit used for simulations of sample stage frequency response.

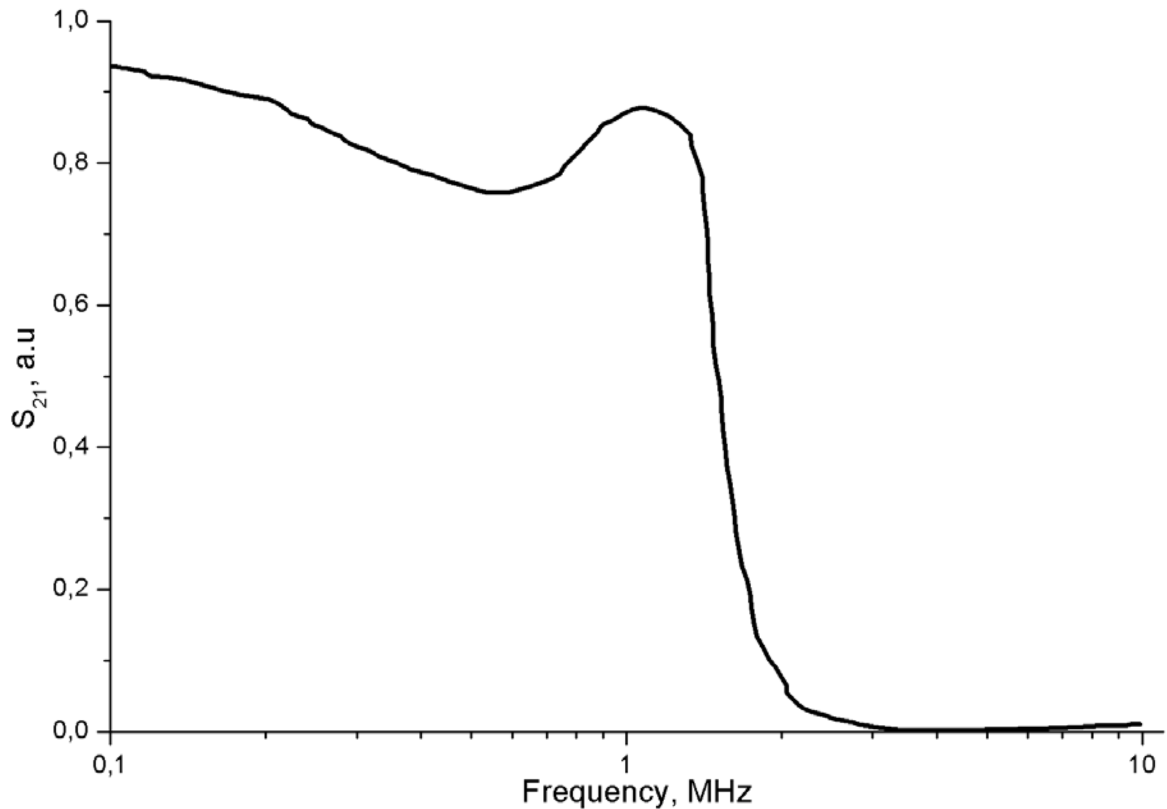


Figure 2.14. The simulated sample stage frequency response shows the position of the cut-off frequency at 1.4MHz.

As a result, one can conclude that measurement setup enables measurements up to moderate frequencies of ~ 25kHz without significant attenuation by the filtering.

3. SINIS thermometer sample

3.1 Sample overview

There is a need of a good temperature sensing device in the region below 1K. One simple choice is to use SINIS junctions made of aluminium and copper. The insulating layer is then the native aluminium oxide. A sample of this type can be fabricated in a very controllable way.

In this thesis, we want to investigate, if an on-chip capacitor can be fabricated together with the SINIS junction, to create another filtering stage on-chip. In order to make the capacitance on the chip, one should introduce two large area electrodes to the sample. Thus the technology of this SINIS-sample fabrication is slightly different from the reference sources [6, 14, 18, 19]. The idealized 3D model of a desired sample is shown in Fig 3.1.

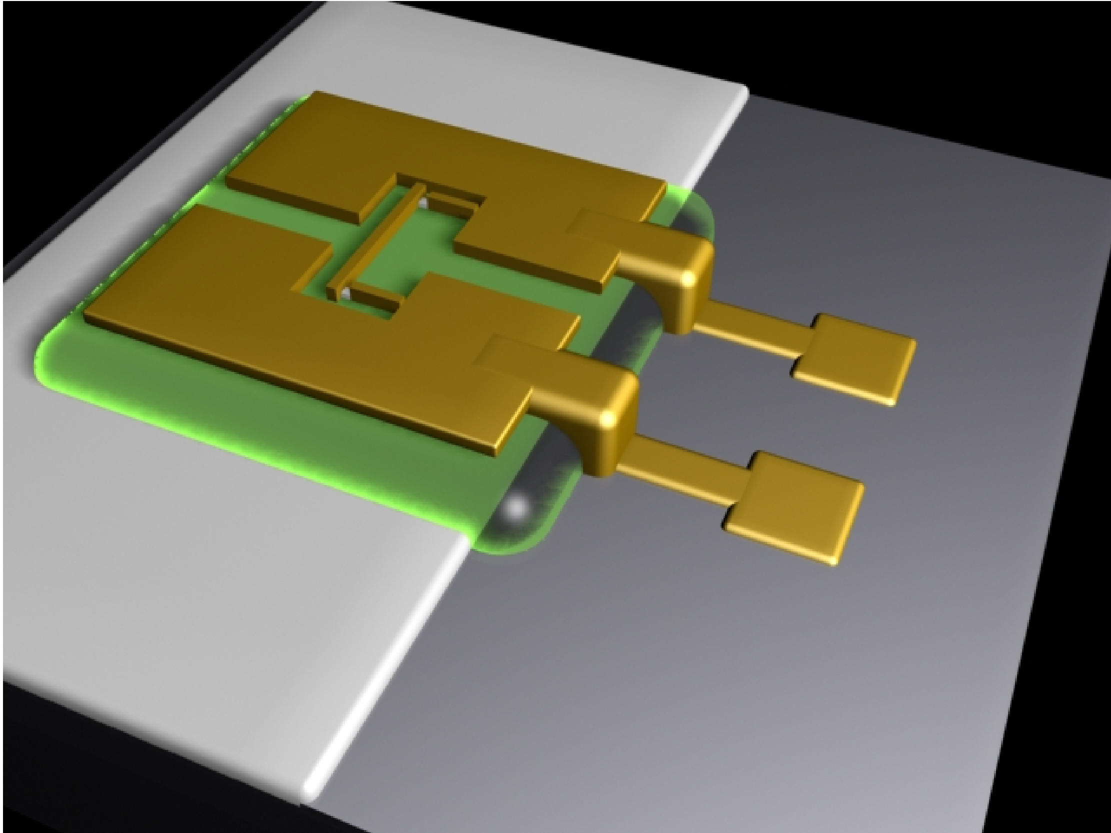


Figure 3.5. Idealized sample 3D modeling (schematics).

It was decided that two samples should be made. The first sample should have one electrode as a ground plane underneath, an insulation layer of reasonable material with reasonable thickness, and the second electrode as a part of sample structure on top. The second sample would be the same, but without on-chip capacitor. The substrate was chosen to be a positively doped Si wafer with a 300nm layer of thermally grown native oxide.

3.2 Sample fabrication steps.

Due to certain restrictions in fabrication facilities, in particular, the small writing field of the electron-beam lithography machine, the maximum size of the sample was chosen to be 2 by 2 mm. This area had to be divided equally to make the two electrodes of the capacitors. In order to maximize the capacitance, only one SINIS junction was designed to fit one sample. So, each of the top electrodes can be fabricated on the area of approximately 2 by 1 millimeters.

The SINIS junction was designed to fit the center area of the capacitor to simplify the writing field alignment during the electron beam lithography. A schematic of the sample design is shown in Fig. 3.2 and Fig. 3.5.

The fabrication procedure included the following steps:

3.2.1 Substrate cutting.

The silicon substrate was p-doped with boron, having the holes as majority charge carriers. This choice was done in order to minimize the electrical conductance of the substrate at low temperatures, as the mobility of holes is lower than that for electrons at low temperatures.

Original 150mm diameter wafer was cut to stripes of 32mm width to fit the oxidizing oven.

3.2.2 Substrate cleaning.

This step is very essential for further processing and sample performance. If any dust particles were left on the Si surface, they might prevent the formation a uniform layer of dielectric silicon oxide, and lead to the formation of so-called "pinholes" in it.

A pinhole is recognized as an area on the substrate, in which the sample structure will have an electrical connection to the substrate common ground. Thus, if several different wires of the sample will be shunted to the common ground, this may destroy any measurement results. Unfortunately, pinholes cannot always be totally avoided, but their number and their effect can be significantly reduced.

Clean original Si chips should not have any contamination, of which major are: silicon dust from the cutting process, organic leftovers and fingerprints, airborne dust particles. All the dust particles with a weak bonding to the surface can be blown out of it using pressurized air, but other ones require wet cleaning to remove.

First, Si chips were dipped into boiling acetone for 2 minutes to remove any soluble organic contamination. Next, chips were dipped to isopropyl alcohol (2-propanol, IPA) and placed in the ultrasonic bath for 20 minutes, and this was repeated 3 times with changing of the cleaning liquid before each time. The ultrasonic device used was made by FinnSonic and is a temperature stabilized water bath to which ultrasonic power is coupled. While being in the ultrasonic bath, Si chips were oriented with the polished surface facing to the bottom of the glass. This ensures that the gravitational pull will not bring any particles to the working polished surface.

After the cleaning procedure, Si chips still stay under the liquid until equipment for the next step is prepared. Polished surface has to be exposed to air for the shortest possible time to prevent airborne particle accumulation.

3.2.3 Substrate oxidizing.

After cleaning, the silicon chips were oxidized in order to form a primary insulating layer of SiO_2. Thermal oxidation process was chosen as the most reliable and controllable. During this process, Si chips are heated to 1100°C in a nitrogen atmosphere and then exposed to oxygen for a certain period of time. This time determines the thickness of the resulting silicon dioxide. The temperature of the oven also influences the thickness and quality of the oxide, thus it was set to maximum possible on the available oven. A 350nm thick SiOx film was obtained with the process of 8 hours of oxidizing and a slow cool-down period of 7 hours.

3.2.4 Sample chip preparation

After oxidizing the 32mm wide silicon chip was cut to smaller dice that fit the sample stage mounting plate. In particular, 8mm by 8mm size was chosen. At this point each chip had to be cleaned one more time to remove silicon dust left after dicing and to ensure that surface is flat.

Cleaning procedure for the small chips is similar to that of the bigger ones. Wet cleaning in hot acetone and ultrasonic bath of 2-propanol is the starting point. Chips also had to be dried of 2-propanol with a jet of dry nitrogen gas. However, optical microscope observations in the dark-field mode revealed that wet cleaning step is not sufficient, and the surface quality is still bad. As one can see in Fig. 3.2, there were aggregates and droplets left on the chip. Wet cleaning itself may be a possible source of these slowly evaporating droplets. Because contaminants were introduced by organic solvents, one can assume

that they are organic compounds themselves. This fact gives us a chance to remove them by selective etching with a highly reactive gas. Thus, dry cleaning with oxygen plasma was chosen as an appropriate next step.

Figure 3.2. The surface of the Si chip after wet cleaning. Dark field optical micrograph, 20X.

Plasma cleaning with oxygen provides excited oxygen molecules and ions, which can hit the surface of the sample. In this particular case, the silicon has already been covered by SiOx, so that the interaction with oxygen plasma was not going to change the existing surface properties.

Cleaning was done with the help of Oxford Instruments Plasmalab 80 system, which is fully automated and computer controlled. Samples were loaded to the main chamber, which was evacuated to reach the pressure of $2.5*10^{-5}$ Torr, filled with oxygen at 400mTorr and subjected to 200W of RF power. Substrate was exposed to high-frequency plasma for 20 minutes. After plasma cleaning, the substrate chip was immediately put to a clean container and moved to the next processing step.

3.2.5 Back gate formation

In this step the first electrode of the designed capacitor was formed. This electrode will be connected to the common electrical ground during the measurement, so it must not be entirely covered by the structure later on. Due to the fact that wet etching in a base will be used for further cleaning purposes (see below) it was decided to deposit two metal layers on the chip. The first layer to be deposited was 45nm of silver, and the second layer was 60nm of aluminium. The silver layer is less

sensitive to wet etching with a base solution, and it remains at the areas where aluminium would be etched. The sample design requires that the back gate has to be formed only on one half of the substrate chip. Another one half of the chip area remains intact (see Fig. 3.1).

Metal deposition took place in the Ultra High Vacuum metal evaporator (UHV) which operates on the principle of electron beam evaporation. The electron gun generates a current of accelerated electrons that hits a metal target, releasing heat and thus causes the target to melt and evaporate its material. The conditions of the inner chamber were kept in vacuum below 10^{-8} mbar, enabling ballistic transport of the evaporated material molecules. Ballistic transport of the molecules allows the so called shadow evaporation, when a 3D structure placed over the chip is making a shadow for the evaporated material. By controlling the shading patterns and choosing the proper angles of deposition, one can make complex structures on chip.

The evaporated material was deposited on the inner walls of the vacuum chamber as well as on the sample. The evaporator provided a possibility to change the incident angle of the material that was deposited to the sample by rotating the sample holder around one axis.

One half of the sample area was shadowed by the holding clamp of the evaporator sample stage during the evaporation. Evaporation of metals took place at an angle of 10 degrees to the surface normal, and aluminium was evaporated on top of silver without exposing the silver layer to air. The evaporation speed for silver was chosen to be 0.5nm/s and evaporation speed for aluminium – 0.1nm/s. The sample was finally exposed to 500 mbars of pure oxygen for 1minute before exposing to air, in order to ensure the formation of an aluminium oxide layer. Angular evaporation was carried out in order to form shadows from possible contaminating particles and to break the layer of silver at pinholes.

3.2.6 Insulating layer formation

On-chip planar capacitor requires an insulating layer to be formed. Taking into account that part of the back gate should not be covered with anything to facilitate bonding, full coverage of the chip with an insulator is not appropriate.

One way to make a suitable dielectric layer is to introduce a shadow mask to the chip and deposit e.g. silicon nitride with the use of PECVD technology. This was tried, but lead to the formation of very large number of micro-cracks in the silicon nitride layer, which in turn provided leakage path to ground. Thus, brittle materials should be avoided, and the choice of negative photoresist epoxy as an insulator seemed promising.

The negative photoresist epoxy SU-8 (from Microchem) was chosen as soft and non-cracking dielectric. In order to get a reasonable thickness of the layer, the initial solution was thinned 1/10 first and then 1/4 with cyclopentanone. The required final insulator thickness was about 800nm, but this was deposited in four steps of 200nm each. The thickness of each layer was determined with the help of an atomic force microscope on a calibration sample, which was made with the same deposition parameters as an actual sample. The advantage of the photoresist multiple layer formation is utilized, as it will be shown below.

The sample chip was spin-coated with one layer of SU-8 at 5000 rpm for 45 seconds and dried at 95C for 3 minutes. After that, electron beam lithography was carried out with the Raith LEO 1430 scanning electron microscope. The pattern transferred to the resist was a simple square of 3mm size, and the exposure parameters were following: specimen current of -17nA, writefield 4096 micrometers, resist sensitivity 260, area step size 1 micrometer, dose factor 250%. The position of 3mm by 3mm square was chosen to be on top of back gate, but still letting 0.5mm to be over the region where there was no metal deposited (see Fig. 3.3 and Fig. 3.4).

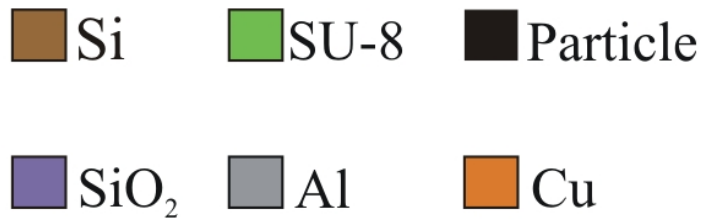


Figure 3.3. Sample schematics. Pinholes and particles in the insulating SU-8 layer are shown in black. In this configuration there is a short from top electrode to the bottom.

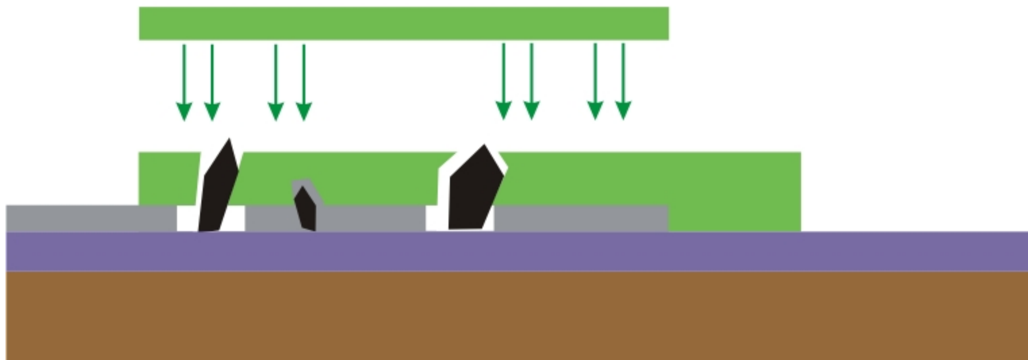


Figure 3.4. Sample schematics. After the NaOH etch and covering of the etched pinholes by another layer of SU-8 there will be no shorts formed.

After the electron beam exposure, the chip was heat treated for 1 minute at 95°C. Developing of the SU-8 was done with the use of acetone, as it will remove the unexposed regions of the resist. Exposed SU-8 resist will remain in place.

After development the sample was put to an etching medium for 120 seconds, which is 1M solution of NaOH in deionized water. This step is essential for further performance of the sample, as it helps to minimize the influence of the pinholes in the insulating layer of the capacitor. Because of deposited aluminium, each source of the pinhole was covered by this metal (see Fig 3.3, Fig 3.4). If the

particle is smaller than the thickness of the first layer of SU-8, it may not cause problems to insulation because it will be covered by the resist, and will not shunt the sample to the ground plate. But if the particle is higher, it will provide an electrical contact to the back electrode. Thus, if the metal will be etched away from these of particles, it may significantly reduce the number of shorting pinholes in the SU-8 layer. The etching solution also penetrated under the resist layer from the pinhole sites to form very small circular holes in the silver layer underneath the regions with no aluminium. These regions are observable with an optical microscope (see Fig 3.5). The back electrode bonding area was also left without aluminium. However, the silver can still provide an electrical contact to the back gate.

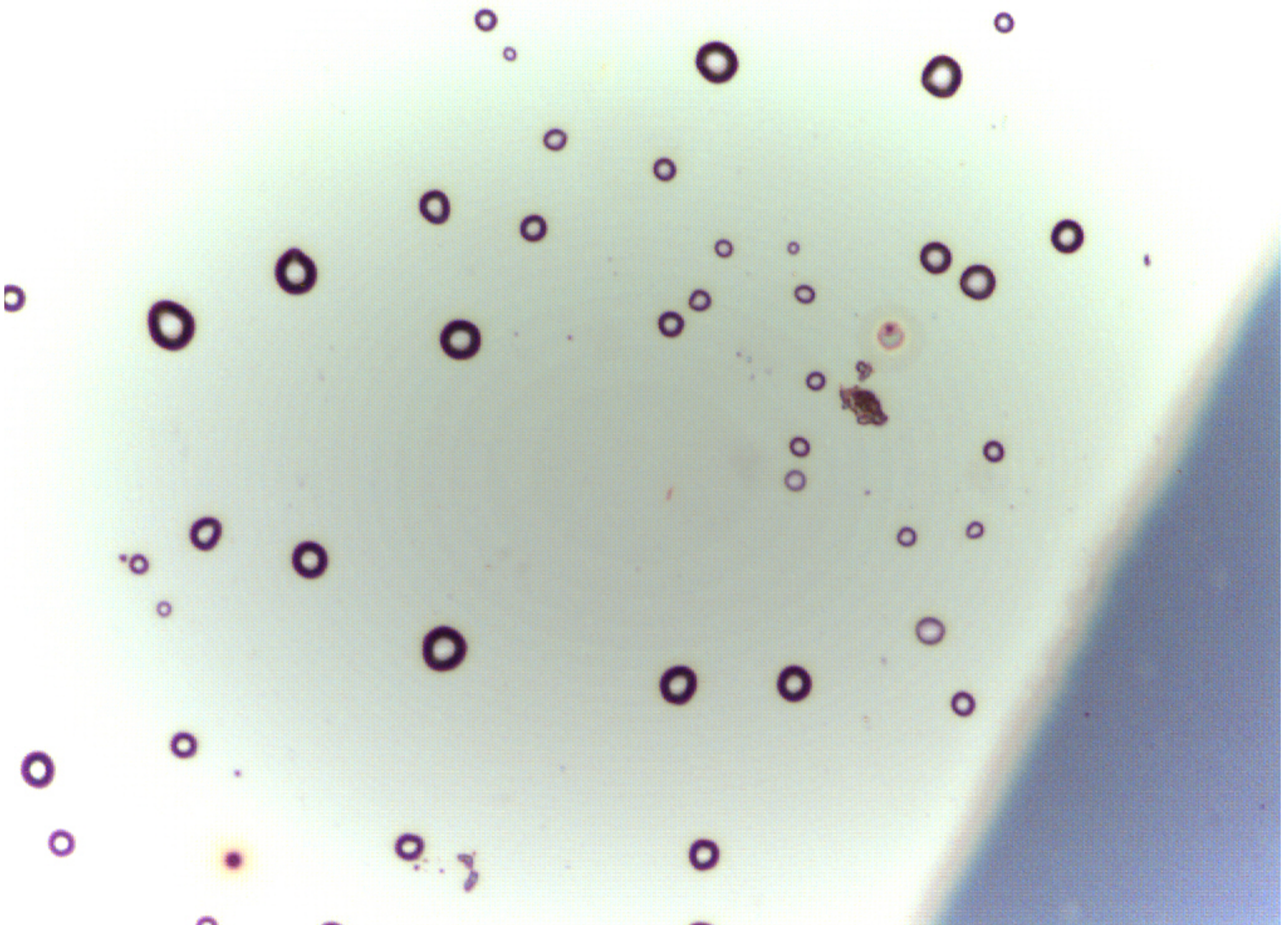


Figure 3.5. Circular regions etched in Al layer at the pinhole sites. Bright field optical micrograph, 20X

After removing the sample from the etching solution it was covered with one more layer of SU-8 with the same spinning parameters and put to the same etching solution one more time to ensure that silver was also removed from the particles. At this step the lithography process was not used and SU-8 covered full chip area, including back gate bonding area. Silver is etched more slowly than aluminium, and in this step it was etched only from the top of those particles, which were higher than the layer of SU-8. Also it can be noted that metal was etched from the particles much faster than from the planar area of the chip.

After etching procedures the chip was covered with a double layer of SU-8 and processed with electron beam lithography step once more to make an insulating layer of area 3mm by 3mm and thickness of 800nm.

3.2.7 SINIS junction design and fabrication.

Electron beam lithography procedure was used to pattern the SINIS tunnel junction area and surrounding capacitor electrodes.

The lithography process consists of several steps: pattern design, photoresist deposition, exposure, resist development, structural material deposition and lift-off.

One very common pattern design for a single NIS junction contains two wires separated by a certain gap. During junction material deposition the first material is deposited at a certain angle, usually by physical vapor deposition. The other material layers are deposited at different angles, thus making different shadows of the pattern.

In the particular case of a double junction SINIS device made of aluminium and copper with native aluminium oxide as the insulating layer, π-shape of the structure was chosen. In this design, two lines of aluminium are deposited with a large evaporation angle along the lines, in order to make the shadow longer than the original pattern. After the oxidation procedure, copper is deposited perpendicular to the aluminium lines at a normal to the sample's plane.

The positive resist used for shadowing, consists of by two layers, both sensitive to electron beam exposure, but the lower layer is more sensitive, which leads to an undercut structure. The undercut also leads to the formation of bridges of the top resist layer, which are needed for NIS tunnel junction formation (see Fig.3.6).

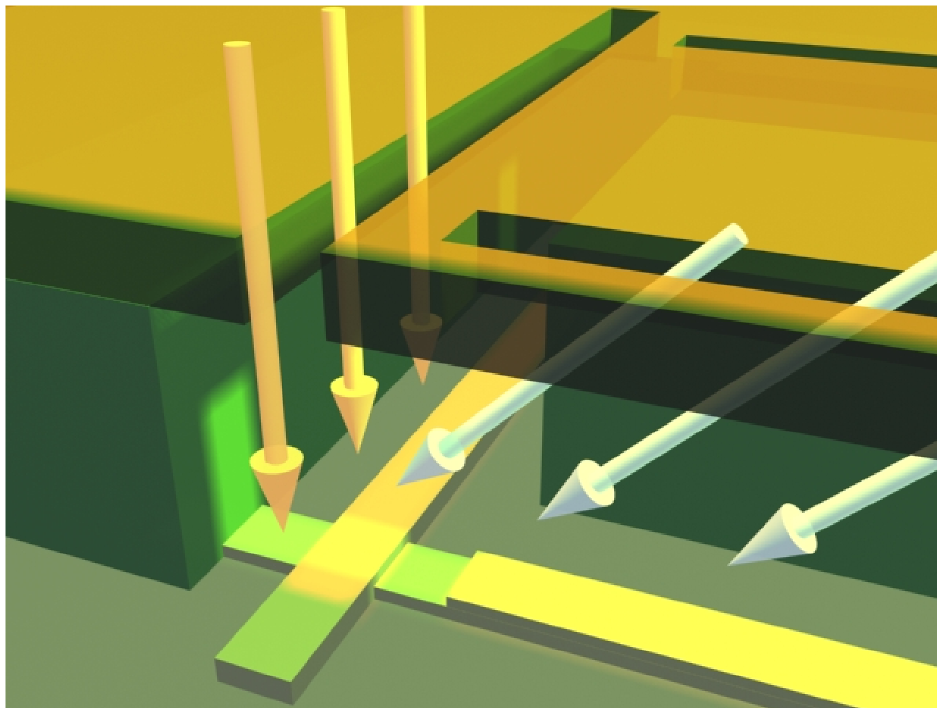


Figure 3.6. Schematic picture of the shadow evaporation technique.

The complexity of the photoresist shape requires extensive and careful modeling. Pattern design usually requires 3D modeling of the deposition process, taking into account off-plane effects during shadow-evaporation.

A computer program (see appendix B) for simulating shadow-evaporation was written and used to choose the optimal evaporation angles. The program allows the user to set the thickness of each of the two layers of the photoresist, and to set the azimuthal and polar angles of the sample plane normal with respect to the source of the deposited material. When the user loads the lithographic mask in the form of black-and-white picture, the program can start calculating the resulted evaporated structures of resist and deposited material. The resulted structures can be saved, loaded or processed further to model a sequential deposition processes. The program code is based on the raster ray tracing algorithm. This algorithm treats every pixel of input bitmap image in the same way, calculating whether there will be shadowing or not for an atom, which crosses the area of the pixel during the deposition process. Thus, the resolution of the method is one screen pixel of the input bitmap image. The calculation of the shadowing takes into account only that features of the sample, which are crossing the virtual trace of an atom that has to be deposited. In order to get a higher accuracy the user has to increase the absolute size (in pixels) of the processed lithographic mask picture. Instuctions for use of the program are given in the appendix B as well.

The EL9 methylmetacrylate copolymer (EL9, 9% solution of MMA in ethyl lactate) was used as the first, lower layer of electron beam resist with 500nm thickness. The chip was preheated for 1 minute at 160°C and after cool down to room temperature it was spin-coated by the polymer at 2500rpm for 45seconds. The second resist layer was a 1500nm of PMMA in A9 solution (9% solution of PMMA in anisole) spin-coated at 2500rpm, as well. Each resist layer was baked for 120 seconds after spin coating at 160°C

Prior to the exposure, the electron beam was focused on the substrate plane in a manual mode with the help of markers. Chip was intentionally contaminated by ultra fine silver powder with grain size up to 100nm. Powder aggregates of irregular shape and 1-1.5 micrometers size were chosen as markers and were imaged with the highest possible sharpness at the targeted exposure current parameters.

3.2.8 Exposure

The lithography procedure was carried out with the Raith LEO 1430 scanning electron microscope.

Exposure took place in two steps. First, the SINIS junction area and the supply wires were exposed at a writefield of 512 x 512nm, area step size 72nm and current of 250pA. Next, the capacitor electrodes were exposed at lower precision: writefield 2048, area step size 312nm and 5nA current. Acceleration voltage and dose factor were set to 28kV and 130% respectively.

The capacitor electrodes themselves cannot be used as contact pads for connection of the sample to further wiring. The Al wire, which is usually welded to the contact pads by an ultrasonic bonder, will break through the insulating layer and short the capacitor. In order to avoid this, the bonding pads had to be fabricated in a following step on the region outside the SU-8 layer, with extra leads connected to the top capacitor electrodes. This leads have to step over the SU-8 edge, located 0.5mm away from the back electrode edge (see Fig. 3.1). Another minor reason to move bonding pads away from SU-8 is that Al wire tends to easily tear off the bonding pad, if it is located over the polymer (see Fig 3.7). The capacitor bonding pads were exposed at the same exposure session as the capacitor electrodes.

Connecting structures of 50 micrometers width with 300 by 300 micrometers bonding pads were patterned starting from capacitor electrodes (Fig 3.1), running over the 0.5mm region and going down to the region without any metal on it. So that, Al wires were bonded to connecting structures over the SiO_2 (see Fig 3.7 – scanning electron micrograph of the bonding wires).

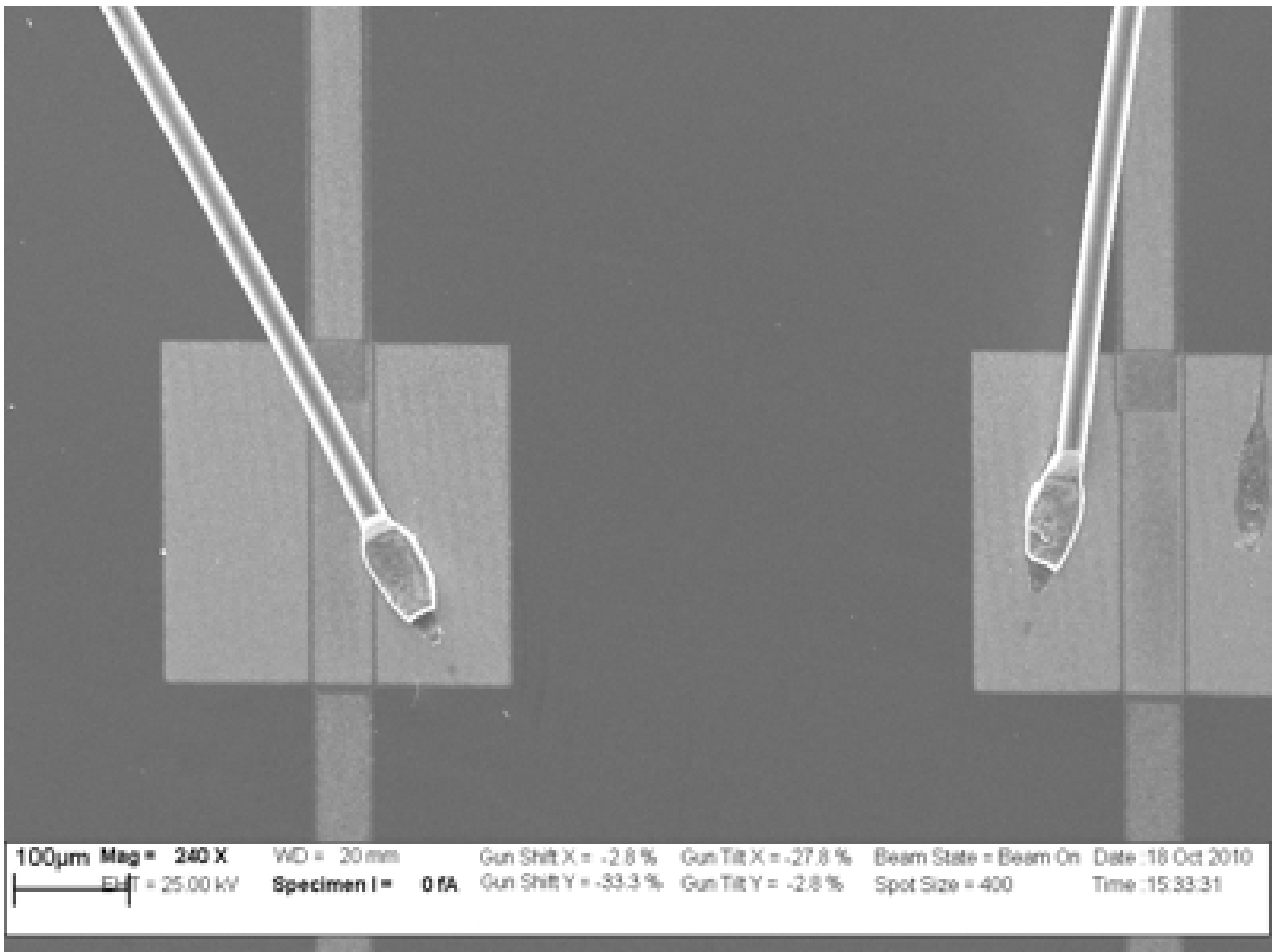


Figure 3.7. Scanning micrograph of bonding wires over the bonding pads of unsuccessful sample. The bonding pads were fabricated over the 200nm of SU-8 polymer, which caused Al wires easily to rip off together with deposited top electrode material.

3.2.9 Development

The PMMA resist development was done, as usual, as a form of wet etching. First, the exposed chip was gently washed with 2-propanol (IPA) jet in order to wash away the silver powder contamination. After that, the sample was dried with a nitrogen gas jet, and it was put into the anisotropic developer (methyl isobutyl ketone (MIBK) dissolved in IPA) for 35seconds and then washed and dried again. All exposed areas of the sample were removed by the first developer and sharp lines with a thickness comparable with the height of the layer were formed (aspect ratio of nearly 1:1). Starting from this point, any contamination could be fatal for further performance of the sample, any airborne particle covering the line would restrict the uninterrupted conducting wire formation. Until the end of metal deposition process the sample had to be kept exposed to the cleanroom environment as short time as possible.

Next, the chip was put into the isotropic developer, which did not modify the top resist layer but made the bottom layer to expand the cavity and to form the undercut. The second developer takes only 6 seconds to etch a reasonable cavity. The second developer consists of methoxyethanol dissolved in methanol. This volatile solution could have easily over-etched the MMA copolymer, and thus required immediate IPA washing of the sample after development.

3.2.10 Metal deposition

Deposition of the material was done in the Ultra High Vacuum electron beam evaporator.

The chip was installed onto the sample holder in such a way that the two aluminium lines were oriented perpendicular to the axis of rotation. After insertion into the high vacuum environment, the sample was oriented at 75 degrees angle to the incident beam (Fig 3.8).

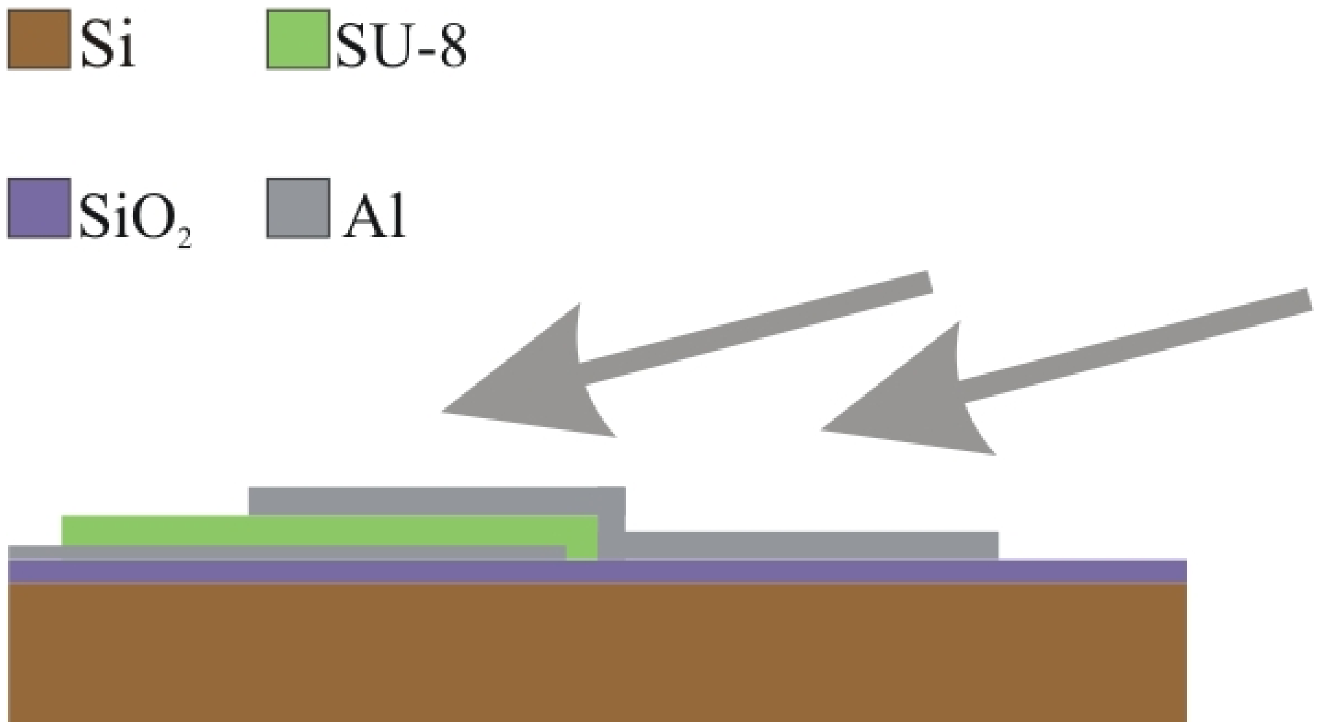


Figure 3.8. Aluminium deposition to the sample (schematics).

The evaporation took place at a rate of 0.2nm per second; 114nm of aluminium were deposited in total. If projected to the normal of the sample plane it would result in 29.5nm of height.

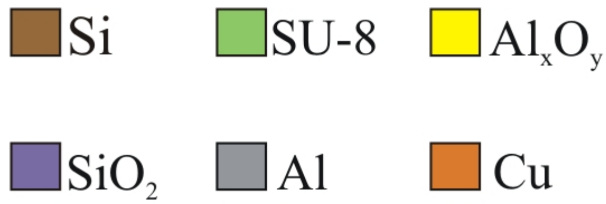
Next, the sample was placed into the loading chamber of the UHV for oxidation of the aluminium. Oxidation was done by introducing pure oxygen to the loading vacuum chamber at a pressure of 100mbar. Oxidation process lasted 310 seconds at room temperature [18].

The normal conductor layer formation was done by deposition of 45nm of copper at a normal to the plane of the sample with the evaporation speed of 0.2nm per second. Copper layer was deposited over aluminium oxide and the cross-bar for the π-shape of the SINIS structure was formed.

Lastly, the lift-off process was carried out. During this step the non-developed PMMA photoresist was removed with hot acetone. Hot boiling acetone was prepared first in glass cup. Next, sample was placed to the cup and acetone was forced to boil one more time. During this, a 5cm3 medical syringe was filled with hot acetone from the cup. Next, the glass cup was taken off the heater and jet of acetone from the syringe needle was pointed towards sample. Jet washing was repeated until there were no visual signs of resist left on the chip.

There were two samples fabricated together, the first one with the on-chip capacitor and the second one without capacitor. Samples were put into the UHV evaporator and the metal evaporation was done at the same time with the same evaporation parameters and were oxidized simultaneously. The structural difference between the samples was caused by the fact that the second sample was not processed though the manufacturing steps “Back gate formation” and “Insulating layer formation”.

The idealized schematic cross-section of the sample is shown in Fig3.9, and Fig 3.10 shows the real sample photograph. The image has been taken after the sample had been measured in the cryostat.



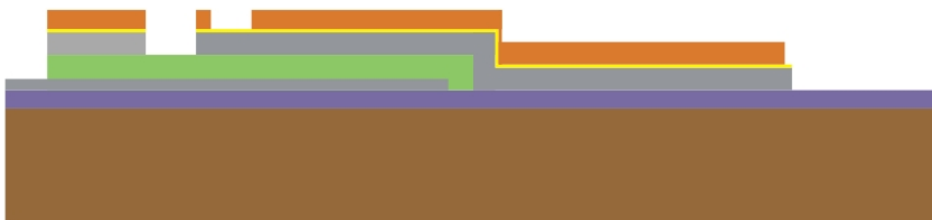


Figure 3.9. Idealized sample cross-section (schematics).

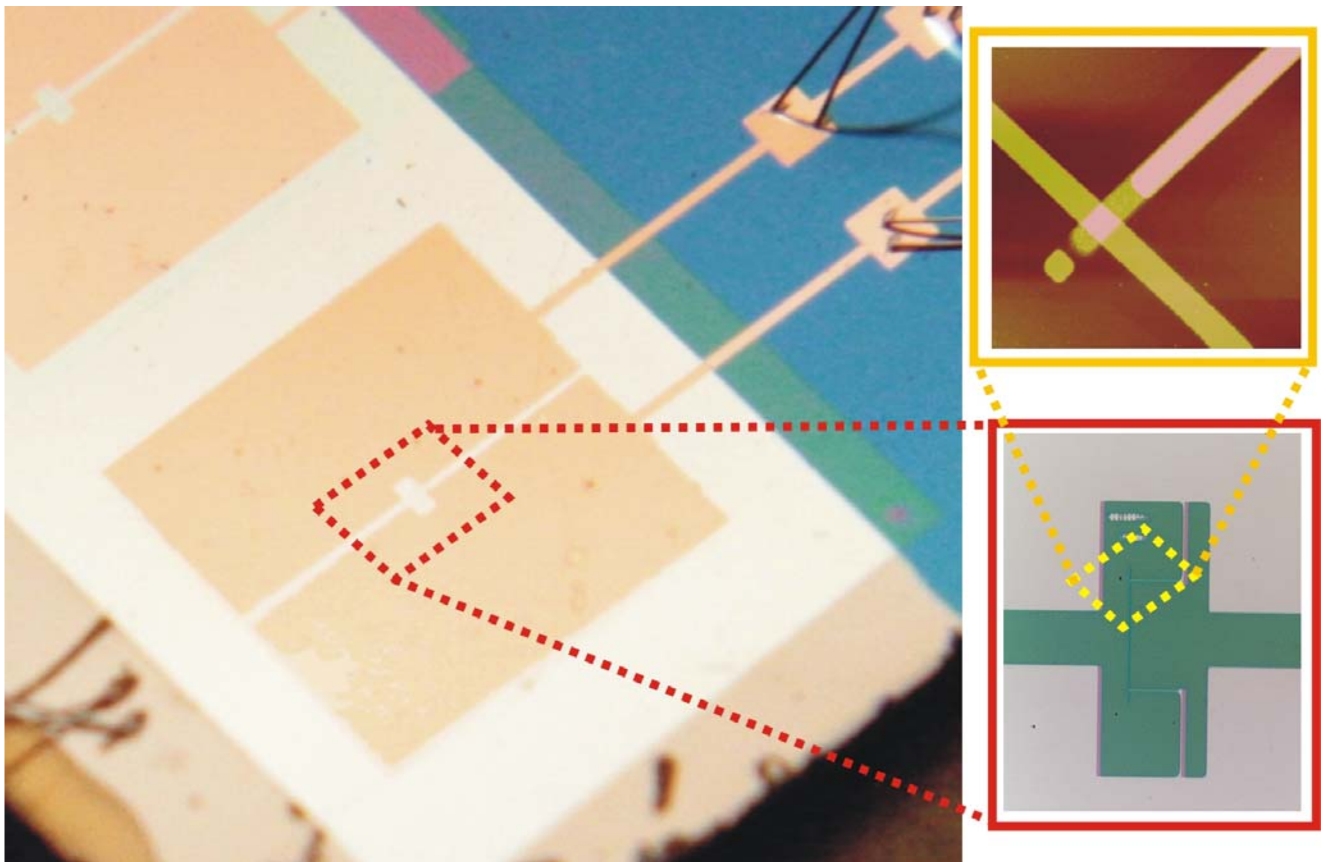


Figure 3.10. The sample photograph, optical micrograph of the SINIS junction area, AFM micrograph of the single NIS junction. The size of each capacitor copper electrode is 1mm by 2mm.

3.3 SINIS junction theoretical background.

The time-independent perturbation theory approach is useful in tunneling description. One can consider the quasiparticle tunneling between two electrodes as elastic scattering from state $\vec{k}_1$ in normal metal region to state $\vec{k}_2$ in superconductor region. The rate of the transition $\Gamma_{1\to 2}$ is described by so-called Fermi's golden rule [33]:

$$\Gamma_{1\to 2} = \frac{2\pi}{\hbar}\left|\left\langle 2\,|\,\widehat{H}_1\,|\,1\right\rangle\right|^2 \delta(\varepsilon_1 - \varepsilon_2), \quad (3.1)$$

here $\left\langle 2\,|\,\widehat{H}_1\,|\,1\right\rangle$ is the expectation value of perturbation Hamiltonian that is called the tunneling matrix element; $\delta(\varepsilon_1 - \varepsilon_2)$ is delta function, ε_1 and ε_2 are energies of initial and final state, they are equal for elastic scattering; $\hbar$ is Planck's constant. It should be noted that here and further the energy is counted from Fermi energy level ε_F.

According to Bardeen's theory the perturbation Hamiltonian [34] is

$$\widehat{H}_1 = \sum_{k_1,k_2,\sigma}(T_{k1,k2}\widehat{C}^+_{k1}\widehat{C}_{k2} + T^*_{k1,k2}\widehat{C}^+_{k2}\widehat{C}_{k1}), \quad (3.2)$$

here $T_{k1,k2}$ is kinetic energy; $\widehat{C}$ and $\widehat{C}^+$ state for the fermionic creation and annihilation operators correspondingly; σ denotes the spin value. The kinetic energy is $T_{k1,k2} = \frac{\hbar^2 k^2}{2m}\delta_{k1,k2}$.

Taking into account non-zero temperature thermal averaging results in

$$\left\langle \widehat{C}^+\widehat{C}\right\rangle = f(\varepsilon,T) = \frac{1}{1+\exp[\frac{\varepsilon}{k_B T}]} \text{ and } \left\langle \widehat{C}\widehat{C}^+\right\rangle = 1 - f(\varepsilon,T) = 1 - \frac{1}{1+\exp[\frac{\varepsilon}{k_B T}]}, \quad (3.3)$$

here $f(\varepsilon,T)$ stands for Fermi-Dirac distribution; k_B is Bolzman factor and T denotes temperature.

Assume that voltage V is applied to NIS junction and consider the tunneling current

One can write the transition rate from normal metal (state 1) to superconductor (state 2) and write the expression for transition rate

$$\Gamma_{1\to 2} = \frac{4\pi}{\hbar}\sum_{k1,k2}|\,T_{k1,k2}\,|^2 f_1(1-f_2)\delta(\varepsilon_1 - \varepsilon_2 - eV), \quad (3.4)$$

here the summation goes over all possible states; f_1 and f_2 are distribution functions for normal metal and superconductor correspondingly, and e is electron charge. Here we did summation over possible spin-states and got an additional factor of 2.

The tunneling from superconductor (state 2) to normal metal (state 1) has to be also considered

$$\Gamma_{2\to 1} = \frac{4\pi}{\hbar}\sum_{k1,k2}|\,T_{k1,k2}\,|^2 f_2(1-f_1)\delta(\varepsilon_2 + eV - \varepsilon_1), \quad (3.5)$$

Thus the tunneling current becomes

$$I(V,T) = e(\Gamma_{1\to 2} - \Gamma_{2\to 1}) = \frac{4\pi e}{\hbar}\sum_{k1,k2}|\,T_{k1,k2}\,|^2 (f_1 - f_2)\delta(\varepsilon_1 - \varepsilon_2 - eV). \quad (3.6)$$

Over a small range of bias voltages $|\,T_{k1,k2}\,|^2$ is usually assumed to be constant, let us denote it here as $|\,\mathrm{T}\,|^2$. Thus, in the continuum limit equation (3.6) becomes

$$I = \frac{4\pi Ae}{\hbar} |\mathrm{T}|^2 \int_{-\infty}^{\infty} N_1(\varepsilon + eV) N_2(\varepsilon)(f_1(\varepsilon + eV) - f_2(\varepsilon)) d\varepsilon \text{ , (3.7)}$$

where N_1 and N_2 are densities of states for normal conductor and superconductor correspondingly, and A is the junction area. For the normal metal we can assume that the density of states is independent of electron energy and equal to the density of states at Fermi energy, so

$N_1(\varepsilon + eV) \approx N_1(0)$. (3.8)

The density of electron states with energies ε in the ideal superconductor at nonzero temperature is given by:

$$N_2(\varepsilon) = \begin{cases} \frac{N_1(0)|\varepsilon|}{\sqrt{\varepsilon^2 - \Delta(T)^2}}, |\varepsilon| \geq \Delta(T); \\ 0, |\varepsilon| < \Delta(T) \end{cases} \text{, (3.9)}$$

where $\Delta(T)$ is energy gap value of the superconductor, which is in the general case temperature dependent. At temperatures close to critical temperature of the superconductor the gap value can be treated as

$$\Delta(T) = 3.2 k_B T_C \sqrt{1 - \frac{T}{T_C}} \text{ , (3.10)}$$

where T_C is a critical temperature of the superconductor.

Below 0.7 T_C the energy gap value is approximately constant and can be calculated using

$$\Delta(0) = 1.76 k_B T_C \text{ (3.11)}$$

or can be also deduced from experimental data.

Taking into account that the tunneling resistance of the junction can be expressed as

$$R_T = \frac{\hbar}{4\pi Ae^2 |\mathrm{T}|^2 N_1^2(0)} \text{, (3.12)}$$

NIS tunneling current can be written as

$$I_{NIS}(V,T) = \frac{1}{eR_T} \int_{-\infty}^{\infty} \frac{|\varepsilon|}{\sqrt{\varepsilon^2 - \Delta^2}} (f_1(\varepsilon + eV, T) - f_2(\varepsilon, T)) d\varepsilon \text{ . (3.13)}$$

The SINIS structure consists of two NIS junctions connected in series, so it is straightforward to get the expression for a symmetric SINIS junction:

$$I_{SINIS}(V,T) = \frac{1}{2eR_T} \int_{-\infty}^{\infty} \frac{|\varepsilon|}{\sqrt{\varepsilon^2 - \Delta^2}} (f_1(\varepsilon + eV, T) - f_2(\varepsilon, T)) d\varepsilon \text{ (3.14)}$$

Where R_T is the resistance of the single junction, and V is the voltage over single junction.

The I-V characteristic of a SINIS becomes increasingly rounded with a temperature increase. If the temperature has to be measured, the voltage response can be taken, while the SINIS junction is biased with a small constant current (5-50pA for $R_T \sim$ 10-90 kΩ). The voltage vs. temperature dependence is determined by only two parameters: the superconducting energy gap and the tunneling resistance. These parameters can be deduced from the I-V measurements as it is shown in Fig 3.11. The differentiated I-V curve contains two peaks, the distance between them gives the value of superconducting energy gap at low enough temperature, and the asymptotic line at higher bias voltages gives the value for total tunneling conductance. The tunneling conductance is equal to inverse of the sum of tunneling resistances of each NIS junctions. If the junctions are identical, the total tunneling resistance is a double of that for a single junction.

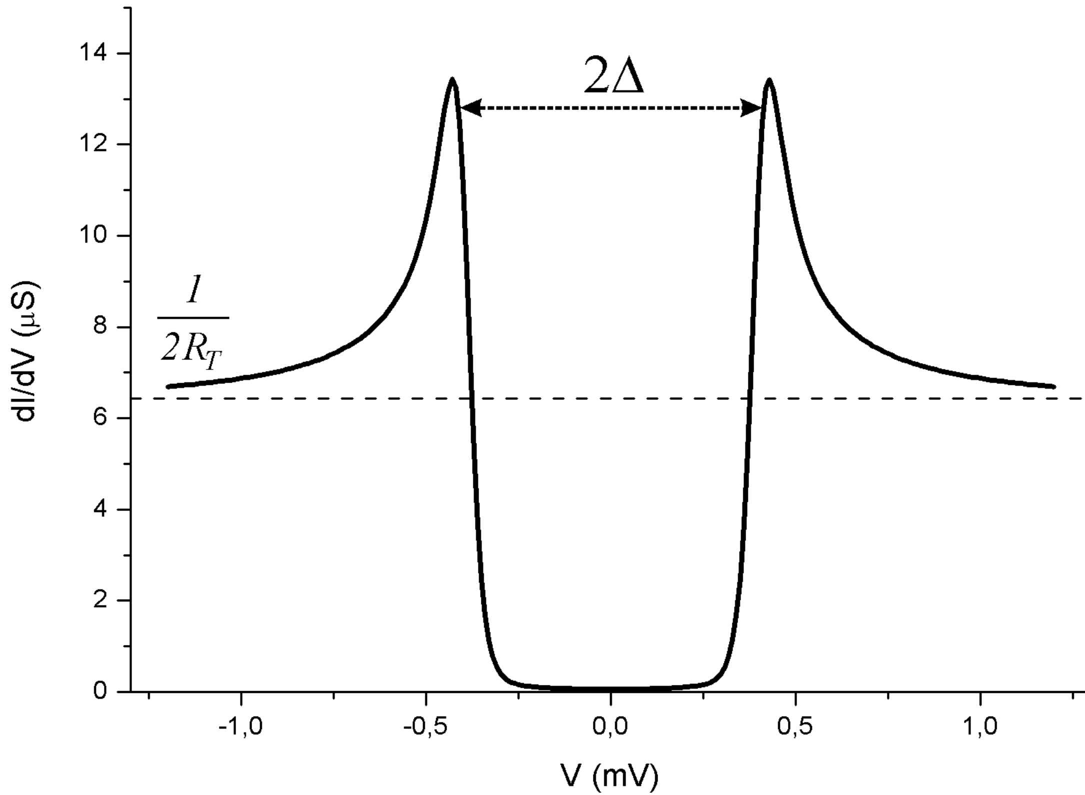


Figure 3.11. Calculated differential conductance of the SINIS structure at 80mK Horizontal line represents SINIS tunneling conductance. Calculation details: Al energy gap value is taken 205 μeV, NIS junction tunneling resistance is 78 kOhm.

In reality the SINIS I-V curves can differ from theoretical ones due to finite sub–gap currents, noise heating of the electron gas and charging effects [35]. Sub-gap currents are particularly harmful for SINIS-based coolers, because they lead to their heating. There is a variety of mechanisms that cause sub-gap currents. One of them is the quasiparticle finite life-time effect. Often it is sufficient to use definition (3.9) to describe the density of states in the superconductor. However, due to the finite quasiparticle life-time the distribution is broadened. The equation (3.9) can be converted to appropriate one by doing a substitution $\varepsilon \rightarrow \varepsilon + i\Gamma$ and considering the real part of the $N_2(\varepsilon)$. Here Γ represents the energy broadening and it depends on the metal film quality [4], [6].

There are other mechanisms, that lead to a the sub-gap current. Among them are Andreev reflection [36], pinholes in the insulator layer, and excitations by incoming thermal radiation.

In particular, sub-gap currents result in saturation of the V(T) curves at low temperatures for the SINIS junctions, thus making this calibration curve for thermometry non-linear at low temperatures. The set of curves showing the dependency of the voltage drop across a SINIS junction on its temperature, when biased with constant current is shown in Fig 3.12, with varying broadening parameter Γ .

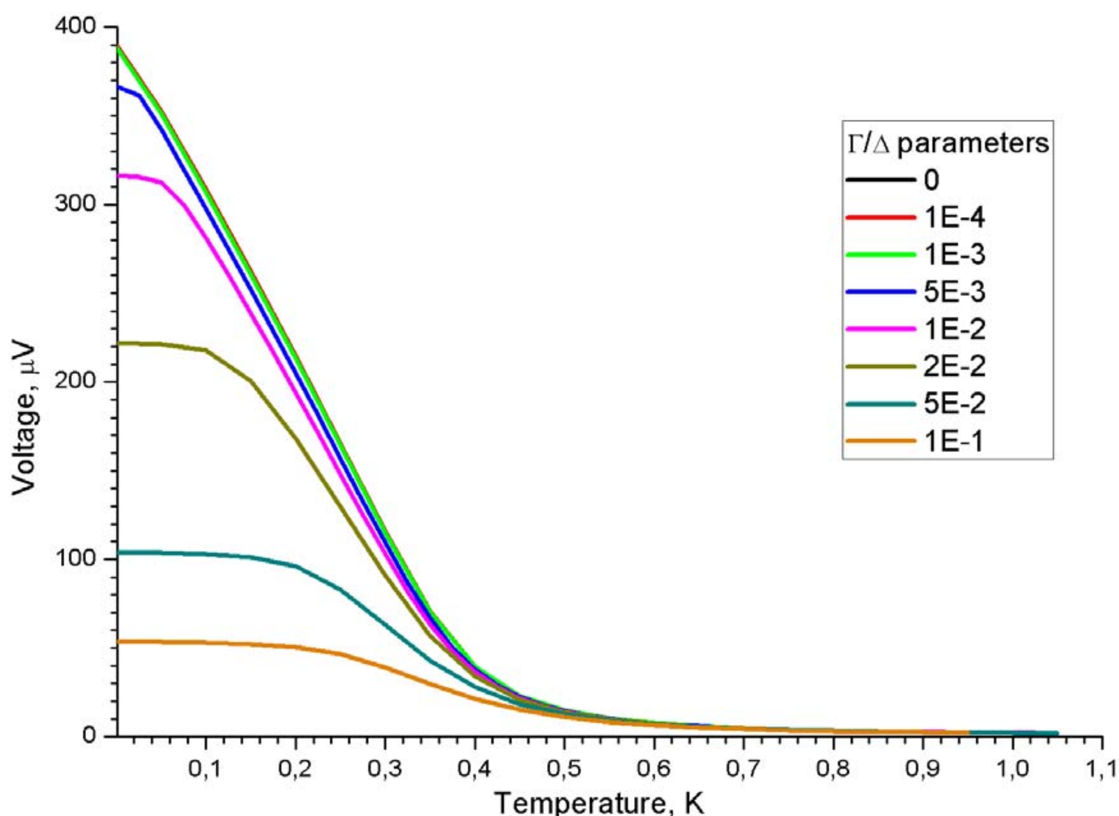


Figure 3.12 The dependency of the voltage drop across SINIS on its temperature with different DOS broadening parameters.

3.4 Sample characterization

First, the sample with the on-chip capacitor was glued to the sample stage copper block of the cryostat with the help of GE-IMI 7031 varnish, thinned with methanol.

The sample was bonded electrically to the sample stage of the cryostat by means of the ultrasonic wedge bonder F&K Delvotec 5432. This machine uses thin aluminium wire. When the operator positions the needle with the wire over the desired region of the contact pad, the machine presses the wire against the metal surface and applies an ultrasonic power to the needle, forcing the Al wire to melt. Molten Al wire bonds to the roughness of the contact pad, and the machine stops applying power and unrolls the wire from the spool to make a loop to another contact pad. At the second contact pad the bonding machine tears the Al wire while still applying the ultrasonic power, thus breaking the wire loop at its end.

The sample was cooled down with the dilution refrigerator, following the common cooling procedure. The steps included precooling with liquid nitrogen, liquid helium, pumping the helium from the 1.5K pot and starting the ^{3}He-^{4}He mixture circulation. Detailed description of the cool-down process was given in section "Refrigeration"

The measurement setup included standard equipment for the cryogenic laboratory of the Nanoscience Center of the University of Jyvaskyla.

A series of measurements were performed to determine the DC characteristics of the SINIS junctions, one with on-chip capacitors and another without capacitors. In the experiment, the SINIS

junction I-V characteristics were measured in a four probe configuration by measuring the current response to a changing bias voltage. A DC source with output voltage linearly sweeping from -2 V to 2 V was used with a sweep time of 1770 s and a 1/1000 voltage divider to reduce the voltage (resistors R1 and R2 in Fig. 3.13). The actual voltage reading across the sample was obtained by a voltage pre-amplier ITHACO (Model 1210), and a current pre-amplier ITHACO (Model 1211) with integration time of 300 ms was used for measuring the current response from the sample. The schematic of this measurement setup is shown in Fig. 3.13.

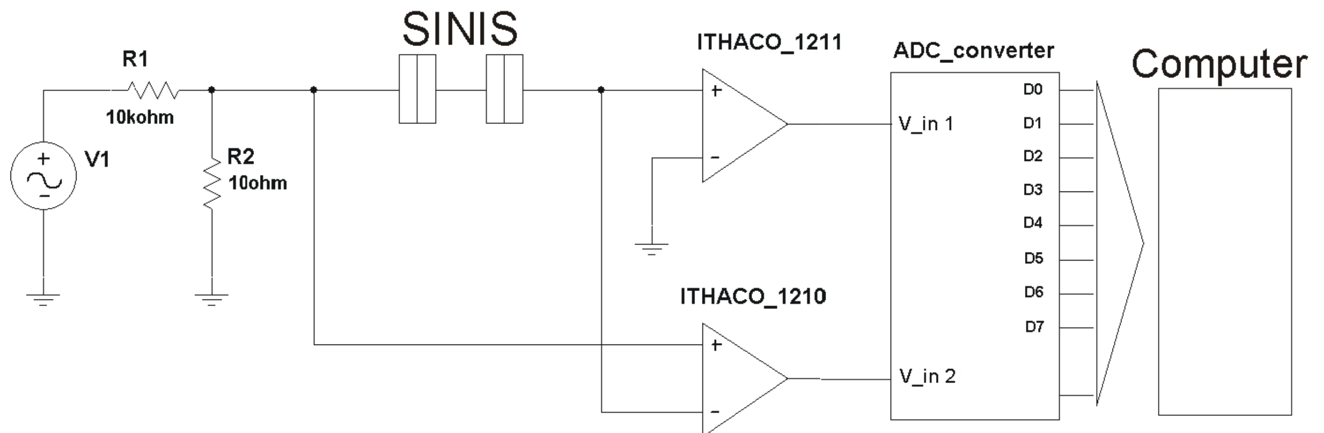


Figure 3.13. The schematics of the I-V curve measurement setup.

During the measurement procedure, the sample was first cooled to 80mK and the I-V curve was measured. After that, the temperature of the sample stage was changed to the next preset value. The on-stage heater of the sample stage was heated by current from the PID controlled register of the DAC card so that the heating power compensated the cooling power of the cryostat at given temperature. The I-V curves of the sample were measured at different temperatures, ending at 750mK. After that, the SINIS junction was biased with a constant current through a 12GΩ resistor and the temperature control PID circuit was switched off. This let the cryostat cool itself starting from 900mK to the base temperature. While cooling, the V(T) characteristics of the SINIS was measured. This measurement was purposely done while cooling and not while heating up by resistor. The cooling process is slow and the temperature variations are free of rapid transient effects caused by the feedback loop of the PID temperature controller.

The first series of measurements was dedicated to the sample with on-chip capacitors (sample #1.) The IV curve of the sample #1 measured at 80mK is shown in Fig 3.14

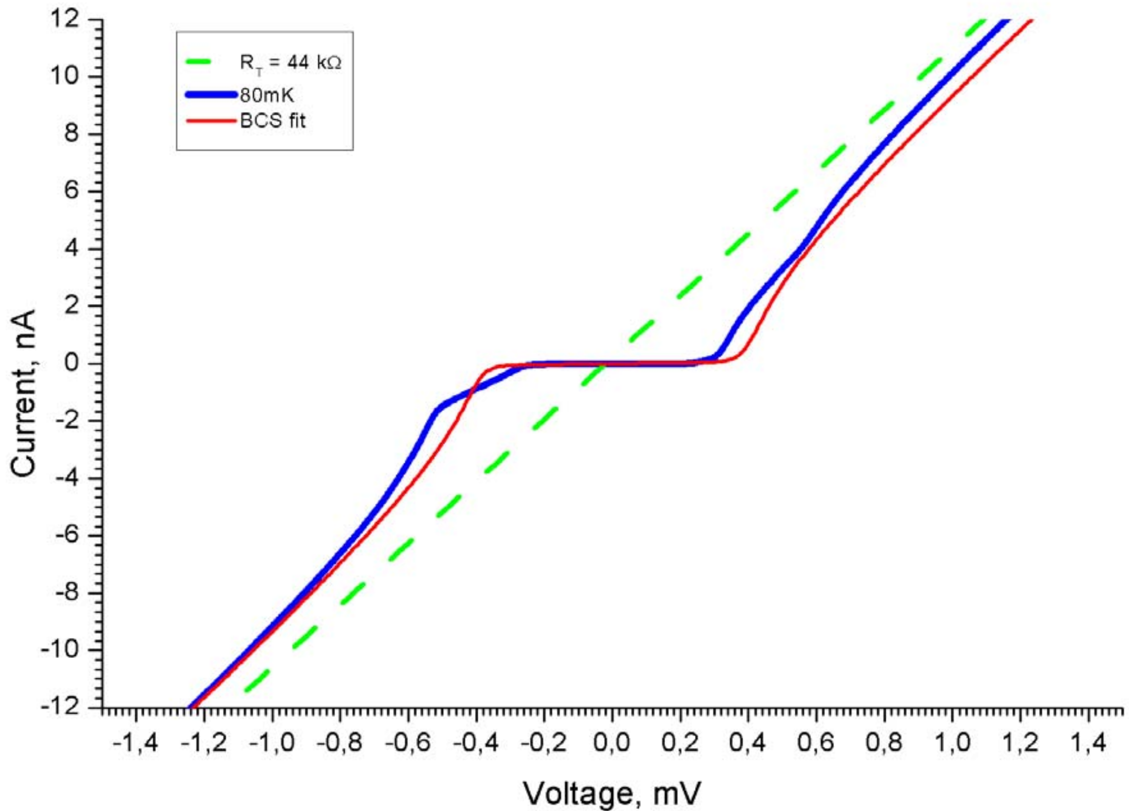


Figure 3.14. The I-V curve for the SINIS sample with on-chip capacitor at 80mK. Green dashed line shows asymptotic ohmic behavior of the 44kΩ resistor. Red line is a theoretical curve of a simple BSC theory prediction.

The derivative of the I-V curve of the sample #1 measured at 80mK is shown in Fig 3.15. Using this data, one can obtain the asymptotic tunneling resistance of the SINIS. The I-V curve of an equivalent resistor is shown in Fig 3.14 as a straight dashed line.

The series of I-V curves of sample #1 measured at different temperatures is presented in Fig 3.16. The same series of curves plotted in log-linear scale is shown in Fig 3.17.

The series of numerically diffentiated I-V curves of the sample#1 measured at different temperatures is presented in Fig 3.18.

Finally, the V(T) characteristics of the sample with on-chip capacitor is shown in Fig 3.19. The biasing current was preset to 4.5pA.

Unfortunately, after the V(T) measurement, the tunnel junction was destroyed electrically and further measurements became impossible.

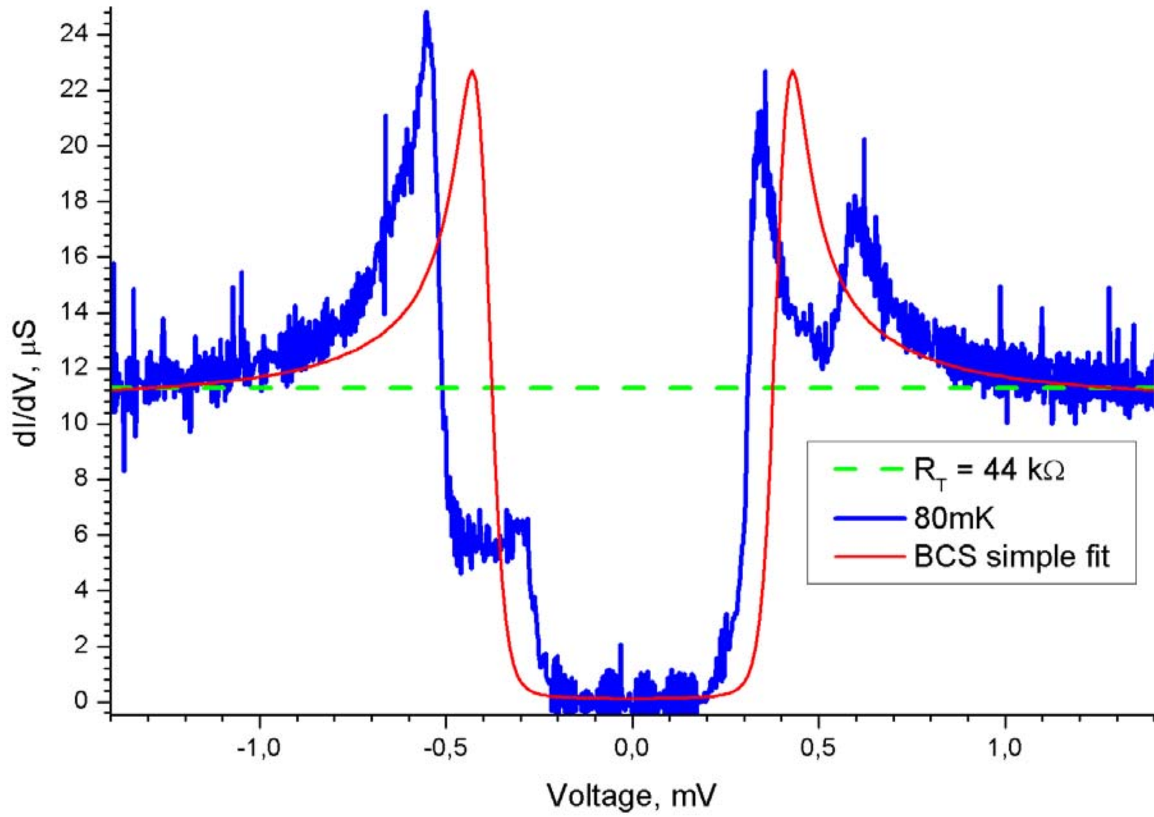


Figure 3.15 The dI/dV characteristics of the SINIS sample at 80mK. Green dashed line shows the asymptotic conductance of the 44 kΩ resistor. Red line is a theoretical curve of a simple BSC theory prediction.

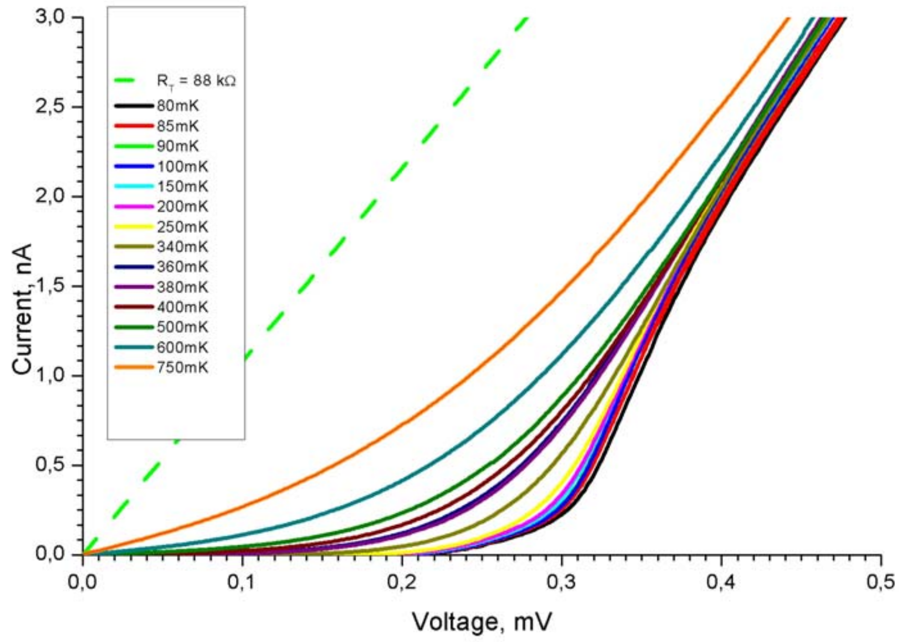


Figure 3.16. The set of the I-V curves for SINIS with on-chip capacitor at different temperatures. Linear scale for the current.

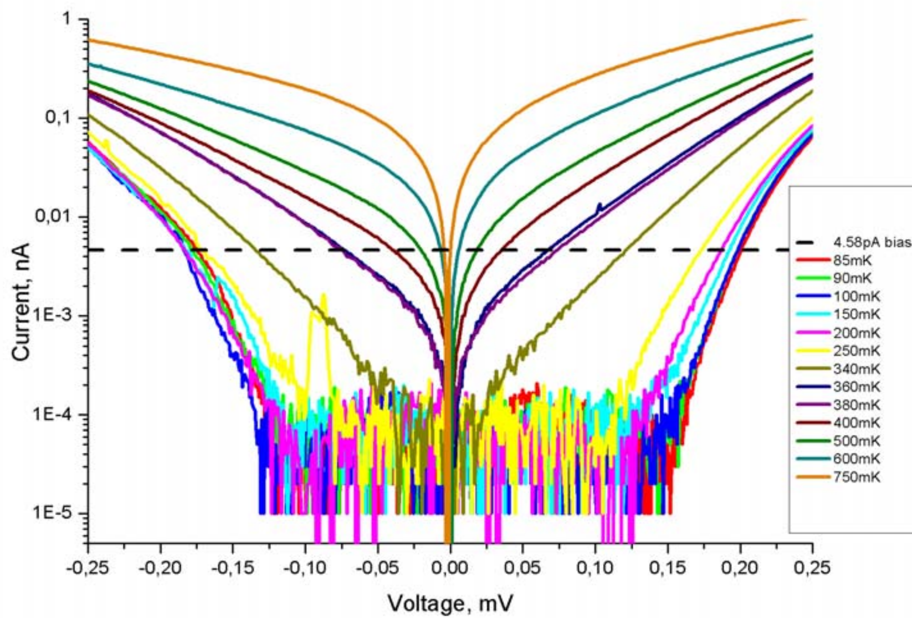


Figure 3.17. The set of the I-V curves for SINIS with on-chip capacitor at different temperatures. Logarithmic scale for the current. The position of the 4.58pA bias current is shown as dashed line.

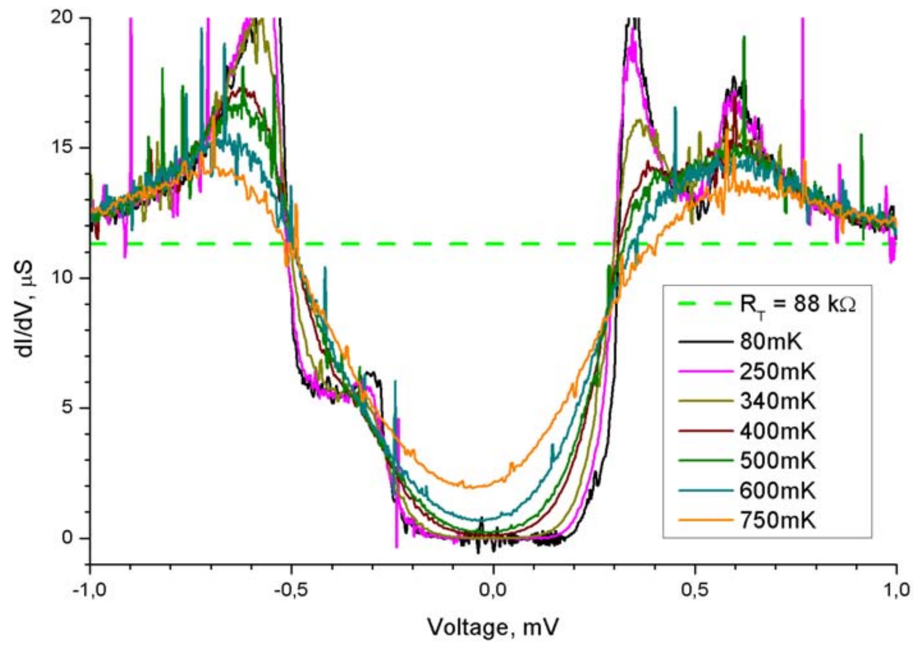


Figure 3.18. The set of dI/dV characteristics of the SINIS sample with on-chip capacitor at different temperatures. The conductance of 88 kOhm is shown as dashed line.

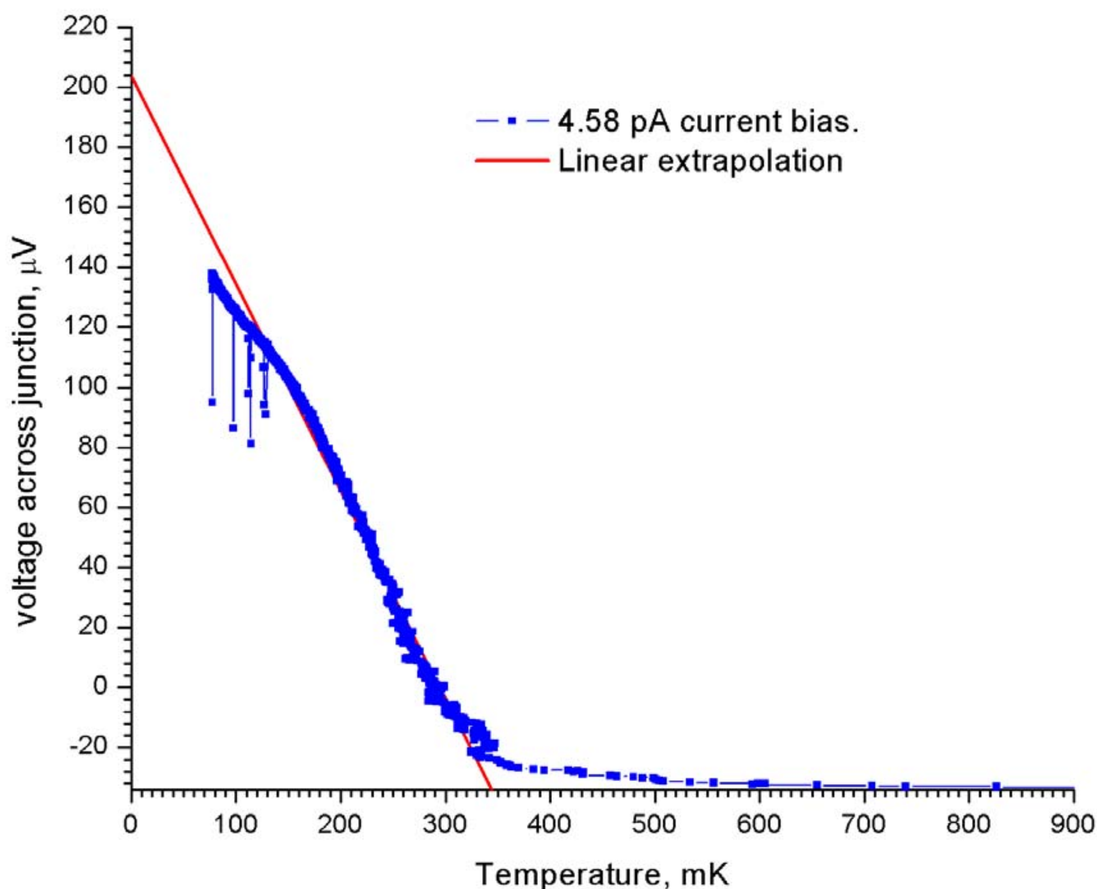


Figure 3.19. The voltage-temperature characteristics for the sample with the on-chip capacitor. Extrapolated linear dependence is shown.

After the first set of measurements the cryostat was warmed up to room temperature and the first sample was detached from the sample stage. The second sample was glued to the sample stage with GE-IMI 7031 varnish and bonded electrically to the measurement lines. After the cooling process a similar set of data was measured from the sample without on-chip capacitor. First, the I-V curve at 80mK was measured. Next, the V(T) characteristic was measured, and then the I-V curves were recorded, starting from the temperature of 900mK down to 250mK. Unfortunately, the second sample was electrically broken after the 250mK measurement.

The measured data are presented in Figs 3.20 – 3.24.

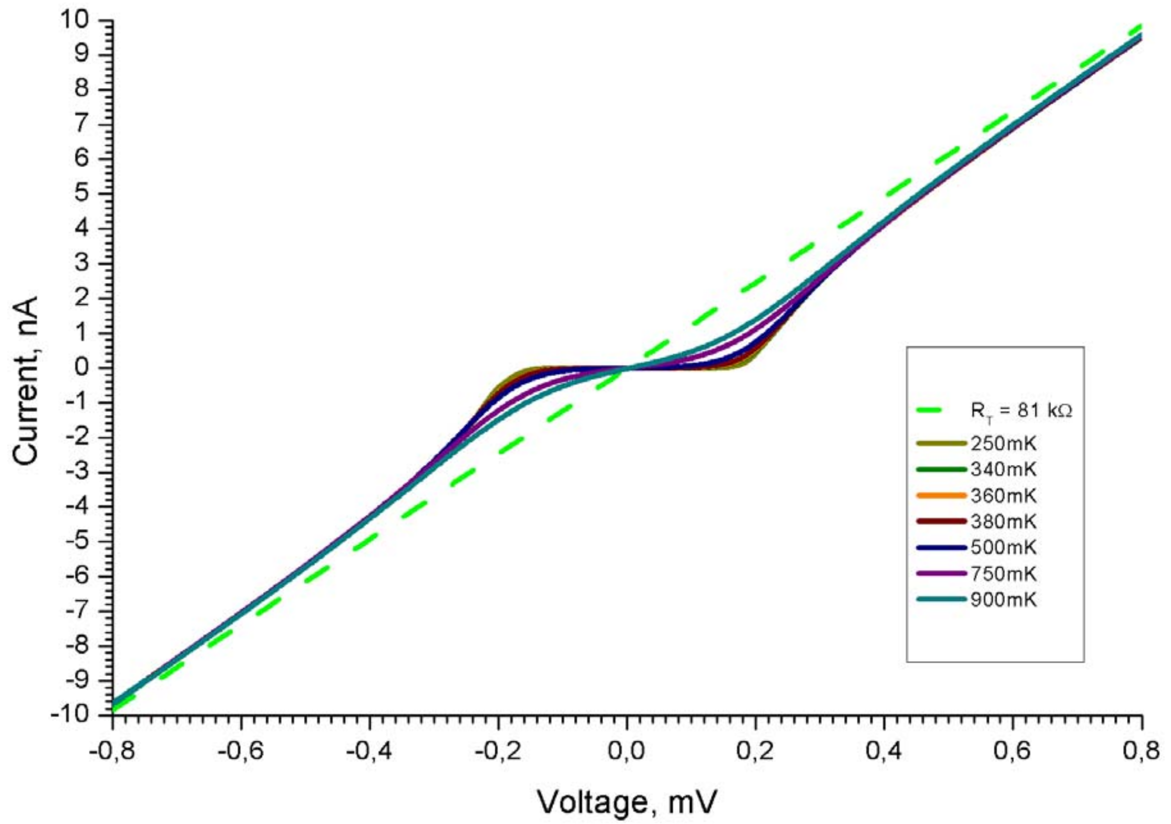


Figure 3.20 The I-V curves for the SINIS sample#2 (without on-chip capacitor). Green dashed line shows asymptotic ohmic behavior of the 81kOhm resistor.

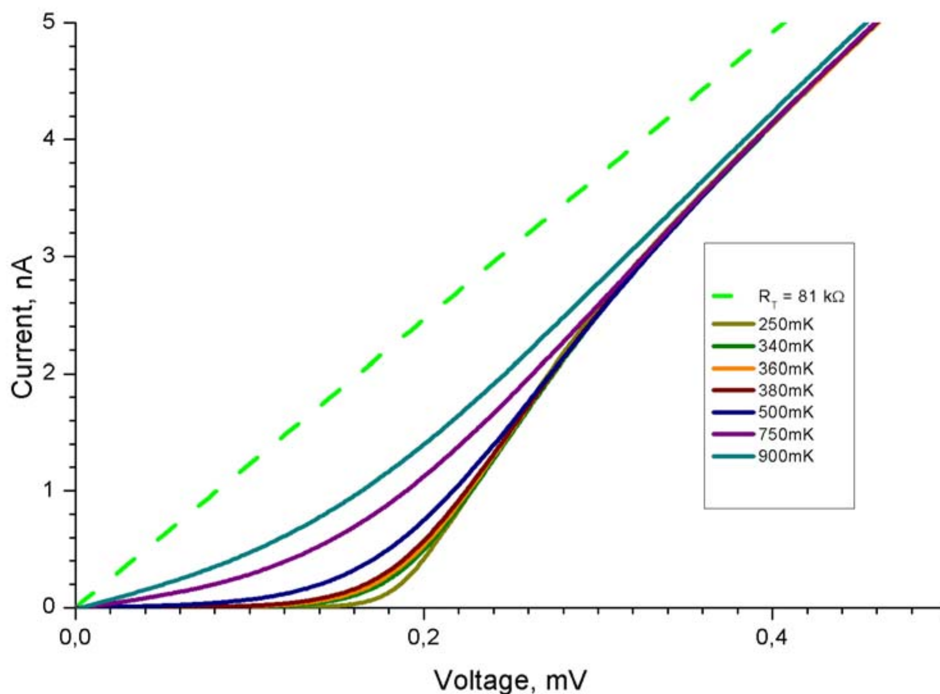


Figure 3.21 The set of the I-V curves for SINIS without on-chip capacitor at different temperatures. Linear scale for the current.

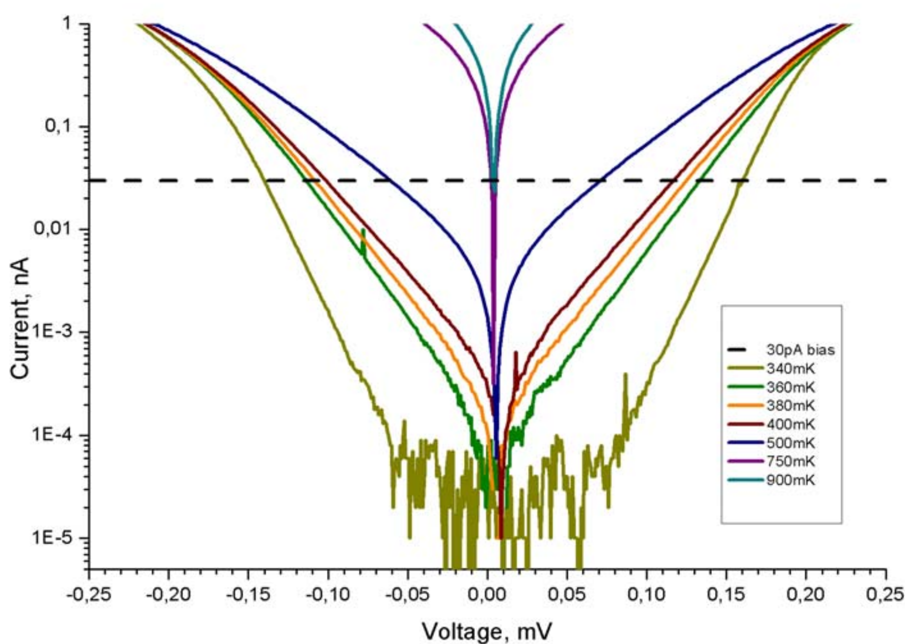


Figure 3.22 The set of the I-V curves for SINIS sample #2 at different temperatures. Logarithmic scale for the current. The position of the 30pA bias current is shown as dashed line

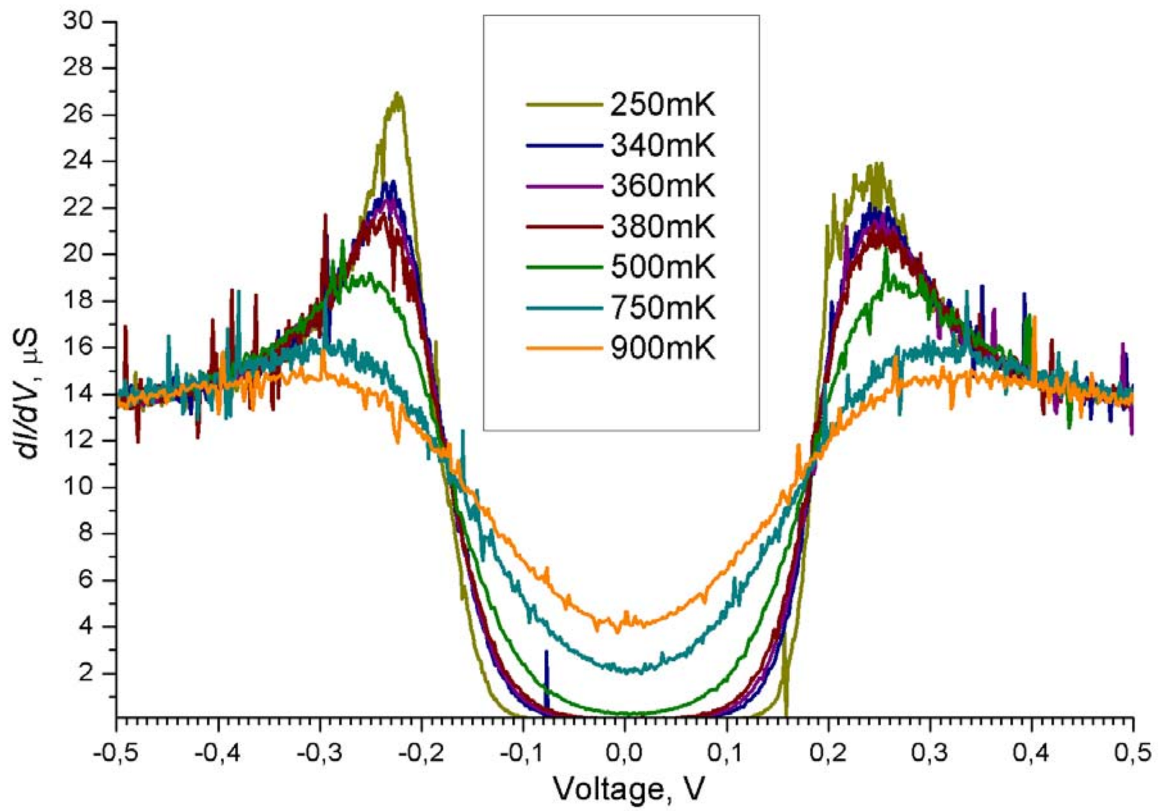


Figure 3.23 The set of dI/dV characteristics of the SINIS sample without on-chip capacitor at different temperatures.

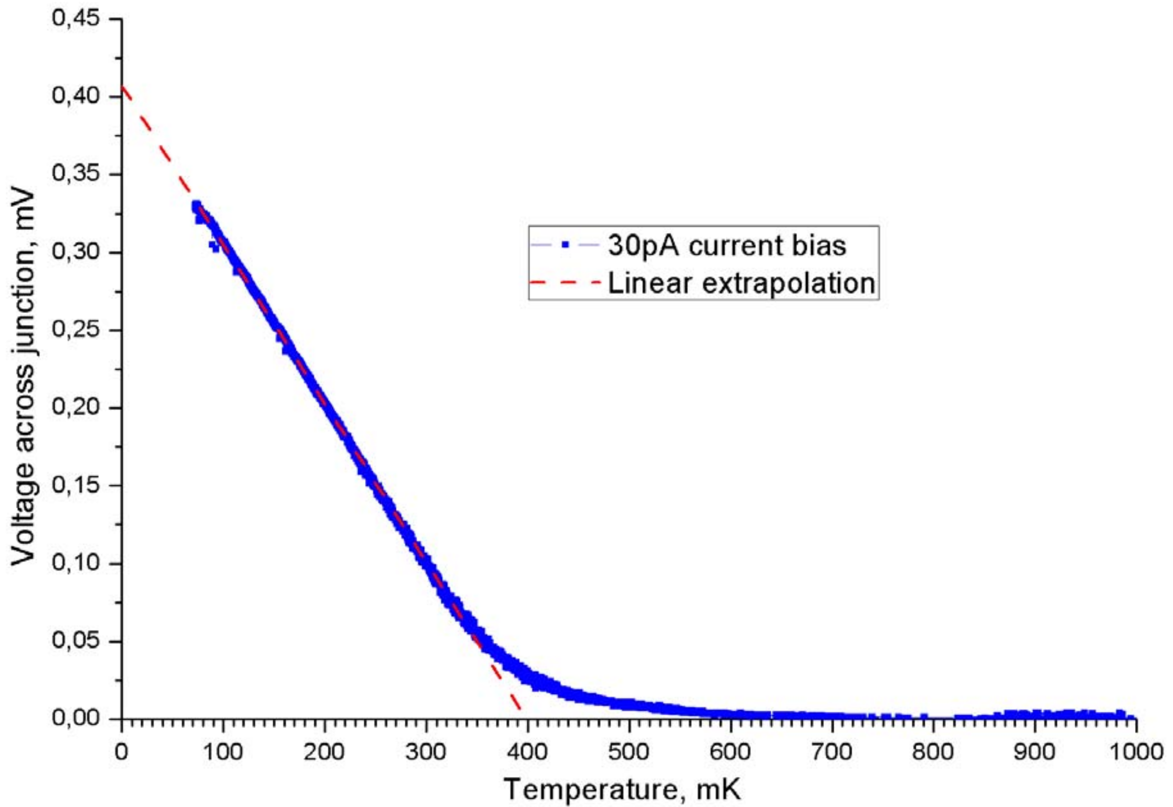


Figure 3.24. The temperature-voltage characteristics for the sample without on-chip capacitor. Extrapolated linear dependence is shown.

3.5 Discussion about the sample data.

3.5.1 Experimental data discussion

Any additional subgap currents can be observed, in log-linear plots as a deviation from the thermally broadened exponential subgap current, which show up as lines in log-linear plots. The plots in Figs 3.17 and 3.22 clearly show that the non-thermal sub-gap currents during this series of measurements was kept under ~ 0.1 pA for both sample types. This result is already one order of magnitude better that in [18], for example in terms of excess subgap current there are no significant differences between two types of samples. This indicates that discrete electronic filtering at the sample stage is effective for low temperature experiments. The additional benefits of on-chip filtering, are harder to quantify based on these measurements..

The voltage-temperature characteristics of both samples (see Fig. 3.19 and 3.24) show almost no deviation from linear behavior at temperatures lower than 150mK. This may indicate that the junction was not affected by sub-gap currents or direct noise heating. However, the first sample (Fig 3.19) shows only half of the voltage of the second sample (Fig 3.24) at the extrapolated point T=0 (0.22mV and 0.42mV). This might happen due to a specific feature of the first sample, which we will explore later.

From the dI/dV data (Fig 3.18) one can see that the I-V curve of the first sample with the on-chip capacitor has a feature that may be described as duplication of the tunnel junction characteristic.

Although the origin of this phenomenon is still somewhat unclear, it did not affect further measurements of V(T) characteristics.

3.5.2 The data description by modified model.

Here we discuss a possible explanation for the modified I-V characteristics of the sample with the on-chip capacitors. A similar modified IV-characteristics can also be found in Ref. [37]. The authors performed an experimental study of electron energy relaxation in a mesoscopic wire placed in a stationary out-of-equilibrium situation. The authors found the distribution function of quasiparticles as a function of their energy. There an Al/AlO_x/Cu tunnel junction was fabricated in the middle of a thin metallic wire of 1.5μm length, connected at its ends to two thick and large electrodes at different potentials. Three regimes of electron interaction were considered. Each regime was described by certain distribution function, different from Fermi-Dirac distribution. In the first regime, when there were no electron interactions and phonon scattering, the distribution function was a weighed sum of Fermi-Dirac functions with zero and non-zero external potential. In the strong electron-electron scattering regime, this function was modified by means of introducing a local electrochemical potential and local electron temperature. In the third, strong phonon scattering regime, the electrons thermalized with the phonons, and only a local electrochemical potential was introduced.

The experimental data presented in Ref. [37] gives a hint that the observed features on the measured conductance vs. voltage curve in our data appeared due to an extra external potential U applied to the junction. Authors in Refs [37, 38, 39] found that the distribution function deduced from the IV-measurements resembled a non-equilibrium electron distribution function in that case. This approach can be adapted to get theoretical description of our measured data. The normal metal distribution function in equation (3.4) can be changed to a linear combination of the Fermi functions of the 2 electrodes, and where we apply the first regime of Ref [37], in other words the limit of non-interacting electrons:

$$f_N(E,T,U)=\frac{1}{2}\left(\frac{1}{1+exp[E/kT]}+\frac{1}{1+exp[(E+eU)/kT]}\right), \quad (3.15)$$

here U is external potential applied to the junction. Fig 3.25 shows the energy dependence of the modified distribution function for several external potentials at 100mK.

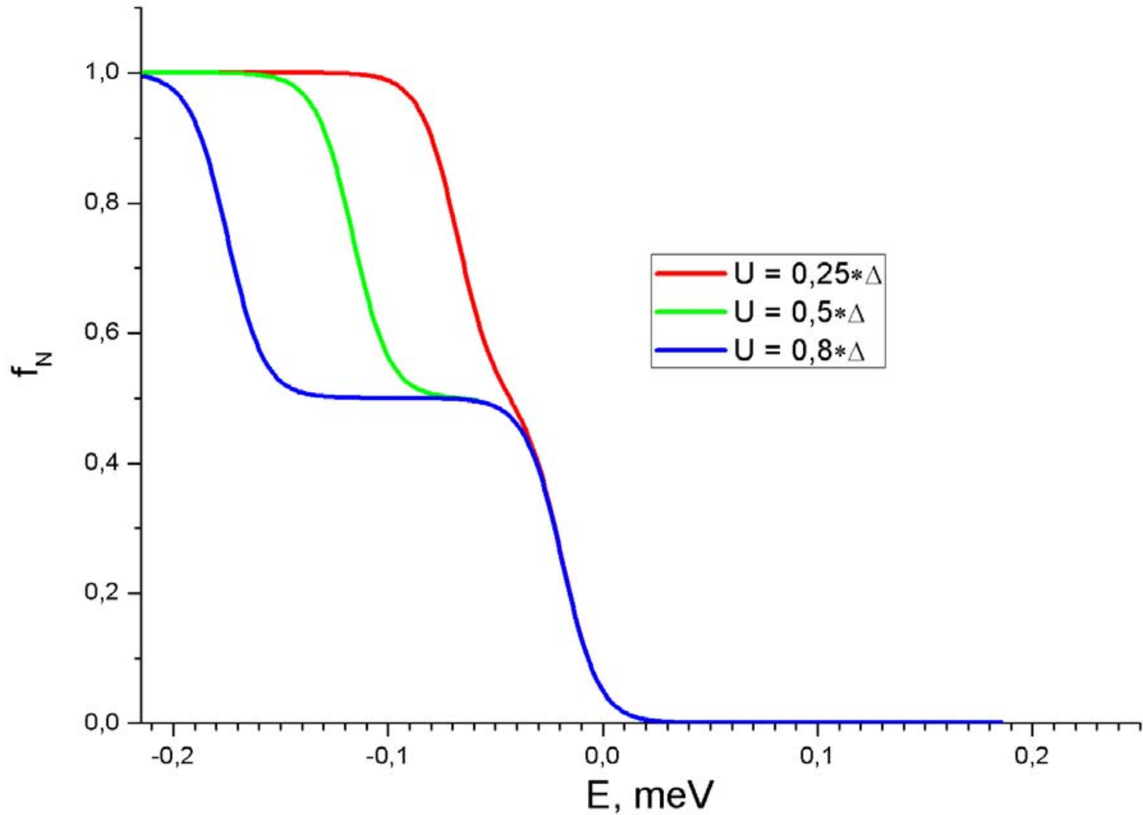


Figure 3.25. The modified distribution function for several external potentials.

It was noted in [37] that the experimental distribution function was different from presented one. The steepness of the experimental function at points $E = \Delta$ and $E = \Delta - eU$ differed significantly from model function. But since there was no function found that could count for mentioned difference, the equation (3.15) could be used.

The expression for tunneling current of a SINIS double junction is then postulated here as:

$$I(V,T,U) = \frac{1}{eR_{tot}} \int_{-\infty}^{\infty} n_S(E)[f_N(E - \frac{eV}{2},T,U) - f_N(E + \frac{eV}{2},T)dE], \quad (3.16)$$

where V is a total voltage across both junctions. Here we used a formula, where only the normal metal distribution is explicit [6, 35].

Fig 3.26 shows calculated conductance using equation (3.16) as a function of bias voltage V at 100mK at several external voltages U. The aluminum energy gap Δ is assumed to be 0.195meV, the tunnel junction resistance is 80kOhm, and damping parameter $\frac{\Gamma}{\Delta}$ is assumed to be 10^{-4}.

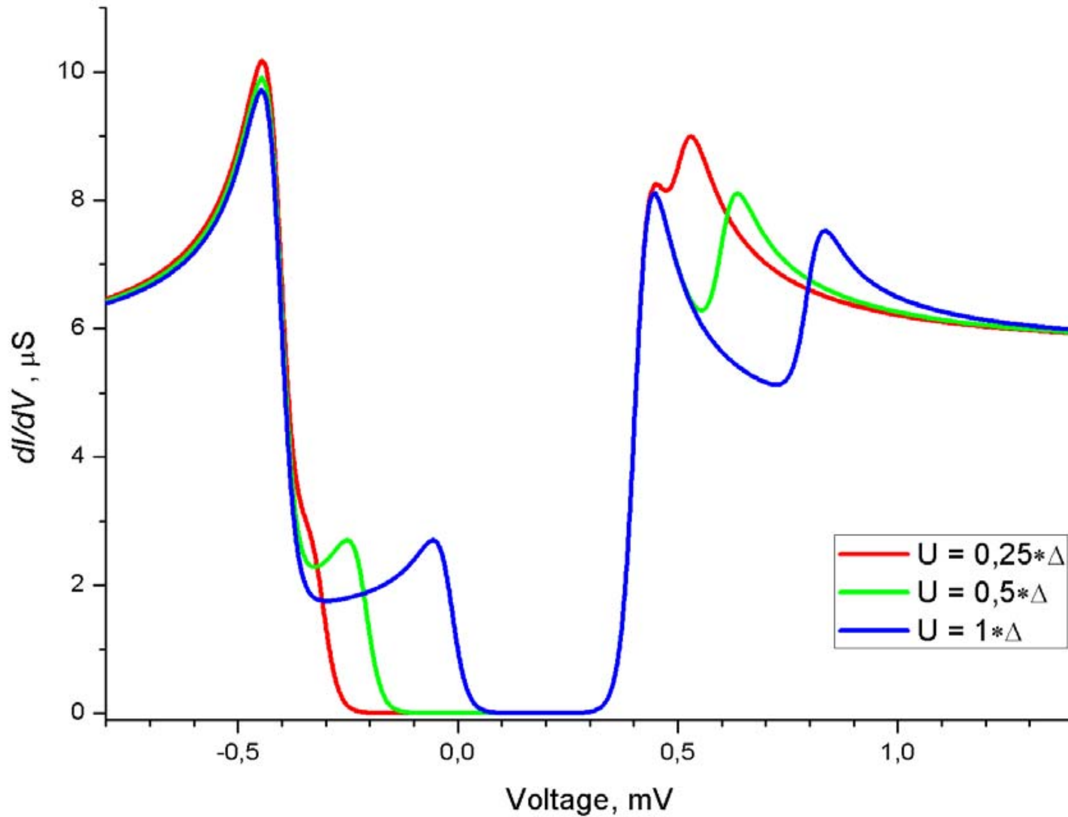


Figure 3.26. The modified conductance for several external potentials applied.

3.5.3 The comparison of experimental and theoretical curves

Using the proposed model of non-equilibrium electron distribution function in the normal metal island one can calculate the I-V curves, differential I-V curves and V(T) curves with different parameter sets. The graphs were calculated using Mathematica 8 environment on a personal computer under Windows 7 x64.

The curves in Figs 3.27 – Fig 3.32 show good qualitative agreement with the experimental data for the sample with the on-chip capacitors. The value of R_T in theoretical calculations for the total SINIS junction tunneling resistance is 88 kOhm, the Al superconducting energy gap value is set at 205 µeV . The DOS broadening parameter $\frac{\Gamma}{\Delta}$ is set at 10^{-4} (if not mentioned explicitly on the legend). The theoretical curves do not exactly follow experimental data. Starting from the curve at 200 mK temperature and higher the theoretical curves behave as if the broadening parameter was too large (Fig 3.27, Fig 3.30), even though it was set 10^{-4}, but the overall agreement is surprisingly good. One can say that the abovementioned model is still not fully describing the experimental data. This is not surprising, considering the simpleness of the form of the distribution function, eq. (3.15) However, one can say that the DOS broadening in these measurements was reduced due to the added filtering.

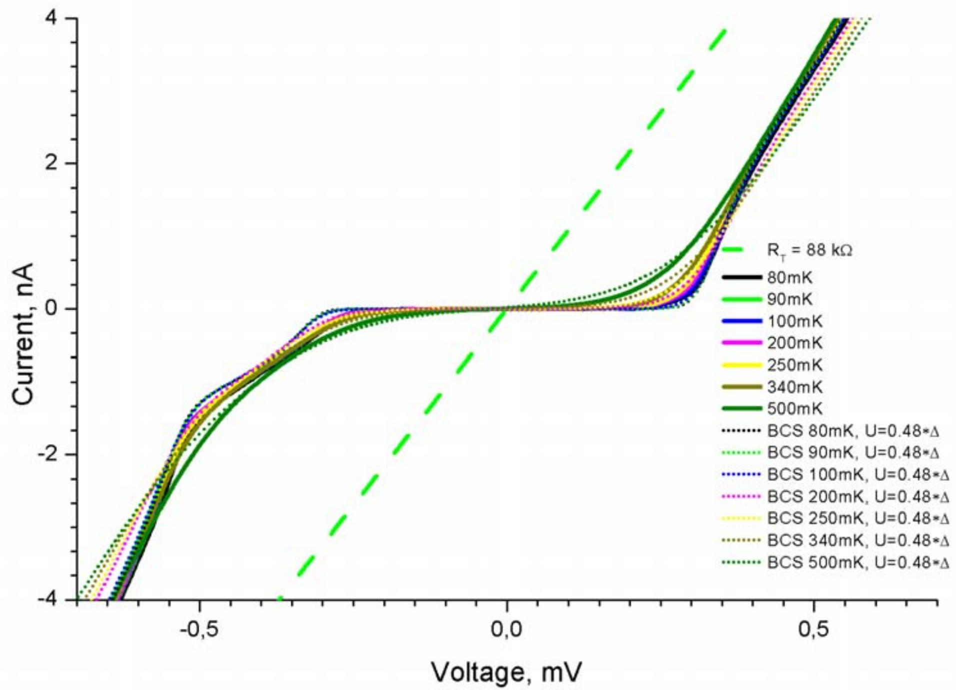


Figure 3.27. The experimental I-V characteristics and theoretically modeled curves for the first sample.

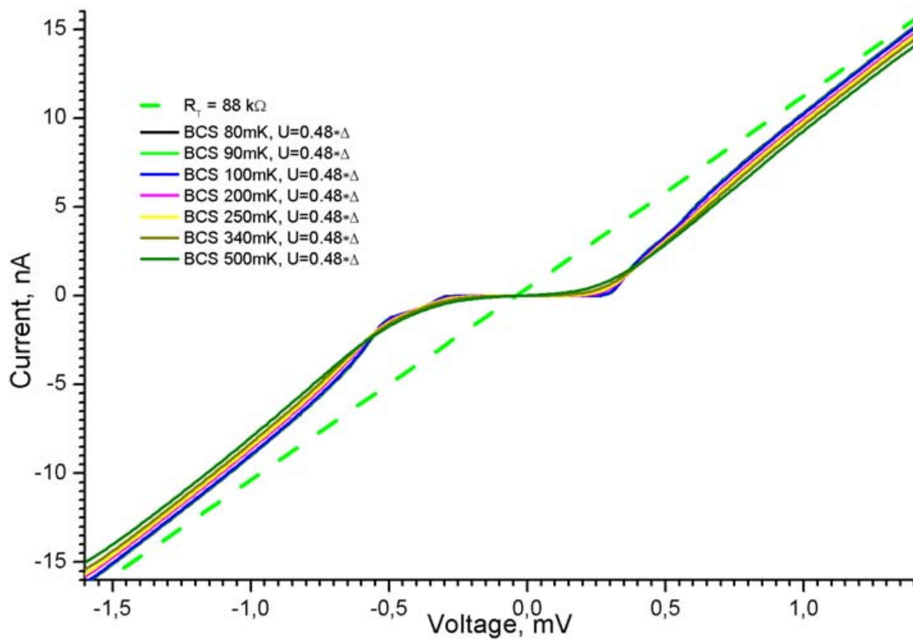


Figure 3.28. The theoretically modeled curves of I-V characteristics of the first sample.

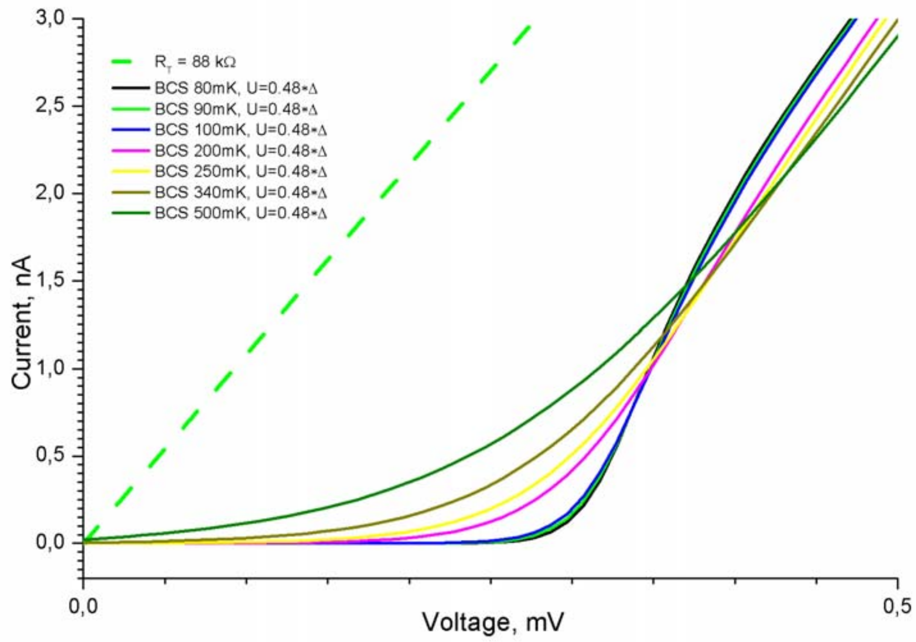


Figure 3.29. The theoretically modeled curves of I-V characteristics of the first sample, expanded view.

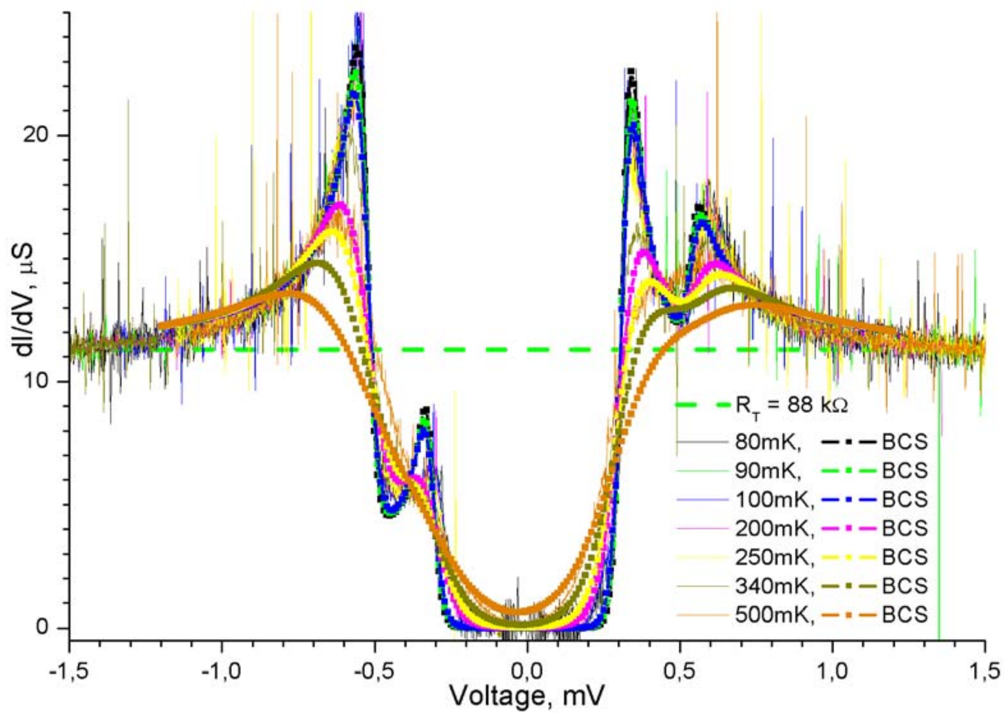


Figure 3.30. The differential conductance curves for the first sample. Experimental and theoretically modeled curves.

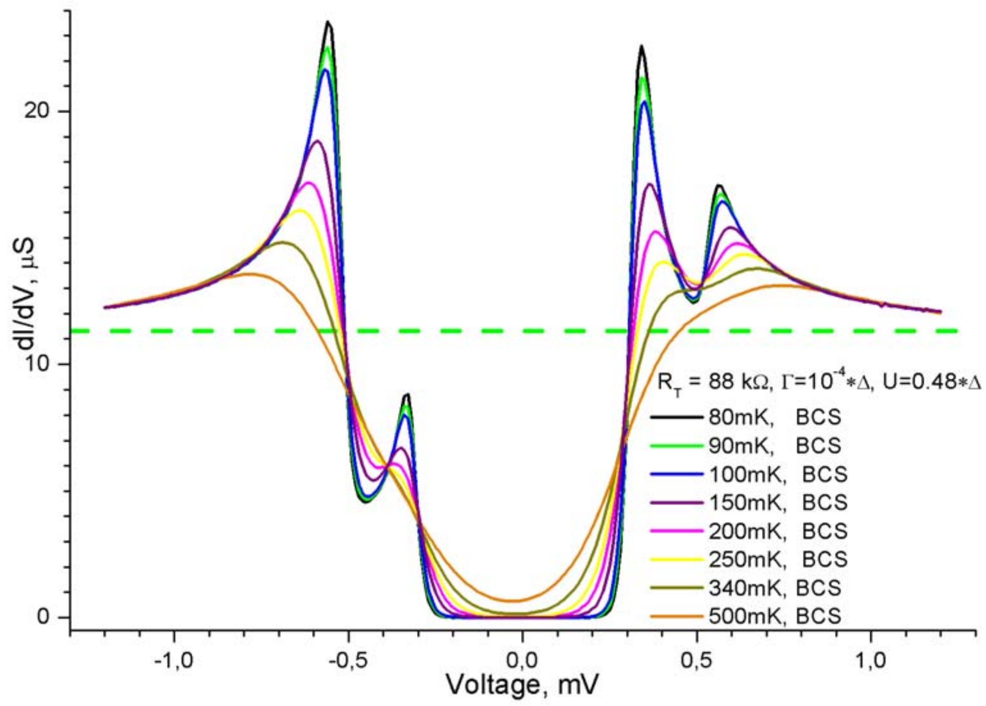


Figure 3.31. The BCS calculation for the differential conductance curves for the first sample.

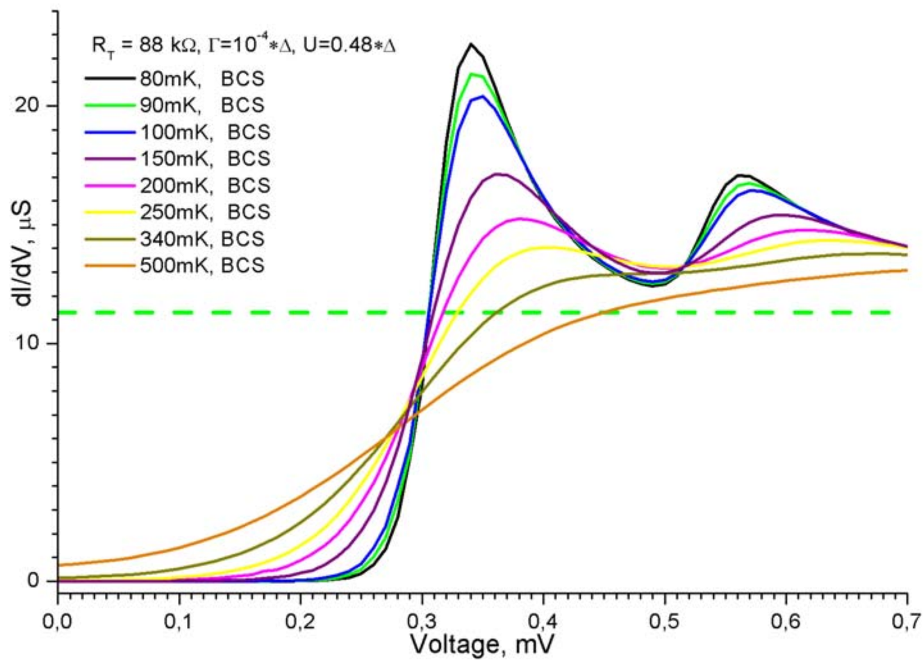


Figure 3.32. The BCS calculation for the differential conductance curves for the first sample. Expanded view.

One can assume that the second sample does not have the abovementioned features, and does not require introduction of an external potential. However, better results may be achieved if a small deviation is assumed. The value of the external voltage parameter U of 0.16 (measured in Δ units) fits the experimental data of 80mK better than the theory without non-equilibrium deviations. Fig 3.33 and Fig 3.34 show the I-V and differential I-V curves for the sample without on-chip capacitors. For the second sample the value of R_T in theoretical calculations for NIS junction is 78 kOhm, the Al superconducting energy gap value is set at 205 μeV. The DOS broadening parameter is set at 10^{-4} (if not mentioned explicitly on the legend).

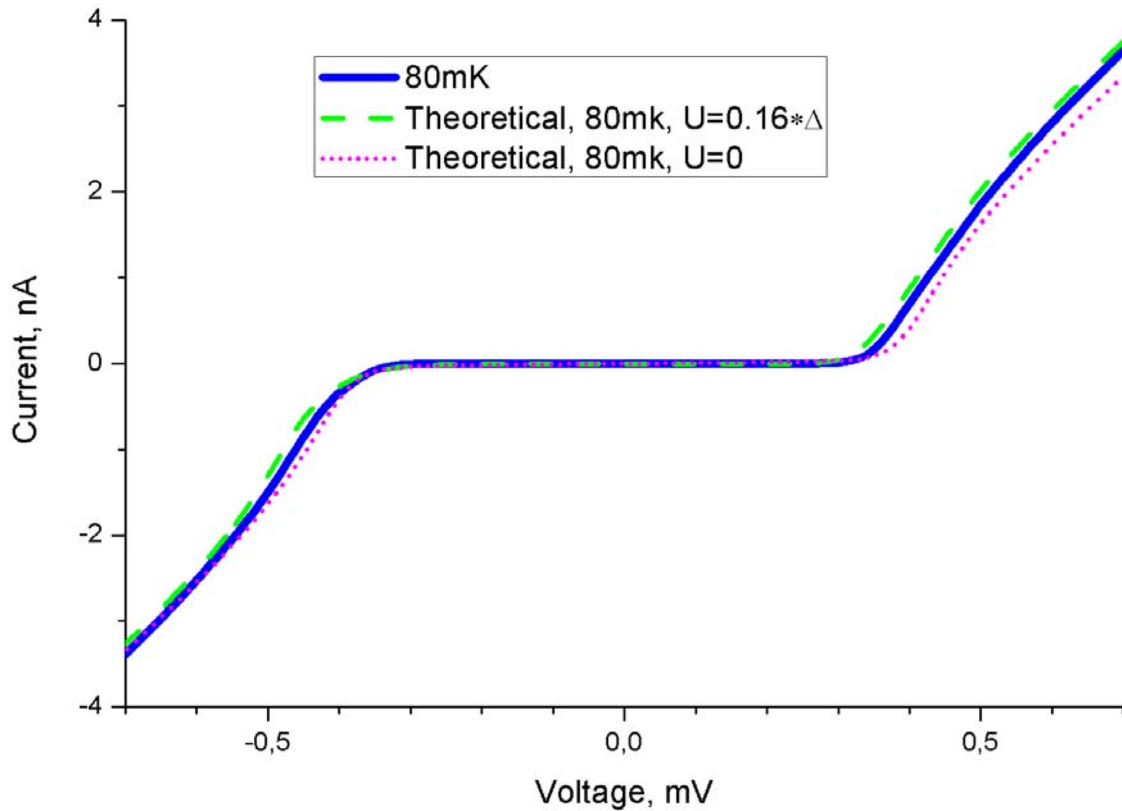


Figure 3.33. The I-V characteristics and theoretically modeled curves for the second sample.

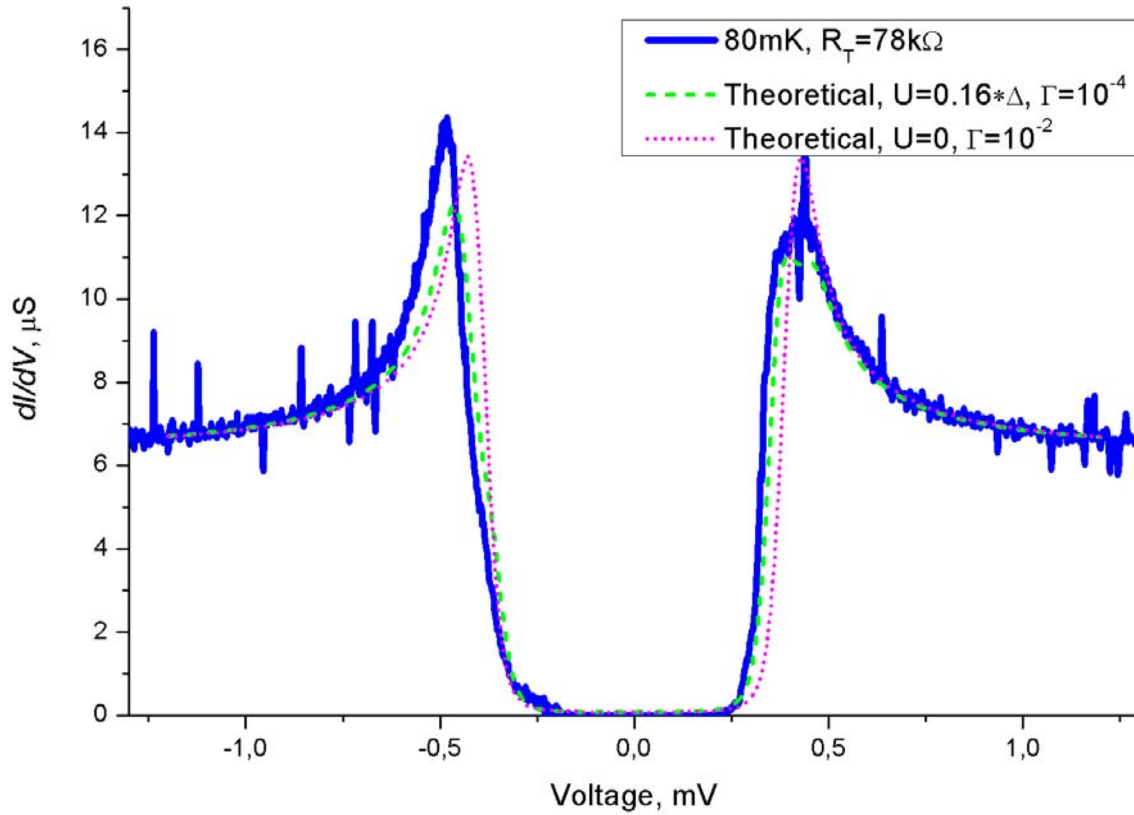


Figure 3.34. The dI/dV characteristics and theoretically modeled curves for the second sample.

Unfortunately, the non-equilibrium extension of the theory did not allow to get good theoretical curves for the V(T) measurements. The theoretical curves, calculated as a function of *U* are shown in Fig 3.35 for the first sample, and in Fig 3.36 for the sample without on-chip capacitors.

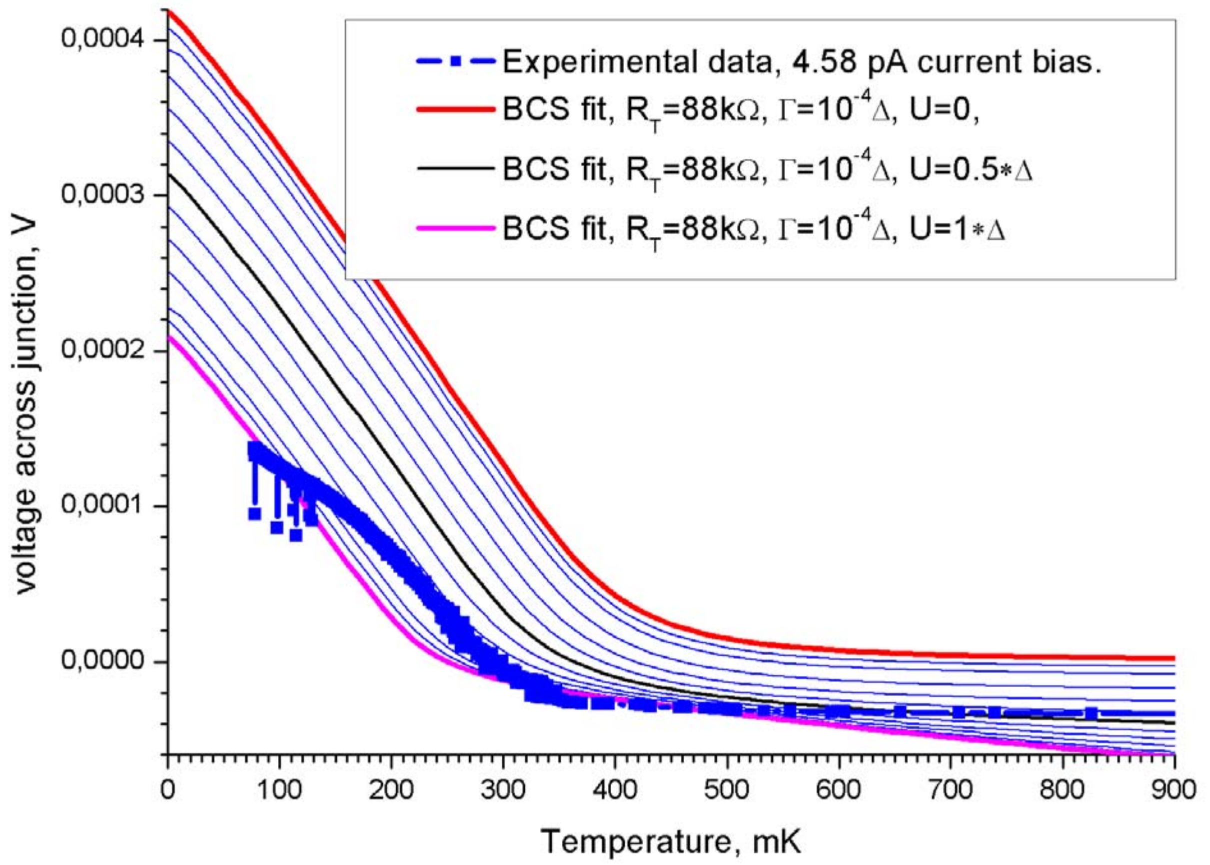


Figure 3.35. The V(T) characteristic and theoretically modeled curves for the sample with on-chip capacitors. The different curves represent different values of external potential difference *U*: 0, 0.05, 0.1, 0.2, …, 0.8, 0.9, 0.95 and 1 in units of superconducting energy gap value Δ.

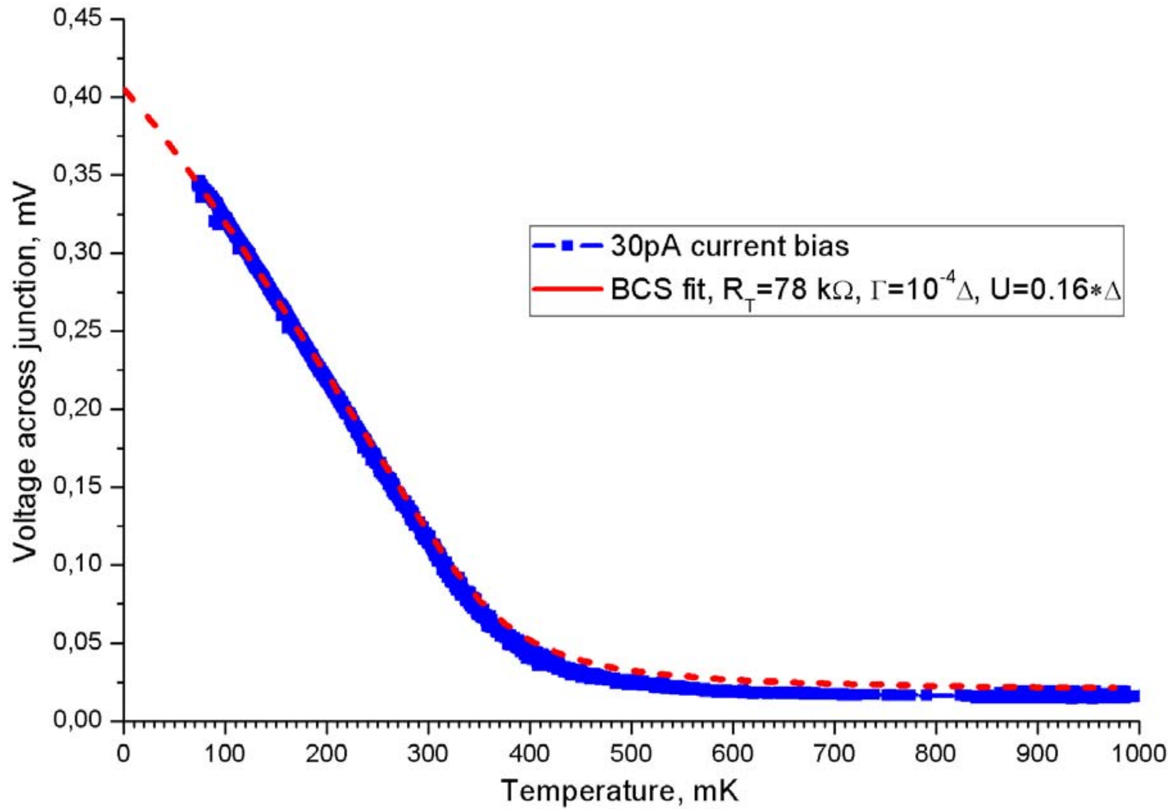


Figure 3.36. The V(T) characteristic and theoretically modeled curve for the sample without on-chip capacitors. The value of U is set at 0.16Δ, R_T=78kΩ.

The remaining task is to answer the question what causes the external potential to be applied to the SINIS structure. It is interesting to note that the value of external potential energy eU deduced from experimental data of the first sample is ~0.2meV for 70-500mK measurements. This value is similar to that of superconducting aluminum energy gap, which may give a hint to the origin of the effect.

4. Conclusions

The goals of this work were to develop, fabricate and test the miniature filters, capable of eliminating thermal noise heating effect from low temperature experiments.

The filters were successfully fabricated and incorporated into an existing dilution fridge. The challenges met during filter fabrication included the high viscosity of epoxy mixed with stainless steel powder and the special elevated temperature requirements for handling of Eccosorb material. The manufacturing process took many working hours of precise handcrafting.

The new design of the sample stage was designed to fit new filtering elements. Presently, only 8 filters out of 16 are installed into electrical wiring setup. This number will be increased to all 16 after ongoing total reconstruction of the cryostat.

Each filter was characterized independently to ensure high enough attenuation at frequencies above 100MHz. The challenges of high-frequency measurements included resonance peak formations due to standing wave conditions in the RF setup.

Two samples were successfully fabricated. The samples contained SINIS junctions, which are extremely sensitive to the alterations in their electron temperature due to noise heating.

The samples were measured using a dilution refrigerator with base temperature as low as 70mK. The setup for measurements was only tested in DC mode, the AC performance will be tested and improved in future as ongoing research.

The series of low temperature experiments showed that with the help of the new filters, the noise heating at low temperatures was avoided. The measured calibration curves for SINIS junction thermometry with fabricated samples show linear behavior in full range of available temperatures. The DOS broadening parameter was shown to be low enough and not causing the problem of excess sub-gap current in SINIS thermometer, which could otherwise restrict the operation of SINIS junctions below 100mK. Finally, the sample with on-chip capacitor showed interesting features in the I-V curves. These were successfully modeled by a non-equilibrium theory.

Appendix A: The set of drawings of the sample stage.

Appendix B: The description of the software for simulation of the angular UHV metal deposition process.

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Φ6,0

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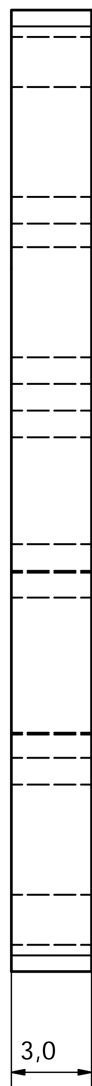

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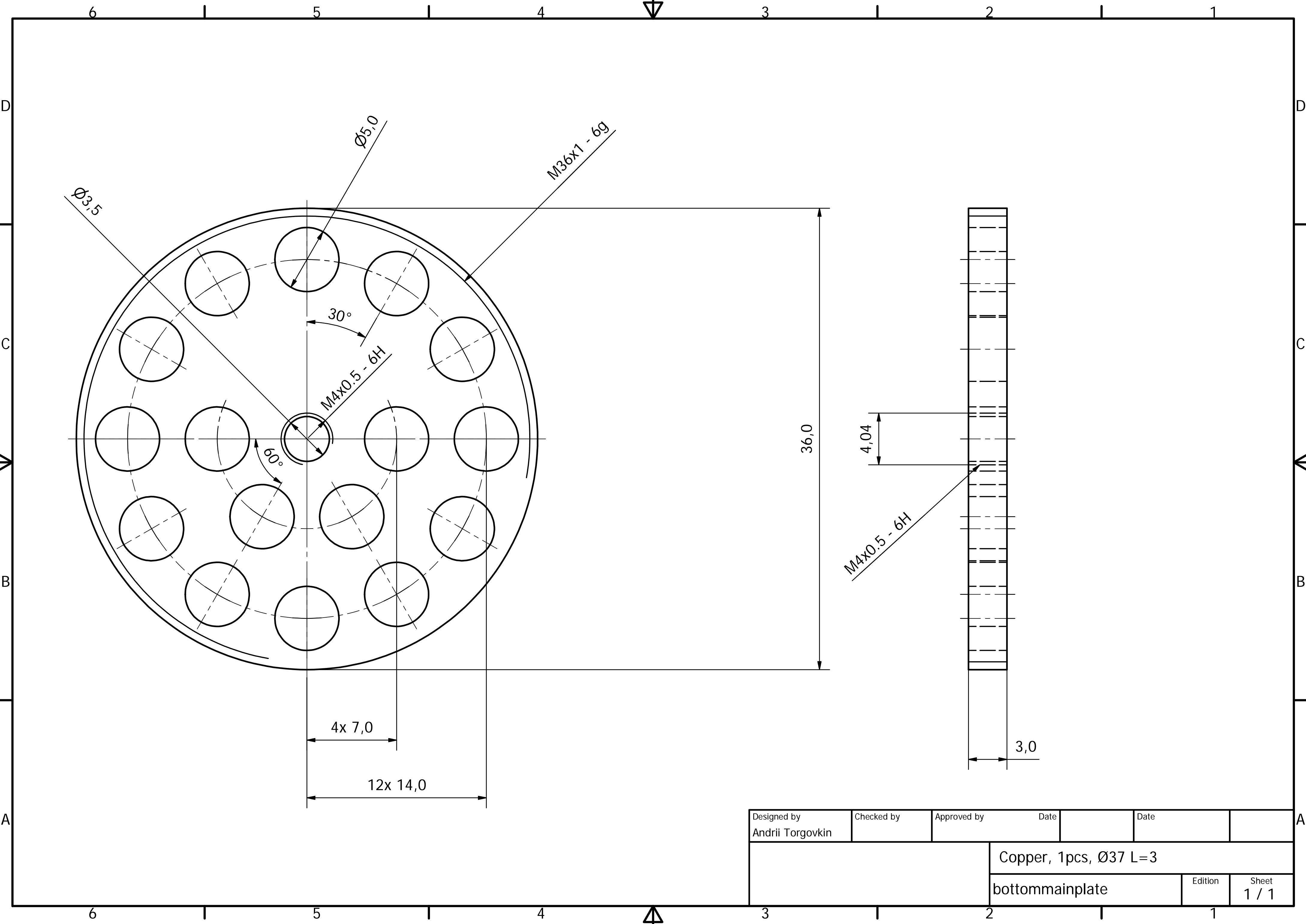
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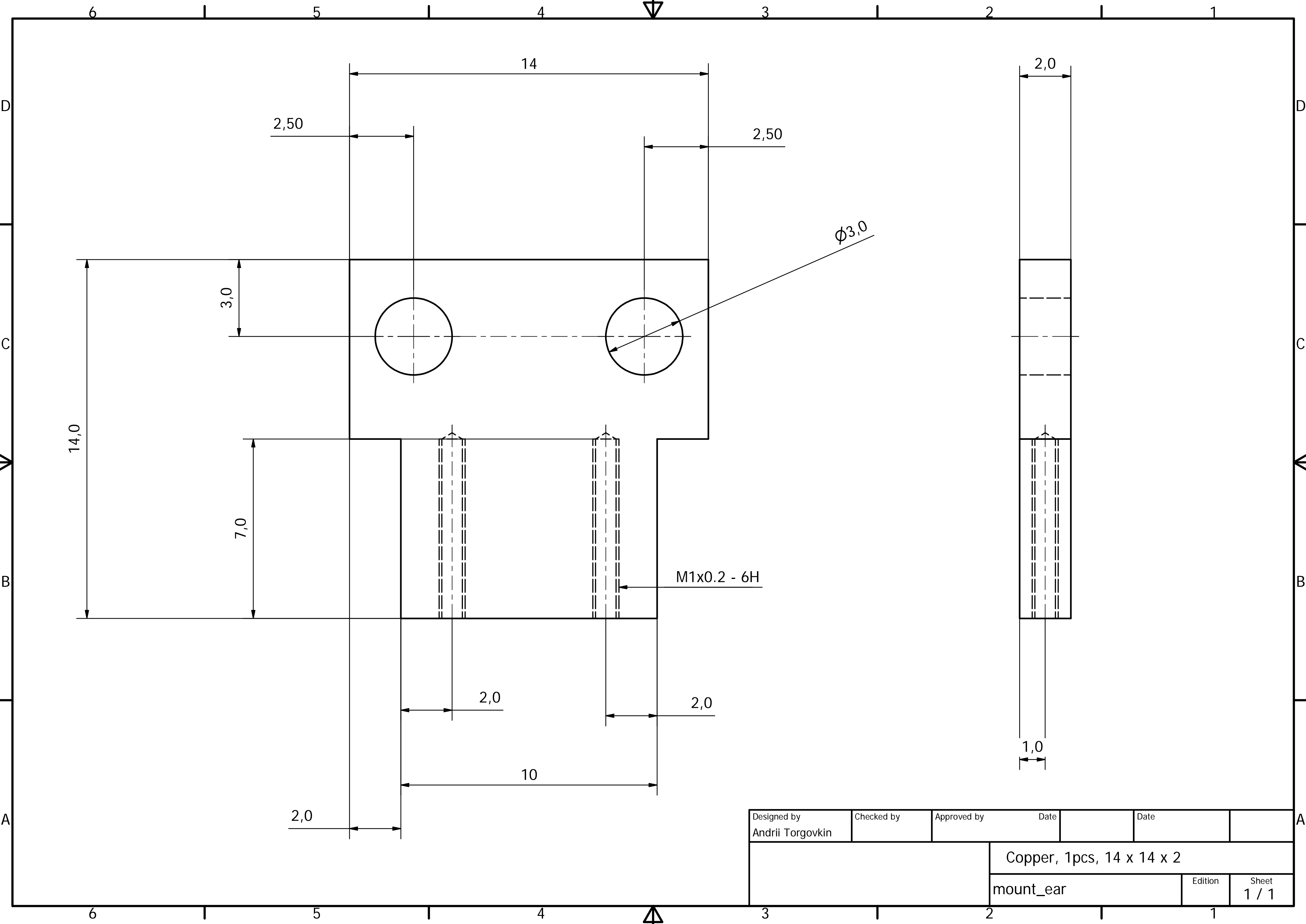
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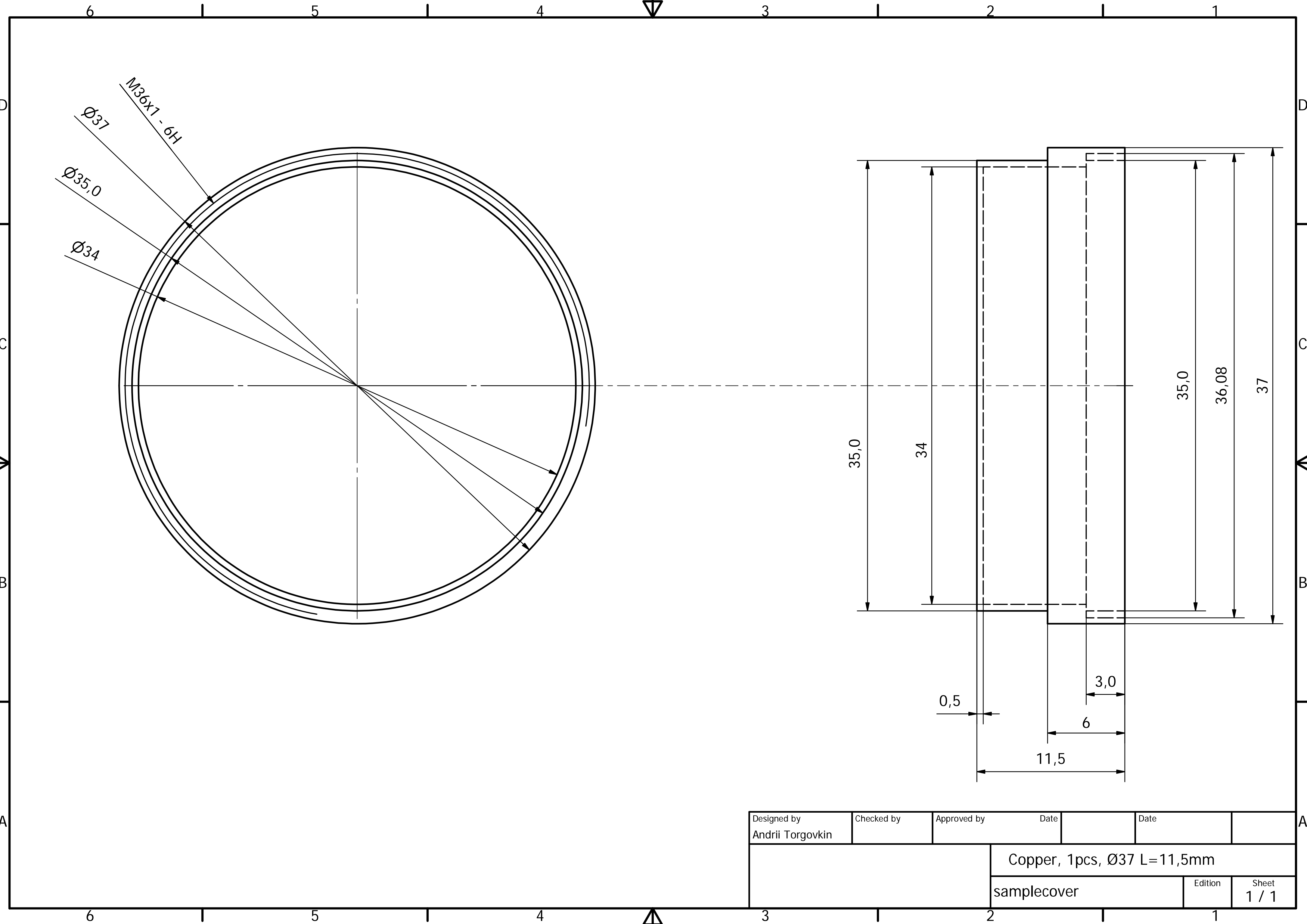

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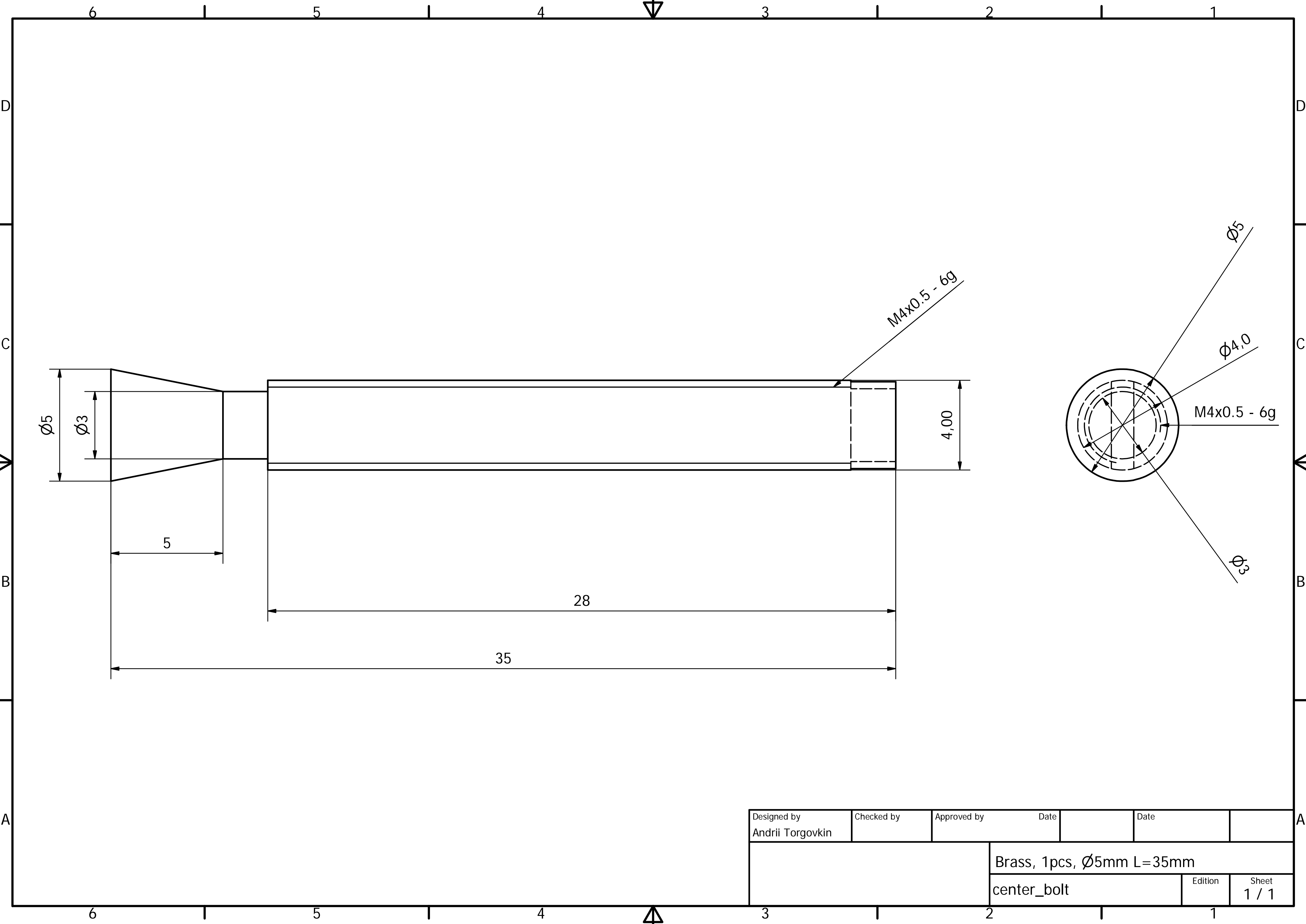

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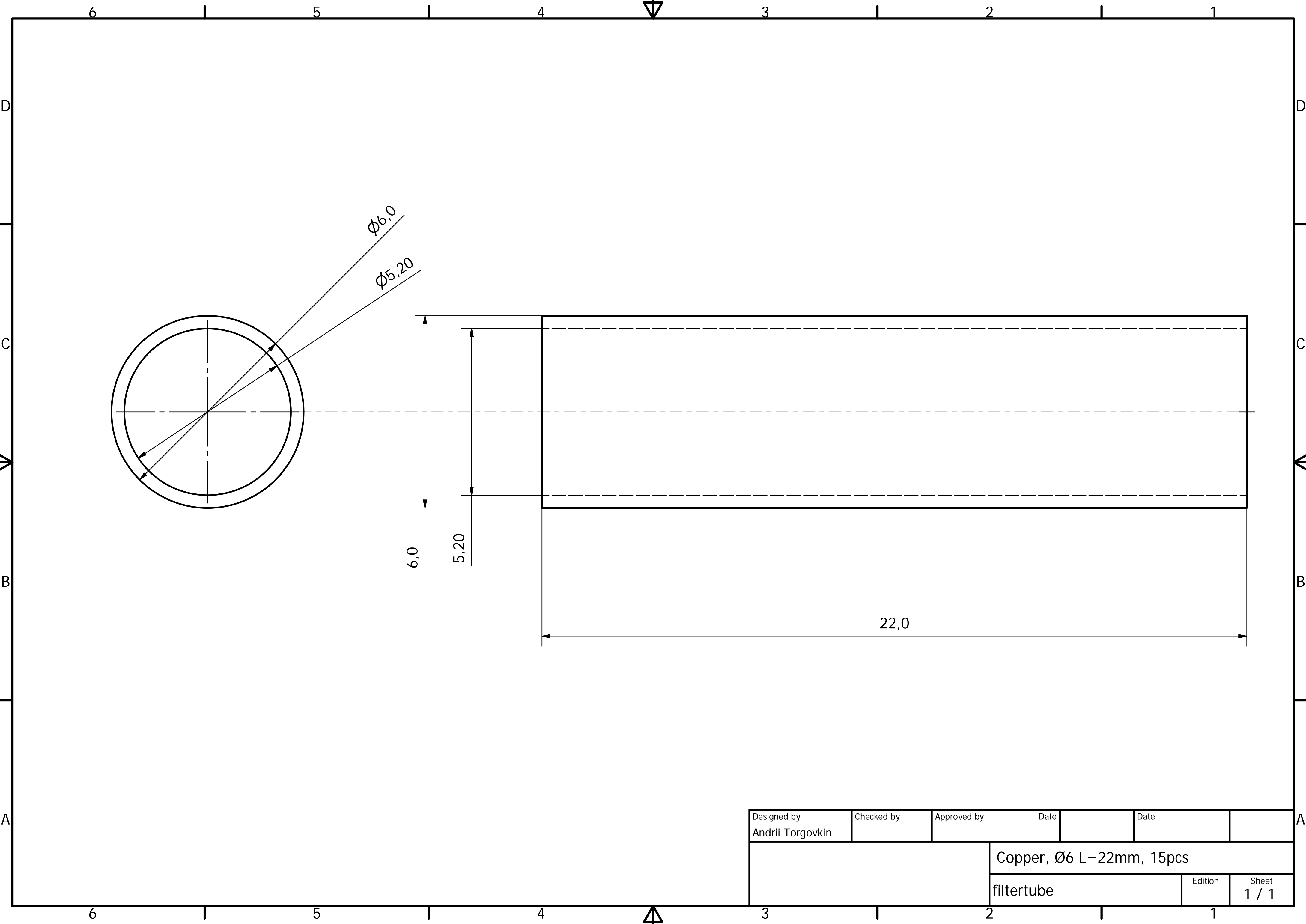
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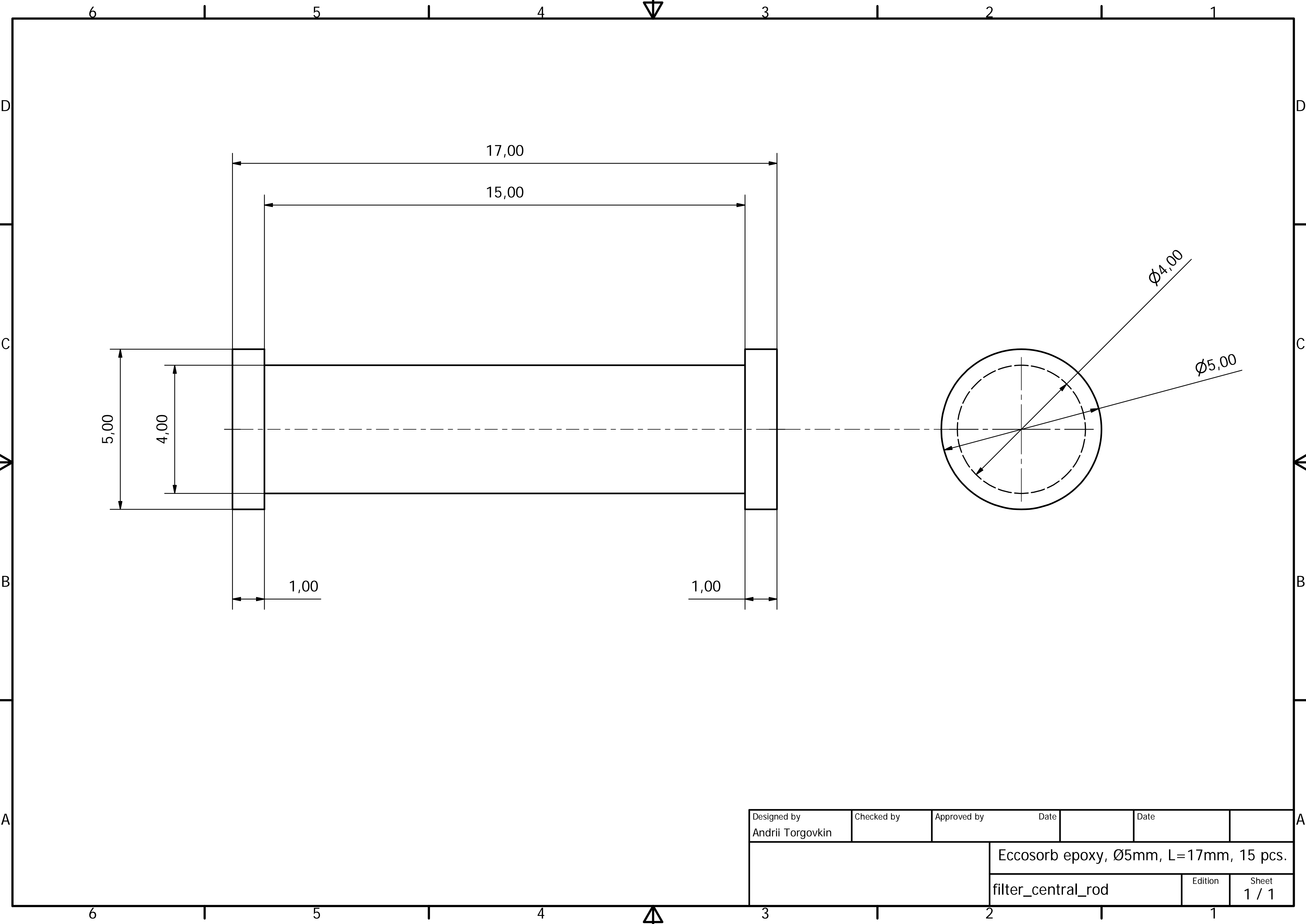
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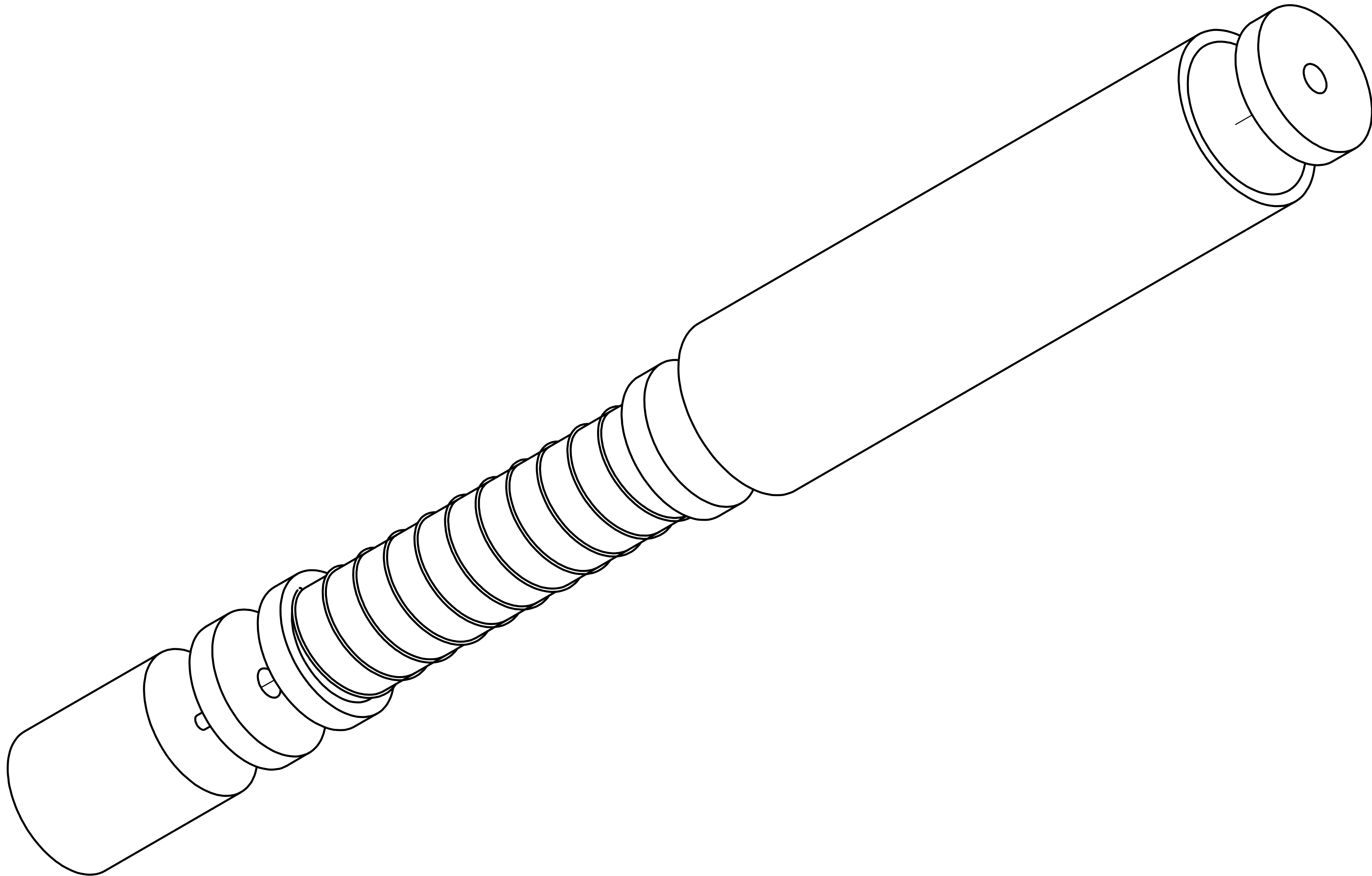

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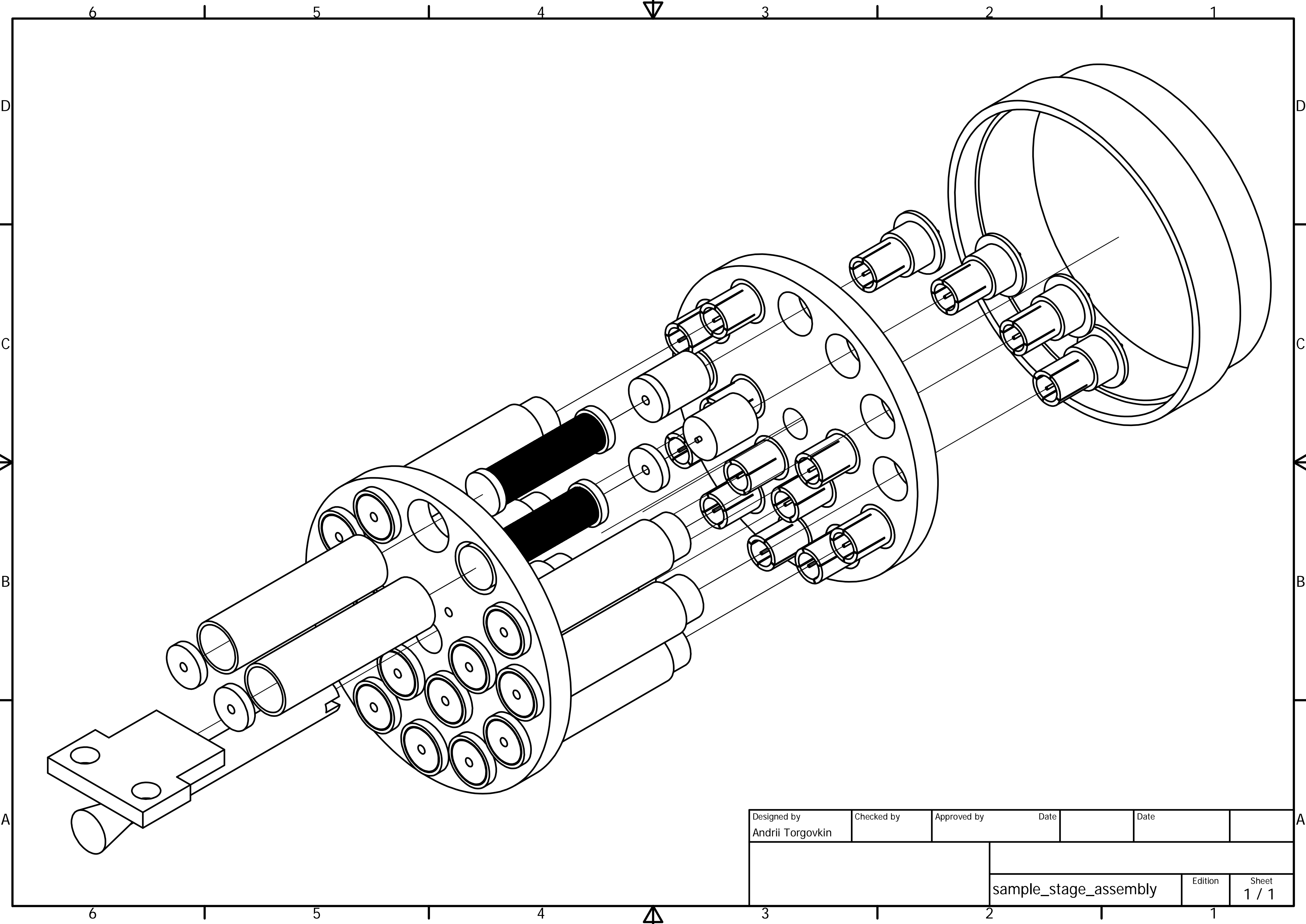

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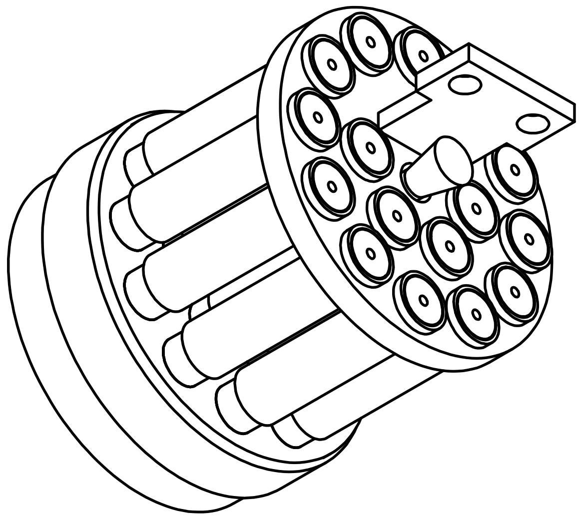

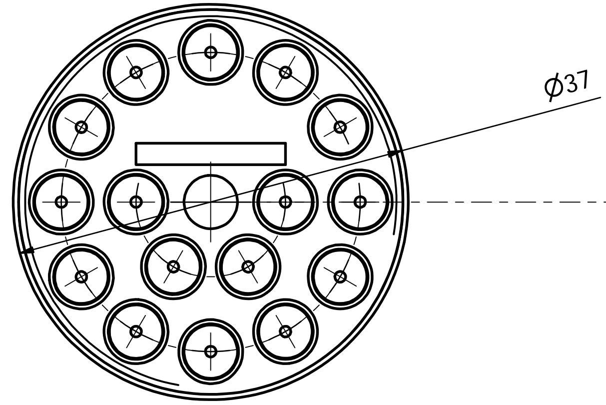

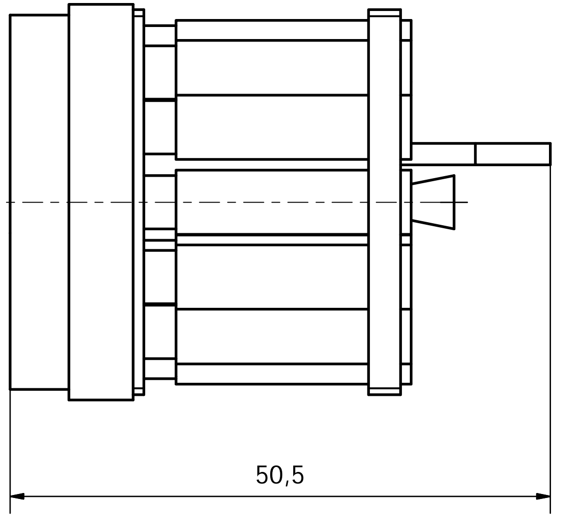

Designed by	Checked by	Approved by	Date	Date
Andrii Torgovkin				

Sample Stage Assembled	Edition	Sheet
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Appendix B

The program for simulation of the angle evaporation process with the shadow mask technique.

Many microfabrication processes rely on a so called angular shadow evaporation technique. The term angular evaporation is related to the physical vapor deposition process, when a material is physically turned into a gas phase and then transported in vacuum to the desired substrate, where the material condenses. In the case of ultrahigh vacuum conditions, the deposition is a line-of-sight process and can be described by ballistic transport. Typical geometrical restrictions for the ballistic line-of-sight evaporation are following:

- the distance between the source of evaporated material and the deposition target must be smaller than the mean free path of the remaining gas molecules in the process chamber;
- the sizes of the source and the target must be much smaller than the distance between them;
- the thickness of deposited material is much smaller than in-plane dimensions of the deposited structure features.

If these conditions are fulfilled, the deposition process can be easily simulated. The main goal for the simulation is computing a shadow map of deposited material on the target, when a set of obstacles that may create shadows is given.

In a considered model of angular evaporation, the source is a point-like object and a target is a plane, containing a predefined structure. The variation of distance from the source to the target along the target is neglected. The deposited material can hit the target plane at different angles; the vector from the target to the source is defined using polar coordinates. The predefined structure on the target can consist of previously deposited structures as well as double-layered photoresist structure.

The way of data handling for the program was chosen to be in the form of uncompressed bitmap images. In the bitmap image each pixel can contain up to 24 bits of information, limiting the number of its states to roughly 16.7 millions. Thus, the use of bitmap image offers easily accessible and editable planar map of integer numbers, stored and viewed in the form of RGB color components.

The program stores the information about height of the structure on the chip in the form described above. Each pixel of the image, responsible for the existing structure, has its own value. In the current version of the program, this value shows the height, measured in nanometers, of the box with in-plane dimensions, limited by the size of the pixel in chosen scale. This in-plane scale can be chosen by user.

The information about the photoresist GDSII layers is also loaded to the program in the form of image. This image defines the size in pixels of the program working area. The color code for this image is following: white color stands for non-exposed photoresist, any other color program interprets as if photoresist was exposed at this area.

In real world, the PMMA polymer and MMA copolymer is a convenient choice of photoresists, because they can be developed in different ways after they were simultaneously exposed. The MMA copolymer is further developed with another chemical, which selectively etches lower molecular weight MMA, but not PMMA. This lead to formation of cavities under PMMA layer as well as overhanging structures of the top resist layer. The cavities reveal the substrate surface and overhanging structures create shadow mask.

During the “grow undercut” operation, the program assumes that exposed PMMA and copoymer are removed during the first stage of development, treating the PMMA as a positive type of resist (see Fig B.1). Thickness of both layers can be defined by user. The “grow undercut” function generates another image with the following color code: white pixels of the substrate have both layers of PMMA and copolymer over them; blue pixels have only the top layer of PMMA over them, with copolymer layer etched; red color appears when there is no resist over the pixel. The red pixels coincide with non-white pixels of the source photoresist

image. The blue pixels' positions are calculated as disks with user-selected radius and with centers at each of non-white pixels of the source image.

The program uses polar coordinate system to set the deposition angles. The azimuth angle φ is counted counterclockwise in the plane of the image. The polar angle θ is counted from the normal to the image plane.

The Fig B.1 shows the program starting conditions before shadow calculation

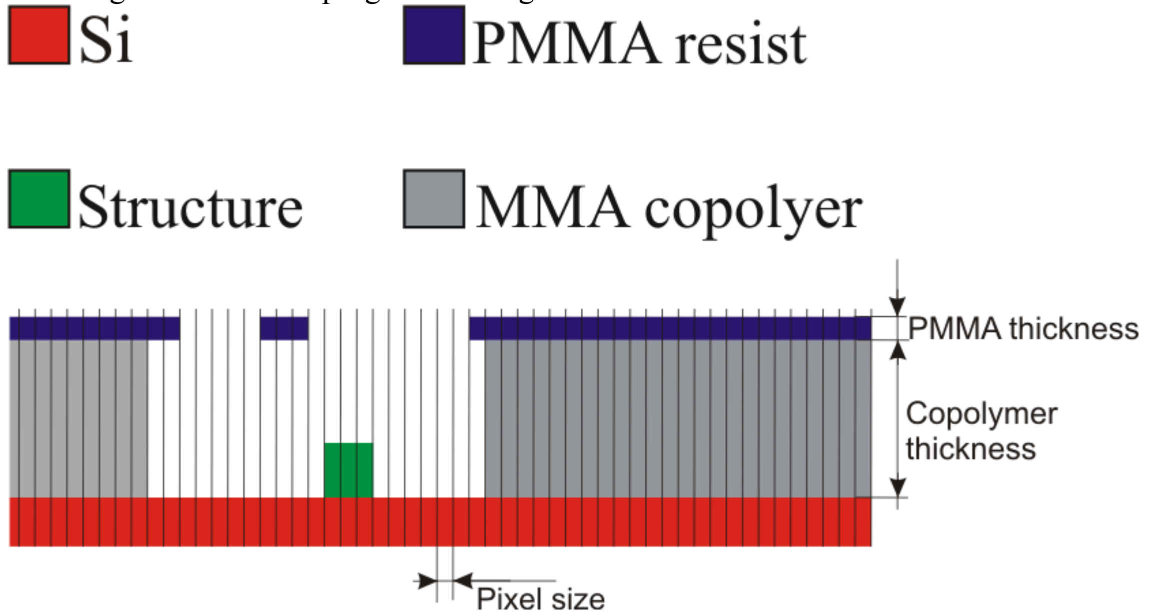

Fig B.1 Initial conditions for simulation.

The main calculation principle of the shadow zones is illustrated on the Fig B.2

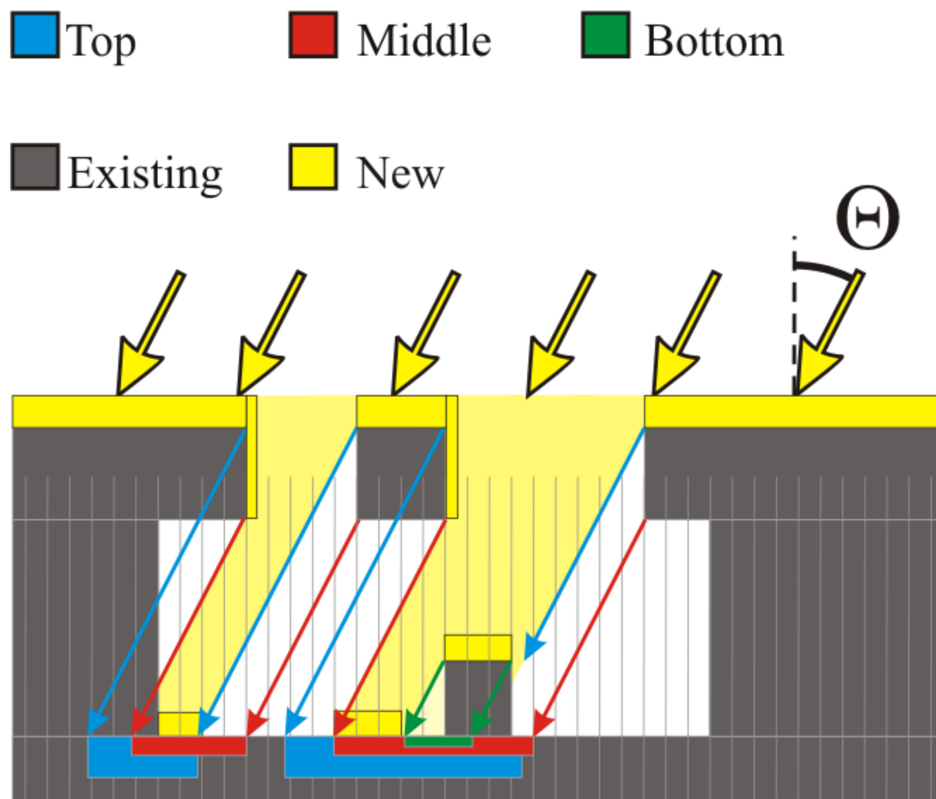

Fig B.2. The main principle of the shadow calculation. Blue bars and arrows show regions allowed by top layer projection, red bars and arrows show regions allowed by middle layer projection.

The calculation goes in following way. The program searches for openings in the top resist layer and projects them on the substrate, taking into account the thickness of both resist layers and deposition angles. The projection algorithm processes every pixel of the image independently of other pixels. Next, the copolymer layer is projected on the substrate. The projected areas are marked as blue and red bars in Fig B.2. The area marked by blue would be covered by deposited material if the top layer was infinitely thin and located at the height of two layers. The area marked with red again would be covered by deposited material if the top layer was infinitely thin and located at the height equal to the copolymer layer thickness. One can see that actual deposition is allowed at the intersections of the two regions, red and blue. However, more rules must be applied to restrict the deposition on the areas that are covered with copolymer. In addition, the algorithm recognizes the existing structures on the substrate and calculates shadows from them.

After the allowed zones for deposition are calculated, the algorithm adds height information to every allowed pixel of the substrate image. The structure height is added as full deposition thickness per simulation round. Although the material grows towards the source in real deposition process, the program can only simulate growth along the normal to the image plane. The added thickness of the deposited material is equal to the user specified thickness multiplied by cosine of the polar angle between the source and the image plane normal.

The program also simulates the growth of the deposited material on the top resist layer, both in upward direction and in plane. This feature helps to simulate the clogging of the shadow mask.

In the case if gradual evaporation assessment is needed, the algorithm can be repeatedly run several times. During this cycle the final structure of the previous iteration is taken as an input for the next iteration.

The resulting output of the program can be saved as a bitmap image. The program can build an arbitrary color map of the resulted image. The height profile along the user-selected section can be constructed as well. The separate program module can visualize the simulation results using 3D graphics with panning, rotating and zooming capabilities.

How to use the program UHVSIM.exe.

In its initial state the program should display **Input** tab sheet. There also should be some numbers in allowed fields. The screenshot of the program with an active Input tab sheet is shown in Fig B.3. The image of photoresist exposure mask is taken as a screenshot from the ELPHY QUANTUM lithography CAD software.

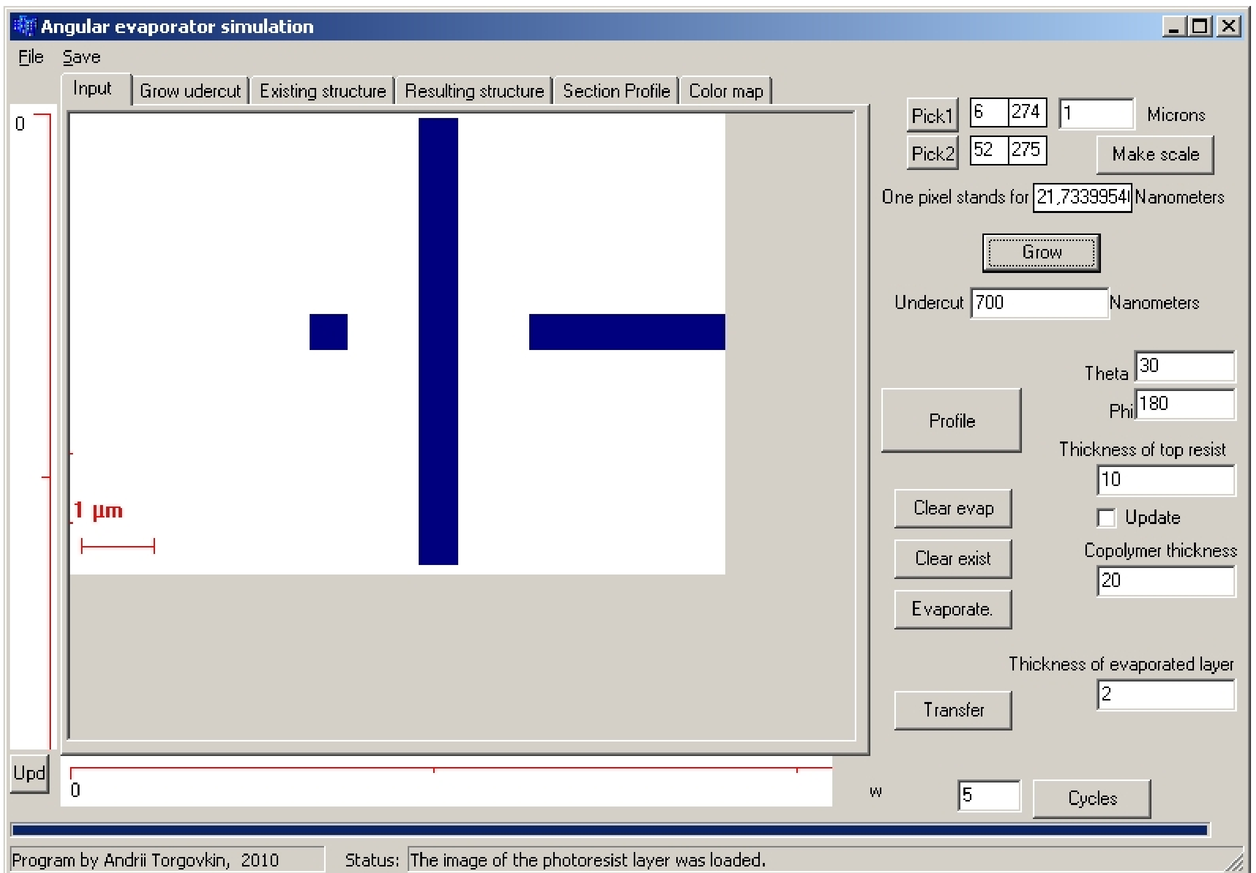

Fig B.3. The screenshot of the **Input** tab.

1) Loading the input photoresist exposure mask.

- Click menu **File** -> **Open photoresist 1** and **Open resist layer picture** dialog will show.
- Choose needed *.BMP (windows bitmap, uncompressed) picture.

This picture should appear in the current tab sheet. Now the working area is made equal to the size of this newly loaded picture.

2) Choosing the right scale is the next step.

- Locate (by your eyes) a scale bar on **Input** image.
- Click **Pick1** speed-button (it must remain in "down" position) and click once to the place where the scale bar begins.
- Now numbers near **Pick1** will change (to some actual coordinates of recently located point) and the button itself will be in "up" state.
- Locate the end of the scale bar with the **Pick2** button.
- The field to the left from the word **Microns** indicates actual length of the scale bar, in micrometers. Input real number there, be careful with "dot, comma and Regional and Language Options".
- Click **Make scale** button. Now some number will appear in the field below button.
- Now one should understand this message **One pixel stands for … Nanometers** literally, as this is the resolution of the simulation. Everything smaller than 1 pixel will not be taken into account at any stage, neither computed nor displayed.

3) Next, introducing undercut in lower resist layer.

- Input a number indicating how much copolymer will be etched into the field to the right from **Undercut** word. The units are nanometers.
- Now program computes the undercut and shows blue progress bar moving at the bottom of the window. When it is 100%, try to switch to the second tab sheet, called **Grow**

undercut. There one can see the lithographic mask that will be further processed. There RED color is for the opening in both layers of resist, and BLUE color shows areas where bottom resist is absent but top layer is present. Red color should appear always at areas where **Input** image is non-white.

- If the undercut is not needed or bottom layer is not modeled at all, **0** nanometers of undercut should be input to the program.

The screenshot of the program window after the "grow undercut" procedure is shown in Fig B.4

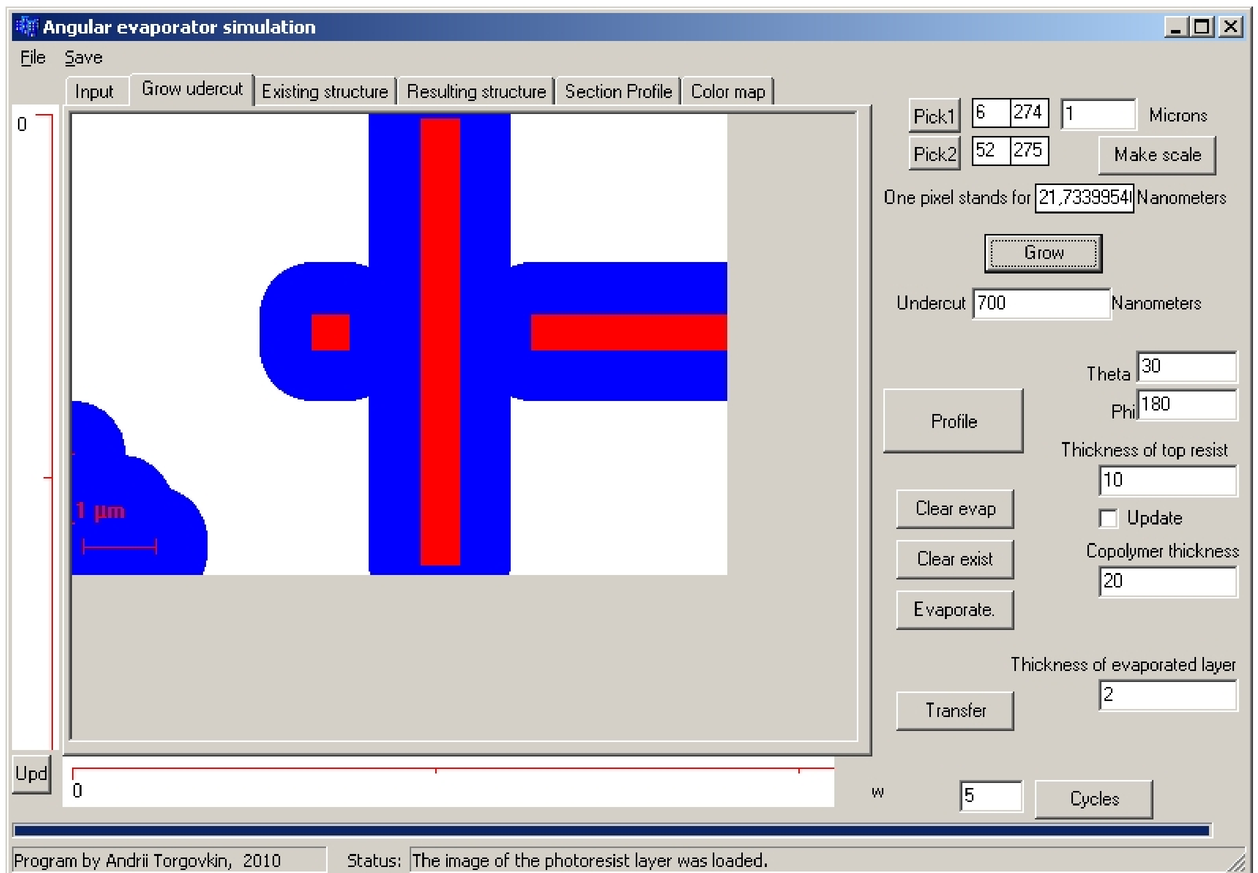

Fig B.4. The screenshot of the **Grow Undercut** tab

4) If nothing was simulated before (program started and only actions 1, 2, 3 were done), click buttons **Clear evap** and **Clear exist**. Now in the tab **Existing structure** one should be able to see black area and in the **Resulting structure** tab – white area. This means that everything is clear.

5) Now input all needed parameters for simulation.

- **Theta** (θ)and **Phi** (φ) are polar and azimuth angles respectively for the ray, showing where the deposited material comes from. The substrate then is considered to lay on X-Y plane. **Phi** is counted from X axis clockwise, **Theta** is counted from Z axis. Values are given in degrees, floating point numbers.
- **Thickness of top resist** is in nanometers, as well as the **Copolymer thickness .**
- **Thickness of evaporated layer** (nanometers) indicates how much material is delivered to the sample as if it was measured by separate sensor in the evaporation chamber. Sensor is considered to be always normal to the beam of the material. The material is put to the sample as "one piece", at once, like if it will be erupted from source and not slowly and gradually deposited.
- The **Update** check-box says whether one should take into account the fact that material is modifying the thickness of the top resist. It is also evaporating on resist's

"vertical" walls, affecting the lithographic mask, if the **Thickness of evaporated layer** multiplied by sine of **Theta** results in more than one pixel size. Modification of the mask will affect further evaporations at other angles. However, **Update** function does not affect current evaporation, only the next ones.

- Try to estimate if **Thickness of evaporated layer** multiplied by cosine of **Theta** is really larger than one. If not – zero thickness will be deposited. Unfortunately, the result is an integer number.

6) Click the **Evaporate.** button. The shadows will be calculated and material deposition will be simulated.

Program will do several steps. During each of them the progress bar will go from 0 to100. Sometimes it may slow down (while casting long shadows). Generally: bigger images will take more time to proceed in overall, more complicated on-chip structures will take more time to calculate shadows.

The **Resulting structure** image will change. This image holds information about "height" of every pixel on it, using non-intuitive color code. This image is not representative, but it is a raw result of simulation and can be saved as *.bmp file. To save this picture click menu **Save->Save result** .

7) In the case when another evaporation (on top of previous result) at different angle should be simulated, click button **Transfer**. The image from **Resulting structure** will be copied to **Existing structure**. Then, during the next simulation, program will take into account the fact that sample surface is not flat and clear, but already contains some structure.

8) Steps 5, 6, 7 may be repeated as many times as needed. In the case that all parameters remain the same and it is just needed to simulate smooth and gradual growth of material, **Cycles** button may be used. The number to the left from the button **Cycles** shows how many times steps 6 and 7 will be repeated automatically. Choose the **Thickness of evaporated layer** to be appropriately small to simulate the growth in small steps, but not too small (see restriction in step 5).

9) On the **Color map** tab sheet the representative result can be obtained. Click **Upd** button to draw a color map of the actual result. The color code is intuitive: zero level is blue, the structure is shown as high contrast, starting from green for lowest heights, passing through yellow and orange colors to red and slightly dark red for highest areas. Scale is automatic, assigning green to 1nm and dark red to maximum height.

The screenshot of the program with the color map of the result is shown in Fig B.5.

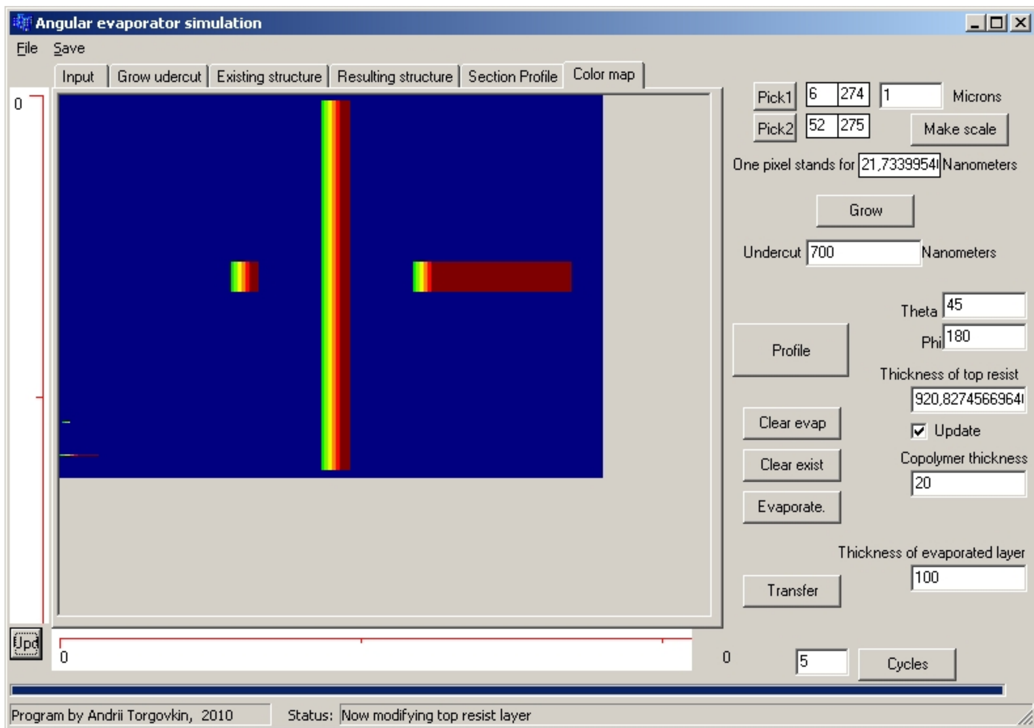

Fig B.5. The screenshot of the program with the color map of the result

10) One can see the cross – section profile of the resulting structure along chosen line

- Click the speed-button **Profile**. It should stay in "down" position and reveal a yellow sign.

- While the button is down, one should find yellow line with start- and end-point markers on the **Resulting structure** image.

- Start and end points of this line are controlled by **Pick1** and **Pick2** buttons. (Only while the **Profile** is down)

- After placing the line, release **Profile** button and watch the result at the Section Profile tab sheet.

The screenshot of the program with the height profile of the result is shown in Figs B.6 – B.7.

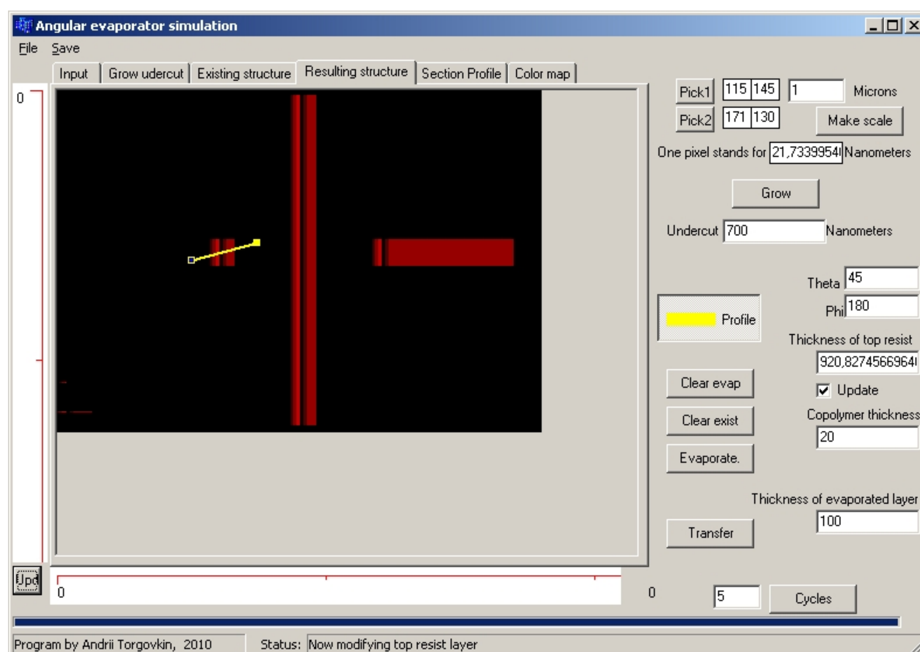

Fig B.6. The screenshot of the program with the cross-section line placement.

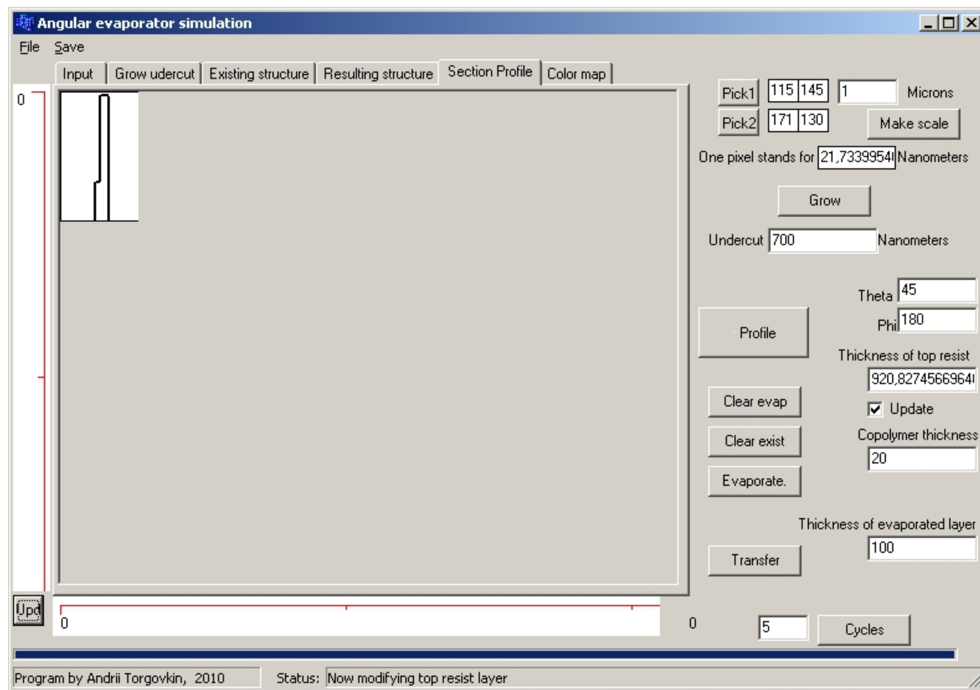

Fig B.7. The screenshot of the program with the height profile along the chosen cross-section line.

The separate program module can visualize the simulation results using 3D graphics. The 3D visualization example is shown in Fig B.8.

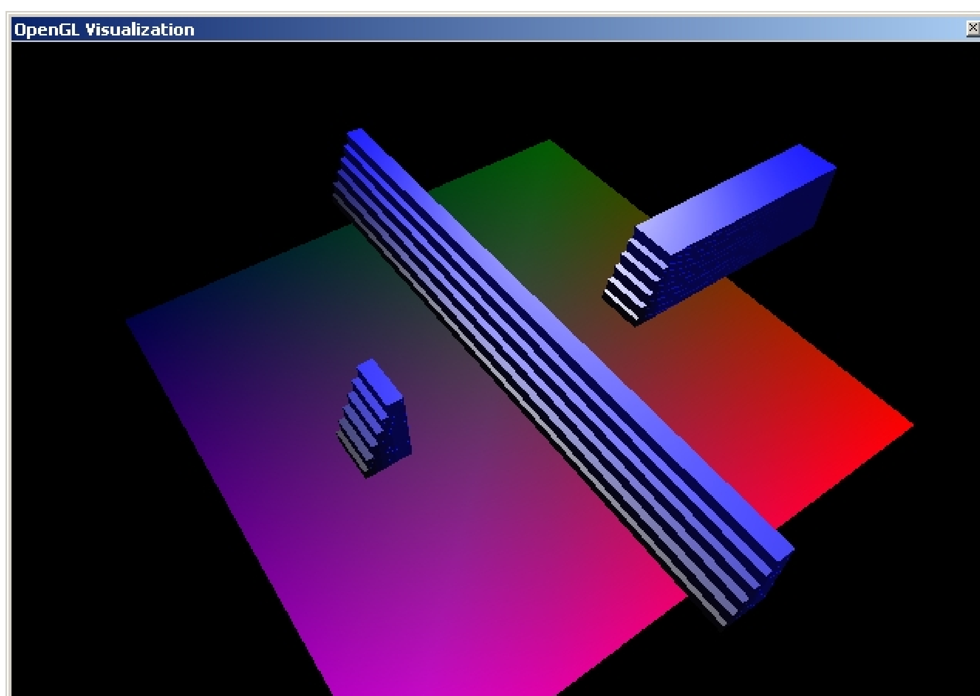

Fig B.8. The screenshot of the program for the 3D visualization.