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ELECTRICAL AND THERMAL TRANSPORT PROPERTIES OF SEMICONDUCTOR AND METAL STRUCTURES AT LOW TEMPERATURE

BY
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Academic Dissertation
for the Degree of
Doctor of Philosophy

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Preface

The work reviewed in this thesis has been carried out during the years 2000-2005 in the Department of Physics at the University of Jyväskylä.

First I would like to thank my supervisors professor Päivi Törmä and Dr. Alexander Savin for the supervision of this work. I would also like to thank professor Jukka Pekola for discussions, Dr. Antti Manninen for hiring me as a graduate student and Dr. Sorin Paraoanu for the collaboration, which resulted as the Chapter 6 in this thesis. I gratefully acknowledge my co-authors whom I thank for a delightful collaboration: Mr. Mika Prunnila, professor Jouni Ahopelto, Mr. Maciej Zgirski, Mr. Ari Halvari and Mr. Mohamed Hassan. Dr. Jussi Toppari is especially acknowledged for the LaTex-support.

The spirit of the Electronics and SoFy groups has been invaluable for the work motivation and therefore I humbly thank each current or former member of these groups for the past five years. In addition I would like to thank all my friends, relatives, 2einsteins-group and Milla for keeping up the positive spirits. Constantem decorat honor.

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Jyväskylä, June 2005

Pasi Kivinen

Abstract

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diss.

This thesis focuses on the electrical and thermal properties of silicon-on-insulator structures at sub-Kelvin temperatures. The heat transport between the electron and phonon systems is governed by the relatively weak electron-phonon coupling and therefore the electron and phonon systems can have different temperatures in the sub-Kelvin region.

A novel method for the electron thermometry is applied for the measurement of the electron temperature in Si. The substantial overheating of the phonon system in the doped silicon film is remarkable and it must be taken into account in the heat conduction analysis.

According to theoretical predictions the electron-phonon thermal conductance is intrinsically dependent on the scattering mechanisms of the conduction electrons and the intervalley scattering determines the electron-phonon energy relaxation. The heat flow between the electron and phonon systems demonstrates a T^6 -dependence, which is in accordance with the predicted theoretical results for many-valley semiconductors (Si). The electron-phonon coupling constant increases as a function of the carrier concentration, which is also in agreement with the developed theoretical model.

Si-based electron refrigerators are studied as a low temperature application for the semiconductor-superconductor junction. The operation principle of the Si-based electron cooler is similar to generally well-known metal-insulator-superconductor -based refrigerators, but Si is in this aspect a superior material for the cooler applications.

Noise characteristics of Nb/Al -based single electron transistors and capacitively coupled Josephson junctions are briefly discussed.

Keywords Silicon, semiconductor-superconductor junction, tunneling, electron -phonon interaction, electron refrigeration, superconductivity

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List of Publications

The main results of this thesis have been reported in the following articles:

A.I SAVIN, A.M., PRUNNILA, M., KIVINEN, P.P., PEKOLA, J.P., AHOPELTO, J., AND MANNINEN, A.J., *Efficient electronic cooling in heavily doped silicon by quasiparticle tunneling*. Appl. Phys. Lett. **79** (2001) 1471 – 1473.

A.II PRUNNILA, M., AHOPELTO, J., SAVIN, A.M., KIVINEN, P.P., PEKOLA, J.P., AND MANNINEN, A.J., *Electron-phonon coupling in degenerate silicon-on-insulator film probed using superconducting Schottky junctions*. Physica E **13** (2002) 773 – 776.

A.III KIVINEN, P., SAVIN, A., ZGIRSKI, M., TÖRMÄ, P., PEKOLA, J., PRUNNILA, M., AND AHOPELTO, J., *Electron-phonon heat transport and electronic thermal conductivity in heavily doped silicon-on-insulator film*. J. Appl. Phys **94** (2003) 3201 – 3205.

A.IV SAVIN, A., PRUNNILA, M., AHOPELTO, J., KIVINEN, P., TÖRMÄ, P., AND PEKOLA, J., *Application of superconductor-semiconductor Schottky barrier for electron cooling*. Physica B **329-333** (2003) 1481 – 1484.

A.V SAVIN, A., PEKOLA, J., PRUNNILA, M., AHOPELTO, J., AND KIVINEN, P., *Electronic Cooling and Hot Electron Effects in Heavily Doped Silicon-on-Insulator Film*. Physica Scripta **T114** (2004) 57 – 60.

A.VI KIVINEN, P., PRUNNILA, M., SAVIN, A., TÖRMÄ, P., PEKOLA, J., AND AHOPELTO, J., *Electron-phonon heat transport in degenerate Si at low temperatures*. Phys. stat. sol. (c) **1** (2004) 2848 – 2851.

A.VII PRUNNILA, M., KIVINEN, P., SAVIN, A., TÖRMÄ, P., AND AHOPELTO, J., *Intervalley Scattering Induced Electron-Phonon Energy Relaxation in Many-Valley Semiconductors at Low Temperatures*. Submitted to Phys. Rev. Lett. Available at cond-mat/0506045.

Author's contribution

The author of this thesis has written the papers A.III and A.VI and participated in writing A.I, A.IV and A.VII. The data analysis was done by the author in A.III, A.VI, A.VII. The data analysis was done partly by the author in A.I and A.V. The author has done all the measurements for A.VI, A.VII and most of the measurements in A.III. The author has actively participated in the measurements for A.I, A.II, A.IV and A.V. The author has also actively participated in the construction of the cryogenic laboratory infrastructure.

Contents

1 Introduction

Silicon is the electronic material *per excellence*, because Si is rather cheap and abundant material and the continuous improvement of Si technology has made it possible to routinely grow today 300 mm single Si crystals at low cost. There are few disadvantages in Si in comparison with other semiconductors, such as the indirect band gap and the lower mobility compared to GaAs, nevertheless the development of the Si technology makes the difference between Si and high mobility semiconductors constantly smaller.

The aims of this thesis is the investigation of the silicon-on-insulator (SOI) structures at sub-Kelvin temperatures. SOI structures consist of a single crystal Si film which is placed on top of amorphous SiO_2, where the thickness of the Si film can be order of 50 nm. The research is mainly focused on the electrical and thermal transport properties. The electron and phonon systems can have different temperatures in the sub-Kelvin region temperature range and the heat transport between them is governed by the electron-phonon interaction. In order to obtain qualitative and quantitative information about the thermal transport properties one must measure the electron (and phonon) temperatures in the Si film.

A novel method is applied for the electron thermometry, which is based on the quasiparticle tunneling through the superconductor - semiconductor (S-Sm) interface. This thermometry, with some limitations, can also be applied for the measurement of the phonon temperature of the Si film in the SOI structure.

S-Sm structures can also be applied for the electron refrigeration analogously to superconductor-insulator-metal (SIN) structures. Moreover, S-Sm-S structures have few advantages compared to traditional SIN -based electron coolers. The efficient operation of S-Sm-S microrefrigerators has been demonstrated in this thesis and the efficiency of the electron coolers was studied as function of the carrier concentration in the Si film. A similar S-Sm-S structure can be also used as a hot electron bolometer for the detection of the cosmic radiation or neutrinos.

Finally, superconducting structures, single electron transistor and capacitively connected Josephson-junctions are studied in brief. The noise properties of Al/Nb -based single electron transistors are measured as a function of the bias voltage. The photon assisted tunneling is considered in a structure, where two Josephson junctions are capacitively coupled together. The interest is focused on creating an on-chip coherent source of radiation and coupling it capacitively to another Josephon junction, which could be interpreted as an excitation of a phase quantum bit.

2 Sample fabrication

2.1 Silicon-on-insulator technology

Silicon is available in a wide variety of sizes, shapes and resistivities. And due to its efficient and cheap production, silicon is today the standard material for the mass production of semiconductor devices. The first major conceptual breakthrough in the development of integrated circuits was the fabrication of multiple transistors on the same Si bulk chip. A hundred million transistors fit nowadays on a chip with the size of a fingernail.

If one wants to increase the transistor density on a Si chip, one will encounter problems related to device isolation, leakage currents, radiation-induced photocurrents, latch-up effects etc. In order to isolate different transistors or other devices from each other one must use reverse biased pn-junctions, wells or interdevice trenches. Also a junction capacitance layer will be formed between the doped area and the substrate, which in turn slows down the speed of the circuit. If semiconducting material is in contact with metal there will be a Schottky junction formed in the interface.

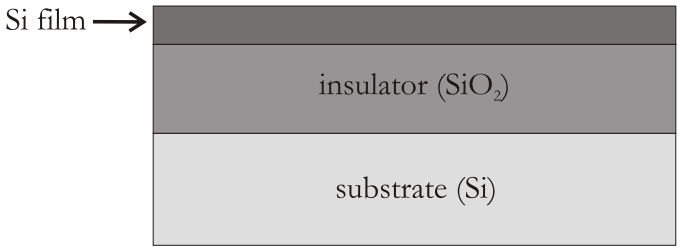

FIGURE 2.1 The layout of the silicon-on-insulator structure. The thickness of the Si film can be between 50 nm and 100 μm and the insulator thickness between 100 nm and 3 μm.

The silicon on insulator (SOI) technology has been originally developed for the fabrication of radiation-hard circuits. The basic concept is to separate the active device from the substrate with a buried oxide (BOX) layer. The Si film is single crystalline but the buried oxide layer is of amorphous SiO_2. This structure, a monolithic

semiconducting film placed on a dielectric insulator, can be very advantageous in many applications. The adjustability of the film thicknesses (both Si and BOX) is a major advantage in terms of an enhanced performance and a superior scalability. The capacitance between the Si film and the substrate is substantially reduced and the leakage currents through the buried oxide layer are negligible. It has been estimated that the complementary metal on semiconductor (CMOS) structures with line width less than 35 nm must be realized by thin-film SOI technology [13, 15]. Minimum-volume metal-on-silicon field effect transistors (MOSFETs), single electron transistors, quantum wires and quantum dots built in SOI pave the transition from the current technology to real nanoelectronics [13].

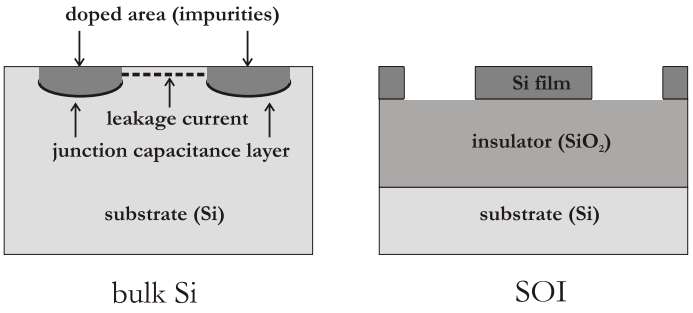

FIGURE 2.2 Schematic illustration of the bulk Si and SOI structures. The major drawbacks of the bulk Si circuit are leakage currents and the junction capacitance, which slows its function. The capacitance between the Si film and the substrate in the SOI circuit is negligible, since the silicon oxide provides an efficient insulation barrier.

SOI wafers have become a very interesting material also for micro-electromechanical systems (MEMS) and for microscale photonics. MEMS applications are based on the superior mechanical properties of SOI, which enable e.g. anisotropic etching and therefore the realization of cantilevers and mirrors. Photonic applications are based on the high refractive index contrast between Si and SiO_2, which permits the photon confinement in small waveguides with sharp bends.

2.2 Fabrication process of SOI wafers

The BOX layer can be thermally grown on the Si substrate and its thickness can be adjusted with a high reliability. Fabricating a single crystalline film on top of BOX is a very demanding task and clearly one cannot use any deposition methods [13]. Therefore SOI structures are fabricated by means of wafer bonding [18, 30]. In this process very flat, mirror-polished and clean surfaces are brought in intimate

contact in ultrahigh vacuum environment. The surfaces will attract each other by van der Waals forces. This bonding is relatively weak compared to the bonding with metallically, covalently, or ionically bonded solids and therefore the wafers must undergo heat treatment to strengthen the bond across the interface.

wafer diameter	100 to 300 mm
Si crystal orietation	<100>
SOI thickness	50 nm to 100 μm
SOI thickness uniformity	$\pm$ 5 nm
BOX thickness	100 nm to 3 μm
BOX thickness uniformity	$\pm$ 10 nm

TABLE 2.1 The characteristics of the Unibond SOI wafers [52].

In this study commercially available Unibond-wafers have been used, which were manufactured by using the SmartCut process. The process is presented in Fig. 2.3 and the wafer characteristics obtained by this process are in Table 2.1. In the SmartCut process the first wafer is implanted by hydrogen ions after an oxidation (the dose is in the range from 3.5×10^{16} to $1.0 \times 10^{17} H^+ cm^{-2}$). This implantation slices the wafer horizontally and enables a high degree of thickness uniformity of the Si film. After the implantation the seed wafer and the handle wafer are carefully cleaned in order to eliminate contamination and to make both surfaces hydrophilic. Wafers are aligned and bonded.

The heat treatment is realized in two steps. During the first phase (400 - 600° C) the bonded wafers split into two parts along the microcavities: to a SOI wafer and to a remainder of the implanted wafer. After the splitting, a high-temperature annealing is performed at 1100°C for 2h to remove any silanol groups from the bonding interface. After the heat treatment the bonding energy is as high as the normal rupture energy of bulk silicon (roughly 2 J/m^2 [37]). Finally the SOI wafer must be polished in order to get rid of the microroughness.

2.3 Sample fabrication

All the SOI samples used in this study have been fabricated at the facilities of VTT Microelectronics (Espoo, Finland). The fabrication process flow is sketched in Fig.2.4. There have been used two similar processes for the sample fabrication.

The samples of the SIN1A-series have been fabricated on a 100 nm thick SOI film (the process A in Fig. 2.4). The wafer was etched in Cl_2/He plasma with photoresist as an etching mask. Si was implanted with phosporous to a dose of 5×10^{14} cm^{-2} at 20 keV. Thereafter it was oxidized in dry ambient at 1000°C and contact windows were opened in buffered hydrofluoric (BHF) acid. After a Standard Clean 1 (SC1, NH_4OH:H_2O_2:H_2O 1:1:5 in megasonic bath at 65°C), deionized water rinse

wafer	N_d (cm^{-3})	d (nm)	ρ_{Si} ($m\Omega \cdot cm$)
SIN1A	$3.5 \cdot 10^{19}$	70	1.04
SIN1F	$6.7 \cdot 10^{19}$	58	0.63
SIN1G	$1.2 \cdot 10^{20}$	58	0.51
SIN1H	$1.6 \cdot 10^{20}$	58	0.44
SIN1L	$2.0 \cdot 10^{19}$	60	2.38

TABLE 2.2 The characteristics of the SOI samples. N_d is the carrier concentration, d is silicon film thickness and ρ_{Si} electrical resistivity.

and a 30 s dip in 2 % HF, a 300 nm thick Al-1% Si layer was sputtered on the wafer. The patterning in this aluminium film (the contacts) was done by using ultraviolet lithography and $BCl_3/Cl_2/CHCl_3/N_2$ plasma etching. The final thickness of the Si film was 70 nm and it had 68 nm of thermal oxide on top of it.

A blanket implantation of phosporous was used for all other wafers (process B in Fig.2.4). After implantation wafer was oxidized in dry ambient at 1000 °C and the sacrificial oxide was stripped in BHF. Cl_2/He plasma was used for etching the mesas and 200 nm thick tetraethylortosilane oxide (TEOS) was deposited at 700°C by a low-pressure chemical vapor deposition. Aluminium was deposited with exactly the same procedure as for the SIN1A wafer. The final thickness of the Si film was 60 nm for the SIN1L wafer and 58 nm for the rest. The thickness of the buried oxide layer was 400 nm in both processes.

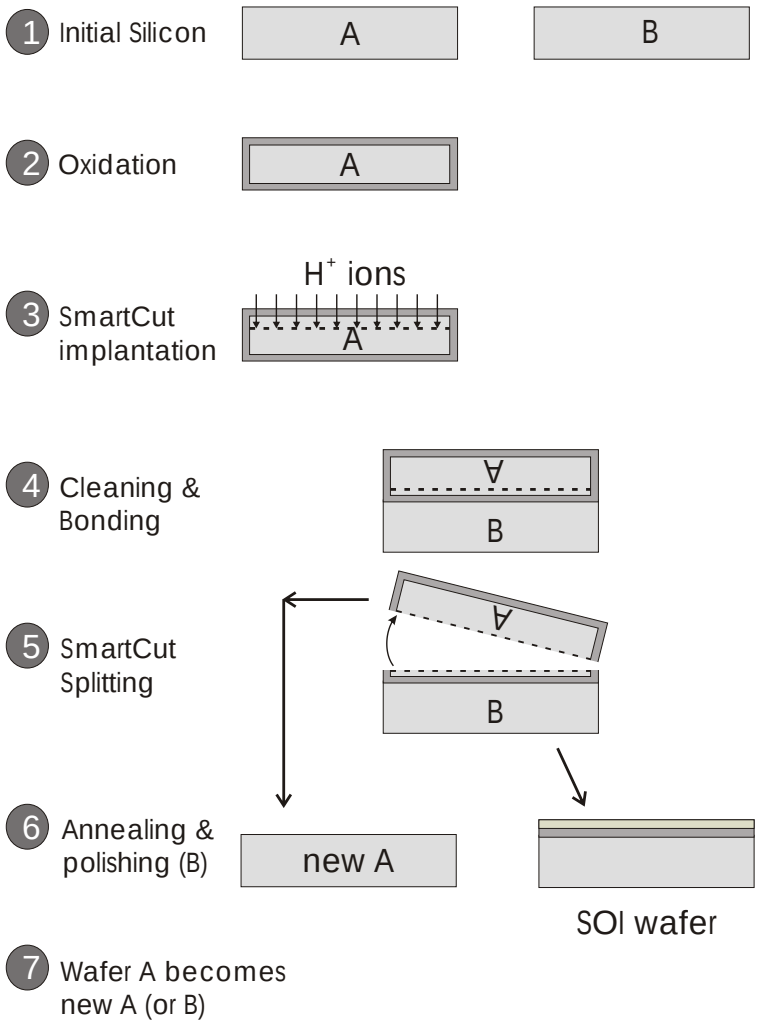

FIGURE 2.3 The Unibond process flow [52]. First one of the wafers (A) is oxidized. Hydrogen implatation (step 3), which produces fine microcavities in the Si lattice, is used as an atomic scalpel. Both wafers are cleaned, polished and bonded together (step 4). After splitting (step 5) the original wafer "A" can be recycled. The SOI wafer is ready for use after annealing and polishing processes (step 6).

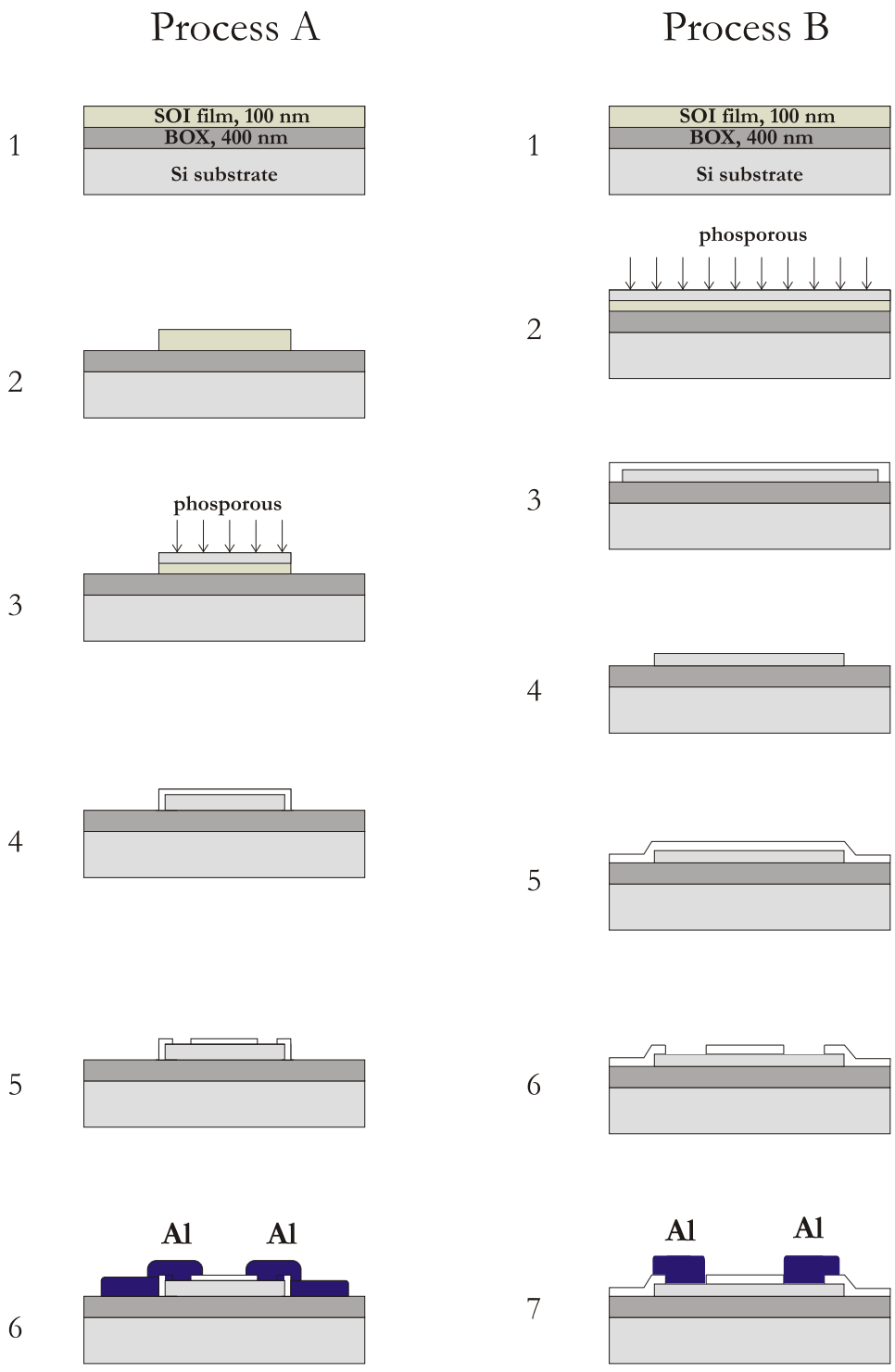

FIGURE 2.4 The sample fabrication processes. Process A: The wafer (1) is first etched (2) and doped (3). After that the wafer is oxidized (4) in dry ambient and the contact windows are opened (5) with buffered hydrofluoric acid. Finally Al is sputtered (6). Process B: The wafer (1) is first doped (2) and oxidized (3) in dry ambient. The Si mesa is etched (4) and after that 200 nm thick tetraethylortosilane oxide is deposited (5). Contact windows (6) and the Al deposition (7) are made similarly as in the Process A.

3 Schottky barrier

3.1 Schottky barrier

The metal-semiconductor contact was discovered in 1874 by F. Braun and 60 years later W. Schottky published the first generally accepted theory describing the contact barrier (for a historical review, see e.g. [46]). In his honor the contact barrier is frequently referred to as the *Schottky barrier*.

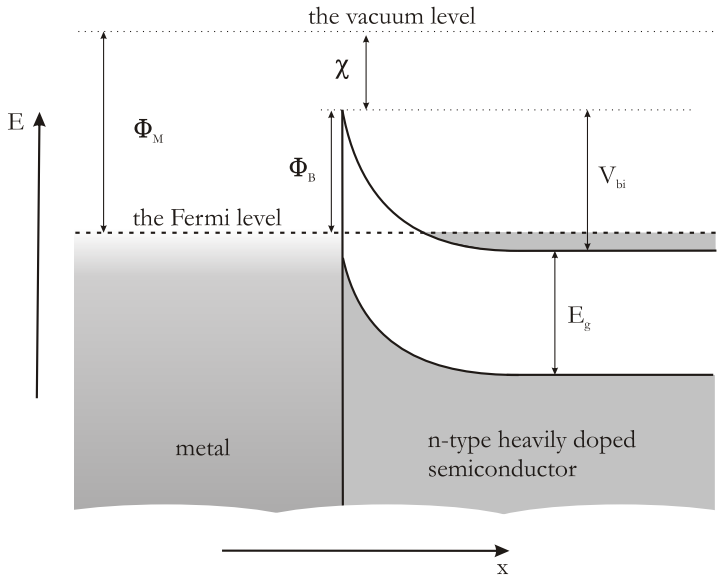

FIGURE 3.1 Schematic illustration of the Schottky barrier. Φ_m is the metal work function, Φ_B the Schottky barrier height, χ the electron affinity, E_g the semiconductor energy gap and V_{bi} is the built-in potential in the semiconductor.

When a metal is placed in intimate contact with a semiconductor, the Fermi levels in the two materials will be coincident due to the thermal equilibrium. The work function Φ_m in metal is defined as the energy difference between the vacuum level and the Fermi level. The electron affinity χ is the energy difference between the bottom of the conduction band and the vacuum level in the semiconductor. A potential barrier, or the Schottky barrier Φ_B, is formed at the metal-semiconductor interface.

Theoretically there are four possible mechanisms for the current transport through the Schottky barrier: thermal excitation, quantum mechanical tunnelling, recombination in the space-charge region (identical to the recombination process in a pn-junction) and the hole injection from the metal (recombination in the neutral region). At low temperature, thermal excitations are negligible and the recombination processes can be neglected in the first order approximation. Therefore the dominating current transport mechanism through the Schottky barrier is the electron tunnelling. Due to a lack of the thermal excitations at sub-Kelvin temperature Si must be doped to a level where it becomes degenerate. The Fermi level resides then above the energy gap in the conduction band and there are carriers also at the lowest temperatures.

The Schottky barrier height depends only on the work functions and not on the doping level [14]. For a detailed analysis one must naturally take into account the image-force-induced lowering of the potential energy (or the *Schottky effect*). Although the Schottky barrier height is unaffected, one can vary the effective Schottky barrier thickness or the quantum mechanical tunneling probability by varying the doping level. One can show [42, 59] that the tunneling current and the tunneling probability have the form

$$J_t \sim T(E) \sim \exp(\frac{-q\Phi_B}{E_{00}}), \tag{3.1}$$

where $q\Phi_B$ is the Schottky barrier height and E_{00} is a characteristic energy defined as

$$E_{00} \equiv \frac{q\hbar}{2}\sqrt{\frac{N_D}{\epsilon_S m^*}}, \tag{3.2}$$

where N_D is the carrier concentration in semiconductor, ϵ_S the dielectic constant of the semiconductor and the m^* is the effective electron mass. In another words, Eq. 3.1 indicates that the tunnelling probability increases exponentially with $\sqrt{N_D}$.

3.2 Contact resistance of the Si/Al interface

Generally the contact resistance is characterized by two quantities: the *contact resistance* (Ω) and the *specific interface resistance* ρ_i ($\Omega \cdot$ cm^2), which is sometimes referred to as the *contact resistivity*, and can be defined as [49]

$$\rho_i = \left.\frac{\partial V}{\partial J}\right|_{V=0} \tag{3.3}$$

where V is voltage and J is the current density. Specific interface resistance is independent of the contact area and therefore can be used for comparison of junctions.

In the *Fowler-Nordheim tunneling*, which is also known as the field emission (see e.g. [43]), electrons tunnel through a barrier in the presence of a high electric field.

The specific interface resistance in this case is [49, 64]

$$\rho_i = C(N_D, T, \Phi_B)\rho_1 \exp\left(\frac{q\Phi_B}{E_{00}}\right) \tag{3.4}$$

where C is a function of the carrier concentration N_D, temperature and the Schottky barrier height Φ_B. ρ_1 is a material-dependent parameter characterizing the residual resistivity and E_{00} is a characteristic energy defined in Eg. 3.2. With these equations, one can show that [49, 64]

$$\rho_i \sim exp\left(\frac{\Phi_B}{\sqrt{N_D}\coth\frac{E_{00}}{kT}}\right) \tag{3.5}$$

or

$$\ln\rho_i \sim 1/\sqrt{N_D} \tag{3.6}$$

In other words, the specific interface resistance is very sensitive to the semiconductor doping level. The contact interface resistance is plotted in Fig. 3.2 as a function of the carrier concentration of four different wafers (SIN1A, SIN1F, SIN1G and SIN1H). The dependence is in agreement with Eq. 3.6.

In contrast to the metal-insulator-metal structures, where controlling of the insulator layer thickness is very hard or impossible, one can vary the Schottky barrier thickness (or the contact resistance) in very wide range by varying the doping level. Another superior advantage of the Schottky barrier is the lack of the pinhole effect, which often restricts the use of metal-insulator-metal structures.

3.3 Semiconductor-superconductor contact

The superconductor - semiconductor (S-Sm) contact is analogous to the superconductor - insulator - normal metal (SIN) tunnel junction (see e.g. [53] p. 32), where an insulator instead of the Schottky barrier separates the superconductor and the normal metal. The main current transport mechanism in the S-Sm contact is the quasiparticle tunnelling, although other mechanisms exist (e.g. pair-quasiparticle conversion [27]) but we do not discuss them here.

A schematic illustration of the quasiparticle tunneling is presented in Fig. 3.3. A voltage V is applied over the superconductor - semiconductor - superconductor structure. The quasiparticles below the energy gap in the right-side superconductor are energetically on the same level as the Fermi level in the semiconductor and this enables the Fowler-Nordheim tunneling of the quasiparticles from right to left. Similarly the superconductor on the left side has vacancies above the forbidden energy gap and quasiparticles can tunnel from the semiconductor to the left superconductor. Similarly to SIN-structures [53], the dynamic conductance of the S-Sm-S structure is dependent on the semiconductor electron temperature.

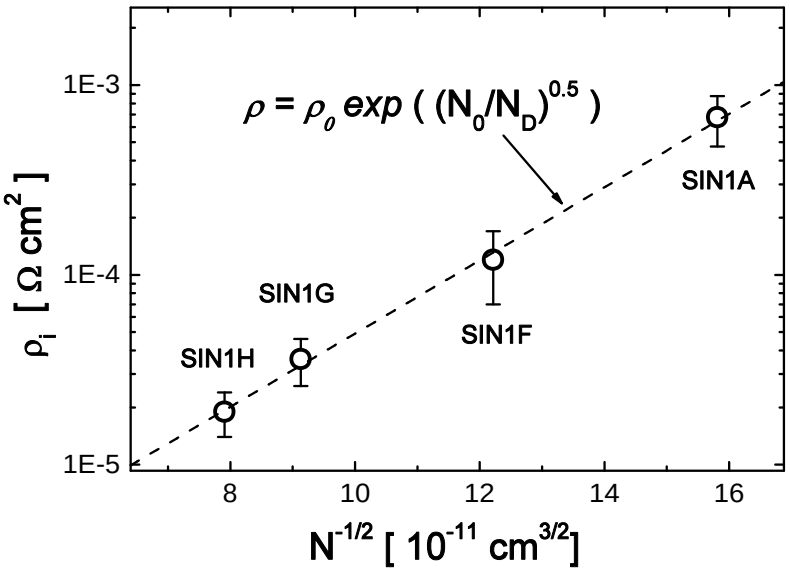

FIGURE 3.2 The specific interface resistance as a function of the carrier concentration [4]. The dashed line corresponds to the equation $\rho = \rho_0 \exp((N_0/N_D)^{1/2})$. The parameters obtained from the fitting are $\rho_0 = 5.8 \cdot 10^{-7} \Omega \cdot cm^2$ and $N_0 = 1.97 \cdot 10^{21} cm^3$.

3.4 Electron thermometry

Measuring the electron temperature by using a superconductor-insulator-normal metal (SIN) structure has been used in several applications (see e.g. [41]). Analogously one can apply the S-Sm-S structure for the electron thermometry [1]. In the first order approximation the current through the structure, where both superconductors are at different temperatures, is dependent only on the electron temperature of the semiconductor. One can show [41, 53] that the tunnelling current is

$$I = \frac{\sqrt{2\pi\Delta k_B T}}{2eR_n} \exp\left(-\frac{\Delta - eV}{k_B T}\right) \tag{3.7}$$

where R_n is the normal state resistance of the junction(s), Δ is the energy gap of the superconducting electrode and V is the applied voltage over the structure. If the structure is biased with a constant current the theoretical temperature sensitivity for the thermometry will be [41]

$$\frac{dV}{dT} = -\frac{k_B}{e}\frac{\Delta - eV}{k_B T} \tag{3.8}$$

In Fig. 3.4 is a micrograph of two S-Sm-S structures, which can be utilized for the electron thermometry. One applies a measurement current bias across the Si mesa, which in turn is heated up by the heating current. As the current bias is several

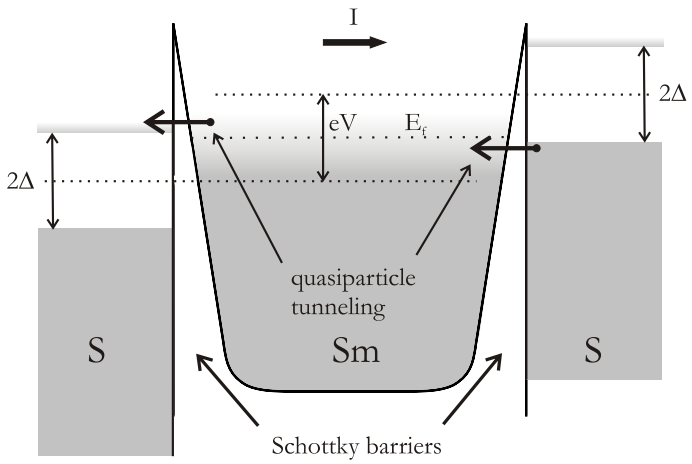

FIGURE 3.3 Schematic illustration of the quasiparticle tunneling. If the superconductors surrounding the semiconductor are properly biased the quasiparticles can tunnel through the Schottky barrier. The tunneling current is dependent on the semiconductor electron temperature.

orders of magnitude smaller than the heating current, to a very good approximation it does not heat the electron gas. If the junction is current biased (the measurement current has a constant value), one directly obtains the Si mesa electron temperature from the voltage over S-Sm-S structure.

In Fig. 3.5a are current-voltage (IV) curves for the S-Sm-S structure in the SIN1A-wafer. The IV curves have been measured at different temperatures between 160 and 490 mK and they have a strong temperature dependence . The setup for the electron temperature measurement is in the inset in Fig. 3.5a. The S-Sm-S structure is biased with a constant current (horizontal line in Fig. 3.5a) and in Fig. 3.5b is the correspondence between the measured voltage over S-Sm-S and the temperature. The temperature value is from a calibrated RuO-resistor.

In order to apply this electron thermometry at low temperature proper low-pass filtering and noise isolation are very important (see Fig. 3.6). The measurement setup is similar as in Fig. 3.5, but without a proper filtering in the measurement lines. RF-signals are induced in the measurement lines and they eventually heat up the electron gas. Due to a finite electron-phonon coupling, the electrons in the Si mesa can attain an independent temperature due to RF-noise heating regardless of the substrate (phonon) temperature.

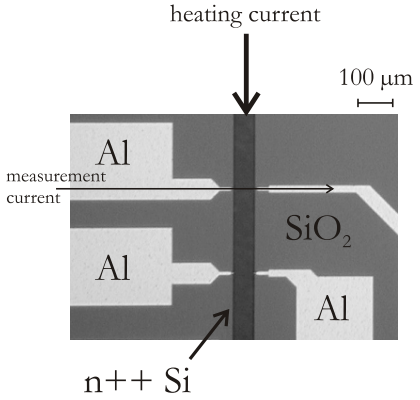

FIGURE 3.4 Micrograph of the sample used for the electron-phonon coupling measurement. The measurement current is negligible in comparison with the heating current. Superconducting contacts (Al) on top of the Si mesa form the Schottky contacts. Al contacts are connected to bonding pads (three of four are on this graph). Two thermometer structures are separated by 250 μm.

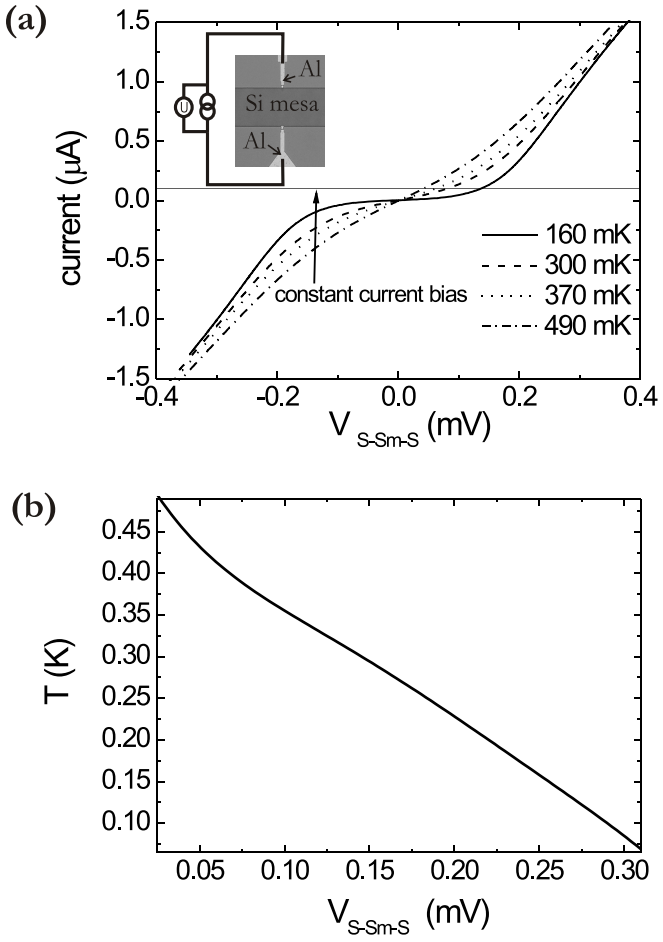

FIGURE 3.5 (a) The I-V characteristics of the S-Sm-S structure at different cryostate temperatures. For clarity only 4 different temperature values have been inserted. Inset: the schematics of the constant current bias setup. The structure is similar to Fig. 3.4. (b) The temperature calibration curve. In the x-axis is the voltage over the S-Sm-S structure at a constant current bias and in the y-axis is the corresponding temperature.

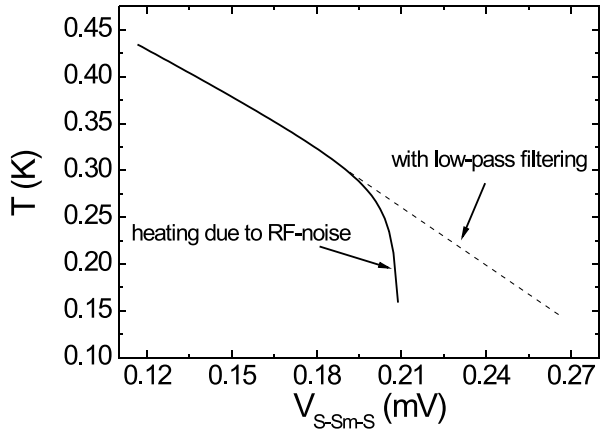

FIGURE 3.6 Measurement setup as in Fig.3.5 but without a proper low-pass filtering. The RF-noise induced in the measurement lines will heat up the electron gas and limit the thermometry temperature scale to 300 mK. The dotted line is a guide to the eye.

4 Thermal transport in SOI films at sub-Kelvin temperature

4.1 Introduction

The thermal transport is strongly degraded in the silicon-on-insulator structures at sub-Kelvin temperature. The electrons in the Si film can have a temperature which differs from the substrate or the phonon temperature due to a weak electron-phonon coupling. It is very crucial to take into account these effects in designing devices working at sub-Kelvin temperature. An uncontrollable overheating can prevent or destroy the function of a SOI based device.

Two aspects of the thermal transport have been studied: the heat conductance between the electron and phonon systems (the eletron-phonon coupling) and the electron thermal conductance along the Si mesa.

4.2 Electron-phonon coupling

4.2.1 Theoretical background

The electron-phonon thermal conductance determines the heat flow between the electron system and the lattice (phonons). This thermal conductance has a strong temperature dependence and at sub-Kelvin temperature it becomes comparatively weak. Depending on the application this can be an advantage or a disadvantage: an advantage in the case when one wants to thermally isolate the electrons from the lattice. This is a disadvantage if one wants to electrically measure the lattice temperature (low temperature thermometry).

Clean and dirty limits

The electron-phonon interaction has qualitatively different temperature dependencies depending on the intrinsic properties of the material. In pure metals the electron-phonon relaxation time τ_{e-ph} is inversely proportional to the number of thermal phonons and therefore $\tau_{e-ph}^{-1} \propto T^3$ for three dimensional (3D) phonons. This dependence is theoretically and experimentally well established (see e.g. [47] or [45]).

The situation gets more complicated if the material is disordered, or the phonon dimensionality differs from 3D. In some materials, such as in $Ti_{1-x}Al_x$ [34] or in Au film on quartz substrate [10], a weaker temperature dependence of τ_{e-ph}^{-1} has been reported ($\tau_{e-ph}^{-1} \propto T^2$). On the other hand in Hf, Ti [20], Bi [28] or Cu [25] the relaxation time demonstrates a stronger dependence on temperature ($\tau_{e-ph}^{-1} \propto T^4$).

In a disordered material the electron scattering from impurities and boundaries significantly changes the single-particle picture of the electron-phonon interaction. Two scattering processes should be taken into account: the "pure" electron-phonon scattering and the inelastic scattering from impurities such as defects or boundaries. Depending on the product of the thermal wave vector q_T and the electron mean free path l_e one can consider two cases for the electron-phonon interaction: the *clean* ($q_T l_e \gg 1$) and the *dirty* ($q_T l_e \ll 1$) limit.

Phenomenologically this means that in the dirty limit electrons scatter mostly from impurities or from defects. In the clean limit the dominating scattering is from phonons and the scattering from impurities or defects do not play a significant role. If in the dirty limit the scattering centers are static then $\tau_{e-ph}^{-1} \propto T^2$ is expected [51]. If the impurities are fully vibrating with the lattice the relaxation rate is proportional to T^4: $\tau_{e-ph}^{-1} \propto T^4 l_e$ [51].

At low temperature electrons have a well-defined temperature. Usually the electron-electron interaction time (τ_{e-e}) is supposed to be significantly smaller than the electron-phonon interaction time (τ_{e-ph}) and in this case the heat flow from electrons to phonons can be described by a model [62], where electrons have the heat capacity $C_e = \gamma T_e$ and the change of the electron temperature is determined by $dP = \tau_{e-ph}^{-1} C_e dT_e$. By substituting $\tau_{e-ph}^{-1} = \alpha T^p$, one obtains

$$P = \Omega\Sigma(T_e^{p+4} - T_{ph}^{p+4}), \tag{4.1}$$

where P is the heat flow from electrons to phonons, Σ is a material-dependent constant characterizing the electron phonon coupling ($\Sigma = \alpha\gamma/(p+2)$), Ω is the volume and T_e and T_{ph} are the electron and the phonon temperatures.

This theoretical analysis has been made for metals, or materials with a spherical Fermi surface, where the free electron model can be applied. The important question is if these results can be directly applied to heavily doped Si [2, 3, 6, 50]. A more correct way for the consideration of the electron-phonon interaction in Si is to take the intervalley scattering process into account [7].

Intervalley scattering

The Fermi surface in Si is six-fold degenerate and the intervalley scattering (see Fig. 4.1) is generally a more important process than the intravalley scattering in relaxing the momentum and energy of the conducting electrons (Ref. [65] p. 215).

The electron-phonon interaction can be considered due to the deformation potential coupling where the intervalley processes are taken into account. In the many-

valley semiconductors acoustic waves are strongly attenuated when the strain associated with them destroys the equivalence of the valleys.

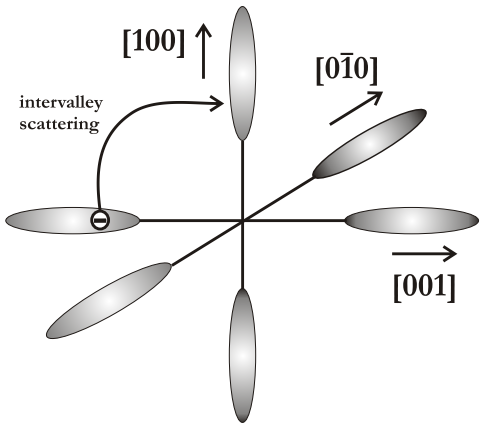

FIGURE 4.1 The principle of the intervalley scattering. The Fermi surface of Si is sixfold degenerate and the intervalley scattering between minima in Si is generally more important than the intraband processes when it comes to relaxing the momentum or the energy of the electrons (Ref. [65] p. 215).

The heat flow from electrons to phonons can be written [7]

$$P = -\sum_{\lambda} \int d\vec{q} \frac{1}{(2\pi)^d} \hbar\omega_{q\lambda} \frac{\partial N(\hbar\omega_{\vec{q}\lambda})}{\partial t}, \tag{4.2}$$

where $N(\hbar\omega_{\vec{q}\lambda})$ is the phonon energy distribution function, $\hbar\omega_{\vec{q}\lambda}$ is the phonon energy, $\vec{q}$ is the phonon wave vector, d is the dimensionality of the phonons and λ includes all the possible phonon modes [21]. The magnitude of $\vec{q}$ depends on the direction, but after the integration this directional dependence results only as a scalar constant. One can use the approximation [44]

$$\frac{\partial N(\hbar\omega_{\vec{q}\lambda})}{\partial t} \approx \frac{N_{T_e}(\hbar\omega_{\vec{q}\lambda}) - N_{T_{ph}}(\hbar\omega_{\vec{q}\lambda})}{\tau_{ph-e,\vec{q}\lambda}}, \tag{4.3}$$

where T_e and T_{ph} correspond to temperature of the electron and phonon systems, respectively. $\tau_{ph-e,\vec{q}\lambda}$ characterizes the electron-phonon energy relaxation.

The relaxation time $\tau_{ph-e,\vec{q}\lambda}$ can be also written as [57]

$$\frac{1}{\tau_{ph-e,\vec{q}\lambda}} = v_{\hat{u}_{\vec{q}}} \alpha_{\vec{q}\lambda} \propto v_{\hat{u}_{\vec{q}}} \omega_{\vec{q}\lambda}^{\nu} \propto v_{\hat{u}_{\vec{q}}}^{\nu+1} q^{\nu} \tag{4.4}$$

where v is the velocity of sound, $\hat{u}_{\vec{q}}$ is a unit vector into $\vec{q}$-direction and α is the ultrasonic attenuation coefficient. By substituting Eqs. (4.3) and (4.4) into Eq. (4.2) and calculating the integral one obtains (compare with Eq. 4.1)

$$P = \Omega\Sigma(T_e^{\nu+4} - T_{ph}^{\nu+4}), \tag{4.5}$$

where Ω is the volume of the sample, T_e is the electron temperature, T_{ph} the phonon temperature and Σ is a parameter which characterizes the magnitude of the thermal coupling between the electron and phonon systems. $\Sigma \propto \tau_{iv} N^{1/3}$, where τ_{iv} is the intervalley scattering relaxation time and N is the carrier concentration.

Sota et al. [54] have theoretically investigated the ultrasonic attenuation in many-valley semiconductors and according to their analysis the ultrasonic attenuation coefficient $\alpha \propto \tau_{iv} N^{1/3} \omega^2$, or in another words, $\nu = 2$. It is therefore expected that the heat flow between the electron gas and the phonon system in Si should have a T^6-dependence.

In the discussion above it is assumed that the phonons in the Si film are three dimensional (3D). This is not necessarily always the case. The acoustic coupling between the Si film and the buried oxide layer (BOX), which is beneath the Si film, determines the phonon dimensionality in the Si film [21]. Another interface where the phonons can be backscattered is the boundary between the Si chip and the cryostat sample holder (Cu). If this interface dominates the phonon reflection the phonon temperature should be to a some degree dependent on the Si chip - Cu contact and therefore the phonon dimensionality in the Si film were effectively 3D.

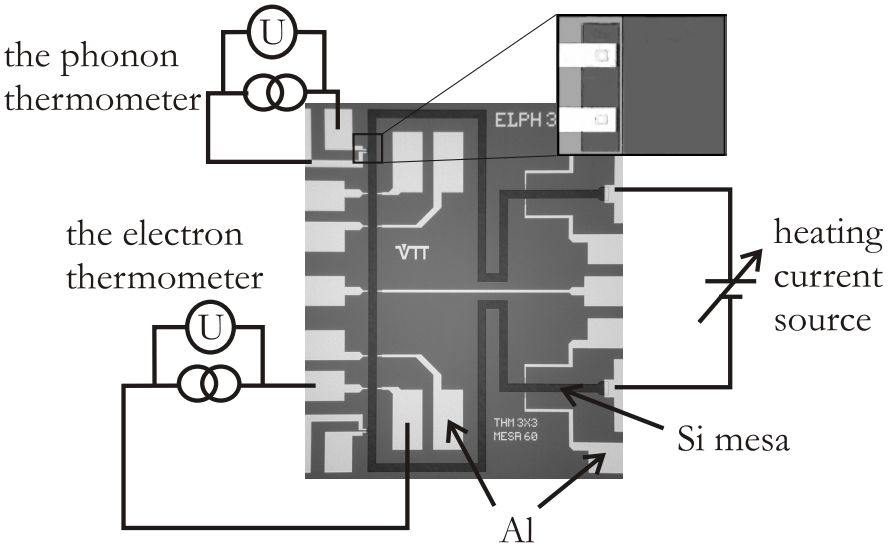

FIGURE 4.2 The sample geometry used in the electron-phonon coupling measurements. The Si mesa line width is 60 μm. The electron and phonon temperatures are measured with S-Sm-S structures. Inset: the electrically isolated phonon thermometer is 1 μm away from the Si mesa.

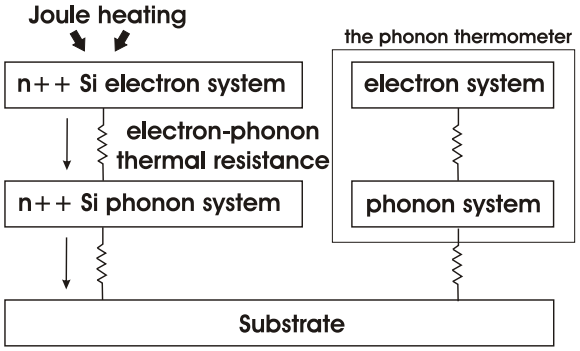

FIGURE 4.3 The heat flow in the sample.

4.2.2 Experimental

The sample geometry and schematics of the measurement setup are depicted in Fig. 4.2 and the heat flow process in Fig. 4.3. The samples were mounted on a Cu sample holder of the dilution refrigerator with GE varnish[1] and the measurements were carried out at bath temperatures between 100 and 400 mK. The electron and phonon temperatures were simultaneously measured by utilizing the superconductor - semiconductor - semiconductor (S-Sm-S) thermometry [1] while the electron gas in the Si film was heated with a DC current. The phonon thermometer is isolated from the main Si mesa by a 1 μm gap and it measures the overheating of the phonon system.

The phonon thermometry is rather complicated task due to possible internal phonon reflections in the sample (see Fig. 4.4). The phonons are emitted from the n++ Si mesa and can be reflected from the SiO_2/Si (substrate) interface or from the Si / Cu interface. It is also possible that the phonons form a 2D system in the SiO_2 layer.

4.2.3 Results and Analysis

The electron-phonon thermal conductance measurements in SOI films have been carried out at substrate temperatures between 100 and 500 mK. The heating current was swept slowly and the electron and phonon temperatures were simultaneously measured. The results of the measurements of the electron and phonon temperatures as a function of the heating power are presented in Fig. 4.5. At power density of $6.0 \cdot 10^5 W/m^3$ the electron temperature is more than 1.5 times higher than the substrate temperature (T_e = 390 mK, T_{subst} = 250 mK). At the same power density $6.0 \cdot 10^5 W/m^3$ the local phonon temperature is about 360 mK.

[1] GE C5-101 (available from Oxford Instruments plc)

wafer	N_d (cm^{-3})	$R_{sq}@1.5K$ (Ω)	d (nm)	ρ_{Si} ($m\Omega \cdot cm$)	Σ (W/m^{3}K^6)
SIN1A	$3.5 \cdot 10^{19}$	148	70	1.04	$2.2 \cdot 10^8$
SIN1F	$6.7 \cdot 10^{19}$	109	58	0.63	$3.1 \cdot 10^8$
SIN1G	$1.2 \cdot 10^{20}$	88	58	0.51	$4.6 \cdot 10^8$
SIN1H	$1.6 \cdot 10^{20}$	77	58	0.44	$6.7 \cdot 10^8$

TABLE 4.1 The characteristics of the samples. N_d is the carrier concentration, which is obtained from the room temperature resistivity, $R_{sq}@1.5K$ is the square resistance at 1.5K, d is silicon film thickness and ρ_{Si} electrical resistivity and Σ is the electron-phonon thermal conductance (see also Eq. (4.5)).

For a correct electron-phonon heat conductance analysis the measured phonon temperature must be taken into account. The situation is illustrated in Fig. 4.6a where the electron, phonon and the substrate temperatures are measured in a sample of the SIN1F wafer. If one applies $T_{ph} = T_{subst}$ the qualitative result for the electron-phonon heat conductance will be (incorrectly) $T_e^5 - T_{ph}^5$ (Fig. 4.6b, dash line) [2]. However, T_{ph} does not remain at substrate temperature and as the measured T_{ph} is taken into account one obtains the correct result $T_e^6 - T_{ph}^6$ (the solid line in Fig. 4.6b).

Originally there were five wafers with different carrier concentrations. One of them (SIN1L), which also had the lowest carrier concentration $N_d = 2.0 \cdot 10^{19} cm^{-3}$, was excluded from the analysis. The electron-phonon thermal conductance in SIN1L was proportional to $T_e^6 - T_{ph}^6$, but the magnitude of the thermal conductance constant (electron-phonon coupling) Σ varied more than 20 % between the samples.

The heating power density is plotted against $T_e^6 - T_{ph}^6$ for SIN1A, SIN1F, SIN1G and SIN1H wafers in Fig. 4.7. Measurements for every wafer were carried out similarly as illustrated in Fig. 4.5. All the measured wafers had the qualitatively similar electron-phonon thermal conductance characteristics, i.e. the electron-phonon heat flow is proportional to $T_e^6 - T_{ph}^6$. The fitting value of the slope in Fig. 4.5 corresponds to Σ in Eq. (4.5).

The values of Σ are plotted as a function of N_d in Fig. 4.8. Electron-phonon coupling constants are presented in Table 4.1 with other electrical parameters. The heat conductance (Σ) increases with the carrier concentration. As the carrier concentration level increases roughly four times, Σ increases three times from $3.5 \times 10^8 W/m^3K^6$ to $6.7 \times 10^8 W/m^3K^6$. The dash line in Fig. 4.8 is a fit of experimental data. Its value, $(4.4 \pm 0.3) \cdot 10^{-12} \frac{W cm^3}{m^3 K^6}$, predicts that at a doping level corresponding to the carrier concentration in normal metals ($10^{22} cm^{-3}$) the corresponding value for Σ would be two orders of magnitude higher such as in Cu [25].

4.3 Electron thermal conductivity

4.3.1 The Wiedemann-Franz law

According to the empirical Wiedemann-Franz law [63], the ratio of thermal and electrical conductivities is proportional to temperature:

$$\frac{\kappa}{\sigma} = LT \tag{4.6}$$

where κ is the thermal, σ the electrical conductance, L is the Lorenz number and T is the temperature. One can show (see e.g. [23] p.216) by using the Fermi-Dirac statistics that the theoretical value for the Lorenz number is

$$L_0 = \frac{\pi^2}{3}\frac{(k_B)^2}{e^2} = 2.44 \cdot 10^{-8} W/K^2 \tag{4.7}$$

where k_B is the Boltzmann's constant and e is the electron charge. L_0 is sometimes called the Sommerfeld value of the Lorenz number. The Lorenz number approaches its theoretical value L_0 when the electron gas is highly degenerate and the electron mean free path l_e is equal for electrical and thermal conductivities.

Generally the Wiedemann-Franz law is valid for degenerate semiconductors at low temperature [29, 26]. Syme et al. [58] have investigated the electronic thermal conductivity in a two-dimensional electron gas in n-channel MOSFETs at low temperature (1-10K) and the obtained temperature dependence of the electronic thermal conductivity was in agreement with the Wiedemann-Franz law. The possible deviation from the theoretical value L_0 could have several origins. The impurities, the presence of magnons and the phonon contribution to the thermal conductivity affect the value of the Lorenz number.

The results of our electron-phonon heat transport measurements in SOI films allow the electronic thermal conductivity from the non-uniform heating experiments to be estimated. The previously obtained data concerning the electron-phonon interaction can be used for calculation of the electronic thermal conductivity in thermal transport.

4.3.2 Thermal conductance

In a steady state the heat flow in the electron system can be determined by the thermal conductivity along the Si film and by the energy flow rate between electrons and phonons [58]

$$\frac{d}{dx}\left(\kappa(T) \cdot \frac{dT}{dx}\right) = w_{ep}(T) \tag{4.8}$$

where $\kappa(T)$ is the electron thermal conductivity and w_{ep} is power density P_{e-ph}/Ω, i.e. heat flow between electron and phonon systems per unit volume.

If one assumes validity of the Wiedemann-Franz law, the electron thermal conductivity can be presented in the form

$$\kappa = L\sigma T \tag{4.9}$$

where σ is the electrical conductivity. Taking into account the linear temperature dependence of electron thermal conductivity, equation 4.8 can be presented in the form

$$T \cdot \frac{dT}{dx} = -\sqrt{\int_{T_{bath}}^{T} 2 \cdot (\sigma \cdot L)^{-1} \cdot w_{ep}(u) \cdot u \cdot du} = -\sqrt{\frac{2}{\sigma \cdot L}} \cdot [I_1(T)]^{1/2} \tag{4.10}$$

This applies for an arbitrary geometry. In the case of a long Si bar, which is heated at one end, the boundary conditions must be taken into account. For a very long sample, where the other end remains at substrate temperature, one obtains

$$(x_2 - x_1) \cdot \sqrt{\frac{2}{\sigma \cdot L}} = \int_{T_2}^{T_1} \frac{T \cdot dT}{[I_1(T)]^{1/2}} = I_2(T_1, T_2) \tag{4.11}$$

where $(x_2 - x_1)$ is the distance between two points along the bar and T_1 and T_2 are the corresponding electron temperatures.

4.3.3 Heat conductance in a silicon bar

The integral I_2 on the right side in Eq.4.11 depends only on the distance between two points along the bar. For the two fixed points x_1 and x_2 the value of the integral is constant in the whole range of the power applied to the system. In fact this is valid only for very long samples (it is assumed that the other end of the sample is at the substrate temperature) and for a moderate energy flow.

The sample geometry used for the thermal conductance measurement is depicted in Fig. 4.9. The silicon bar was 30 μm wide and S-Sm-S thermometers T_1 and T_2 were placed 40 μm apart. To obtain the temperature profile along a film one usually measures the electron temperature in several points along the line. In this experiment only two S-Sm-S thermometers were usually used for measuring the temperature gradient along the sample, and the thermometer at the "cold" end of the sample was used for the control of its overheating in respect to the bath temperature.

The heating current was slowly swept and the electron temperature in two points along the bar (T_1 and T_2) was recorded. If the Si bar is sufficiently long (the

cold end at the bath temperature), then the temperature T_2 is determined only by temperature T_1. In other words if T_1 is the electron temperature at 0 μm and T_2 at 40 μm and later T_1' at 0 μm and T_2' at 40 μm, where $T_1' > T_1$ and $T_2' = T_1$, it follows that the temperature at 80 μm must be T_2.

The calculated temperature decay along the bar (solid line) and the measured electron temperature values (circles) are plotted in Fig. 4.9(b). The only fitting parameter is the Lorenz number L, which is $2.45 \cdot 10{-}8 W \Omega K^{-2}$. The result of the fitting may be considered as rather good, but the actual deviation of the calculated $(T_e - T_{bath})$ from experimental data is rather large for large distance from the heater. The temperature of the S-Sm-S thermometer T_2 situated in point x_2 (see Fig. 4.9) is plotted as a function of the first temperature in Fig. 4.10(a). The Lorenz number L, which was calculated from this dependence on the basis of Eq. 4.11 is plotted as a function of the electron temperature T_1 in Fig. 4.10 (b). The Lorenz number slightly increases with the increase of the heating power at $T_1 < 2T_{sub}$ and demonstrates very rapid growth when the electron temperature exceeds the substrate one by a factor of 2.

In calculating the Lorenz number it was assumed that the phonons in the silicon film are similarly heated as in the electron-phonon interaction measurement and the phonon thermal conductivity was ignored in the doped Si film. This assumption might be incorrect. The phonon contribution to the thermal conductivity leads to an increase of the Lorenz number value derived from Eq. 4.11. Parallel heat conductivity in substrate is responsible for the increase of the Lorenz number. The heat flow in the phonon system leads to an additional increase of the phonon temperature and to a decrease of the heat flow between electrons and phonons system, and to a corresponding decrease of the value of I_1 (see Eqs. 4.5 and 4.11).

The circles in Fig. 4.10(c) represent the measured phonon temperature in the electron-phonon interaction experiment as a function of the electron temperature. Results correspond to a uniform heating of the SOI film. The solid line is the model phonon temperature dependence taking into account the phonon overheating due to a parallel phonon thermal conductivity. By introducing the parallel heat conduction model the situation is significantly improved (see Fig. 4.10 (d)). In the temperature range below 300 mK phonons are overheated above the substrate temperature approximately in the same manner as in the electron-phonon interaction measurement and the effect of the phonon thermal conductance can be neglected. At higher temperature the phonon system is heated more strongly and the phonon temperature approaches the electron temperature. Physically this means that the parallel heat conductivity of the phonon systems in substrate and in the SOI film starts to dominate in the heat transfer process at higher temperature.

4.4 Conclusions

The electron-phonon thermal conductivity has been studied in the heavily doped Si with doping concentration from $3.5 \cdot 10^{19}$ to $1.6 \cdot 10^{20} cm^{-3}$. The heat conductivity has qualitatively the same dependence ($\Sigma \sim T^6$) in this doping range and it increases with the carrier concentration. Overheating of the phonons in the Si film in respect to the substrate cannot be neglected in the analysis. Experimental results of the electron-phonon thermal conductance are in agreement with theoretical predictions, which are based on the intervalley scattering in many valley semiconductors.

The heat conductance along the Si mesa was also studied. This investigation was done only in one doping level ($3.5 \cdot 10^{19} cm^{-3}$). The agreement with the Wiedemann-Franz law is achieved when the phonon heat conductance along the Si film is taken into account.

These results can be applied in the design of micro- and nanoscale devices operating at sub-Kelvin temperature range. One must regulate the power consumption, because phonons can be locally overheated and the heat conductance via phonons is very significant.

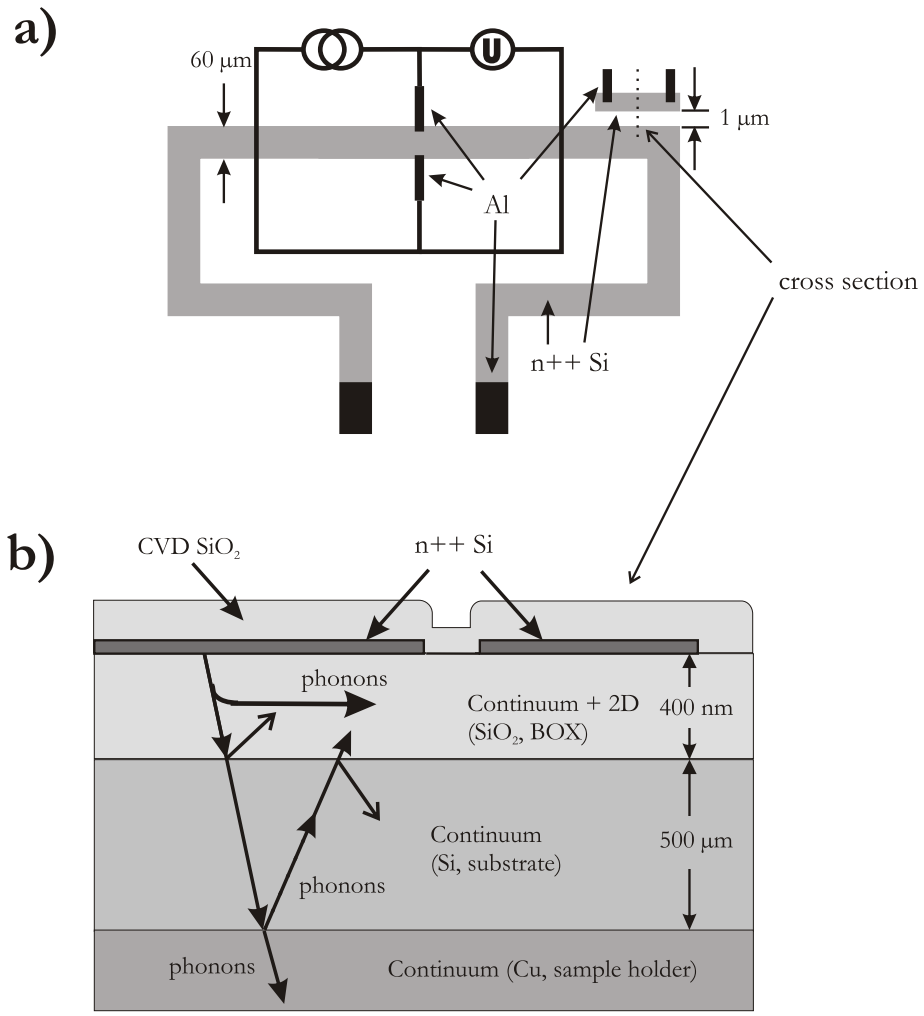

FIGURE 4.4 a) The schematics of the sample geometry and connections to external circuitry in the measurements. The long Si mesa is uniformly heated with a DC current. The electron temperature is measured using S-Sm-S (Al-Si-Al) thermometers. The S-Sm-S structure is biased with a DC current, and the voltage over the S-Sm-S contacts is dependent on the electron temperature in the Si mesa. The structure of the phonon thermometer is similar to the electron thermometer, but it is electrically isolated from the heated mesa. For clarity the measurement setup for the phonon thermometer has been omitted from the figure. b) The cross section of the SOI sample and the illustration of the phonon reflections from different interfaces (note: thicknesses are not in scale). In the SiO_2 layer the phonons can be both 2D and 3D, which complicates the phonon temperature analysis.

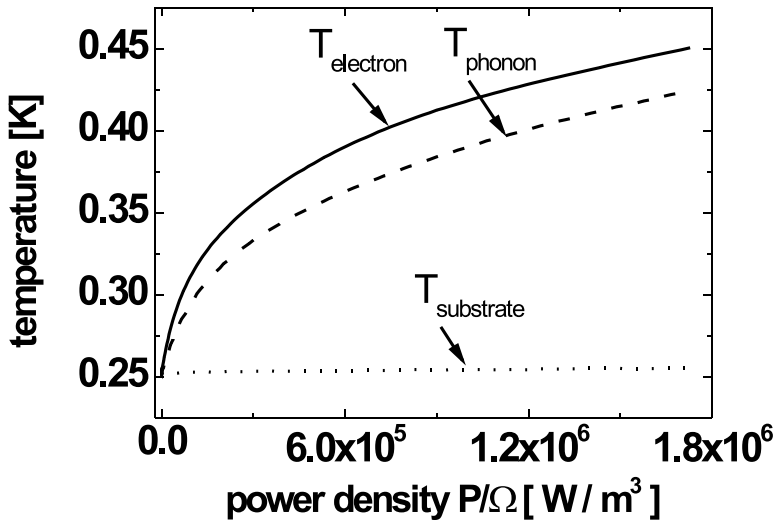

FIGURE 4.5 The electron and phonon temperatures as a function of the heating power density (SIN1G). The n++ Si film is heated by the Joule heating and the electron and the phonon temperatures are simultaneously measured. The substrate during the measurement is at a constant temperature (T_{SUB} = 255 mK).

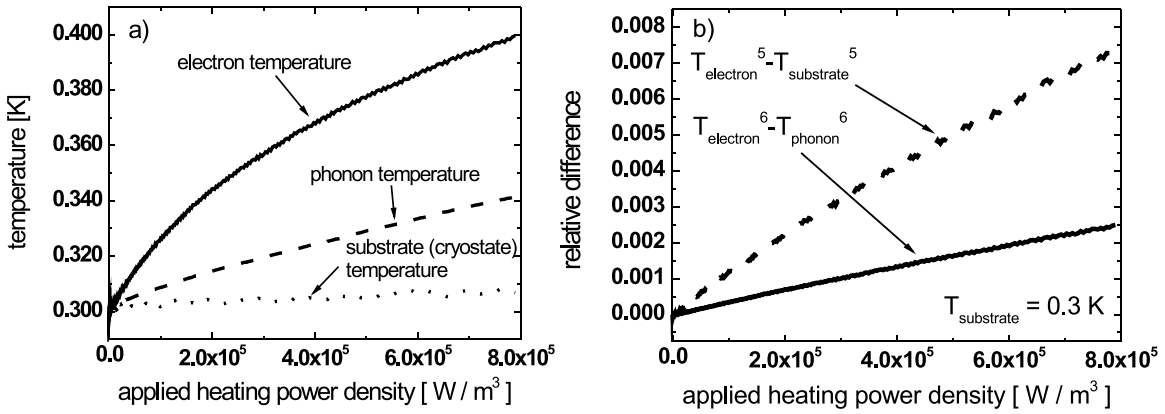

FIGURE 4.6 a) The electron, phonon and substrate temperatures as a function of the applied heating power density (SIN1F). b) Neglecting the phonon overheating leads to an incorrect temperature dependence (dash line). The solid straight line, indicating the electron-phonon heat transfer, has a T^6-dependence.

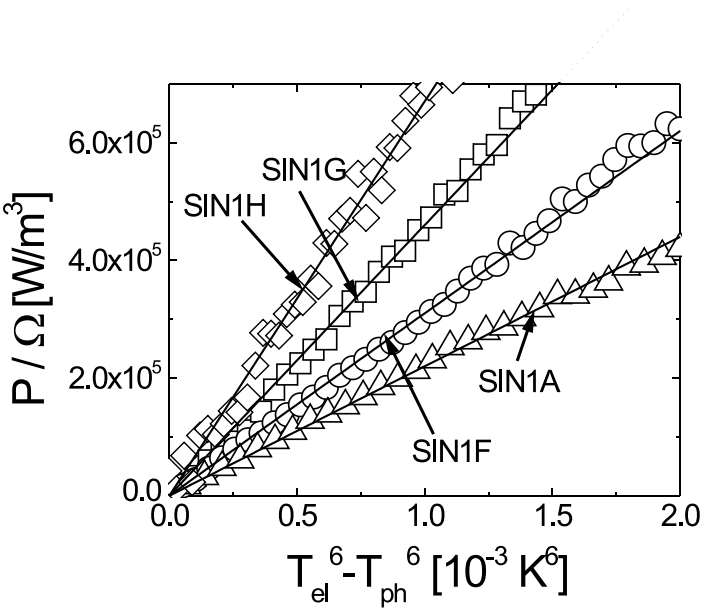

FIGURE 4.7 The power density vs. $(T_e^6 - T_{ph}^6)$ for samples with different carrier concentrations. Σ for SIN1A, SIN1F, SIN1G and SIN1H-wafers can be obtained from the fitting (see also Eq.(4.5)). For the SIN1H-wafer $\Sigma = 6.7 \cdot 10^8 W/K^6 m^3$, for the SIN1G-wafer $\Sigma = 4.6 \cdot 10^8 W/K^6 m^3$, for the SIN1F $\Sigma = 3.1 \cdot 10^8 W/K^6 m^3$ and for the SIN1A-wafer $\Sigma = 2.2 \cdot 10^8 W/K^6 m^3$. The substrate temperature is between 250 and 330 mK.

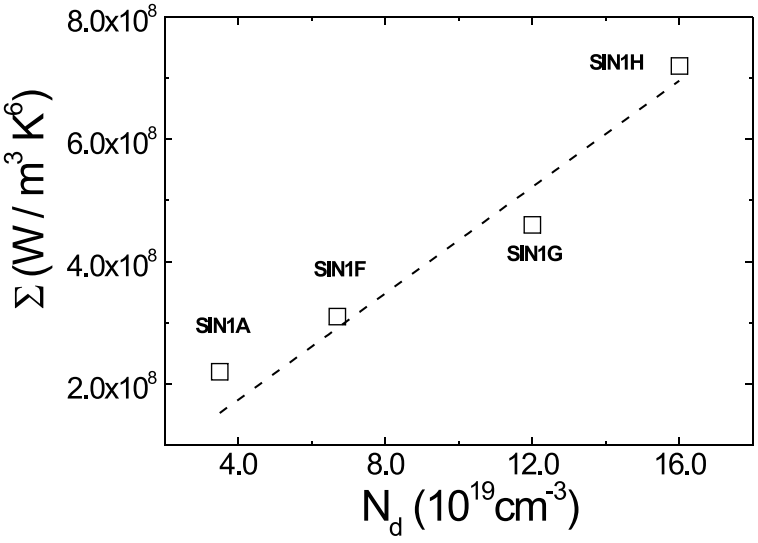

FIGURE 4.8 Electron-phonon thermal conductance Σ vs. N_d, where N_d is the carrier concentration. The dashed line is a fitting and the slope of the dashed line is $(4.4 \pm 0.3) \cdot 10^{-12} \frac{W cm^3}{m^3 K^6}$.

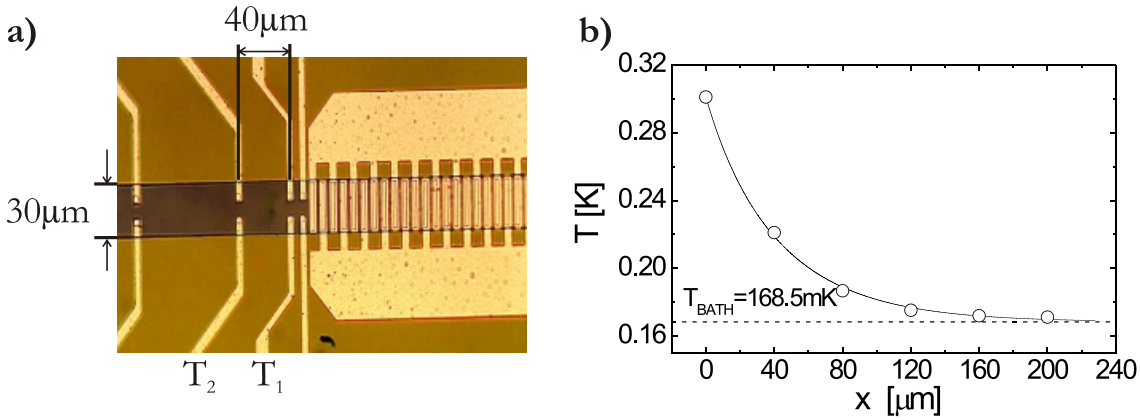

FIGURE 4.9 (a) micrograph of the sample. The mesa width is $30\mu m$ and the distance between the thermometers is 40 μm. The heating structure is on the right. (b) the electron temperature profile along the sample (circles) represent experimental data (see also the text). The solid line is Eq. 4.8 (the Lorenz number obtained from the fitting is $L = 2.45 \times 10^{-8} W\Omega/K^2$). The dashed line corresponds to the bath temperature T_{bath} = 168.5 mK.

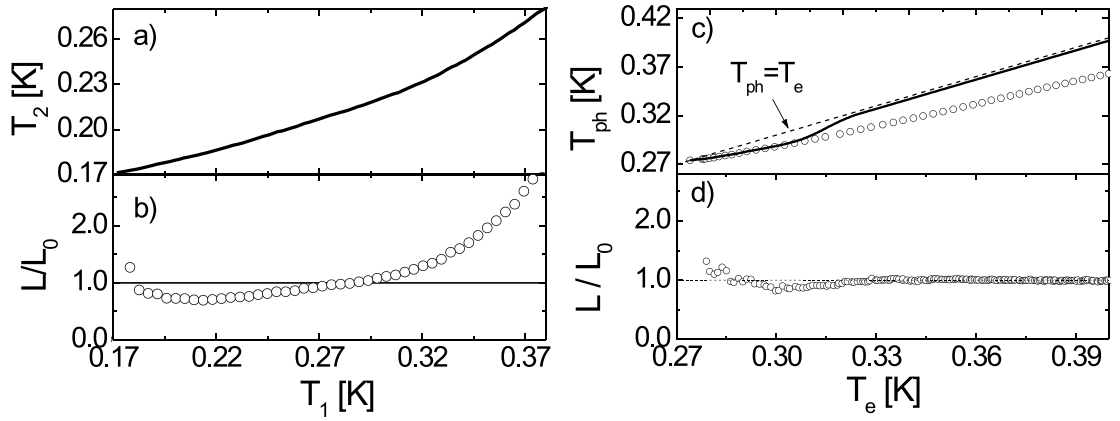

FIGURE 4.10 (a) The electron temperature T_2 plotted against T_1. The thermometers are placed 40μm apart and the bath temperature is 168.5 mK. (b) The relative Lorenz number as a function of the electron temperature T_1. (c) The phonon temperature in the SIN1A SOI film in the case of uniform heating of the film as a function of the electron temperature (open circles) and that from the model used to analyze the electron heat conductance experiment (solid line). (d) The Lorenz number calculated by taking into account the predicted phonon temperature profile.

5 Si applications at sub-Kelvin temperature

5.1 Electron refrigerator

5.1.1 The cooling principle

Cooling of the electron system in a normal metal [40, 31, 32], quasiparticles in a superconductor [36] or the lattice of a thermally isolated system [35] have been demonstrated using normal metal - insulator - superconductor (NIS) structures. In this approach heavily doped semiconductor (Si) has been used instead of the normal metal [1, 4, 5]. The Schottky barrier at the interface behaves as the insulator barrier in the NIS structure. Moreover, the utilization of the heavily doped semiconductor instead of a metal gives more possibilities for the adjustment of the material parameters for a particular application. As a result of its intrinsic properties, the superconductor - semiconductor (S-Sm) contact is very stable and reproducible compared with NIS, which is very important in regarding practical device applications.

The quasiparticle tunneling between the superconductor and the semiconductor is affected by the energy gap in the superconducting electrode. If the S-Sm (or S-Sm-S) structure is properly voltage biased, the quasiparticle tunneling current through the semiconductor will cool down the electron system in the normal (semiconductor) electrode (see Fig. 5.1).

The cooling of the normal electrode (semiconductor) can be observed at low temperatures when $k_B \ll \Delta$ (Δ is the superconducting energy gap) if a small voltage $V > 2\Delta/e$ is applied across the structure. At small bias only the most energetic electrons in the thermal tail of the Fermi distribution can tunnel from the semiconductor through the right Schottky junction to the superconductor. On the other hand, the quasiparticles below the energy gap in the left superconductor can tunnel to the semiconductor. The net effect is now that electrons are removed above (Sm -> S tunneling) and added below the Fermi level (S -> Sm tunneling) in the semiconductor. This reduces the total energy of the electron gas and leads to the cooling effect. The cooling power is inversely proportional to the normal state junction resistance

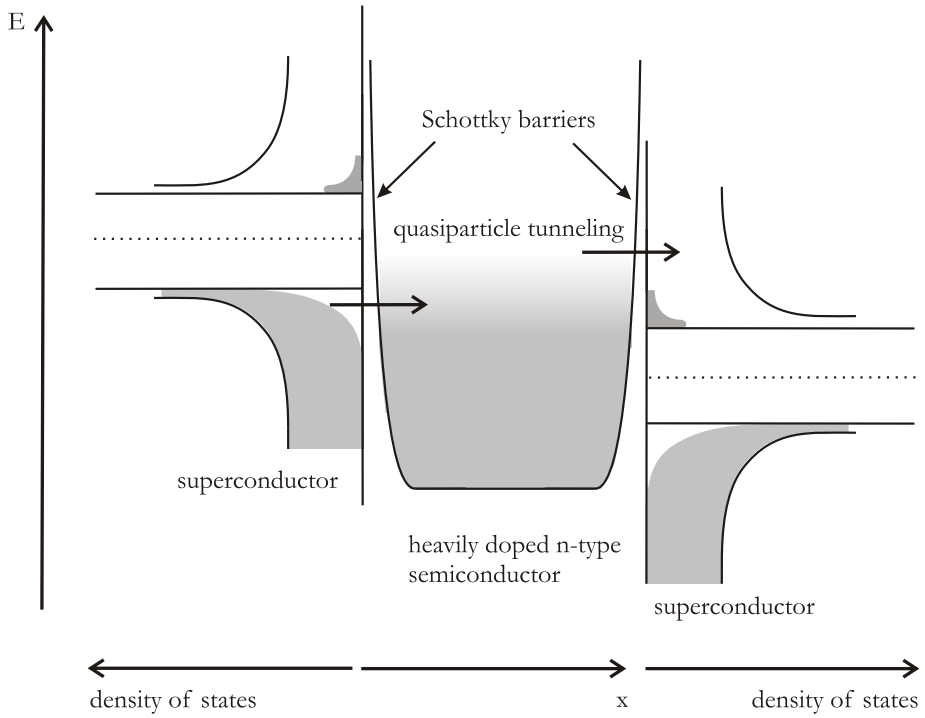

FIGURE 5.1 The principle of the cooling of the electron system by the quasiparticle tunneling. The S-Sm-S structure is properly biased that the "cooler" quasiparticles can tunnel from the left-side superconductor and the "hotter" quasiparticle will tunnel away from the semiconductor to the right-side superconductor. As an consequence the average electron temperature in the semiconductor will be decreased.

R_T [31,35]:

$$P_{max} \approx 2 \times 0.6 \frac{\sqrt{\Delta}}{e^2 R_T} (k_B T_e)^{3/2}, \tag{5.1}$$

where e is the electric charge, k_B is the Boltzmann constant and T_e is the semiconductor electron temperature. Reduction of the tunneling resistance R_T leads to an increase of the cooling power. With the decrease of the tunnel resistance and the corresponding increase of the electrical current through the structure the back tunneling of hot quasiparticles and the recombination phonons from the superconductor start to limit the cooler operation [24].

The performance of the electron refrigerator depends on the thermal conductance between the electron and phonon systems. As it has been shown in Ch. 4.2, the heat flow in Si[1] is [3,6,7]

$$P_{e-ph} = \Sigma V (T_e^6 - T_{ph}^6) \tag{5.2}$$

[1]The equation 5.2 also applies to certain metals such as Cu [25]

where V is the semiconductor volume and Σ is the material-dependent constant characterizing the electron-phonon heat conductance. If there is no additional heat flow in the system, the heat balance in the Si film is determined by the power P introduced into the electron system by the Joule heating (or the cooling power in the case of a S-Sm-S cooler) and the heat flow between the electron and phonon systems. The electron temperature can be found by solving the equation for the power balance in the system:

$$P + P_{e-ph} = 0 \tag{5.3}$$

5.1.2 Samples and thermometry

The typical cooler structure is depicted in Fig. 5.2. The physical size of the cooler is $20\mu m \times 30\mu m$ and the size of the cooler current contact is $18\mu m \times 5\mu m$. Smaller contacts ($3\mu m \times 3\mu m$) were used for the electron thermometry. The thickness of the Si film is 70 nm (SIN1A) or 58 nm (SIN1F, SIN1G, SIN1H). The details of the sample fabrication is described in Ch. 2.3. A ^{3}He/^{4}He dilution refrigerator was used for measurements in the temperature range between 50 mK and 1 K.

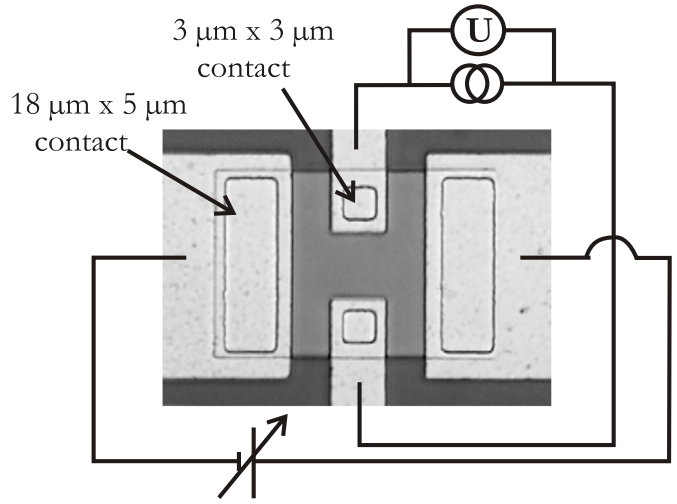

FIGURE 5.2 Micrograph of the cooler structure. The size of the cooler is $20\mu m \times 30\mu m$ and it has two pair of contacts: one ($3\mu m \times 3\mu m$) for the electron thermometry and the other ($18\mu m \times 5\mu m$) for the cooler current.

5.1.3 Results and discussion

The maximum cooling of electrons with respect to the substrate temperature has been observed in the SIN1A samples ($N_d = 3.5 \times 10^{19} cm^{-3}$). The electron temperature in the Si film as a function of the bias voltage across the cooler structure is shown

in Fig. 5.3 for SIN1A and SIN1F wafers. For SIN1A at temperatures below 450 mK all curves exhibit two clear minima at $V \approx \pm$ 0.34 mV. For a structure with two junctions in series the maximum cooling power is obtained at $V \approx \pm 2\Delta/e$ and from there the value of the energy gap is obtained for the Al-1% Si film $\Delta \approx 0.17$ meV. With a decrease of the substrate temperature the amplitude of the cooling peaks increases, which is due to the faster decrease of the electron-phonon coupling than the decrease of the cooling power. The electron system in SIN1A cools down to half of the bath temperature. The cooling was observed at substrate temperatures down to 40 mK. The voltage across the S-Sm-S thermometer as a function of the cooler voltage is presented in Fig. 5.4 for substrate temperatures below 150 mK, where electrons cool down to temperatures below the thermometer calibration range.

The samples with higher carrier concentrations ($N \geq 6.7 \times 10^{19} cm^{-3}$) having a lower charasteristic resistance of the junctions and thus a higher cooling power exhibit cooling only in the limited range of temperature. At low temperature the cooling curves demonstrate a rapid increase of the electron temperature with an increase of the applied voltage in the sub gap region (SIN1F in Fig. 5.3). The power corresponding to the Joule heating in Si is too small to describe this heating effect. According to our numerical modeling [4] the observed behavior cannot be described by the back tunneling of hot quasiparticles and phonons.

The heating of the phonon system in the Si film takes place in all samples, but this effect is stronger in the samples with more transparent junctions (higher operation current). The coefficient of performance the cooler θ_{max} (the ratio between the maximum cooling power and the total electric power applied to the cooler) is proportional to the electron temperature in the normal electrode $\theta \approx 0.3 \cdot T_e/T_C$ [5], where T_C is the critical temperature of the superconductor. The cooling power and the substrate thermal conductivity decrease when the temperature is lowered and this leads to the local overheating near the cooling junctions and to an increase of the phonon temperature in the Si film. As a result the electron cooling in respect to the phonons in the Si film does not produce cooling any more. Reduction of the contact resistance does not lead to a stronger cooling without modification of the cooler geometry and a more effective thermal contact between the cooler and the bath.

The characteristics of the coolers with carrier concentrations are represented in Table 5.1. The relative minimum electron temperature T_{min}/T_0 as a function of the substrate temperature T_0 is presented in Fig. 5.5. In the case of SIN1A the electron cooling increases with the temperature decrease within the temperature range under investigation. In the other wafers (SIN1F, SIN1G and SIN1H) the heating limits their operation at lower operation.

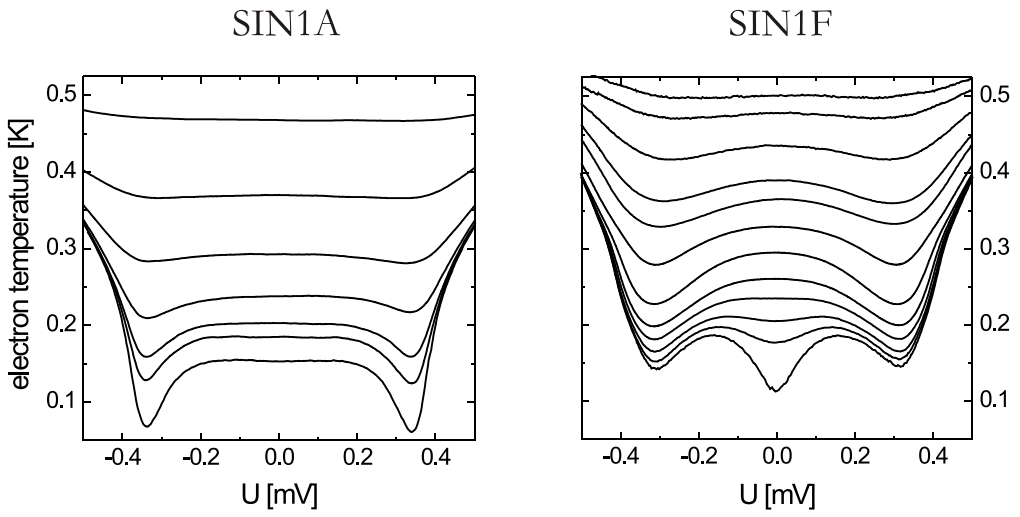

FIGURE 5.3 The electron temperatures as a function of the bias voltage in two different structures (SIN1A and SIN1F). At a higher carrier concentration (such as in SIN1F) the cooling occurs only in the limited range of temperature.

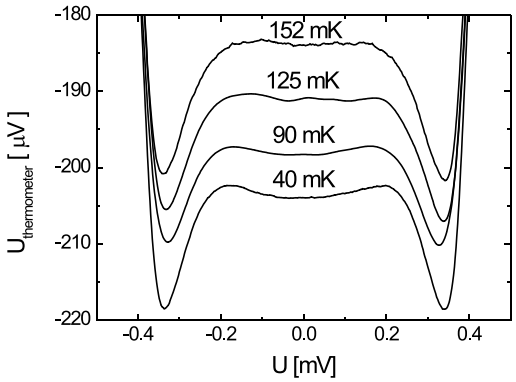

FIGURE 5.4 The electron temperature as a function of the bias voltage of the SIN1A. Electrons are cooled down below the thermometer calibration range.

5.2 Hot electron bolometer

One needs large-format pixel arrays of detectors ($10^3 - 10^5$ pixels) for the deep-space mapping in the sub-millimeter band [48] with the noise equivalent power (NEP) is below $5 \cdot 10^{-18} W/\sqrt{Hz}$. The working principle of a hot electron bolometer is quite simple: sub-millimeter radiation will heat up the electrons and one can deduce the energy of the absorbed radiation by measuring the electron temperature. The efficiency of the bolometer depends on the strength of the electron-phonon coupling. This makes Si very interesting material in comparison with metals, because

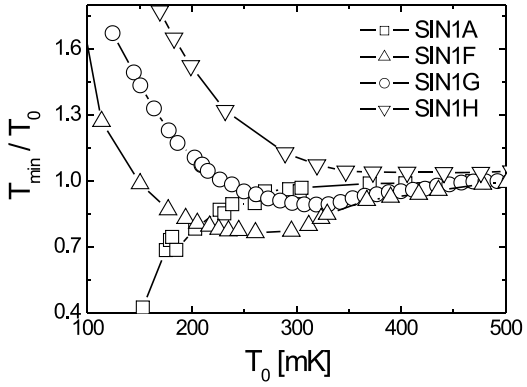

FIGURE 5.5 The relative minimum electron temperature T_{min}/T_0 as a function of the substrate temperature T_0 for coolers with different carrier concentration. The solid curves are guides for the eye.

wafer	N_d [cm^{-3}]	R_T@$1.5K$ [Ω]	P_{max} (175 mK) [pW]
SIN1A	$3.5 \cdot 10^{19}$	~ 750	~ 1.3
SIN1F	$6.7 \cdot 10^{19}$	~ 130	~ 7.6
SIN1G	$1.2 \cdot 10^{20}$	~ 40	~ 25
SIN1H	$1.6 \cdot 10^{20}$	~ 20	~ 50

TABLE 5.1 The characteristics of the SOI coolers. N_d is the carrier concentration, R_T the normal-state resistance of the $18\mu m \times 5\mu m$ junction and P_{max} is the maximum cooling power at 175 mK.

the electron-phonon coupling is in Si tunable and generally lower than in metals.

The performance of the detector is also limited by thermal fluctuations. The thermal fluctuation noise limit is given by [48]

$$NEP_{ph} = \sqrt{4k_B T^2 G} \tag{5.4}$$

where k_B is Boltzmann's constant, T temperature and G is the total thermal conductivity. With a proper geometry and design one can approximate that $G \approx G_{e-ph}$ where G_{e-ph} is the electron-phonon thermal conduction. Furthermore, the electron-phonon thermal conductance can be approximated in Si as

$$G_{e-ph} = 6 \cdot \Sigma V T^5 \tag{5.5}$$

where Σ is the electron-phonon coupling constant depending on the carrier concentration and V is the volume of the bolometer. The thermal fluctuation noise limit is then

$$NEP_{ph} = \sqrt{24 k_B \Sigma V T^7} \tag{5.6}$$

The parameter Σ for the SIN1A wafer is $2.2 \cdot 10^8 W/m^3 K^6$. If the operating temper-

ature is 50 mK and a volume of the Si island is $1.0\mu m^3$, the NEP will be order of $10^{-20}W/\sqrt{Hz}$ which is clearly below $5 \cdot 10^{-18}W/\sqrt{Hz}$.

If one would like to increase the performance it is always possible to attach an S-Sm-S based electron refrigerator to the bolometer (see Fig. 5.6 and 5.7). If the temperature is lowered to 25 mK, the NEP level in turn would be less than $10^{-21}W/\sqrt{Hz}$.

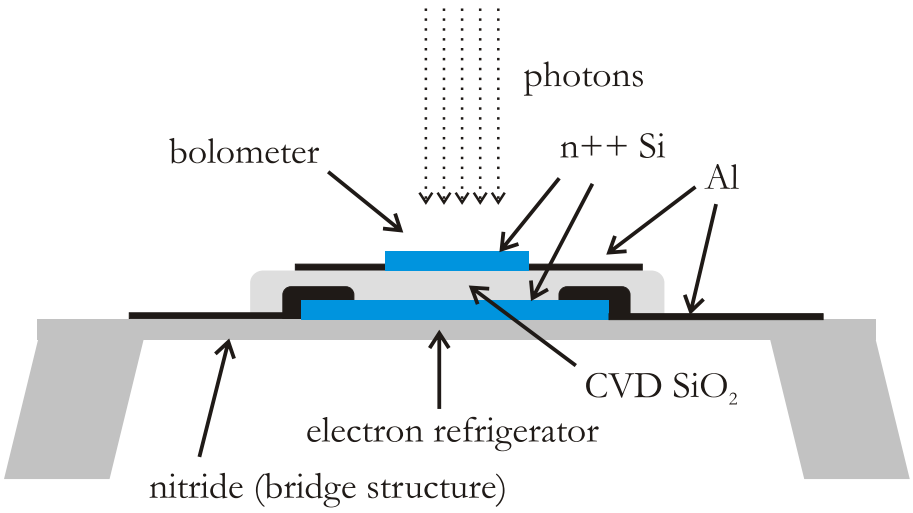

FIGURE 5.6 The bolometer structure from side. For the thermal insulation the whole structure is on a nitride structure. For an extra cooling the bolometer is placed on top of an electron refrigerator. The refrigerator in this setup must also cool down the SiO_2 insulator layer. Antennas needed for the bolometer have been omitted from the picture for clarity.

5.3 Neutrino detector

The bolometer described in Ch. 5.2 can also be applied in macroscopic scale for the detection of neutrinos. Si has been proposed as a possible candidate for the detection material [12]. In order to observe neutrino interaction rates through low-energy recoil electrons and nuclei one needs large detectors. Si is therefore very promising material, because it is available with extremely high purity in large amounts. Furthermore, in Si there is a nearly total absence of radioactive impurities, which could limit the accuracy of the neutrino detection.

Si has already been successfully applied for X-ray calorimetry at 100 mK [38]. S.H. Moseley et al. [39] estimate that in the interaction between an X-ray and the Si crystal 30 % is converted to free electrons or holes and 70 % directly to phonons. In addition, many of the free holes and electrons form excitons (bound hole-electron

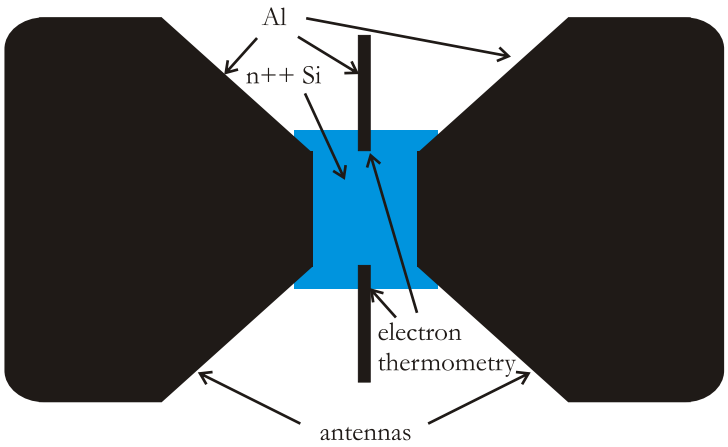

FIGURE 5.7 The bolometer structure from above. The antennas are made of superconducting Al and a similar but smaller S-Sm-S structure is used for the electron thermometry .

systems), which decay by emitting phonons, photons and Auger electrons. The phonon spectrum following the incidence of an X-ray is highly nonthermal, which complicates the analysis.

It has been estimated that for Si the neutrino yield will be 5.5 events per ton [22]. If one applies microscale electron and phonon thermometry discussed in Ch. 3.4 to a macroscopic single crystal Si, one could obtain a very sensitive device detecting neutrino incidents.

6 Superconducting metal structures

6.1 Motivation

For the low temperature electronics, in addition to semiconductor-based structures which have been discussed in Ch. 2 - 5, one can take advantage of phenomena related to superconducting metals (Josephson junctions). In this chapter the current noise properties in a superconducting single electron transistor and the photon assisted tunneling in capacitively coupled Josephson junctions will be discussed.

6.2 Noise in single electron transistors

6.2.1 Single electron transistor

A single electron transistor (SET) is a device which consists of an island connected to the external circuit by two junctions. The charge transport through the device is ensured by sequential tunneling through the junctions due to an external bias voltage. A gate electrode, evaporated in close proximity to the structure, creates a so-called gate capacitance with respect to the island. With modern nanolithography one can design these devices so that the total electrical capacitance associated with the island (the sum of the junction capacitances and that of the island) is small enough, therefore the charging energy could be larger than the temperature. In this regime, the transport through the device is controlled in a sensitive way by the gate voltage (Coulomb blockade effect) [19].

Below a critical temperature, the structure could become superconducting. In this case, several new transport mechanisms appear at different bias voltages, due to combinations between quasiparticle generation and Josephson effects in each junction.

The current noise properties of Al/AlOx/Nb/AlOx/Al-based SETs are studied, where AlOx builds up the insulating layer and Nb forms the Coulomb island. In comparison with Al, Nb can be in some sense more attractive material: Nb has a larger superconducting gap and therefore its critical temperature T_C is much higher than that of aluminium ($T_C^{Al} \approx 1.2K, T_C^{Nb} \approx 9.3K$ [9]).

6.2.2 Fabrication and experimental setup

The Al/AlOx/Nb/AlOx/Al single electron transistors were fabricated on oxidized p– Si substrate by using the standard self-alignment lithography process with a double layer resist of PMMA - P(MMA-MAA). The layer thicknesses were 300 nm and 400 nm respectively. P(MMA-MAA) was baked at 160°C for 45 min and PMMA for 60 min. The patterns were drawn by using a scanning electron microscope and the actual structures were evaporated with the self-aligning shadow technique [17]. The line width of the source/drain lines was approximately 130 nm.

Samples were measured at sub-Kelvin temperature by using two different ^{3}He/^{4}He dilution refrigerators. The base temperature of the cryostat was around 250 mK. The measurements were carried out in a shielded room with a battery powered DL-Instrument 1211 current preamplifier and a 1201 voltage preamplifier. The output of the current amplifier was directly connected to Stanford Research 760 Fast Fourier Transform spectrum analyzer.

6.2.3 Results and conclusions

The SET was connected to a battery source and the current was amplified and fed to the spectrum analyzer. The bias voltage was varied between 0 and 700 μV as the gate voltage was kept constant (0 and 100 mV).

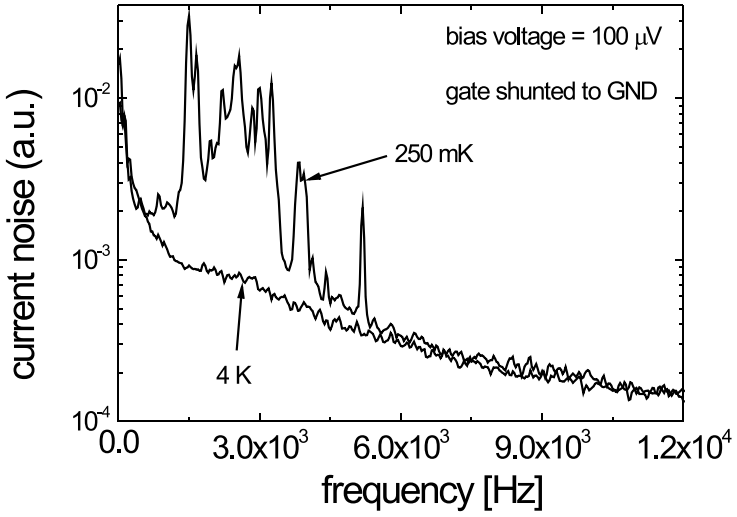

FIGURE 6.1 The noise spectrum of an Al/Nb - SET (B1606) at two different temperatures (250 mK and 4 K). A noise spectrum can be seen between 1 and 6 kHz at superconducting state which vanishes at 4 K.

In Fig. 6.1 is presented the noise spectrum of an Al/Nb single electron transis-

tor at two different temperatures. In the superconducting state an anomalous noise spectrum appears between 1 and 6 kHz. The amplitude of the noise is at least one order of magnitude larger than the 1/f-noise on the background.

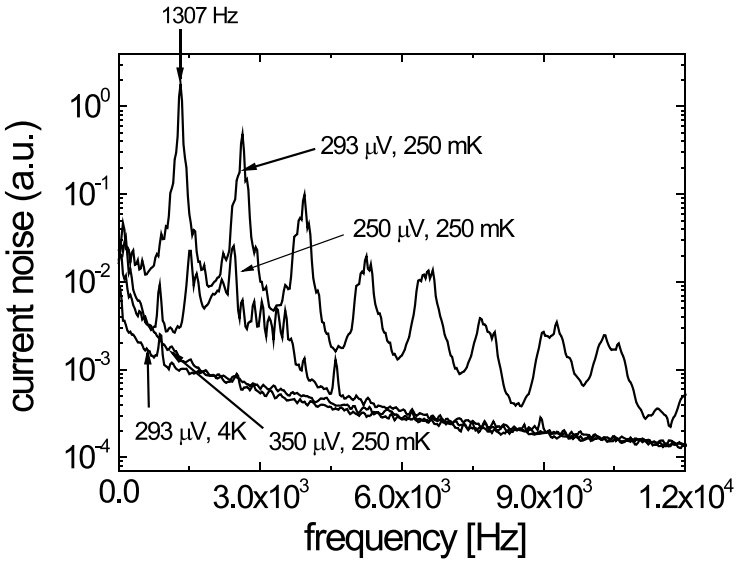

FIGURE 6.2 A similar noise spectrum of an Al/Nb - SET (A1606) as in Fig. 6.1. The noise level starts to build up at 250 μV and at 293 μV there is an induced AC-current, which frequency 1.3 kHz.

In Fig. 6.2 is the noise spectrum of another SET on the same chip. At 293 μV an AC-current, which frequency is 1.3 kHz, is induced. This AC-current is strongly dependent on the bias voltage and it vanishes as the bias voltage is increased to 350 μV.

In Fig. 6.3 is the frequency band from 0 to 2 kHz. The frequency of the AC-current decreases as a function of the increasing bias voltage and vanishes at 350 μV. The voltage dependence showed little or no hysteresis. In addition the variation of the gate voltage (between 0 and 100 μV) had a negligible effect on the current spectrum.

The measurements were done in a dilution refrigerator, which had commercial radio frequency pi- and strip filters near the sample holder at 4 K. Although the role of the filters is crucial for good thermalization and attenuating nonequilibrium fluctuations coming from the room temperature and the outer electrical lines, their presence makes the results difficult to interpret. For a correct analysis one must vary the cut-off frequency and the attenuation in order to exclude possible interference effects.

The series of peaks in the spectrum appears when the transistor is biased in a voltage range in which a resonance effect called the Cooper pair resonances have been seen before [60]. This effect is due to a combination of Josephon tunneling

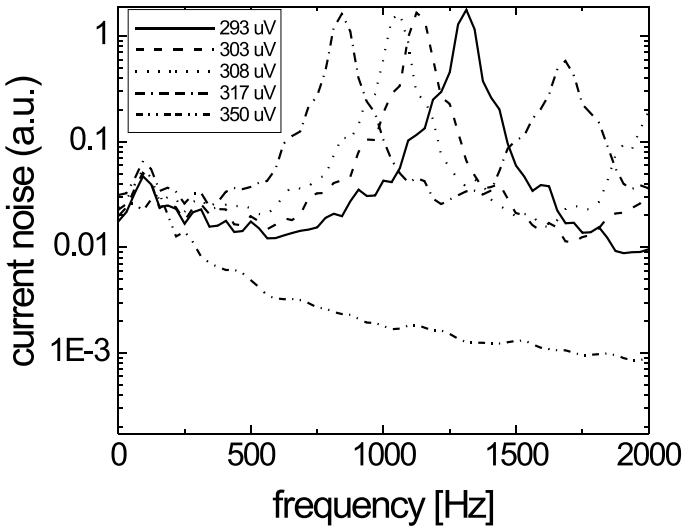

FIGURE 6.3 The noise spectrum below 2 kHz. The frequency of the AC-current decreases as a function of the bias voltage from 1.3 kHz to 800 Hz. At 350 μV the AC-current is vanished.

followed by quasiparticle de-excitations. The time scales involved in this process are not yet fully understood, but one can speculate that the peaks seen in the data are an indication of oscillations in the system induced by this effect.

6.3 Photon assisted tunneling

6.3.1 Background and motivation

Noise measurements are a powerful method to probe mesoscopic systems. Recently it has been realized that one can measure the shot noise of electrons tunneling through a single electron transistor by using a superconducting junction biased closed to the quasiparticle gap [16]. In this paper, the junction is coupled capacitively to the system under study and the detector junction has a similar function with the standard SIS detectors used in astronomy applications. An analog system has been proposed but not yet realized with double quantum dots [8].

A simpler configuration but still interesting is obtained if two Josephson junctions are capacitively coupled together, see Fig. 6.4. This is a well-studied system of two coupled phase qubits [11]. The energy levels for this system have been calculated and confirmed by spectroscopy measurements and entanglement between the macroscopic quantum states of the two systems has been demonstrated.

Another view can be taken on this system: in what follows, one junction will be regarded as a radiation source with an intrinsic noise, and the detector as a po-

tential qubit (the photons will be mainly transmitted capacitively). In other words, the interest is in creating an on-chip coherent source of radiation and demonstrating that the coupling can be sufficiently strong to excite a phase qubit. Unlike the case of Deblock *et al.* [16], one can look at the influence that the radiating junction has on the Josephson effect of the detector/qubit.

For example, for a good enough coupling one can expect the appearance of Shapiro steps in the IV of the detector. Preliminary results presented in this thesis demonstrate that there is indeed a measurable influence on the Josephson current of the detector/qubit. Also, it would be interesting to study the effect of thermal and quasiparticle noise on the radiation spectra of the source (the linewidth of the radiation), a subject that received recently a renewed attention (Ref. [33] and references therein) since the classical work of Stephen [55,56].

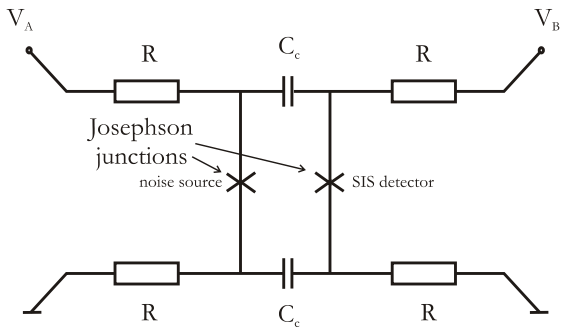

FIGURE 6.4 The schemactics of the capacitively coupled Josephson junctions. Junctions are identical and both can act as noise source or detector. The resistors are Pt wire evaporated on chip and are order of 2 kΩ.

Around the energy gap of the detector, if the bias V_{SIS} in the detector is less than the energy gap (Δ) the tunneling of quasiparticles is prohibited. However, the absorption of a photon of energy $\hbar\omega$ that exceeds the value of ($2\Delta - eV_{SIS}$) can assist in the tunneling. This process is called the photon assisted tunneling and the tunneling current carries information of the quantity and the energy of the absorbed photons in the SIS detector [61].

In the case of the source, the interesting bias is that for which V is sligthly larger than $2RI_c$, where R is the on-chip resistor and I_c is the critical current of the Josephson junction. In a schematic description, the junction will be in the running phase state and therefore, by the Josephson effect, the macroscopic relative phase γ will evolve according to the Josephson relation as $\gamma = \omega t$ where $\omega = 2e/\hbar(V - 2RI_c)$. The current will then be oscillating as $I_c sin\omega t$, and one expects that the value of ω is roughly given by the smearing of the current-voltage characteristics of the detector near the quasiparticle threshold 2Δ.

6.3.2 Fabrication and experimental setup

The samples were fabricated in a similar process as described in Ch. 6.2.2. Soft O_2 reactive ion etching cleaning was used for 30 s to remove the residual resists in the exposure areas before the evaporation. Ti was evaporated 4 nm as a sticking layer and after that 20 nm of Pt. Pt was used for the resistors and the lower part of the capacitors. After that 60 nm AlOx was used for the dielectric material between the capacitor plates. The upper capacitor plates, the Josephson junctions and the contact pads were made by evaporating 90 nm Al. The insulating layer was made with oxidation, which lasted 3 minutes at 20 mbar. The sample is depicted in Fig. 6.5. It is estimated that the capacitance of the capacitors to be order of 100 fF.

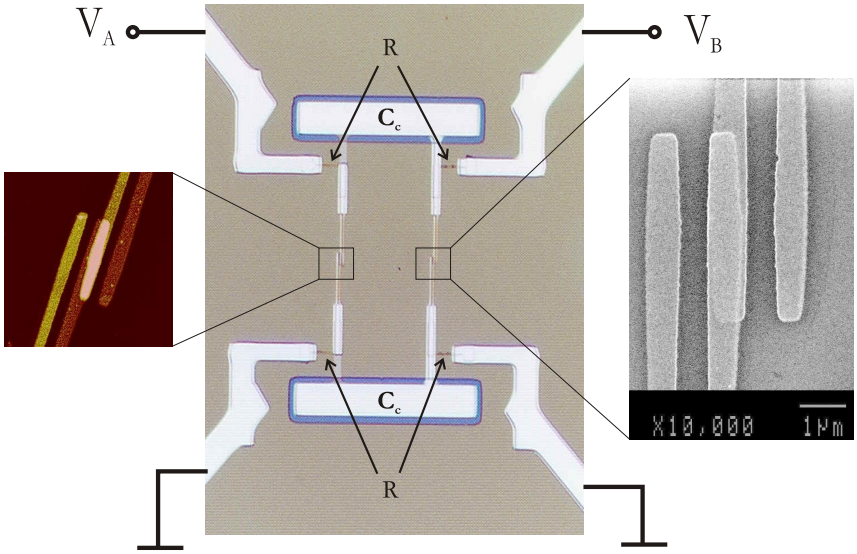

FIGURE 6.5 The sample used in the measurements. In the middle is an optical photograph, on the left a photo taken with an atomic force microscope, on the right a photo by a scanning electron microscope.

The samples were cooled down to sub-Kelvin temperature by a ^{3}He/^{4}He dilution refrigerator. Both junctions were applied as a noise source and a SIS detector respectively. In order to distinguish a small changes in the IV-curve Stanford SR530 lock-in amplifier was used to measure the dynamic conductance of the SIS detector as the voltage bias of the noise source was changed.

6.3.3 Results and conclusion

Several samples were measured and a change due to photon assisted tunneling was observed. First the structure A (Fig. 6.6) was applied as a detector and B (Fig. 6.7) as a detector. After that the measurement was repeated by using A as a noise source

and B as a detector. The voltage bias was changed from positive to negative and the effect on the measured dI/dV-curve was identical in the detector, i.e. the polarity of the bias voltage of the noise source had no effect. In Fig. 6.6 are the dI/dV and IV-curves of the junction A. The junction was in no means ideal, because there was considerable leak current through the junction. The change due to noise bias in the dI/dV graph was however clearly observable. In Fig. 6.7 is the junction B (counterpart of A), which has a better IV characteristics. However the observed change in the dI/dV curve is close to the noise level. This may be due to the fact that the junction A acts as a poor noise source. Also if there is leak current (as in A) through the detector the variations in the IV-curve can be more easily detected.

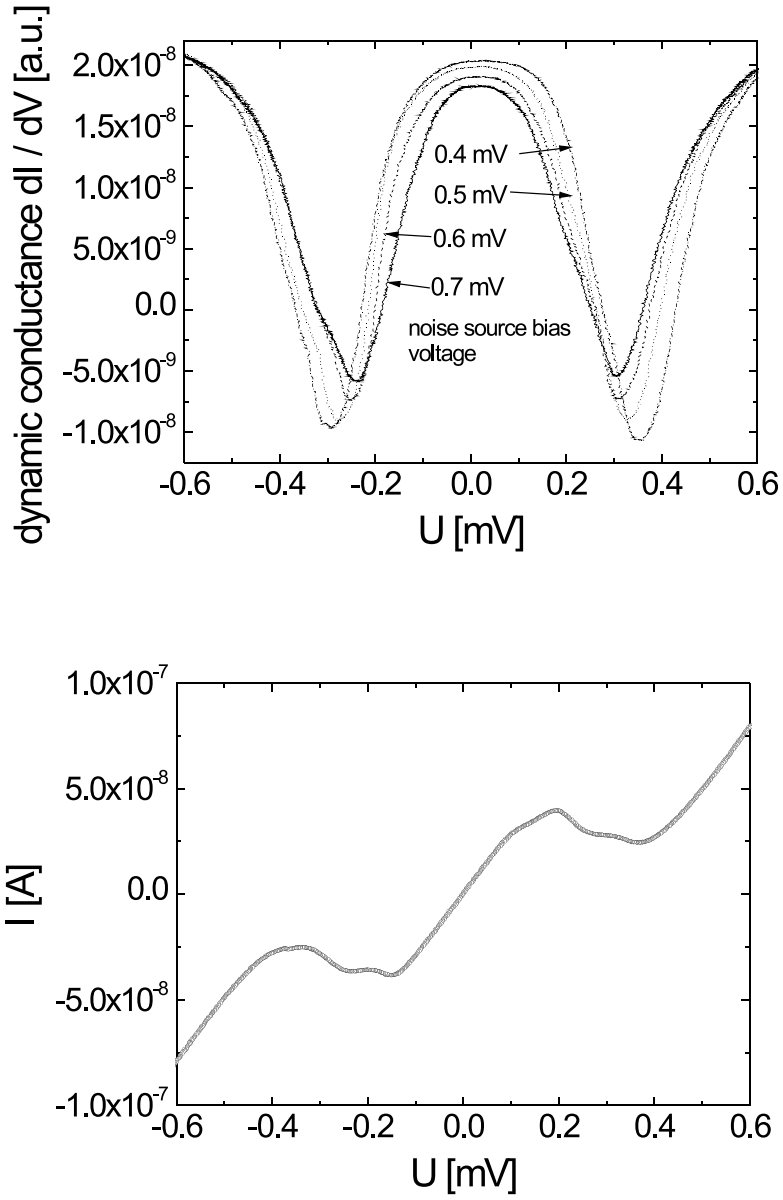

FIGURE 6.6 Above: dynamic conductance of a Josephson junction A as a function of the noise source voltage bias. For clarity only four voltage bias values are plotted. The cryostate temperature in the measurement was 60 mK. Bottom: The IV-curve of the detector junction. The total resistance of the junction and resistors is 4.3 kΩ.

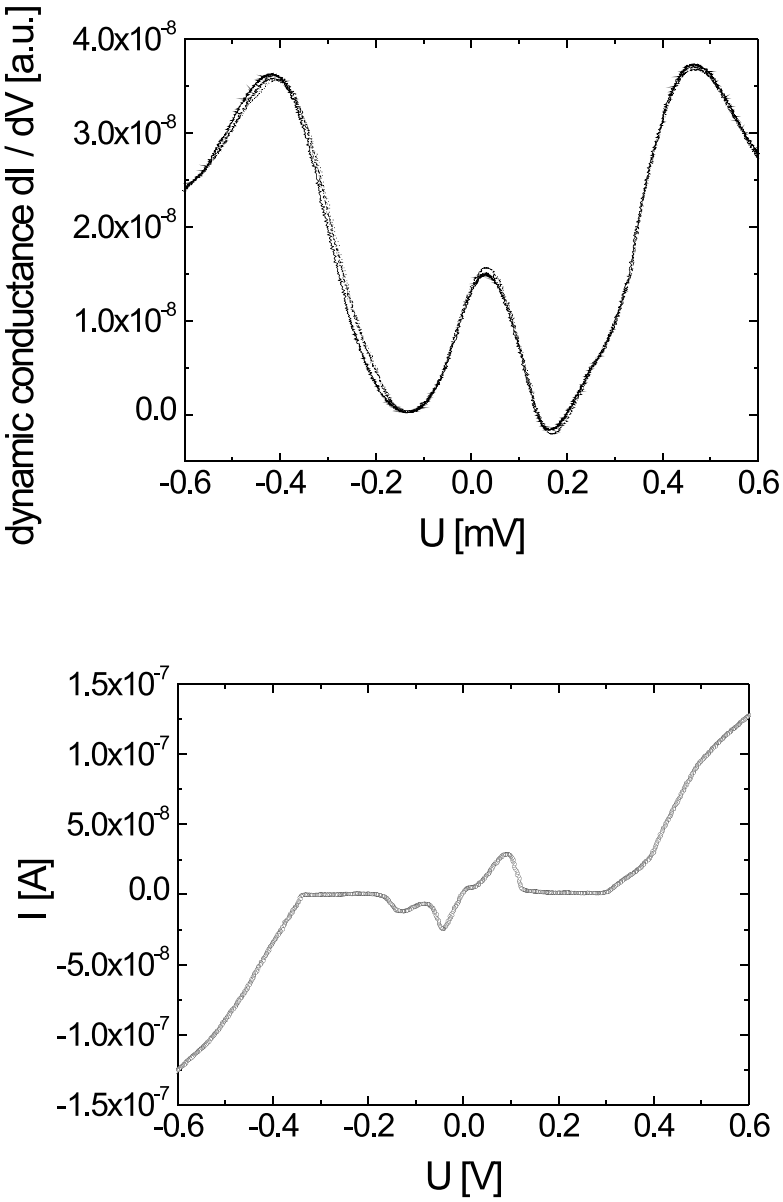

FIGURE 6.7 Above: dynamic conductance of a Josephson junction B as a function of the noise source voltage bias. This junction and that of Fig. 6.6 are capacitively connected together. Bottom: The IV-curve of the detector junction. The total resistance of the junction and resistors is 3.6 kΩ.

7 Conclusions

The main focus of this thesis is the electron and thermal transport properties of the heavily doped silicon thin film structures with doping levels 3.5 - $16.0 \cdot 10^{19}$ cm^{-3} at sub-Kelvin temperature. According to theoretical predictions the electron-phonon thermal conductance is intrinsically dependent on the scattering mechanisms of the conduction electrons and the intervalley scattering determines the electron-phonon energy relaxation.

The electron-phonon measurements have been carried out at sub-Kelvin temperature. The substantial overheating of the phonon system in the doped silicon film is remarkable and it has been taken into account in the heat conduction analysis. The heat flow between the electron and phonon systems demonstrates a T^6-dependence, which is in accordance with the predicted theoretical results for many-valley semiconductors (Si). The electron-phonon coupling constant increases as a function of the carrier concentration, which is also in agreement with the developed theoretical model.

The heat conductance of electrons along the Si mesa has been studied. The electron thermal conductivity dominates at low temperature and at temperatures above 300 mK the parallel heat conduction in the phonon system must be taken into account.

Si-based electron refrigerators have been suggested and studied as a low temperature application for the S-Sm-S structures. The operational principle of the Si-based electron coolers is similar to generally well-known SINIS electron refrigerators, where the quasiparticle tunneling current cools the normal metal. Si is however a more versatile material as normal metals in respect of applications and in addition the Sm-S contact is very stable and reproducible compared with the NIS structures.

The performance of the S-Sm-S coolers have been investigated as a function of carrier concentration in heavily doped Si. The variation of the doping level (in addition to the electron-phonon interaction) affects the characteristic resistance of the Al-Si junction and the performance of the S-Sm-S cooler. It was found out, that heavily doped Si with carrier concentration $3.5 \cdot 10^{19}$ cm^{-3} is optimal for the direct cooling of electrons. The devices with higher carrier concentrations produce a higher cooling power, but an unwanted heating may exceed the cooling effect and limit the effective temperature range of the coolers.

S-Sm-S structures could be also applied for the hot electron bolometry. Due to a low electron-phonon coupling the electrons in Si are more easily to be overheated

than in normal metals. The low electron-phonon coupling results in a low noise equivalent power level, which can be further improved by lowering the electron temperature in Si by combining the bolometer with a S-Sm-S refrigerator. In principle, but in larger scale, this structure could also be utilized for a neutrino detector.

The noise characteristics in Al/Nb based single electron transistors have been studied in the sub-Kelvin temperature range. The current noise spectrum has been measured as a function of the bias and gate voltages. Anomalous noise has been detected which is also strongly dependent on the bias voltage. Its origin remains vague, but it could be related to Cooper pair resonances, which are due to a combination of Josephson tunneling followed by quasiparticle de-excitation.

The photon assisted tunneling in capacitively connected Josephson junctions has been discussed. The first junction has been applied as a voltage biased radiation source and the second junction as a detector. It has been observed that the current-voltage (or dI/dV) characteristics of the detector varies as a function of the absolute magnitude of the noise source bias voltage. A similar setup could be applied for the excitation of a phase quantum bit.

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