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Heavy-ion induced single event effects and latent damages in SiC power MOSFETs☆

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ABSTRACT

The advantages of silicon carbide (SiC) power MOSFETs make this technology attractive for space, avionics and high-energy accelerator applications. However, the current commercial technologies are still susceptible to Single Event Effects (SEEs) and latent damages induced by the radiation environment. Two types of latent damage were experimentally observed in commercial SiC power MOSFETs exposed to heavy-ions. One is observed at bias voltages just below the degradation onset and it involves the gate oxide. The other damage type is observed at bias voltages below the Single Event Burnout (SEB) limit, and it is attributed to alterations of the SiC crystal-lattice. Focused ion beam (FIB) and scanning electron microscopy (SEM) were used to investigate the damage site. Finally, a summary of the different types of damage induced by the heavy ion in SiC MOSFETs is given as a function of the ion LET and operational bias.

1. Introduction

The wide-bandgap silicon carbide (SiC) semiconductor has emerged as the most viable alternative to silicon (Si) for the next-generation material for high-efficiency and high-power density applications [1,2]. Compared to Si, SiC exhibits an order of magnitude higher critical field for breakdown, three times larger bandgap, and three times higher thermal conductivity, resulting in about three times more efficient cooling capability [1]. The higher critical field allows manufacturing SiC power devices with much thinner drift layer compared to Si devices, reducing the resistance per unit area, and therefore reducing the conduction losses. Due to the wide bandgap, the intrinsic carrier density at room temperature (i.e., the electrons and holes generated by thermal excitation), is extremely low, enabling the SiC electronic devices to operate at high temperatures with low leakage current. These properties make SiC an attractive material to manufacture power devices by far exceeding the performance limits of their Si counterparts. A three-dimensional representation of the 4H-SiC polytype used to manufacture power devices is shown in Fig. 1.

Although the research on SiC material has been performed for several decades, only after the late 1980s its use has been suggested for power device manufacturing. The first SiC MOSFET appeared on the market in 2011. Since then, it has taken time for the technology to mature, to address the reliability concerns and for the price to drop sufficiently, but eventually these milestones have been achieved by multiple manufacturers, and in the past few years SiC MOSFETs have seen tremendous commercial progress. Nowadays SiC power MOSFETs are found in a variety of applications in the automotive, photovoltaic and power supply segments [3].

Due to the higher energy required for ionization and defects formation respect to Si, SiC technology has been considered very suitable for harsh working conditions, including radiation exposure [4]. These advantages make SiC technology desirable also for space, avionics and high-energy accelerator applications [3,5,6]. Despite that, the current commercial technologies are still susceptible to Single Event Effects (SEEs) caused by the radiation environments encountered in these

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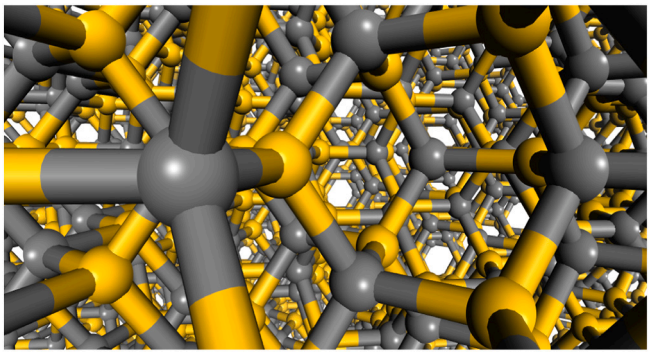

Fig. 1. Three-dimensional perspective of a 4H-SiC crystal in a ball-stick model. Yellow and gray circles represent respectively carbon (C) and silicon (Si) atoms. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

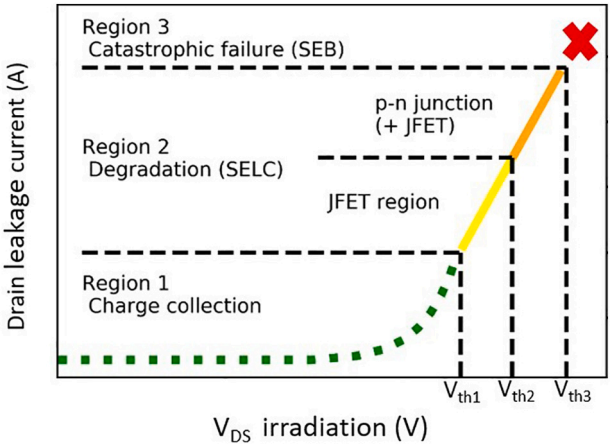

Fig. 2. Conceptual definition of three regions of response of a SiC MOSFET exposed to heavy-ions, represented with the drain-leakage current as a function of the drain-source bias during the irradiation.
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Table 1
Characteristics of the ion species.

Ion	Energy/nucleon [MeV/amu]	LET [MeV cm^2/mg]	Range SiC^{SRIM} [μm]
$^{40}Ar^{+14}$	16.3	7.7	175.0
$^{56}Fe^{+15}$	16.3	14.6	136.4
$^{82}Kr^{+22}$	16.3	25.3	125.7
$^{131}Xe^{+35}$	16.3	49.1	112.2

applications. These effects are a perturbation of the normal operation of the device, which increase the risk of partial degradation or complete failure of the components, preventing the implementation in these fields. In the case of heavy-ions, the primary ionization induced by the impinging particle causes excess charge (electron-holes) that, combined with the electric fields within the device, can lead to different effects. Single Event Burnout (SEB), Single Event Leakage Current (SELC) or degradation, and Single Event Gate Rupture (SEGR) have been observed for SiC power MOSFETs and diodes, when exposed to different radiation environments, and previously described in [7–22].

1.1. SEEs in planar SiC MOSFETs exposed to heavy-ions

Three regions of response are observed when monitoring the drain leakage current (I_D) of SiC power MOSFETs exposed to heavy-ions (a planar-gate is considered). The three regions are represented in Fig. 2 as a function of the drain-source bias (V_{DS}). At low voltage, the ionization caused by the impinging particle induces only enhanced charge collection, with no permanent damage in the device (Region 1). Increasing the bias, degradation occurs, recently named Single Event Leakage Current (SELC) [10] (Region 2). This effect is characterized by a permanent increase in drain and gate leakage currents with increasing heavy ion fluence. Even though the SELC is non-destructive, the device operation is altered, and it complicates the assessment of radiation reliability for the tested parts. Two sub-regions were identified for this effect, as described in [10,11]. Initially, at a sufficiently high V_{DS} above V_{th1}, the drain and gate leakage currents increase with the same magnitude during the exposure, having a linear proportionality to the fluence. The conductive path is observed between the gate and drain terminals. The induced damage is permanent, and the leakage currents do not recover to the pristine values after the irradiation. From the ion microbeam studies, it was observed that the area underneath the gate (JFET and channel regions) is the most sensitive for this type of damage [10]. For V_{DS} higher than V_{th2}, the second mechanism of degradation becomes active; the gate current (I_G) keeps increasing linearly with respect to the fluence, whereas the drain current (I_D) starts increasing with a much larger magnitude respect to I_G. From the microbeam studies, the p-n junction was identified as the sensitive region at these voltage levels. This second mechanism of degradation was suggested to be the same as observed in SiC diodes, and to be caused by Joule heating, which results in increasing temperature and phase change in the SiC substrate, as confirmed by molecular dynamics simulations [23,24]. These affected regions are unlikely to recover completely, leaving permanent structural modification in SiC lattice, causing the creation of permanent extended defects (ED), such as different dislocations, amorphous pockets, stacking faults, different SiC solid-phase (polytype) inclusions, clusters, and so on [10]. Finally, at V_{DS} higher than V_{th3}, a destructive SEB occurs (Region 3).

After an initial debate concerning the role of the parasitic BJT in the SEB mechanism, a common explanation was suggested in [9] for SiC MOSFETs and SiC junction barrier Schottky (JBS) diodes, where in the latter there is no such parasitic BJT structure. Highly localized energy pulses induced by the ion strike were suggested as responsible for the SEB damage. Furthermore, in the same work lower magnitude energy pulses were identified as responsible for non-destructive degradation, assuming the SEB being a more catastrophic form of degradation.

The threshold voltages shown in Fig. 2, can vary with the manufacturer and the ion linear energy transfer (LET); a summary for the studied devices is presented in Section 4. In this case, the transition between the two types of degradation was always observed at $V_{th2} \geq 350$ V for LET > 10 MeV cm^2/mg, as reported in [11].

In addition, the SiC power MOSFETs studied in this work exhibit two types of latent damage. The first is observed when the device is exposed in the pre-degradation region (Region 1), therefore supposedly de-rated to protect from degradation. This type of damage was previously discussed in [21,25] and it involves the gate oxide. The sensitivity on different ion LET values is reported below (see Section 3.1).

The second type of latent damage is observed in the pre-SEB region (Region 2), where the devices are sufficiently de-rated to be protected from SEB, but not from the second type of degradation. This latent damage is attributed to effects in the SiC crystal lattice, whose structure is altered by the presence of ED created by the ion strike. The failure site was investigated using plasma FIB-SEM analysis (see Sections 3.2 and 3.3).

2. Heavy-ion experiments

2.1. Heavy-ion broad beam facility

The experiments were performed at the RADiation Effects Facility (RADEF) in the Accelerator Laboratory of the University of Jyväskylä

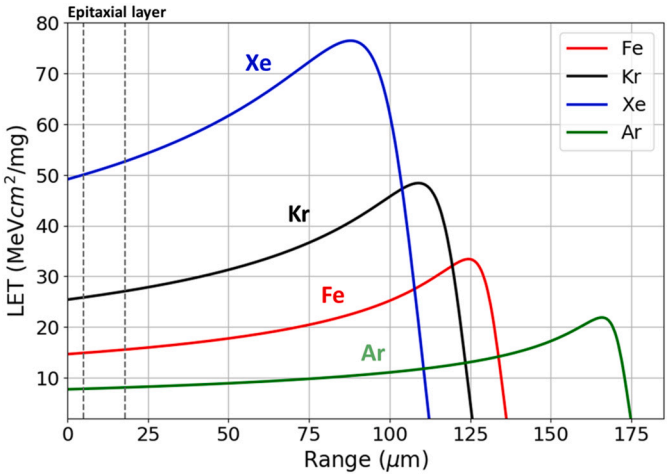

Fig. 3. LETs as a function of the penetration range for the 16.3 MeV/amu heavy-ion species used during the experiments. The dashed lines highlight the thickness of the epitaxial layer of the device.

Table 2
Characteristics of the DUTs.

Reference	$R_{DS(on)}$ [mΩ]	V_{DS} [kV]	$I_{D\ @\ 25^{\circ}}$ [A]	Experiment
CPM2-1200-0160A	160	1.2	18	1st
CPM2-1200-0040A	40	1.2	60	2nd

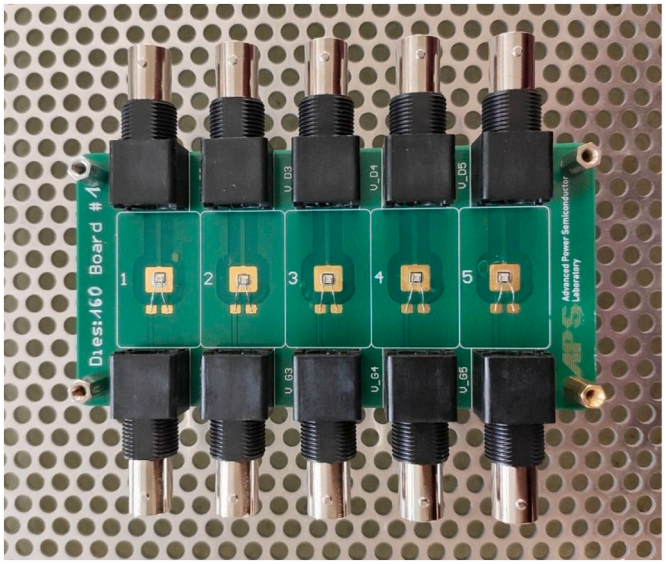

Fig. 4. Experimental board used at RADEF. Each board hosted five die, which were irradiated individually under vacuum. In the picture the die are from the 2nd generation Cree/Wolfspeed, rated for 1.2 kV and with $R_{DS(ON)} = 160$ mΩ. The BNC connectors allow to bias drain and gate and monitor the leakage currents (I_G and I_D).

Table 3
Results first experiment.

Ion	LET [MeV cm²/mg]	$V_{DS\ oxide\ l.\ d.}$ [a] [V]	$V_{DS\ degr.\ I}$ [a] [V]
$^{40}Ar^{+14}$	7.7	350–370	450
$^{56}Fe^{+15}$	14.6	80–100	300
$^{82}Kr^{+22}$	25.3	50–80	170
$^{131}Xe^{+35}$	49.1	50–60	120

[a] Fluence of 10^6 ions/cm².

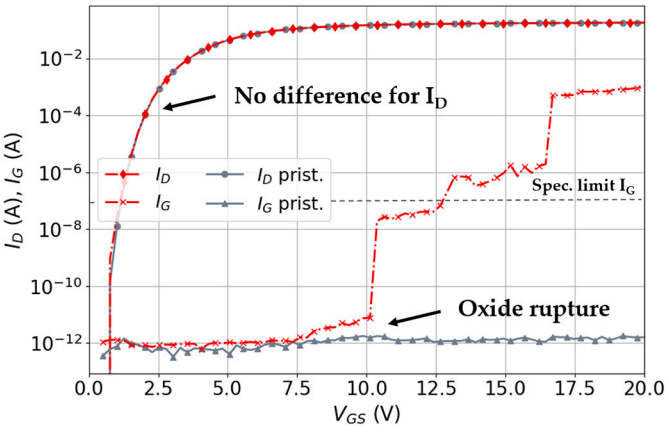

Fig. 5. I_DV_{GS} and I_GV_{GS} of a DUT exposed to $^{131}Xe^{+35}$ at $V_{DS} = 60$ V. No degradation was observed during exposure, but oxide breakdown occurred due to the latent damage during the PIGS test at $V_{GS} = 10$ V.

Table 4
Results second experiment.

Ion	LET [MeV cm²/mg]	ΔI_D [μA]	ΔI_G [μA]	$V_{DS\text{-}failure}$ [V]
$^{40}Ar^{+14}$	7.7	67.2	0	660
$^{56}Fe^{+15}$	14.6	75.1	0	580
$^{82}Kr^{+22}$	25.3	24.7	0	700
$^{131}Xe^{+35}$	49.1	27.4	0	620

(Finland). Two experiments were carried out in order to study the latent damage in the gate oxide and in the SiC crystal lattice. Ion broad beams from the 18 GHz Electron Cyclotron Resonance (ECR) ion source, HIISI [26], were used to irradiate commercial SiC MOSFETs. In both cases the irradiations were performed using the 16.3 MeV/amu heavy-ion cocktail, with $^{40}Ar^{+14}$, $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ as the ion species selected for the test. The whole die was homogeneously exposed. The beam characteristics are reported in Table 1. The LET as a function of the penetration range for the four ion species is graphically represented in Fig. 3, where the thickness of the epitaxial layer of the devices is highlighted.

2.2. Experimental setup

Bare die from the 2nd generation of Cree/Wolfspeed, rated for $V_{DS} =$ 1.2 kV were selected as devices under test (DUTs). Using bare die, the chip surface was directly exposed to the beam, allowing sufficient penetration of the heavy ions through the sensitive active layers of the device, without being stopped in the package materials [27]. The characteristics of the DUTs are listed in Table 2. The gate and source were connected by aluminum wire bonds with 300 μm wire diameter, while the drain connection was made by the soldered bottom pad. The source terminal was directly grounded on the board. Only two wires (gate and source) were used to minimize the shadowing effect. Each board hosted five die, which were irradiated individually in vacuum conditions. Two Keithley Source Measure Units (SMUs), models 2636 and 2410, were used to bias gate and drain through BNC connectors and monitor the gate and drain currents (I_G and I_D), respectively. A picture of the experimental board is shown in Fig. 4.

2.3. Plasma FIB-SEM analysis

A Tescan Xe plasma FIB-SEM model Fera3 was used for inspection of the damage site of the devices that failed due to the crystal latent damage. The configuration is such that the electron and ion beam focal points coincide, enabling simultaneous SEM imaging during FIB milling

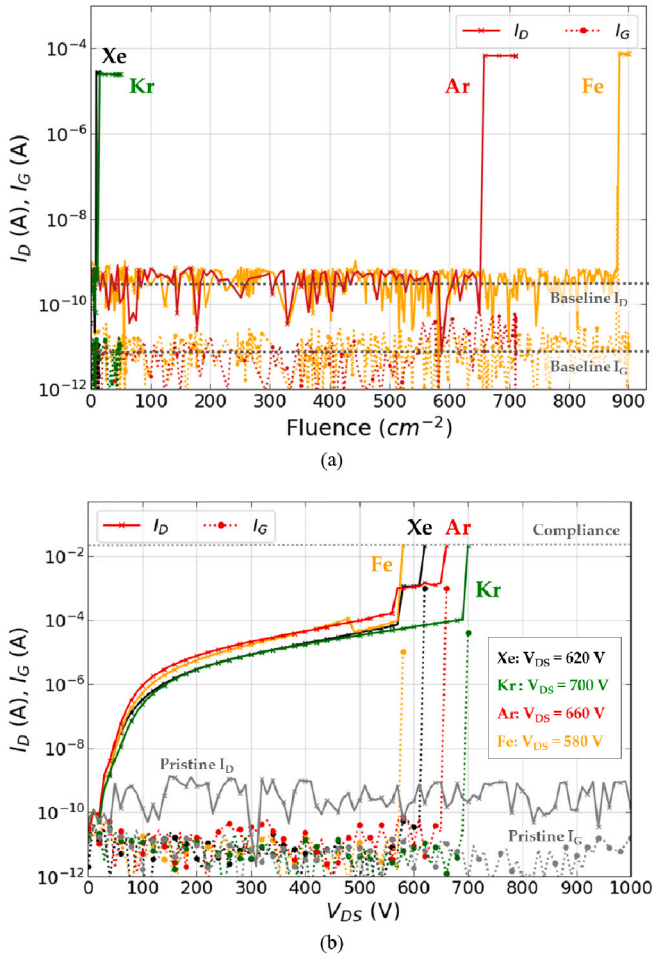

Fig. 6. Results from irradiations with $^{40}Ar^{+14}$, $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$ ions. a) First degradation step during the exposure at V_{DS} = 450 V. b) Post-irradiation V_{DS} sweep; all the devices failed at 580 V < V_{DS} < 700 V. The pristine I_D and I_G are shown in gray.

tasks with Xe plasma. In the SEM two types of signals can be detected; the secondary electrons (SE) and the backscattered electrons (BSE). The first provides information on the topography of the surface, whereas the second provides images that convey information on the sample composition.

3. Experimental results

3.1. Gate oxide latent damage

The first experiment was performed with the objective of investigating the latent gate damage as observed during the post-irradiation gate stress (PIGS) test for devices exposed in the pre-degradation region. Bare die with $R_{DS(ON)}$ = 160 mΩ (CPM2-1200-0160B) were irradiated at V_{DS} sufficiently low to protect from degradation, whereas the V_{GS} = 0 V, to force the DUTs in off-state. Each run was performed with a flux of 10^4 ions/(cm^2 s) and up to a fluence of 10^6 ions/cm^2. If the degradation was observed during the exposure (i.e., steps of I_D or I_G higher than 10 nA), the run was repeated with a pristine device decreasing the V_{DS} during the irradiation. After each run, the following measurements were performed:

- I_DV_{GS} and I_GV_{GS} with V_{GS} = [0 V − 20V] and V_{DS} = 0.1 V;
- I_DV_{GS} and I_GV_{GS} with V_{GS} = [0 V − (−5V)] and V_{DS} = 0.1 V;

where V_{GS} = − 5V/ + 20 V are the recommended operational values from the datasheet.

For each ion species, a range for the V_{DS} threshold was identified for the oxide latent damage, as reported in Table 3. The V_{DS} threshold is defined as the minimum bias at which no degradation is observed during the exposure, but the latent damage at the gate is sufficient to cause the oxide rupture during the PIGS test (i.e., V_{GS} = [0 V − 20 V]). For comparison, also the threshold voltages for degradation are reported. The latter were measured either during the current experiment, or during previous experiments with devices from the same generation [10,11]. The results from the run with $^{131}Xe^{+35}$ at V_{DS} = 60 V (and V_{GS} grounded) are shown as an example in Fig. 5. No degradation was observed during the exposure with a fluence up to 10^6 ions/cm^2, however the gate oxide failed at V_{GS} = + 10 V during the PIGS test, showing a gate latent damage induced by the ion-exposure. From the application point of view, the device is considered not operable anymore, as I_G > 100 nA, and therefore out of specifications.

3.2. Latent damage in SiC crystal lattice

The second experiment was performed with the objective of

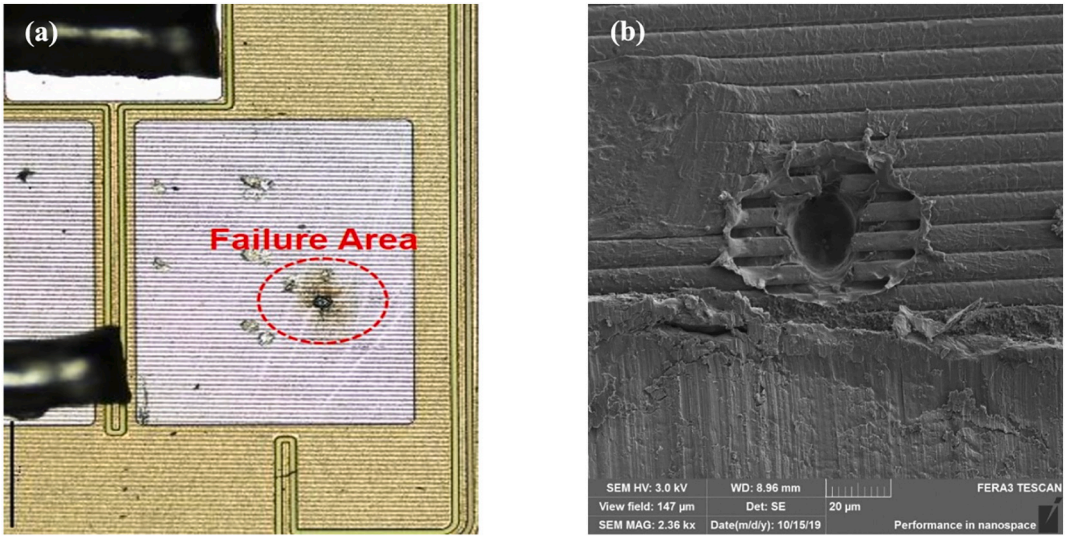

Fig. 7. Images of the failure are on the die surface obtained with (a) microscope and (b) SEM analysis measured with SE detector.

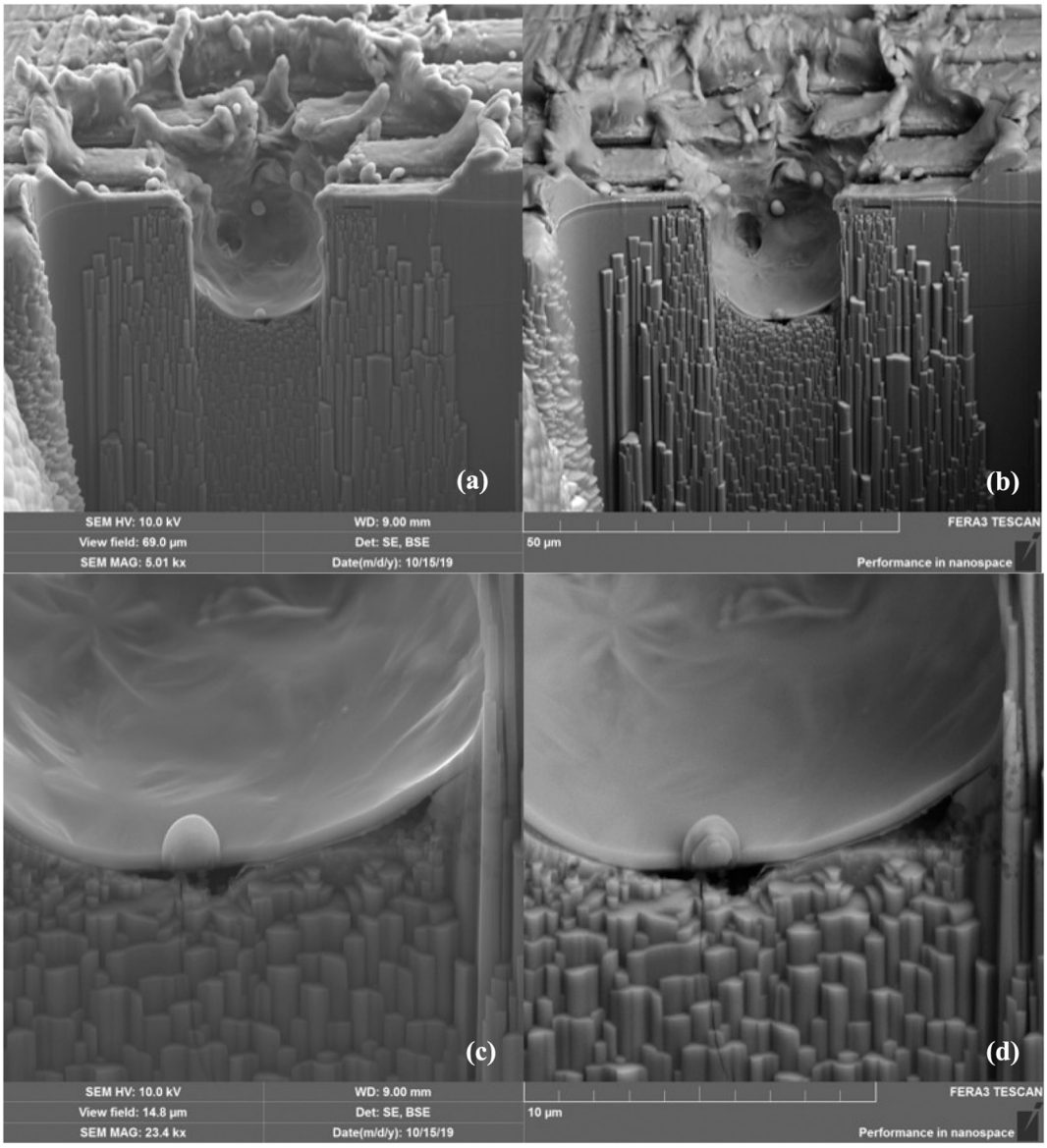

Fig. 8. In the top row: cross-section of the damaged area after FIB milling, measured with (a) SE and (b) BSE detectors. In the bottom row: magnified view of the hole showed in the previous images, measured with (c) SE and (d) BSE detectors.

investigating the latent damage in the SiC crystal lattice in the pre-SEB region. Bare die with $R_{DS(ON)}$ = 40 mΩ (CPM2–1200-0040B) were irradiated at V_{DS} = 450 V in order to protect from SEB (for these parts approximately at V_{DS} = 500 V with LET > 10 MeV cm^2/mg [13]) and V_{GS} = 0 V. A flux of few tens of ions/(cm^2 s) was used, and each die was exposed until the first radiation-induced step was observed. At this bias condition, the devices are experiencing the second type of degradation, which involves the p-n junction and the creation of EDs. The first degradation step was observed only in the I_D, which reached tens of µA, whereas the I_G remained in the order of magnitude of the pristine values. The I_D and I_G results are reported in Table 4 for four DUTs irradiated with $^{40}Ar^{+14}$, $^{56}Fe^{+15}$, $^{82}Kr^{+22}$ and $^{131}Xe^{+35}$. The same results are graphically represented in Fig. 6(a) as a function of the fluence during the exposure. The pristine values are reported for comparison in the same image (in gray). After the exposure, I_D and I_G were measured simultaneously using the same setup, having V_{DS} = [0 V − 1000 V] and V_{GS} = 0 V. As visible in Fig. 6(b), all four DUTs exposed at V_{DS} = 450 V failed during the post-irradiation V_{DS} sweep at voltage range of 580 V < V_{DS} < 700 V. The failure was defined as I_D = 20 mA, which is the level of the compliance. As visible in Table 4, in this case the failure voltage does not show a clear trend with the ion LET. This is probably caused by the different ion-strike position in the unit cell of the MOSFET.

3.3. Plasma FIB-SEM results

The damage site caused by the post-irradiation V_{DS} measurement was investigated using a plasma FIB-SEM analysis. The device analyzed was tested on a previous experiment performed with a microbeam as described in [10] but showed the same type of post-irradiation damage. The device was exposed to Ca ion (LET = 17 MeV cm^2/mg) with an accumulated fluence of 6 × 10^3 ions/cm^2. Initially, the failure area was identified using a microscope, as visible in Fig. 7(a). Fig. 7(b) shows a SEM image of the damage site on the die surface measured with SE detector. The hole generated by the failure extends over more than three gate stripes, for a length of ~30 µm and a width of ~20 µm. Fig. 8(a) and Fig. 8(b) show the cross-section of the hole after FIB milling, measured with SE and BSE detector, respectively. The hole has a depth of ~18 µm, and it extends over the entire epilayer (which has a depth from 5 µm to 18 µm). The image shows that the SiC crystal has decomposed, meaning that the localized temperature in the failure region reached the

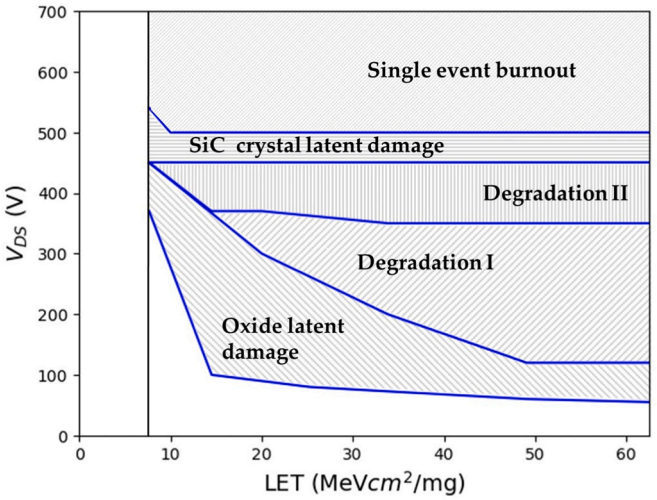

Fig. 9. Overview of the different types of damage induced by heavy-ion in SiC power MOSFETs as a function of the ion LET. The data were collected testing planar-gate MOSFETs from the 2nd generation Cree/Wolfspeed. The plot follows the representation as proposed in [10] for SiC diodes.

decomposition temperature of 4H SiC (3103 K ± at 35 atm [28]), and the materials in the layers above, which have a lower melting point, filled the hole. Fig. 8(c) and Fig. 8(d) are magnified views of the hole showed in the previous images, measured with SE and BSE detector, respectively. A crack which starts at the bottom of the hole is visible in both images. Finally, the vertical columns that appear in the cross-sections are artifacts due to the preparation of the sample.

4. Discussion

The heavy-ion-induced effects in the 2nd generation SiC MOSFET devices from Cree/Wolfspeed are graphically represented in Fig. 9 as a function of the ion LET and the V_{DS} during the exposure. The plot follows the representation as proposed in [17] for SiC diodes. The data were collected in the current work and previous ones [10,11] for devices irradiated in off-state. Five different regions of damage with the respective thresholds are identified.

A "hockey stick" trend is observed for all the effects, with the regions becoming narrower and the threshold voltages less distinguishable with decreasing LET. No data was collected for LET $<$ 7.7 MeV cm^2/mg, but eventually the ion damage is insufficient to induce degradation and latent damage, and the device directly experience SEB at higher bias.

At low drain-source bias, the first type of effect observed is the gate latent damage discussed in Section 3.1. The V_{DS} necessary to observe this effect is extremely low compared to the maximum rated voltage (less than a tenth). The threshold for this effect was identified for a fluence of 10^6 ion/cm^2. At higher bias, the heavy-ion exposure induces the first type of SELC, named "degradation I" in this graph, where the area underneath the gate oxide is the most sensitive (JFET region + channels). Increasing the voltage, the second type of SELC, labelled "degradation II", is observed. In this case the damage involves mostly the p-n junction region, but a smaller leakage remains also through the gate-oxide. This type of degradation involves damage in the SiC lattice and generation of EDs. The transition between the two types of degradation might vary between device generations and manufacturers, as recently reported in literature [5]. Furthermore, over a certain V_{DS} threshold in the pre-SEB region ($V_{DS} \geq$ 450 V in this case), a second latent damage involves the SiC crystal lattice which is altered by the presence of EDs. After the irradiation, when drain-source bias is applied, the localized power density induces an increase of local temperature, which ultimately causes the decomposition of the SiC crystal and the creation of a crater, as described in Sections 3.2 and 3.3. Finally, for higher voltages, the device experiences directly a destructive SEB, as reported in [13] for $V_{DS} >$ 500 V and LETs $>$ 10 MeV cm^2/mg.

This graph can be used as a qualitative baseline also for other devices with a planar gate. However, since in this work all the heavy-ions experiments were performed using planar MOSFETs from Cree/Wolfspeed and considering that design and carrier concentrations vary between device types and manufacturers, the results cannot be transferred to all SiC power devices without further analysis.

5. Conclusions

The wide-bandgap SiC power MOSFETs have emerged as the most viable alternative to Si for high-efficiency and high-power density applications. The advantages of SiC make this technology desirable also for space, avionics and high-energy accelerator industries. However, the adoption in these fields is still hindered by the susceptibility to SEEs. In addition to the leakage current degradation and SEB effects, this work highlighted that commercial SiC power MOSFETs are also sensitive to two types of latent damage when exposed to heavy ions. These effects can affect the long-term reliability of the parts and should be considered when performing a test campaign.

The first mechanism involves the pre-degradation region and the gate oxide, causing the failure of the devices during the post-irradiation gate stress (PIGS) tests. The sensitivity for this type of latent damage was presented for different ion LET, identifying a safe operation area for a fluence of 10^6 ion/cm^2.

The second latent damage is observed in the pre-SEB region, and it involves the decomposition of the SiC crystal lattice as confirmed by the SEM-FIB images.

Finally, an overview of the different heavy-ion effects in SiC MOSFETs was presented, highlighting the regions of risk for SEEs and latent damages as a function of the ion LET and operational bias.

CRediT authorship contribution statement

C. Martinella: Term, Conceptualization, Methodology, Software, Validation, Formal analysis, investigation, Data curation, Writing - Original draft, Writing - Review & editing
P. Natzke: Investigation, Resources, Writing - Review & editing
R. G. Alia: Conceptualization, Writing - Review & editing, Supervision, Project administration, Funding acquisition
Y. Kadi: Conceptualization, Writing - Review & editing, Supervision, Project administration, Funding acquisition
K. Niskanen: Methodology, Investigation, Resources, Writing - Review & editing
M. Rossi: Resources, Writing - Review & editing
J. Jaatinen: Resources, Writing - Review & editing
H. Kettunen: Resources, Writing - Review & editing
A. Tsibizov: Methodology, Validation, Writing - Review & editing
U. Grossner: Term, Conceptualization, Writing - Review & editing, Supervision, Funding acquisition
A. Javanainen: Term, Conceptualization, Investigation, Writing - Review & editing, Supervision, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare no conflict of interest for the following work: "Heavy-ion induced single event effects and latent damages in SiC power MOSFETs".

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