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Ion-Induced Energy Pulse Mechanism for Single-Event Burnout in High-Voltage SiC Power MOSFETs and Junction Barrier Schottky Diodes

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***Abstract*- Heavy ion data suggest that a common mechanism is responsible for single-event burnout in 1200 V power MOSFETs and junction barrier Schottky diodes. Similarly, heavy ion data suggest a common mechanism is also responsible for leakage current degradation in both devices. This mechanism, based on ion-induced, highly-localized energy pulses, is demonstrated in simulations and shown to be capable of causing degradation and single-event burnout for both the MOSFETs and JBS diodes.**

***Index Terms*- Silicon Carbide, SiC, power, MOSFET, diode, heavy ion, single-event burnout, SEB, degradation**

I. Introduction

Silicon carbide (SiC) is superior to silicon for use in many power device applications. SiC power devices have higher breakdown electric fields and thermal conductivity, with significantly lower on-state resistance [1]. SiC devices can provide high voltage, high power-density power solutions for a variety of applications, both at ground level and in space. However, SiC power MOSFETs and junction barrier Schottky (JBS) diodes are both susceptible to heavy-ion irradiation [2-7], including device degradation due to increased leakage currents as well as single-event burnout (SEB).

It has generally been thought that there are separate mechanisms responsible for the catastrophic failures observed in silicon power diodes (localized avalanche breakdown due to ion-induced electric field spikes) and silicon power MOSFETs (parasitic bipolar junction transistor) [8]. A natural assumption is that separate mechanisms are also responsible for SEB in SiC power diodes and MOSFETs. However, the data presented in Figure 1 show that 1200 V SiC power MOSFETs and 1200 V JBS diodes from Wolfspeed [9-12] have the same SEB threshold (bias at which SEB may occur) as a function of ion LET. The devices also show the same degradation threshold (bias at which the device off-state leakage current begins to increase) as a function of ion LET [2,3,6,7].

SEB in silicon power MOSFETs has been linked to the parasitic bipolar junction transistor, which is an integral part of the device structure [13]. Some success has been achieved in simulating SEB in SiC power MOSFETs by assuming that impact ionization, coupled with the parasitic bipolar junction transistor, results in a positive-feedback loop during an ion event causing SEB [9]. However, power diodes do not have a positive-feedback loop related to a parasitic bipolar structure, suggesting that there is another mechanism responsible for SEB.

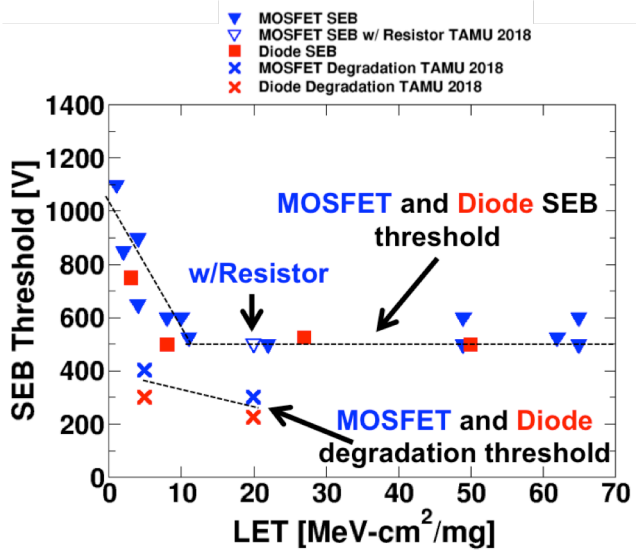

Figure 1: Single-event burnout threshold bias voltages vs. LET for 1200 V SiC power MOSFETs and diodes [8-11]

In this paper, ion-induced, highly-localized energy pulses are proposed as a common mechanism responsible for catastrophic SEB in 1200 V SiC power MOSFETs and JBS diodes, with lower magnitude energy pulses responsible for degradation. Analysis of heavy-ion data indicates that the devices have matching

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SEB thresholds suggesting that there is a common mechanism responsible for the catastrophic failures. Similarly, the devices have matching degradation thresholds suggesting a common mechanism responsible for degraded performance. 3D TCAD simulations are used to identify similarities in both structures during an ion event showing a resistive shunt effect capable of generating very high localized current transients, and consequently, significant energy dissipation. For LET and bias conditions matching the SEB threshold data, a constant amount of energy dissipation is calculated through analysis of TCAD simulation results. Similarly, a constant amount of energy dissipation is calculated for conditions matching the degradation threshold data. These extreme energy pulses may exceed the capabilities of the semiconductor or the metal-semiconductor interface, leading to degradation or SEB.

II. Heavy Ion Data

Heavy ion data for SiC MOSFETs from Wolfspeed, the C2M0080120D (1200 V, 80 mΩ) and SiC JBS diodes from Wolfspeed, the C4D020120A (1200 V), showing SEB threshold as a function of ion LET are given in Figure 1 [9-12]. New data are presented for the MOSFETs taken at Texas A&M University Cyclotron (TAMU) using a non-destructive test technique in an attempt to suppress SEB. The LET considered is 20 MeV-cm^2/mg at normal incidence, and the device was at room temperature. A resistor was inserted inline between the power supply and the drain node in an attempt to limit current and allow the drain node voltage to drop below critical levels required for SEB. The data shown in Figure 1 indicate that this test technique was not effective in suppressing SEB using a 100 kΩ resistor (for LET = 20, SEB occurred at the same voltage, with or without the resistor). Similar data were presented previously, indicating that inserting a 1 MΩ resistor inline with the drain of a 1200 V SiC power MOSFET had little to no impact on ion-induced degradation in the device [14]. All data presented in this work are for heavy ions at normal incidence, however SiC power devices have a significant SEB dependence on angle [15,16], and while angular effects are not analyzed in this work, it is important to remind the reader that heavy ions at normal incidence are the worst case.

Table 1: Parameters used in TCAD simulations for the MOSFET and Diode

Parameter	Value
4H-SiC	Bandgap=3.26 eV
N-Epi Doping/Depth	10^{15} cm^{-3}, 10 µm
Body Doping/Depth	10^{19} cm^{-3}, 1 µm
N+ Drain Doping	10^{19} cm^{-3}
Ion Track Radius/Length and Gausian time profile	50 nm, 15 µm, 2ps
Impact Ionization Model	Anisotropic Avalanche - Okuto

III. Bias-Induced Avalanche For Electrical Breakdown

3D TCAD models of a 1200 V SiC power MOSFET and JBS diode, Figure 2, were developed in the Synopsys Sentaurus suite of TCAD tools, version K-2015.06, [17], based on information from published literature [9,10,18]. The devices have an epi thickness of 10 µm, with doping in the mid-10^{15} cm^{-3} range, with an additional 15 µm of highly-doped drain (the highly-doped drain is truncated in Figure 2 for visualization purposes). Otherwise, the models shown in Figure 2 are to-scale, with the thickness of the epitaxial region indicated for guidance. Additional parameters are listed in Table 1. The JBS diode has been designed in such a way that the device can operate as a p-i-n diode when reverse-biased, and as a Schottky diode when forward-biased [19]. Consequently, the diode and the MOSFET surface structure are nearly identical, as seen in Figure 2.

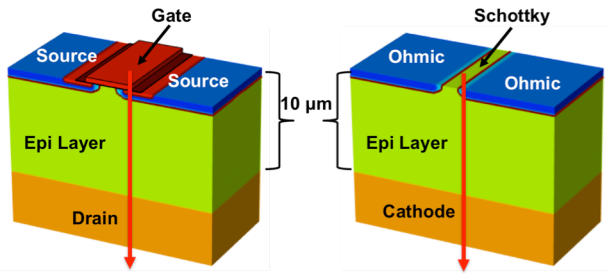

Figure 2: 3D TCAD model of a 1200 V SiC power MOSFET (left) and JBS diode (right) showing device structure (epi doping/depth). Also shown is a long-range ion track in a channel strike location.

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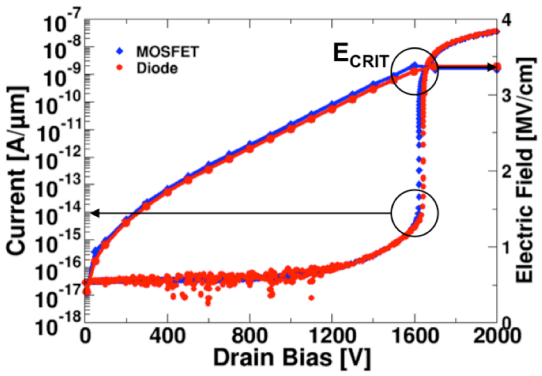

Figure 3: 3D TCAD-simulated electrical avalanche breakdown for 1200 V SiC power MOSFET and diode (left y-axis) and peak electric field (right y-axis).

3D TCAD electrical breakdown simulation results are shown in Figure 3 for the power MOSFET and JBS diode. Both devices were simulated in a reverse-bias condition up to 2000 V, and the simulation results in Figure 3 show that both devices enter avalanche breakdown with approximately the same current and voltage relationships. The peak electric field as a function of position in each device is also shown in a 2D-cutline in Figure 4, and when this field reaches approximately 3.2 MV/cm, defined as E_{CRIT}, avalanche breakdown can occur, and is consistent with ranges of electric field required for avalanche breakdown in 4H-SiC [20]. As the bias increases, the entire n-drift region (epitaxial layer, or epi) becomes depleted, and with no additional area for the depletion layer to grow, the electric fields at the corners of the p-regions increase rapidly, shown in Figure 4 just as the devices enter avalanche breakdown at 1600 V. The key feature is the similarity of the surface structure in both devices, with each having a p-body region that terminates under either the gate metallization (MOSFET) or the Schottky barrier (JBS diode). The p-region design results in a lateral p-dopant roll-off, with a sharp corner, where the electric field is the strongest. This high electric field region is where avalanche breakdown occurs. 1D-cutlines for the internal device potential and electric field are shown in Figure 5. The potential drops smoothly over the entire epitaxial region, and the electric field curves show the classic triangular shape described by Poisson's equation, governed by the doping and potential.

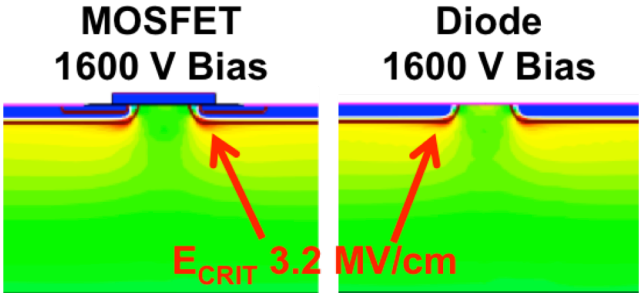

Figure 4: 2D-cutline in TCAD showing electric field at the p-body/n-epi junction reaching E_{CRIT} 3.2 MV/cm (red region) at 1600 V on the drain contact for 1200 V SiC power MOSFET (left) and diode (right). The electric field in the epi-region is 1-2 MV/cm (green region)

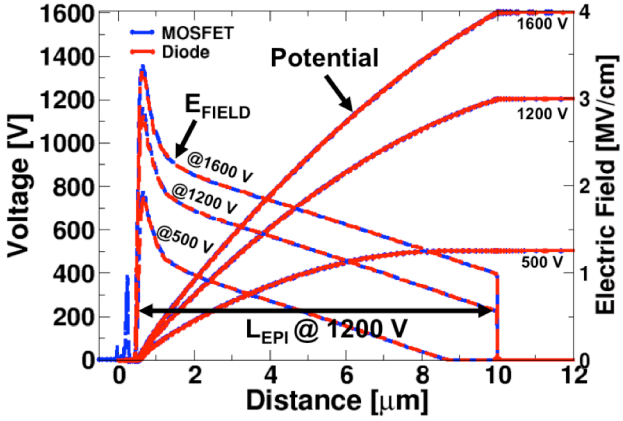

Figure 5: 1D-cutline of the internal device potential (left y-axis) for 1200 V SiC power MOSFET and diode (left y-axis) and peak electric field (right y-axis).

In a typical power device calculation for equilibrium conditions, the resistance of the epitaxial layer can be described by Equation 1 as:

$$R_{EPI} = \rho * \frac{L_{EPI}}{A_{EPI}} \quad (1)$$

where ρ is the conductivity and L_{EPI} and A_{EPI} are the thickness of the epitaxial layer and cross-sectional area of the device, respectively. In the 1200 V SiC power devices, L_{EPI} is approximately 10 μm, which is shown in Figure 5 as the distance where the majority of the potential is dropped, or the area underneath the sloping electric field. This region is extremely important during an ion strike as it relates to the magnitude and location of total energy dissipation during the event, and is discussed in more detail in Sections IV and V.

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IV. Ion-Induced Resistive Shunt

An ion deposits energy in a semiconductor device by generating electron-hole pairs. At very short times, the ion track has an extremely high density of electrons and holes, and acts as a shunt, or low resistance path, between two regions [21-23]. In a vertical power MOSFET, an ion strike at normal incidence can create a shunt between the source and the drain. In a power JBS diode, the shunt is between the anode and the cathode. The low resistance path of the shunt results in a localized current spike for the device, and is illustrated in Figure 6 using 3D TCAD simulation results for an ion with LET = 10 MeV-cm^2/mg and a drain bias of 500 V for both the 1200 V SiC power MOSFET and the 1200 V JBS diode. For approximately 100 ps after the ion strike occurs, the current transients for both devices behave identically, while at longer time scales they begin to deviate.

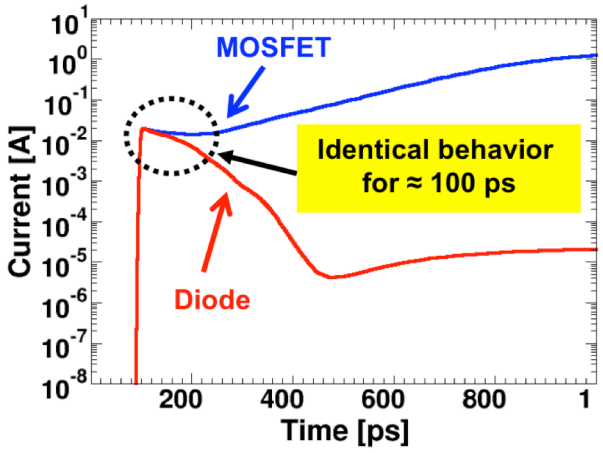

Figure 6: Ion-induced current transient for a 1200 V SiC power MOSFET and diode for particle with LET=10 MeV-cm^2/mg and 500 V drain bias.

Previous work [9,24] discusses the role of a parasitic bipolar junction transistor in the power MOSFET. Avalanche breakdown, coupled with a parasitic BJT in a positive feedback loop in the MOSFET, is suggested as the reason for the simulated runaway drain current. However, the JBS diode has no such parasitic structure, and at longer times, the charge from the ion is collected or recombines and the device appears to recover in simulation. Yet the heavy ion data presented in Figure 1 show that the the SiC power MOSFETs and diodes have matching SEB thresholds, suggesting that there is a common mechanism responsible for the failures. Further, the common mechanism likely occurs at short times on the order of picoseconds, shown by simulation to be the timeframe in which the MOSFET and diode behave similarly.

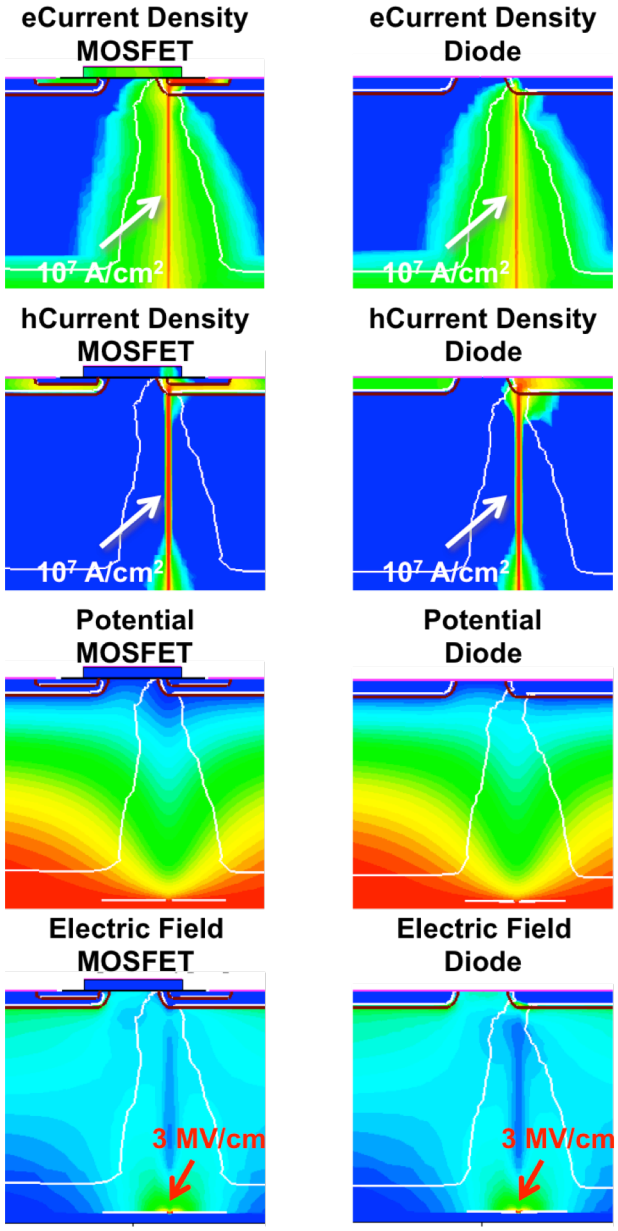

Figure 7: 2D-cutline in TCAD showing electron and hole current densities exceeding 1x10^7 A/cm^2 and electric fields exceeding 3.2 MV/cm for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 2D-cutlines taken at 5 ps following the ion strike.

The ion-induced effects can be seen in Figure 7 as a series of 2D-cutlines for the MOSFET and JBS diode at 5 ps after the strike has occurred. Electron and hole current densities are on the order of 1 × 10^7 A/cm^2 at 5 ps after the strike has occurred (current densities fall off to 1 A/cm^2 approximately 3μ away from the ion core for electrons and a few hundred nanometers for holes). The ion-induced redistribution of the electrostatic potential and the electric fields are also shown in Figure 7, with 1D-cutlines taken along the center of the ion track, shown in Figure 8, to establish a quantitative measure in

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lieu of a colored legend. The ion strike is centered above the corner of the p-region, where the pre-strike maximum electric field is located [9,18]. This point in time, 5 ps, corresponds to the peak current transient shown in Figure 6, which is identical for both the MOSFET and JBS diode. For both devices, the peak electric field immediately after the ion strike is approximately 3.2 MV/cm, which is the critical electric field (E_{CRIT}) determined from simulation required for avalanche breakdown shown in Section III. The ion strike redistributes the potential in a way that leads to avalanche breakdown. This can be seen in greater detail through 1D-cutlines, taken along the center of the ion track, shown in Figure 8, which compares the pre- and post-strike electric fields and potentials. This effect has also been discussed for silicon power DMOSFETs [25].

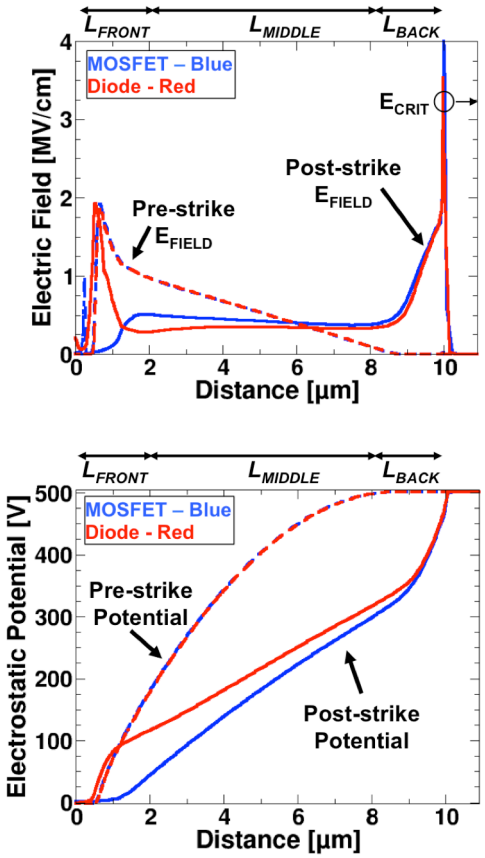

Figure 8: 1D-cutline in TCAD showing pre- and post-strike electric fields exceeding 3.2 MV/cm (top) and pre- and post-strike potential (bottom) for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

At this point in time, the charge deposited by the ion has generated a low-resistance path, or shunt, through the MOSFET and JBS diode. However, this low-resistance path is not a linear resistor over the entire epitaxial region; rather, three distinct conductive regions have developed due to non-equilibrium conditions and each region can be defined in terms of length in Equation 2 as:

$$L_{EPI} = L_{FRONT} + L_{MIDDLE} + L_{BACK} \quad (2)$$

with L_{BACK} shown in Figure 8 as the region with the greatest peak electric field and gradient (greatest change in potential), located near the junction where the lightly-doped epitaxial layer meets the highly-doped drain. The surface region, defined as L_{FRONT}, also shows a sharply peaked electric field and gradient. However, the middle of the epi region, defined as L_{MIDDLE}, has a significantly lower electric field and very low gradient (small change in potential). This results in three distinct regions, defined by the rate of change of electric field, for power dissipation (current density times electric field), as shown in Figure 9. The cumulative power density curve, also shown in Figure 9, indicates that approximately 40% of the power is dissipated in the region defined as L_{BACK} (2 μm) and 15% in the region defined as L_{FRONT} (1 μm), with only 35% attributed to the region of L_{MIDDLE} (7 μm).

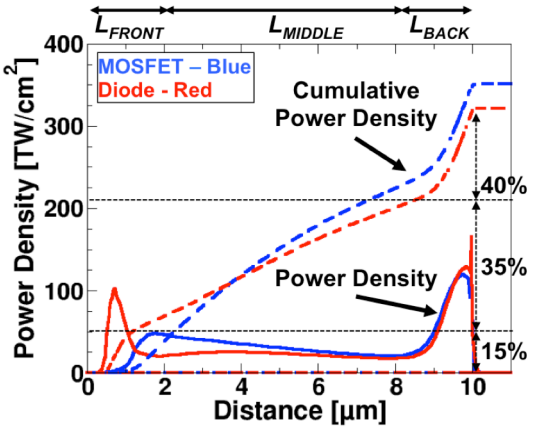

Figure 9: 1D-cutline in TCAD showing post-strike power density and cumulative power density for a particle with LET = 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

V. Analysis of Ion-Induced Energy Pulse Mechanism for SEB and Degradation

Power MOSFETs and diodes are designed specifically to block high voltages in the off-state and conduct high currents in the on-state. In normal operation, high current and high voltage do not exist at the same time (at least not for very long!). During an ion-initiated event, the device begins with high voltage dropped across it and the ion increases the current, possibly leading to excessive power dissipation. TCAD simulations are used to generate power density curves for a range of ion LETs

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and device biases, for both the MOSFET and JBS diode, with examples shown in Figure 10 comparing two LET values at a fixed bias. The power density vs. position curves for both the MOSFET and diode exhibit the same overall shape in all cases, however, the magnitude of the power density increases with increasing LET and bias.

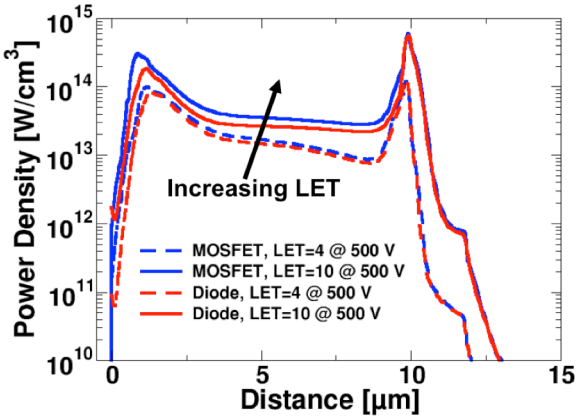

Figure 10: 1D-cutline in TCAD showing post-strike power density and cumulative power density for a particle with LET = 4 and 10 MeV-cm^2/mg with 500 V drain bias. 1D-cutlines taken at 5 ps following the ion strike.

This sensitivity can be more easily analyzed by integrating the power density spatially across the entire epi region of the ion track and temporally to determine the amount of energy dissipated during each event using Equation 3:

$$Energy \approx \iint J * A_{ION} * E_{FIELD}\ dx\ dt \quad (3)$$

where J is the current density, and A_{ION} is the area of the ion track. The calculated energy during each event is shown in Figure 11.

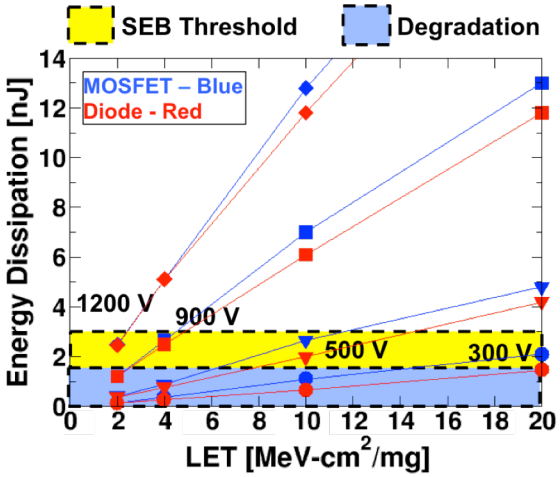

Figure 11: TCAD calculated energy dissipation for 10 ps following the strike with the SEB$_{TH}$ conditions highlighted.

For bias and LET conditions consistent with the experimentally-determined SEB thresholds shown in Figure 1, the energy dissipated during the 10 ps immediately following the event ranges from 2-3 nJ, as shown in Figure 11 (depicted by the yellow region). For example, an ion strike for LET = 2 MeV-cm^2/mg and 1300 V results in 2.5 nJ/2.4 nJ in the MOSFET/JBS diode, while LET = 10 MeV-cm^2/mg at 500 V results in 2.6 nJ/2nJ in the MOSFET/JBS diode. For events that are above the SEB threshold, more energy is dissipated, and for events that are below the SEB threshold, less energy is dissipated (blue region in Figure 11). For events that occur at bias and LET conditions consistent with experimentally-determined degradation threshold, the result is virtually identical to the SEB analysis, just lower in magnitude, suggesting that SEB is a more catastrophic form of degradation. In all cases, this energy dissipation occurs over 10 ps, which is a very short time, considering that power devices have switching speeds on the order of microseconds. Also in all cases, both the MOSFET and the JBS diode behave almost identically.

Due to the short timeframes of ion-induced transients, experimentally measuring this effect is challenging. For example, a typical avalanche stress test pulses a device with current transients lasting tens of microseconds, compared to ps-ns timeframes for single events. A non-destructive test technique of inserting a resistor inline with the drain node was not effective for mitigating SEB in these devices, as shown in Figure 1, as well as in other work [14]. Due to the time constant of the circuit, if the SEB failures resulting from transients occur on the order of nanoseconds to microseconds, then inserting a resistor should have provided some protection.

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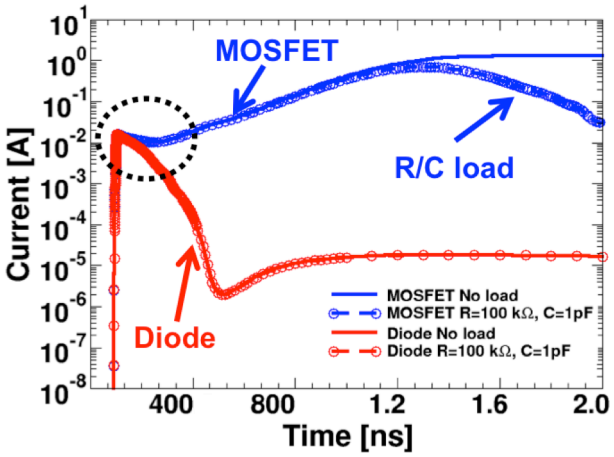

Figure 12: TCAD mixed-mode ion-strike simulations for both the MOSFET and JBS diode using non-destructive technique for adding a resistor inline with the power supply. Ion LET=10 MeV-cm^2/mg and devices biased at 500 V.

3D TCAD mixed-mode simulations indicate that this technique works as designed for the MOSFET, shown in Figure 12, provided that the device can survive at least a nanosecond following the ion strike. The inline resistor has allowed the bias across the device to decrease, effectively decreasing both avalanching and parasitic BJT responses, and the MOSFET drain current shows a recovery. However, for time scales on the order of tens of picoseconds, the simulated ion-induced current pulse is identical for both the MOSFET and diode, independent of the inline resistor. As noted above, data shows no impact on SEB by adding an inline resistor. Thus, data shown in Figure 1 and in other work [14], combined with TCAD simulations, indicate that the inline resistor provides no benefit and confirms that damage is occurring faster than the time constant of the device. The response time of the R/C loaded circuit is far too slow to suppress the energy pulses that result in catastrophic SEB or degradation.

VI. Conclusions

Ion-induced, highly-localized energy pulses are proposed as a common mechanism responsible for catastrophic SEB in 1200 V SiC power MOSFETs and JBS diodes, with lower magnitude energy pulses responsible for degradation. Analysis of heavy-ion data indicates that these devices have matching SEB thresholds suggesting that there is a common mechanism responsible for the catastrophic failures. Similarly, the devices have matching degradation thresholds suggesting a common mechanism responsible for degraded performance. 3D TCAD simulations are used to identify similarities in both structures during an ion event showing a resistive shunt effect capable of generating very high localized current transients, and consequently, significant energy dissipation. For LET and bias conditions matching the SEB threshold data, a constant amount of energy dissipation is calculated through analysis of TCAD simulation results. Similarly, a constant amount of energy dissipation is calculated for conditions matching the degradation threshold data. These extreme energy pulses may exceed the capabilities of the semiconductor or the metal-semiconductor interface, leading to degradation or SEB.

While these results are focused specifically on 1200 V SiC power MOSFETs and JBS diodes, similar analyses may be useful for other materials (silicon, GaN) and for other device architectures (lateral, trench, super-junction, etc). Under a given set of conditions for device bias and ion energy, electric field perturbations that result in internal electric fields reaching, or exceeding, the critical field required for avalanche breakdown may result in conditions that are catastrophic for power devices. Understanding the sensitivities of a specific device material and architecture to these parameters is important for being able to describe failure mechanisms resulting from heavy ion exposure.

VII. Acknowledgements

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