STUDIES OF TWO-DIMENSIONAL AND THREE-DIMENSIONAL PHONONIC CRYSTAL STRUCTURES

BY

YAOLAN TIAN

Academic Dissertation
for the Degree of
Doctor of Philosophy

*To be presented, by permission of the
Faculty of Mathematics and Science
of the University of Jyväskylä,
for public examination in Auditorium Fys-1 of the
University of Jyväskylä on September 2, 2016
at 12 o'clock noon*

Jyväskylä, Finland
September, 2016

Preface

The work presented in this thesis has been carried out at the Department of Physics and Nanoscience Center at the University of Jyväskylä.

Jyväskylä, September 2016

Yaolan Tian

Abstract

This thesis focuses on studying phononic crystal structures. More specifically, it is aimed at fabrication and measurement of thermal properties of two-dimensional (2D) periodic microstructures and three-dimensional (3D) nanostructures. There is great interest in understanding, manipulating and considering application perspective of minimizing of thermal transport in periodic structures. Periodic structures have been studied more on their optical properties, but this thesis places emphasis on their application of manipulating heat.

A process of fabricating two-dimensional hole array phononic (2D PnC) structures is described here. It consists of membrane preparation, superconductor-insulator-normal metal-insulator-superconductor (SINIS) tunnel junction fabrication and etching of 2D PnC structures. Simple square array geometries of periods 4, 8, 16 μm were fabricated, keeping filling factor of holes as 0.7. Thermal conductance of phononic structures with the three different periods were measured and compared with uncut membranes at temperatures from 50 mK to 1.2 K. All PnC structures gave a lower thermal conductance than membrane. In addition, thermal conductance was measured on membranes by different types of SINIS junction pairs. The variables were the geometry, the normal metal material and the normal metal length, which all affected the measured result. It is thus important to keep the SINIS heaters and thermometers the same when studying thermal conductance and its dependence on the period of the PnC structure. Additionally, sometimes superconductor-normal metal-superconductor (SNS) junction pairs were accidentally made. Thermal conductance measured using a SNS structure as a heater and SINIS structure as a thermometer is

also shown.

We also address the fabrication of 3D colloidal polystyrene(PS) nano-sphere PnC structures on plain chips and the statistics of the deposition process, self-assembly by vertical dipping. Combinations of dipping angle of 45° and 90°, withdrawal speed of 0.01 mm/min to 0.05 mm/min and nano-sphere colloidal solution concentration of 0.02%, 0.2%, 2%, 5% and 10% were studied. Colloidal 3D PnC structure of face-centered cubic (fcc) crystal domains were self-assembled. Silicon chips with etched microscale boxes were fabricated and dipped vertically into 10% concentration PS colloidal solution at withdrawal at speed of 0.01 mm/min to 0.04 mm/min. Lower speed, higher concentration and 90° vertical dipping produce larger 3D PnC domain sizes on average. It was found that one big domain could fill a 20 μm deep confined box no larger than 200 μm length. However, there were always cracks between the domains and the edges of the box. Therefore, a polymer box was developed and used instead as a confinement box. It was fabricated by three dimensional lithography (3DL), using two types of resist: IPL 780 and IPDIP. Glass substrates with 10 μm high IPL780 resist polymer boxes of hollow area of 100 μm × 100 μm were dipped into a solution of 0.5%, 1% and 2% concentration of 260 nm diameter polystyrene nano-spheres at withdrawal speed of 0.01 and 0.02 mm/min. Only the sample with 1% concentration at withdrawal speed of 0.01 mm/min gave good results. There were no PS nano-sphere self-assembled on top of IPL780 box. However, there were several domains inside one box. So, a 20 μm high polymer box of 50 μm × 50 μm area was fabricated on silicon chips. They were dipped into a PS nano-sphere solution of 1%, 2 % and 5 % concentration at the speed of 0.01 mm/min. Finally, a method was also developed to protect PS colloidal PnC structures from deformation and dissolution. As expected, there was only one domain inside the box formed from the concentration of 1%. Unexpected, there were PS nano-spheres also on top of the sides of IPDIP boxes. PnC structures were treated by e-beam irradiation and protected by a capping layer of AlO$_x$. Aluminum wires were successfully deposited on top of the PnC structures, which is promising for mounting thermal conductance measurement devices on top.

Author's address   Yaolan Tian
                         Department of Physics
                         Nanoscience Center
                         University of Jyväskylä
                         Finland

Supervisor   Professor Ilari Maasilta
                         Department of Physics
                         Nanoscience Center
                         University of Jyväskylä
                         Finland

Reviewers   Dr. Pierre-Olivier Chapuis
                         Centre d'Energétique et de Thermique de Lyon
                         CNRS
                         INSA de Lyon
                         France

                         Dr. Karwan Rostem
                         NASA Goddard Space Flight Center
                         John Hopkins University
                         USA

Opponent   Professor Karl Joulain
                         Université de Poitiers
                         France

List of Publications

The main results of this thesis have been reported in the following articles:

A.I. Y.-L. TIAN, T. PUURTINEN, Z. GENG, I.J. MAASILTA, *Minimizing thermal conductance by controlling the periodicity of two-dimensional phononic crystals*. manuscript.

A.II. Y.-L. TIAN, T. J. ISOTALO, MIKKO P. KONTTINEN, J.-W. LII.J. MAASILTA, *Intregrating metallic wiring with three-dimensional polystyrene colloidal crystals using electron-beam lithography and three-dimensional laser lithography*. submitted.

A.III. I.J. MAASILTA, T.A. PUURTINEN, Y.-L. TIAN, Z. GENG, *Phononic Thermal Conduction Engineering for Bolometers: From Phononic Crystals to Radial Casimir Limit*. J. Low Temp. Phys. **184** 211-216 (2016).

A.IV. T. J. ISOTALO, Y.-L. TIAN, MIKKO P. KONTTINEN, I.J. MAASILTA, *Statistical characterization of self-assembled colloidal crystals by single-step vertical deposition*. Colloid. Surface. A**443** 154-170 (2014).

A.V. T. J. ISOTALO, Y.-L. TIAN, I.J. MAASILTA, *Fabrication and Modelling of Three-Dimensional Sub-kelvin Phononic Crystals*. J. Phys.:Conf. Ser. **400** 052007 (2012).

Author's contribution

The author of this thesis has written first drafts of article A.I and A.II. The author is totally responsible for the fabrication samples for articles A.I, A.III, A.IV, and A.V and most parts the fabrication sample in article A.II. The author has measured all of the data in A.I and A.III. The author is responsible for the data analysis in article A.I and partly responsible article A.II.

Contents

Chapter 1

Introduction

A phononic crystal (PnC) is analogous to a photonic crystal, where instead of a periodic dielectric constant one has periodic material density and elasticity. This can lead to complete bandgaps of certain frequencies due to Bragg interference [1, 2]. Because of technical limitations, early experimental studies of PnCs were focused on macroscopic systems with millimeter-scale periodic structures, whose dominant frequency are sonic or ultrasonic waves in MHz frequency range [3]. Typical applications for such structures are acoustic filtering, wave-guiding or focusing [3, 4]. Recent improvements in nano-fabrication technologies enabled people to create micro- and nano-scale periodic structures as small as the characteristic wavelength of GHz frequency hypersonic waves [5, 6], where applications are in RF communication technologies [7]. However, there is not so much work on thermal properties of micro- and nano-scale phononic structures, especially at sub-kelvin temperatures. It is significant to control thermal transport, which can improve or decrease heat dissipation out of devices and increase the sensitivity of bolometric detectors [8]. Controlling thermal transport has previously been achieved by tuning the scattering of phonons by including various types of scattering centers in the material, such as nano-particles and impurities [9, 10]. It can, however, also be achieved by with the help of periodic phononic crystal (PnC) structures [11--15]. At low temperatures, the PnC device coherently modifies the phonon band structure, which was demonstrated for the first time both theoretically and experimentally in Ref. [16]. In this thesis, two-dimensional holey phononic crystal (2D PnC) structures of periods 4, 8, and 16 μm were fabricated on 300 nm thick SiN$_x$ membranes with a hole filling factor of 0.7, and their thermal conductance was measured below 1 K. The result shows in contrast to the theory [17] that the thermal conductance does not decrease all the way, as the period increases. In addition, many types of SINIS junctions were fabricated on uncut membranes to improve the fabrication. Thus, comparison was also done

for thermal conductance measured by different types of SINIS junction pairs heaters and thermometers. Differences were observed due to the ballistic nature of transport. This means that the SINIS junction pairs should be kept the same when comparing results of PnCs and membranes.

Self-assembled structures of mono-disperse spherical particles have successfully been used for fabrication of three-dimensional (3D) photonic crystals [18--20]. Another application for 3D self-assembled colloidal crystals is in phononic crystals, which can have potential applications such as thermal isolation and phononic waveguides [21]. 3D Phononic crystals with 100 nm scale dimensions produce phononic band gaps in the GHz range [6]. Polystyrene (PS) nano-spheres of about 100 nm size range are thus an option for fabrication of GHz bandgap phononic crystals. Self-assembled colloidal crystals of PS nano-spheres were fabricated on silicon nitride (SiN_x) substrates coated with titanium oxide (TiO_x) using the vertical deposition method [18, 22--24]. In most cases, the investigation of thermal properties of nano-scale structures requires the integration of lithographically fabricated metallic thermometers and heaters into the phononic crystal structure [25]. Integrating these devices on top of the 3D colloidal crystal surfaces is challenging. Some problems were solved by us. For example, by hardening the PS spheres by cross-linking the polymers using high doses of electron-beam irradiation, combined with the evaporation of an aluminum oxide (AlO_x) capping layer, metallic wires were successfully deposited on top of PS PnC structures by e-beam lithography. Fabrication of colloidal crystal domains without cracks was achieved by applying a self-assembling process with in-situ silicon box confinement. However, there was still a big challenge left as there were always gaps between the domain of the PS nano-spheres and the in-situ box on silicon wafer. One possible reason is that the inside wall of the silicon box is not vertical due to the anisotropic wet etching method used to fabricate the box itself. Also, the fact that PS nano-spheres self-assembled almost everywhere is not good for integrating measurement devices onto the phononic crystals. For that reason, a polymer box was also fabricated by 3D laser lithography and dipped into PS solution. Gaps between the 3D PnC crystal domains and the box side walls sometimes disappeared. Also, PS nano-spheres did not self-assemble on top of the box made by photoresist IPL780, which is promising.

Chapter 2

Background

In this chapter, theories of thermal conductance and phonons are generally introduced, giving the simplest power laws in terms of temperature. The Debye model is utilized to calculate the dominant frequency of phonons. In addition, basic theory of the SINIS junction as a thermometer is also introduced. Finally, results observed previously in our group on 2D PnC structures are reviewed.

2.1 Thermal conductance

There are three mechanisms to transfer heat: convection, conduction and radiation. Convection happens in a gas or a liquid. The power radiated from a body can be expressed in terms of its temperature by the Stefan-Boltzmann Law [26]:

$$P = A_S \epsilon(\lambda) \sigma T^4, \tag{2.1}$$

where A_S is the surface area of the body, $\epsilon(\lambda)$ ($\epsilon(\lambda) \leq 1$) is the emissivity of this body ($\epsilon(\lambda)$=1 when it is a black body), and σ is the Stefan-Boltzmann constant,

$$\sigma = \frac{\pi^2 k_B^4}{60 c^2 \hbar^3}. \tag{2.2}$$

Here c is the speed of light in vacuum, k_B is the Boltzmann constant, and $\hbar$ is the reduced Planck constant, so that σ is a natural constant.

Heat conduction dominates in solids at low temperatures. Heat transfer in solids is often described by the Fourier's Law [27]:

$$\overrightarrow{q} = -k \nabla T, \tag{2.3}$$

where, $\overrightarrow{q}$ is the local heat flux density, ∇T is the temperature gradient, k is the

thermal conductivity of the material. In a 1D case, Equation 2.3 is simplified to:

$$q = -k\frac{dT}{dx}.$$ (2.4)

However, it is important to point out that Fourier's law can be broken at the lowest temperatures, if scattering processes responsible for k die out, i. e. if the diffusion length is larger than the sample size. In that case, heat conduction is ballistic, and in 3D solids emitted power follows a law similar to Equation 2.1 with a phononic Stefan-Boltzmann factor [28]

$$\sigma_p = \frac{\pi^2 k_B^4}{120\hbar^3}(\frac{1}{c_L^2} + \frac{2}{c_T^2}),$$ (2.5)

where c_L and c_T are the longitudinal and transverse speeds of sound.

2.2 Properties of phonons

It is well known that the quantization of electromagnetic waves leads to the concept of photon. Analogously, the quantization of lattice vibrations carrying the heat in insulators are named phonons. Therefore, the total energy of a 3D crystal can be expressed as:

$$E_{tot} = \sum \left(n_{\vec{q}m} + \frac{1}{2}\right) \hbar\omega_{\vec{q}m},$$ (2.6)

where $\omega_{\vec{q}m}$ is the eigenfrequency of a phonon corresponding to eigenmode $\vec{q}m$ with $\vec{q}$ the wavevector, $n_{\vec{q}m}$ is occupation number and m is the polarization. Each mode acts as an independent harmonic oscillator, so that the thermally-averaged occupation number is described by the Bose-Einstein distribution [29]:

$$\langle n_{\vec{q}m}\rangle = \frac{1}{e^{\frac{\hbar\omega_{\vec{q}m}}{k_B T}} - 1}.$$ (2.7)

By setting $\beta = \frac{1}{k_B T}$, we can write for the average energy

$$\langle E_{tot}\rangle = \sum_{\vec{q}m} \left(\frac{1}{e^{\beta\hbar\omega_{\vec{q}m}} - 1} + \frac{1}{2}\right) \hbar\omega_{\vec{q}m}.$$ (2.8)

The zero-point factor of $\frac{1}{2}\hbar\omega_{\vec{q}m}$ can be ignored in the consideration of thermal conduction and heat capacity, as it is temperature independent. By considering large crystals, the $\vec{q}$ sum in Equation 2.6 can be converted to an integral over the first

Brillouin zone, so that:

$$\langle E_{tot} \rangle = \frac{V}{(2\pi)^3} \sum_m \int_{BZ} d\vec{\mathbf{q}} \frac{\hbar\omega_{\vec{\mathbf{q}}m}}{e^{\beta\hbar\omega_{\vec{\mathbf{q}}m}} - 1},$$ (2.9)

where V is the total volume of the crystal. Using the density of states per branch $D_m(\omega)$, E_{tot} can then be written as an integral over frequency ω:

$$\langle E_{tot} \rangle = \frac{V}{(2\pi)^3} \sum_m \int_0^\infty D_m(\omega) \frac{\hbar\omega}{e^{\beta\hbar\omega} - 1} d\omega.$$ (2.10)

The specific heat capacity is then:

$$C_V = \frac{1}{V} \frac{\partial \langle E_{tot} \rangle}{\partial T}.$$ (2.11)

The emitted ballistic heat flux (power) is, on the other hand

$$P = \frac{A}{(2\pi)^3} \sum_m \int_{BZ} d\vec{\mathbf{q}} \frac{\hbar\omega_{\vec{\mathbf{q}}m}}{e^{\beta\hbar\omega_{\vec{\mathbf{q}}m}} - 1} v_{\vec{\mathbf{q}},m},$$ (2.12)

where A is the surface area and $v_{\vec{\mathbf{q}},m}$ is the component of the group velocity of a mode normal to the surface [16].

2.2.1 Debye model

At low temperatures, in regular 3D solids (not in PnCs or membranes) one can approximately describe the phonons with the so called Debye Model [29].

There the assumption is that for all phonon modes, the dispersion relation is linear. This leads to a DOS

$$D(\omega) = \frac{3\omega^2}{2\pi^2 \overline{c}^3},$$ (2.13)

where $\frac{1}{\overline{c}^3} = \frac{1}{3} \left(\frac{1}{\overline{c}_l^3} + \frac{1}{\overline{c}_{t1}^3} + \frac{1}{\overline{c}_{t2}^3} \right)$ is the averaged speed of sound factor, with $\overline{c}_l, \overline{c}_{t1}$, and $\overline{c}_{t2}$ the directionally averaged longitudinal and the two transverse speeds of sounds of the solid.

Finally, at very low temperature $T << \Theta_D$, where Θ_D is the Debye temperature, the specific heat capacity can be calculated by plugging Equation 2.13 into Equation 2.11:

$$C_V = \frac{\partial}{\partial T} \int_0^\infty D(\omega) \frac{\hbar\omega}{e^{\beta\hbar\omega} - 1} d\omega = \frac{12\pi^4}{5} \left(\frac{T}{\Theta_D} \right)^3.$$ (2.14)

For a 2D Debye model, the total crystal area is S and each atom has two degrees

of freedom. Then, the density of states is:

$$D(\omega)_{2D} = \frac{\omega}{2\pi\bar{c}^2},\tag{2.15}$$

and at very low temperature, $T << \Theta_D$, the specific heat for the 2D case is thus:

$$C_V(2D) = \frac{\partial}{\partial T} \int_0^\infty D(\omega)_{2D} \frac{\hbar\omega}{e^{\beta\hbar\omega} - 1} d\omega = \alpha \frac{9k_B}{2\pi} (\frac{T}{\Theta_D})^2,\tag{2.16}$$

where $\alpha = \int_0^\infty \frac{x^2}{e^x - 1} dx$. Note that suspended membranes do not actually follow this model, because the lowest mode in that case has a quadratic dispersion [30].

2.2.2 Dominant frequency
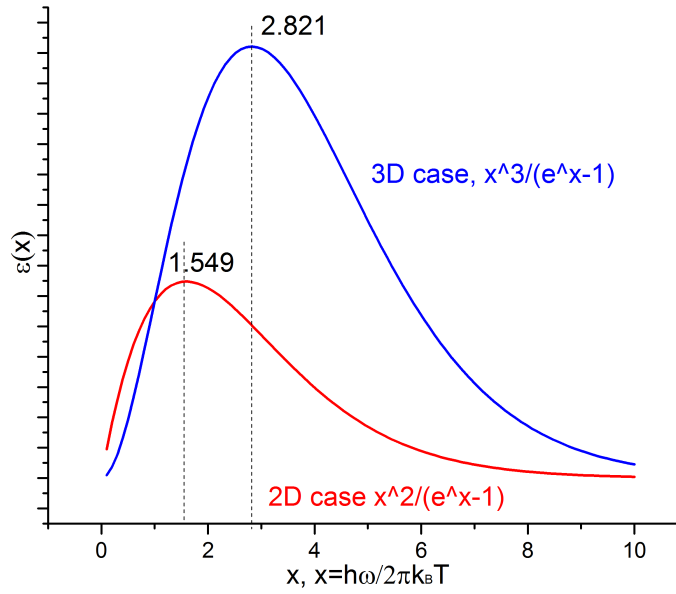
FIGURE 2.1 Phonon energy density vs. phonon frequency. The multipliers depending on $\bar{c}$ for both 2D and 3D cases are ignored. The red line stands for 2D while the blue line stands for 3D.

The total energy can also be expressed with frequency dependent energy density $\epsilon(\omega)$, as $\langle E_{tot} \rangle = \int_0^\infty \epsilon(\omega) d\omega$. Thus

$$\epsilon(\omega) = \frac{\hbar\omega}{e^{\beta\hbar\omega} - 1} D(\omega) = \frac{3\hbar}{2\pi^2\bar{c}^3} \frac{\omega^3}{e^{\beta\hbar\omega} - 1},\tag{2.17}$$

where the last equation assumed the Debye model. There is thus a dominant frequency for each temperature, which can be found by finding the maximum, giving for the dominant frequency in the 3D Debye model $\nu_T = \frac{\omega_T}{2\pi} = \frac{2.821 k_B T}{h}$.

For 2D Debye Model, the energy density is $\epsilon(\omega)_{2D} = \frac{\hbar \omega^2}{2\pi \bar{c}^2 e^{\beta \hbar \omega} - 1}$, so that the dominant frequency is $\nu_T = \frac{1.594 k_B T}{h}$. For example, at 100 mK, the dominant frequency is 3.3 GHz. If we know the average speed of sound, the dominant phonon wavelength in the 2D Debye model is:

$$\lambda_T = \frac{h\bar{c}}{1.549 k_B T}. \tag{2.18}$$

For a SiN_x membrane, the average speed of sound is $\bar{c} = 5800 m/s$ [16], giving for the wavelength of the dominant phonon at 100 mK $\lambda_T = 1.8\ \mu$m.

2.2.3 Phonon band structure in membrane and PnCs

The lateral dimensions of the suspended membrane of 300 nm thickness used in this thesis are $\sim 300\ \mu$m $\times$ 300 μm, which is much larger than the dominant wavelength. Therefore, the suspended membrane can be treated as infinite with free top and bottom boundaries. With the free boundaries, phonon modes rearrange from their bulk waveforms into so-called Lamb modes [30], which can be grouped into horizontal shear modes (h), and symmetric (s) and antisymmetric Lamb modes (a) [31]. Figure 2.2 (a) shows the lowest branches of the dispersions of these phonon eigenmodes. The dispersion relations of the lowest mode of the h modes, the s modes and the a modes [31] can be written

$$\omega_{h,0} = c_t k_\parallel, \text{the lowest h mode} \tag{2.19}$$

$$\omega_{s,0} = 2\frac{c_t}{c_l}\sqrt{c_l^2 - c_t^2} k_\parallel, \text{the lowest s mode} \tag{2.20}$$

$$\omega_{a,0} = \frac{\hbar^2}{2}\left[2c_t b\sqrt{\frac{(c_l^2 - c_t^2)}{3c_l^2}}\right] k_\parallel^2, \text{the lowest a mode,} \tag{2.21}$$

where b is the thickness of the membrane, $k_\parallel$ the wave vector of the component of the bulk wave along the surface of the membrane , c_l and c_t the bulk longitudinal and transverse speeds of sound, shown in the long wavelength limit in Figure 2.2 (a). The behavior of the lowest h mode and s mode is linear, and the lowest a mode is quadratic.

The band structure of the full $\text{SiN}x$ membrane of 300 nm thickness can be calculated by both the results of Lamb-mode theory and the finite element method (FEM), which are consistent with each other [16]. In addition, the band structure
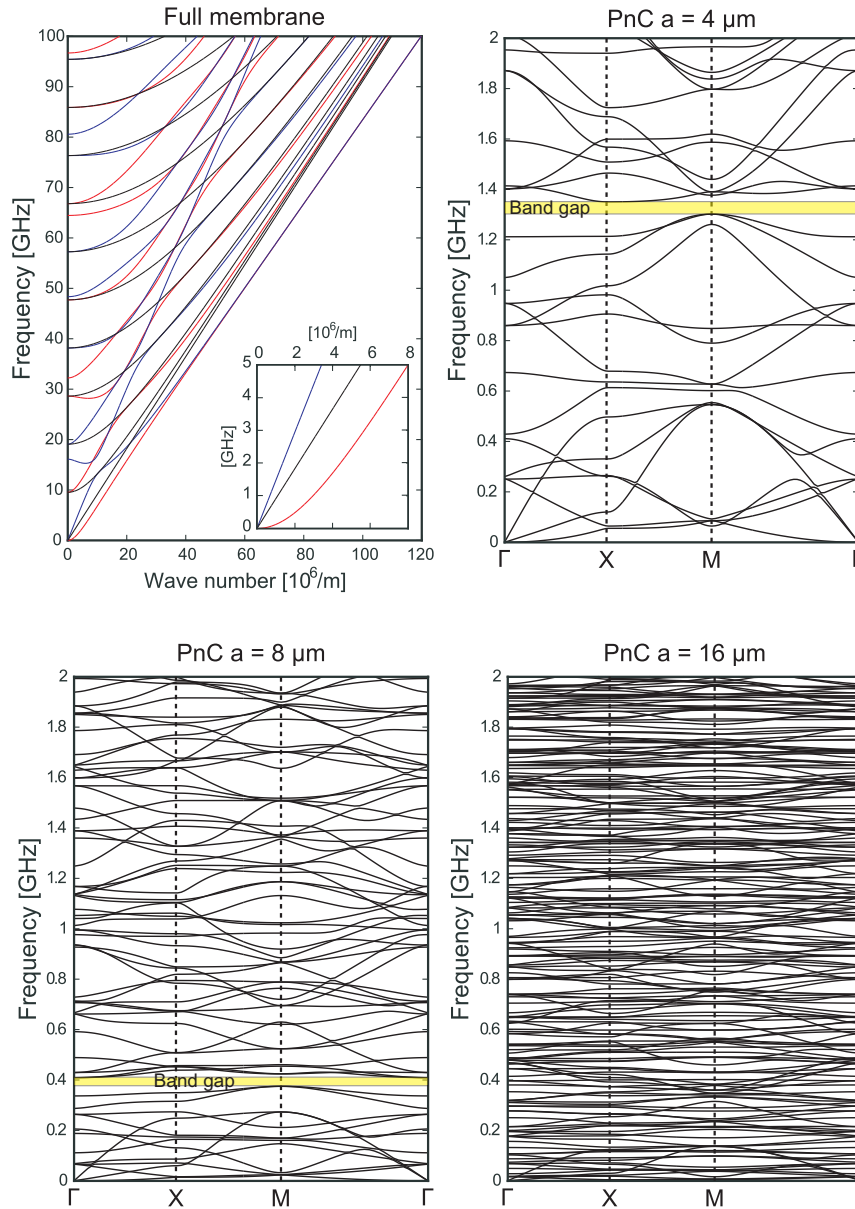
FIGURE 2.2 (a) The branches of the dispersion relations of the phonon eigenmodes of a free standing thin membrane. The black line stands for h modes, the blue line stands for s modes, and the red lines stand for a modes. The zoom in of the boxed area shows the lowest branches of the dispersion relations of the phonon eigenmodes of a free standing thin membrane shown in the limit of long wavelengths. The linear behavior of the h and s branches as well as the quadratic behavior of the a branch can be seen here. (b) (c) and (d) show dispersion relations in the main symmetry directions of the Brillouin Zone for the square lattice phononic crystals with $f = 0.7$, $a = 4$ μm, 8 μm and 16 μm respectively. Complete bandgaps are observed at $\nu \approx 1.33$ GHz for the PnC with $a = 4$ μm and at $\nu \approx 0.4$ GHz for the PnC with $a = 8$ μm.

of the PnC structures can be calculated by FEM. Figure 2.2 (b), (c) and (d) show the calculation results of PnC structures with periods $a = 4$ μm, 8 μm and 16 μm respectively, which were measured in Chapter 4. There is a complete bandgap either at $\nu \approx 1.3$ GHz for the PnC with $a = 4$ μm, or at $\nu \approx 0.4$ GHz for the PnC with $a = 8$ μm. In contrast there are no bandgaps at all for either the full membrane or the 16 μm periodic PnC structure at frequencies no larger than 2 GHz.

2.2.4   The power emitted by the heater

The net phonon heat, emitted by a heater placed in the center of the suspended membrane, flows outwards along the membrane in all directions. At such low temperatures less than 1 K, where the measurements were carried out, this heat flow is typically ballistic, which means that the phonon emission is radiative, not diffusive.

Only the phonon modes (mode index j and wave vector $\boldsymbol{k}$) with outward propagation carry this energy, so the radiated power for both the PnCs and the uncut membranes follow

$$P(T) = \frac{1}{2\pi^2} \sum_j \oint_\Gamma d\Gamma \int_K d\boldsymbol{k}\hbar\omega_j(\boldsymbol{k})n(\omega_j, T)\frac{\partial\omega_j}{\partial\boldsymbol{k}}\cdot\hat{n}_\Gamma\Theta\left(\frac{\partial\omega_j}{\partial\boldsymbol{k}}\cdot\hat{n}_\Gamma\right), \qquad (2.22)$$

where Γ is the element boundary of the heater, $\hat{n}_\Gamma$ is an outer unit normal of that boundary (in the membrane plane) and Θ is the Heaviside step function. Here $n(\omega, T)$ is the Bose-Einstein distribution describing the (assumed) phonon thermal occupation of the emitted phonons and $\frac{\partial\omega_j}{\partial\boldsymbol{k}}$ the group velocity of each mode. Thus the unknown set of dispersion relations $\omega_j := \omega_j(\boldsymbol{k})$ for the emitted phonon modes j in the membrane have to be calculated for example by FEM. The integration of the 2D K-space extends over all K-space for the uncut membranes, however it is replaced by the integration over the first Brillouin zone for the PnCs. [17]

2.2.5   Electron-Phonon coupling at low temperatures

At sub-Kelvin temperatures, electrons and phonons in a metal can have different temperatures, T_e and T_p. The electrons thermally decouple from phonons. T_e can be much higher than T_p when electrical power is dissipated in the electron gas, which is the 'hot-electron' effect [32]. The power flow from electron gas of volume V to phonons is then:

$$P = \Sigma V(T_e^5 - T_p^5), \qquad (2.23)$$

where Σ is coupling constant, it is a material parameter.

2.3 Normal metal-insulator-superconductor junction devices

2.3.1 Superconductivity

Superconductivity is a physical phenomenon with perfect conductivity below the critical temperature T_C, first discovered by Dutch physicist H. K. Onnes in 1911 [33]. Perfect diamagnetism of a superconductor was discovered by W. Meissner and R. Ochsenfeld in 1933 [34]. The critical temperature (T_C), a characteristic of a material, varies from one superconductor to another. For example, the bulk T_C of the superconducting material used here, Al, is 1.2 K. The highest T_C of an elemental metal is 9.2 K and belongs to niobium.

The microscopic theory explaining the origin of superconductivity was proposed by Bardeen, Cooper and Schrieffer, the so called BCS theory in 1957 [35]. The ground state of superconductivity is formed by Cooper pairs formed by electron-phonon interaction. An electron moving in a solid will distort the ion cores around it, creating a small positively charged disturbance in the lattice. Another electron nearby will then be attracted to this disturbance, thus creating an effective attractive interaction between the two electrons, bonded as a Cooper pair. Full analysis requires quantum field theory. One of the most important predictions is that there is an energy gap (2Δ) between the ground state (all electrons paired) and the first excited state. In other words, a minimum energy of 2Δ, which depends on temperature, is required to break one Cooper pair and form two quasi-particle excitations. BSC theory also predicts the relation between the critical temperature and the energy gap at $T = 0K$, if the electron-phonon interaction is not too strong (weak coupling limit) [35, 36]:

$$2\Delta(0) = 3.528 k_B T_C. \tag{2.24}$$

It also predicts how the gap value $\Delta(T)$ increases from 0 to $\Delta(0)$ when temperature decreases from T_C to 0 [35, 37]. The implicit equation from which $\Delta(T)$ can be solved is

$$-\ln(\frac{T}{T_C}) = \int_0^\infty (\frac{\tanh(y)}{y} - \frac{\tanh\sqrt{y^2 + \frac{1.764\Delta(T)/\Delta(0)}{2(T/T_C)}}}{\sqrt{y^2 + \frac{1.764\Delta(T)/\Delta(0)}{2(T/T_C)}}})dy, \tag{2.25}$$

where $y = \frac{\epsilon}{2k_B T_C}$, and ϵ is the energy of single excited quasi-particle. There-

fore $\Delta(T)/\Delta(0)$ is a universal function of T/T_C [37]. Near T_C, Equation 2.25 can be simplified to

$$\frac{\Delta(T)}{\Delta(0)} \approx 1.74(1 - \frac{T}{T_C})^{\frac{1}{2}}. \tag{2.26}$$

2.3.2 Normal metal-insulator-superconductor tunnel junction

In classical mechanics, a particle cannot pass through a barrier. However, quantum mechanically it can happen, with a process called tunneling. Specifically, an electron can penetrate a thin layer of an insulator. The tunneling probability drops exponentially with the thickness of insulator [36, 38], so a very thin layer of the insulator is required, normally an in-situ oxidized layer of a few nanometers. The first normal metal-insulator-superconductor (NIS) tunneling experiment was performed by Fisher and Giaever using $Al/Al_2O_3/Pb$ structure where Pb was the superconductor and Al was the normal metal [39].

A thin enough insulator allowing tunneling combined with two electrodes is called a tunnel junction. Electrodes can either be normal metals or superconductors. Therefore, there are three kinds of junctions, the normal metal-insulator-normal metal (NIN) junction, the normal metal-insulator-superconductor (NIS) junction and the superconductor-insulator-superconductor (SIS) junction [36, 38]. The tunneling current in an NIS junction depends on the bias voltage V, and the normal metal temperature T_N, highly non-linearly. In contrast, it does not depend directly on the temperature of the superconductor, T_S. Therefore, NIS junction can be utilized as a thermometer measuring accurately the local temperature in sub-Kelvin range. [25, 40, 41].

Here, the BCS semiconductor model [36] is used to write the normalized density of states n_S of the quasi-particle excitations of the superconductor

$$n_S(\epsilon, T_S) = \frac{N_S(\epsilon)}{N(0)} \quad = \quad 0, \text{if } |\epsilon| < \Delta \tag{2.27}$$

$$= \quad \frac{|\epsilon|}{\sqrt{\epsilon^2 - \Delta(T_S)^2}}, \text{if } |\epsilon| > \Delta, \tag{2.28}$$

where $N(0)$ is the normal state density of states at Fermi energy.

The tunneling current is thus given in the single-particle tunneling theory
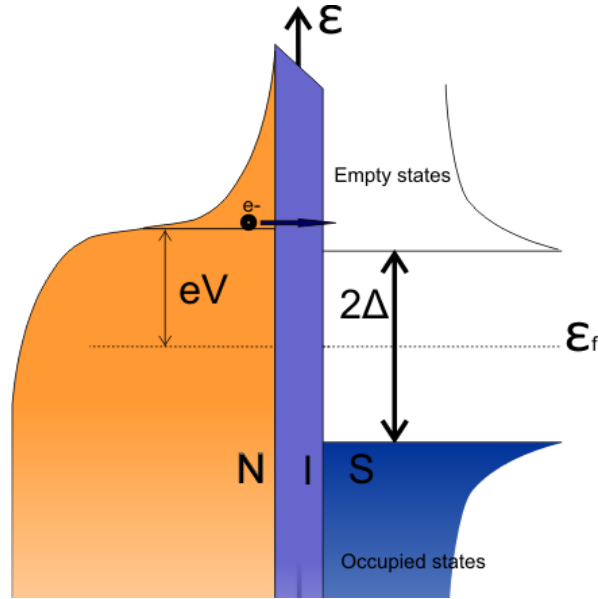
FIGURE 2.3 The energy graph of a NIS junction. Electron in the normal metal with energy above the superconducting energy gap can tunnel through the barrier.

[36, 42, 43], as:

$$I_{NIS} = \frac{4\pi^2 e A \, |t_0|^2 \, N(0) N_S(0)}{\hbar} \int_{-\infty}^{\infty} d\epsilon \, n_S(\epsilon, T_S) \left[f_S(\epsilon, T_S) - f_N(\epsilon + eV, T_N) \right], \quad (2.29)$$

where $f_S(\epsilon, T_S)$ and $f_N(\epsilon, T_N)$ are Fermi functions in the superconductor and the normal metal respectively, A is the junction area, $|t_0|^2$ is the tunneling probability of one electron, $N_S(0)$ is the normal state density of states at Fermi energy of the superconductor and $N(0)$ is that of the normal metal. Equation 2.29 can also be simplified by introducing the tunneling resistance R_T:

$$I_{NIS} = \frac{1}{eR_T} \int_{-\infty}^{\infty} d\epsilon \, n_S(\epsilon, T_S) \left[f_S(\epsilon, T_S) - f_N(\epsilon + eV, T_N) \right], \quad (2.30)$$

so that

$$R_T = \frac{\hbar}{4\pi^2 A \, |t_0|^2 \, N(0) N_S(0)}. \quad (2.31)$$

In most cases, however, it has been discussed [44] that the density of states of the superconductor is not ideal as shown in Equation 2.28, but is broadened by lifetime effect, e.g. due to photon-assisted tunneling. Then the expression for n_s

becomes

$$n_S(\epsilon, T_S) = \left| Re \left\{ \frac{\epsilon + i\Gamma}{\sqrt{(\epsilon + i\Gamma_D)^2 - \Delta^2(T_s)}} \right\} \right|, \tag{2.32}$$

where Γ_D is the Dynes parameter, describing the broadening of the DOS singularity. In the case of photon-assisted broadening, it is set-up dependent [25]. In the cryostat set-up used for all the measurement in this thesis, Γ_D/Δ was around $\sim 10^{-4}$ for Al as the superconductor.
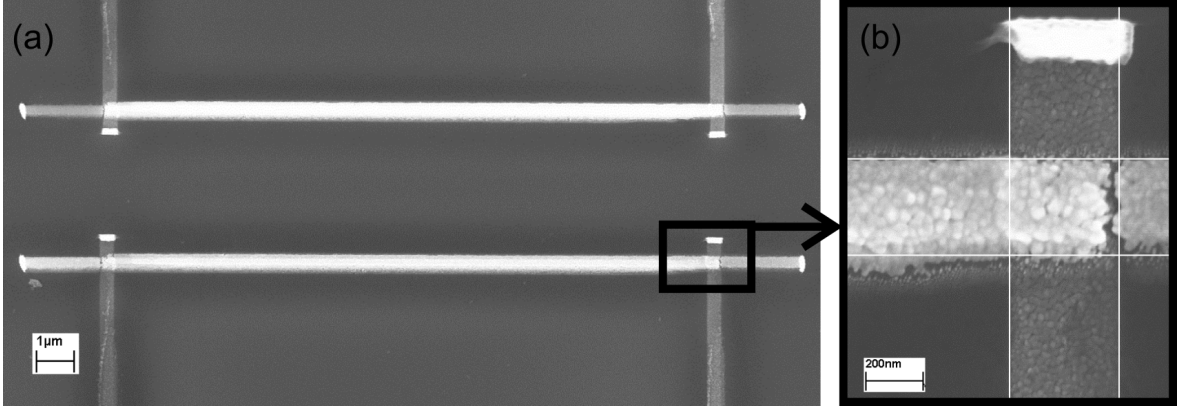

FIGURE 2.4 (a) SEM image of two SINIS junction pairs. (b) Zoom in of the boxed area with a single NIS junction, the junction area is about 340 nm by 380 nm.

Usually, two NIS junctions are fabricated in series forming a SINIS junction pair, see Figure 2.4. As thermometers, they have an increased signal response by a factor of 2 as compared to a single junction. If we suppose that the two NIS junction are symmetrized, the tunneling resistance of each single junction is R_T so that the voltage drop on each junction is V. Now the tunneling current for each single junction separately are:

$$I_{NIS} = \frac{1}{eR_T} \int_{-\infty}^{\infty} d\epsilon\, n_S(\epsilon, T_S) \left[f_S(\epsilon, T_S) - f_N(\epsilon + eV, T_N)\right] \tag{2.33}$$

$$I_{SIN} = \frac{1}{eR_T} \int_{-\infty}^{\infty} d\epsilon\, n_S(\epsilon, T_S) \left[f_N(\epsilon - eV, T_N) - f_S(\epsilon), T_S\right], \tag{2.34}$$

and those two currents must be equal. The current can also be written in symmetric form, where the dependence on f_S is explicitly removed [45].

$$I_{SINIS} = \frac{1}{2eR_T} \int_{-\infty}^{\infty} d\epsilon\, n_S(\epsilon, T_S)(f_N(\epsilon - eV, T_N) - f_N(\epsilon + eV, T_N)). \tag{2.35}$$

Equation 2.35 shows that the tunneling current I_{SINIS} is highly non-linear with respect to the bias voltage V and the normal metal temperature T_N, but not on T_S. Therefore, T_N can be detected by measuring V at a constant bias current I_b. Data on thermometry is shown in Chapter 4.

2.4 Previous 2D phononic crystal results by our group

It has been demonstrated both experimentally and theoretically for the first time by our group [16] that coherent band structure effects can be used to control phonon thermal conductance at low temperatures with the periodic structures, i.e. phononic structures. The samples were all fabricated from 485 nm thick SiN_x. SiN_x membranes were perforated into square arrays of holes to get 2D PnC structures (Figure 2.5) with filling factor of 0.7. Two lattices were chosen in such a way that one had a period of 970 nm with a complete band gap at the characteristic energy of thermal dominant phonons at 0.1 K, and the other had a period of 2425 nm with no band gap at all. SINIS junctions with Cu as normal metal were mounted to measure local phononic temperature, one SINIS junction pair as a heater and the other one as a thermometer. Since the bridges between two holes were so narrow, there were a few column of holes were removed to make a platform for the fabrication of SINIS junction pairs (Figure 2.5 a).

Figure 2.6 shows the measured emitted power P versus the measured membrane temperature T for both 2D PnC samples and the full membrane, up to a temperature as high as about 1K. It is clear that the emitted power is much reduced for both 2D PnC membranes at all temperatures, compared with the full membrane. Initially unexpected, the larger period 2D PnC structure actually has a lower thermal conductance than the smaller period structure. This shows that the band-gap is not the only main reason for the reduction of the thermal conductance of periodic structures. Additionally, the reduction amount also depends on the measured membrane temperature. It is obvious that reduction of thermal conductance is not a result caused by simple geometry, as classically the reduction factor is dependent only on the hole filling factor [46], which remained constant here. Dependencies of emitted power on measured membrane temperature are about P$\sim T^{3.3}$ and P$\sim T^{2.3}$ at low T for the full and 2D PnC membranes respectively, while closer to 1 K both the full membrane and the 970 nm period 2D PnC samples have P$\sim T^4$ and the 2425 nm period 2D PnC closer to P$\sim T^5$. Everything is consistent with the idea that the transport of phonons in 2D PnC structures is suppressed by the coherent modification of the phonon band structure, which is caused by the periodic hole array. The theoretical P-T curves for both the PnC samples and the full membrane were calculated by finite element
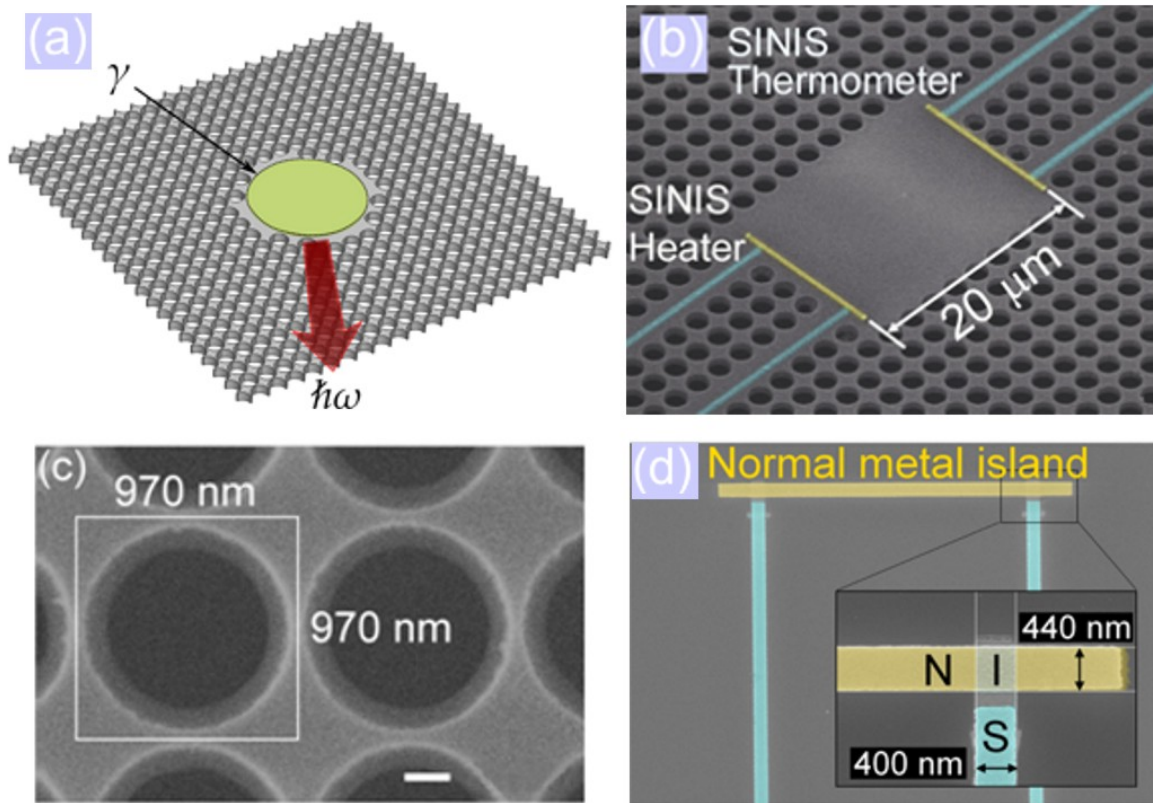
FIGURE 2.5 The 2D membrane PnC device. (a) Schematic representation of a perforated membrane PnC geometry with a square array of circular holes, fabricated by e-beam lithography. The central region has a heater, which emits thermal phonons into the 2D PnC structure. (b) A false colour scanning electron micrograph (SEM) of the central region of the larger period a = 2425 nm 2D PnC sample. The blue (Al) and yellow (Cu) lines are the metallic wiring which form the heater and thermometer elements at the centre of the PnC. The shorter period sample has the same wiring locations and dimensions. The full size of the perforated membrane is 100 mm × 100 mm. (c) A scanning electron micrograph of a region of the shorter period sample (black areas, empty space, grey areas SiN membrane), showing the unit cell size 970 nm × 970 nm and the width of the narrowest region ∼ 60 nm. The sidewalls have a slight angle so that the bottom end of the hole is slightly smaller. Scale bar has length 200 nm. (d) A false colour s.e.m. of the heater/thermometer structure, consisting of a Cu normal metal wire (yellow) sandwiched between two normal metal-insulator-superconductor (NIS) tunnel junctions, connected to the measurement circuit by superconducting Al leads (blue). [16]
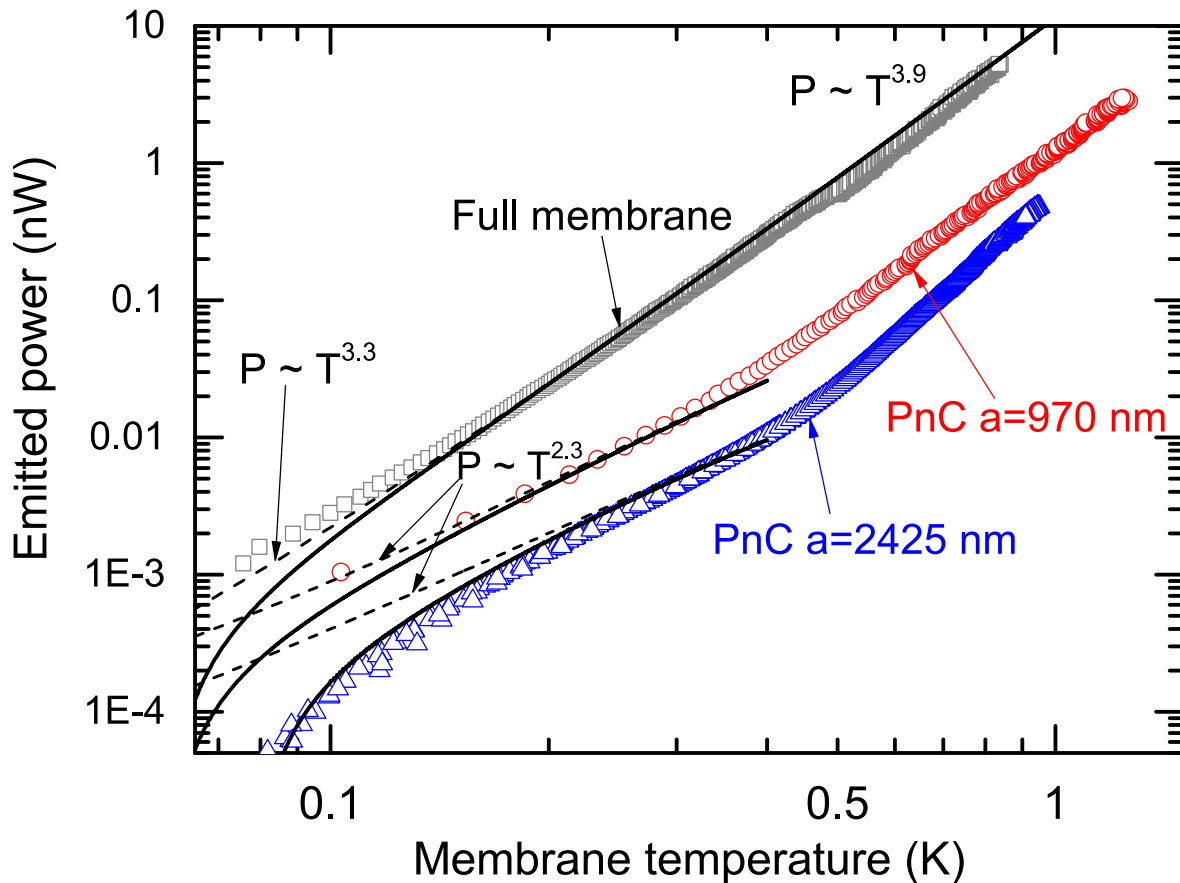
FIGURE 2.6 Measured emitted phonon power versus temperature. Grey squares show the data for the full, uncut membrane, red circles (a = 970 nm) and blue triangles (a = 2425 nm) the data for the two square PnC samples. The theoretical lines are given by ballistic theory, using the computed band structures for each case, with (solid lines) or without (dashed lines) a phonon back radiation power from the substrate at bath temperature (60 mK for full membrane and PnC with a = 970 nm, 80 mK for PnC with a = 2425 nm). All three theory curves were fitted to the data with one common scale parameter. The size of symbols represent measurement errors. [16]

method (FEM) from the elastic Lamé equations, and a ballistic transport model [16]. A constant multiplier, the effective heater length, was required to fit the theoretical lines to the measured data, which was found by fitting the membrane data. It was kept the same for all the 2D PnC data, the showing plot the theory for the reduction of thermal conductance has a quantitative agreement with the experiment. Fitted theoretical lines in Figure 2.6, with and without a phonon back radiation power from the substrate are shown as solid and dashed lines, respectively.

To further understand the suppression of the thermal conductance by the PnC structures of Figure 2.6, one can study the theoretical density of states, group velocities of the phonons, and the spectral power, shown in Figure 2.7 for two different temperatures [16]. It is clear from Figure 2.7 that the width of the band-gap for the smaller period structure is less than 5% of the full thermal bandwidth even at 100 mK, so its direct effect is small. Most of the reduction comes from the large reduction of the group velocity [16].
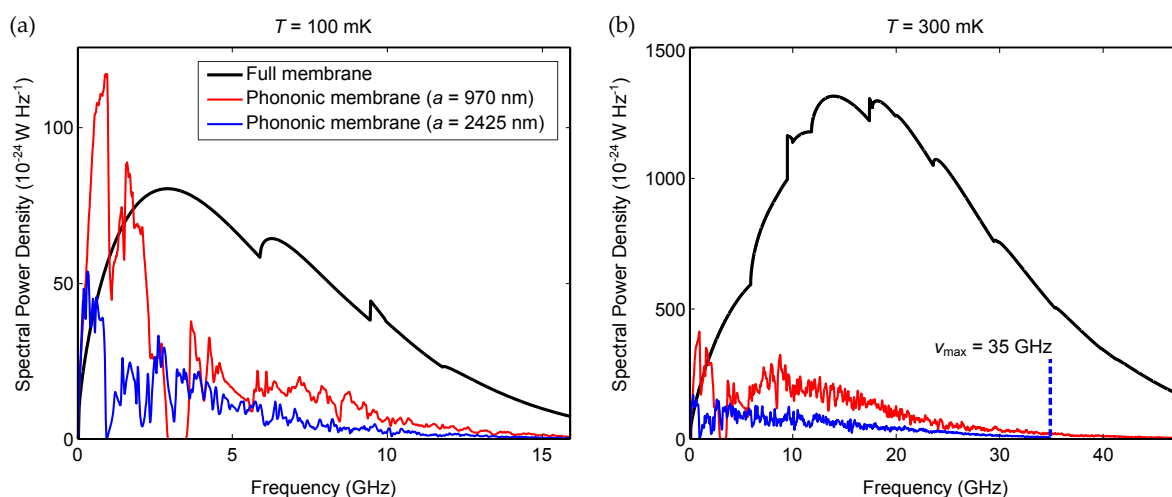

FIGURE 2.7 The spectral phonon power. The spectral powers $P(\nu)$ of a full membrane (black line) to the PnC devices (a $\sim$ 970 nm, red line; a $\sim$ 2425 nm, blue line), at (a) T $\sim$ 0.1 K, and (b) T $\sim$ 0.3 K. For the a $\sim$ 2425 nm structure, power was calculated up to 35 GHz. [16]

Chapter 3

Fabrication techniques

In this chapter, the most important techniques utilized for the sample fabrication in this thesis is introduced, including electron beam lithography (EBL), three-dimensional lithography (3DL), ultrahigh vacuum metal evaporation (UHV), reactive ion etching (RIE), wet etching (WE), and vertical deposition of colloidal crystals (VD).

3.1   Electron beam lithography

A scanning electron microscope (SEM) was employed both for patterning structures with e-beam lithography (EBL) and imaging of samples, performed with the Raith e-Line system. In an SEM, an electron beam emitted from the electron gun biased with high voltage is focused by a condenser lens. When it reaches the sample, it interacts with atoms of the sample producing various signals, such as low-energy secondary electrons by inelastic collisions and high-energy back scattered electrons by elastic collision (Figure 3.1). There could be various detectors placed simultaneously in one SEM. In the Eline Raith system at Nanoscience Center (NSC), there are two types of secondary electron (SE) detectors. One is an in-lens detector that detects SEs that experienced only one inelastic collision; the other one is a SE2 detector that detects SEs that experienced many inelastic collisions. The in-lens detector was utilized for all SEM images in this thesis. In lithography, the electron beam is used to pattern electron sensitive polymers, or resists. The electron beam with high energy can break some chains of polymers, or make cross-links between polymers. Thus, there are two kinds of resists: positive and negative. Area exposed to e-beam will be removed for positive resist (chain breaking) and stay for negative resist chain (cross-linking). All resists used for EBL in the thesis were positive resists.
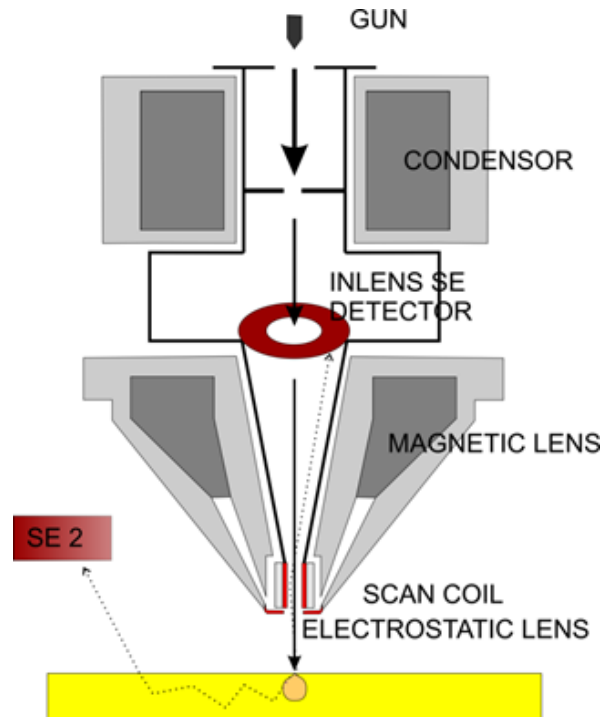
FIGURE 3.1 Schematic of an SEM column.

3.2 Three dimensional lithography

Three dimensional lithography is similar with 3D printing, it is patterning in the 3D space. It is performed by laser photo polymerization using an instrument from Nanoscribe GmbH. It is based on two-photon absorption, where tightly focused infrared laser light develops the resist with energy corresponding to a single UV photon, but only at the 3D focus of a micro-space [47--49]. 3DL is thus a maskless drawing process. Line by line drawing establishes layers, and layer by layer drawing accomplishes a 3D shape. The resist can be liquid or solid. Both normal and Dip-in Laser Lithography (DILL) modes were utilized in this paper, using a liquid resist (see Figure 3.2). In normal mode, the microscope objective lens is immersed into an oil droplet on top of the substrate and the laser light travels through the substrate, is focused and writes on the other side of substrate, requiring thus a transparent substrate. Glass is a common and cheap choice. The DILL mode is designed for opaque substrates, for instance a silicon wafer, which is the most used substrate in a cryogenic lab. In this mode, the objective lens is immersed into a liquid photo resist on top of the substrate. There are two ways of controlling drawing: using a piezo and using a stepper motor. At piezo mode, the x, y, and z directions ranges from 0 to 200 μm.
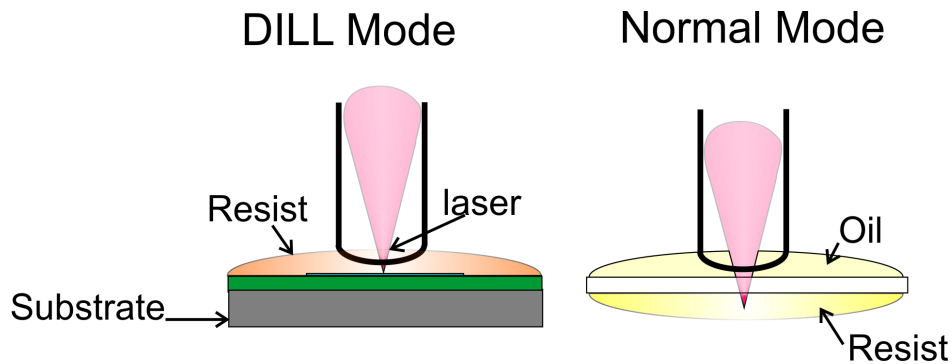
DILL Mode   Normal Mode

FIGURE 3.2 The two patterning modes of Nanoscribe, DILL mode on opaque substrate and normal mode on transparent substrate.

3.3 Metal evaporation

There are many techniques to realize physical vapor disposition (PVD) [50]. The one applied most at NSC is electron-beam evaporation in a ultra high vacuum (UHV) evaporator, consisting of a loading chamber and a main chamber. As shown in Figure 3.3, inside the ultra high vacuum chamber, i. e. the main chamber, an electron beam is generated by voltage as high as 11 kV, and directed towards a metal source using magnetic field, in a pressure of about 10^{-8} mbar. The metal is heated and evaporated when the e-beam hits the metal. As long as the metal vapor reaches the surface of a substrate placed above the metal crucible, it will deposit on top of the substrate. If the distance between the substrate and the metal source is long enough, vapor is uniformly deposited. Deposition rate is detected by a crystal detector, and it is typically about 0.1 nm per second for the fabrication processes here, which is approximately one atom per second. An oxygen line is connected to the loading chamber, so that it is convenient to do in-situ oxidization, which is important for the fabrication of superconductor-insulator-normal metal-insulator-superconductor (SINIS) junction.

Multi-angle evaporation is employed in the metal deposition. There are at least two layers of resist to produce an undercut for the evaporation. Figure 3.4 shows that the first layer of metal (superconducting Al) is deposited from one angle, and then from the opposite side with the same angle. A second layer and the further layers can be deposited the same way as the first layer. If the angle is large enough, no metal is depositing through the vertical line of the mask. Usually, a second type of metal (normal metal, Cu or TiAu) is required for junction fabrication. It is deposited the same way as the horizontal metal after a rotation of 90° of the stage, so that there is no normal metal deposited on top of leads of the first metal, except at cross-sectional area of the two lines, which forms the junction.

22

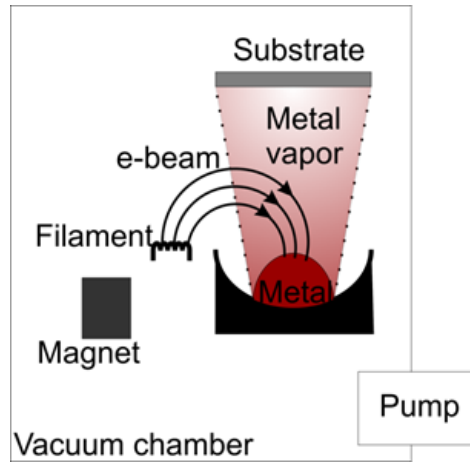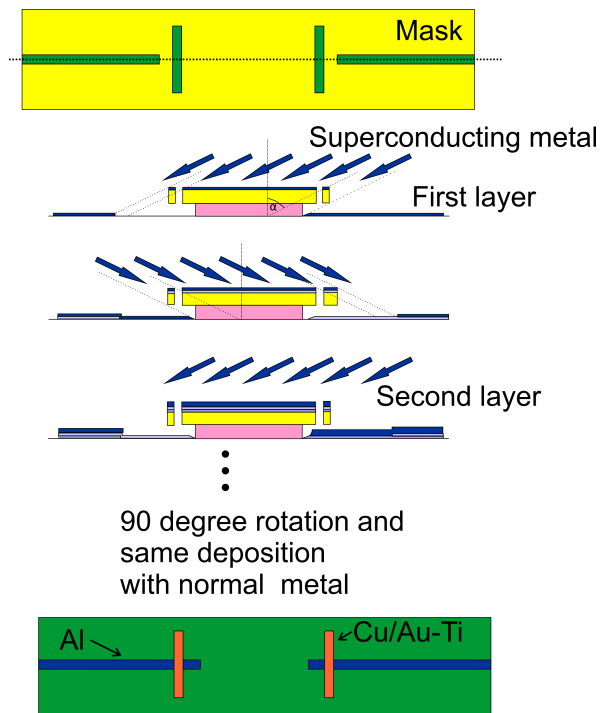**FIGURE 3.3** Principle of metal deposition in the UHV evaporator.

FIGURE 3.4 The multi-angle evaporation technique for junction fabrication. Top: mask from top view. Green lines are opening in the mask. Middle: cross-sectional view along the horizontal dashed line in the top figure. Bottom: final metallization geometry with two different metals, green lines are superconductor oranges are normal metal.

3.4 Reactive ion etching

Reactive ion etching is a form of dry etching [51], it was performed by Oxford Plasmalab 80 Plus system. Reactive gas is injected into the chamber, where plasma is generated. The ions in the plasma accelerate towards the bottom electrode of the chamber, where sample is placed, reacting with the material on the surface of the sample (see Figure 3.5). Meanwhile, the reaction products are pumped away. A resist layer is used to protect those areas that do not need to be etched, as the resist has a much lower reactivity than the material being etched. The types of gases used depend on the etching process, for instance, O_2 is used for poly(methyl methacry-late) (PMMA) resist residue cleaning, and CHF_3 and O_2 are used together to etch away SiN_x.
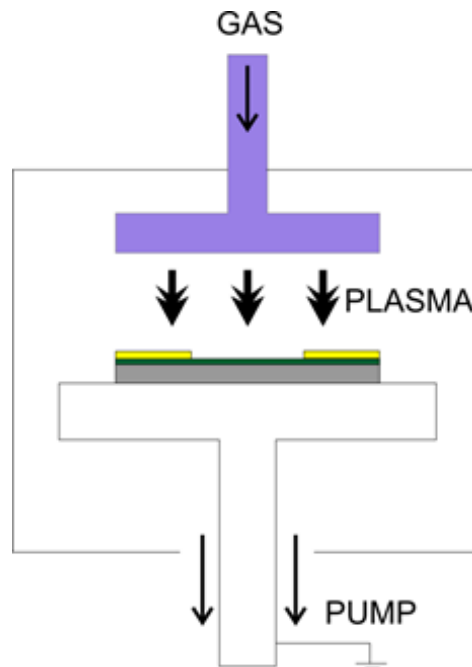
FIGURE 3.5 Schematic of a reactive ion etcher.

3.5 Wet etching

Wet etching is a process that uses a liquid chemical to remove material from the sample. Usually, there is water bath to keep a constant temperature for an optimal etch rate. In wet etching, etching rate can depend on which crystal face is exposed to the liquid etchant. For example, etching of a (100) silicon wafer surface in KOH results in a flat and angled walls (see Figure 3.6). The angle to the surface of the

FIGURE 3.6 Wet etching of Si in 34% KOH liquid.

wafer is 54.7°. In this thesis, 34% (weight to weight) KOH in deionized water at 98 °C water-bath is utilized for etching through Si wafers to make suspended SiN_x membranes.

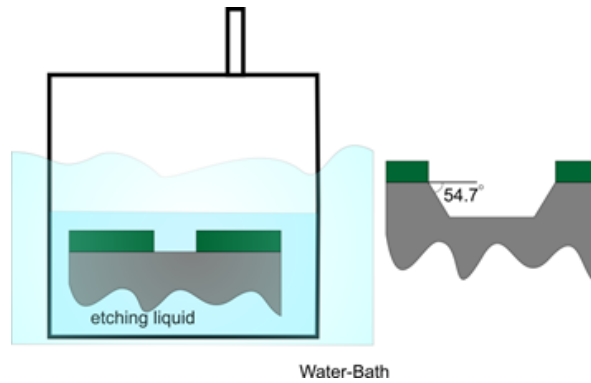## 3.6 Vertical deposition of colloids

The vertical deposition set-up was modified from a Langmuir-Blodgett thin film coating device from KSV Instruments. In our dipping process, the only factor controlled by this machine is the dipping speed of a programmable stepper motor. The speed can be set as low as 0.01 mm/min and increased in steps of 0.01 mm/min. Even though the dipping set up was later placed in a humidity controllable chamber (see Figure 3.8 (f)), all samples for this thesis were dipped without control of humidity (see Figure 3.7).
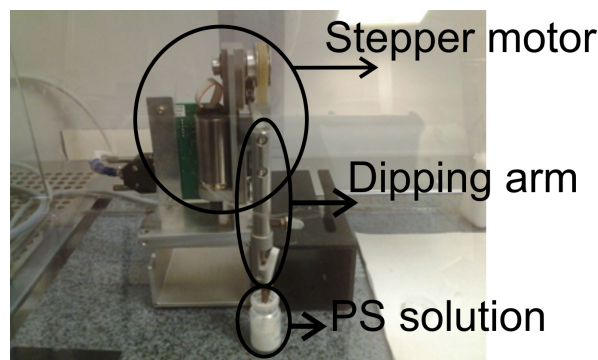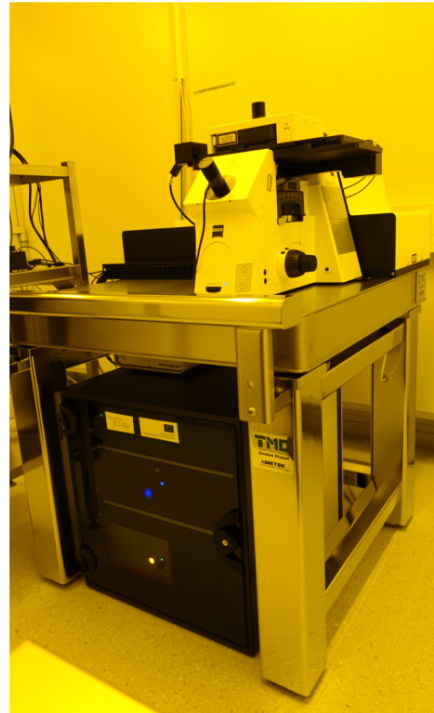

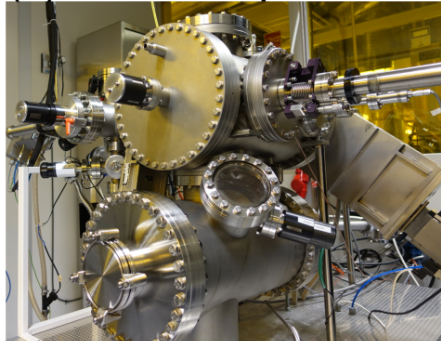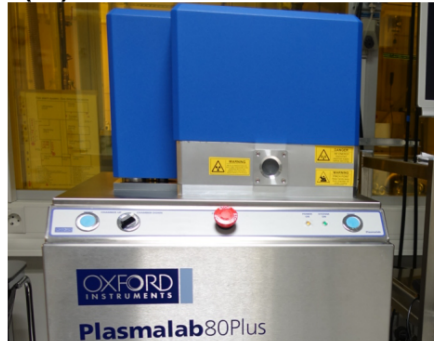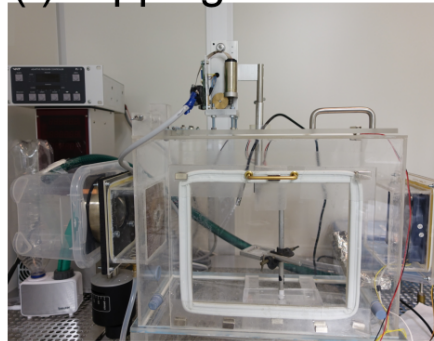**FIGURE 3.7** Old dipping set-up used in this thesis.

FIGURE 3.8 Equipments at NSC. (a) Eline, e-beam lithography. (b) Nanoscribe 3DL. (c) UHV evaporator. (d) RIE. (e) Wet etching bench. (f) The current vertical dipping chamber.

Chapter 4

New two-dimensional phononic crystal structures

This chapter is a summary of articles I and III. The fabrication processes and the thermal properties of novel 2D PnC structures are discussed. The samples consist of suspended SiN$_x$ membranes with square array of holes and SINIS junction pairs at the center of the membranes. One SINIS junction pair was used as a heater, locally emitting phonons into the PnC structures and simultaneously the other SINIS junction pair was used as a thermometer, measuring the local phonon temperature, to obtain thermal conductance. The idea of these new samples was to extend the periodicity to even higher values and to see if thermal conductance is reduced even more.

4.1   Sample designs

For a simple square array, the narrowest width of the bridge between two holes is $\Delta d = a \left(1 - 2\sqrt{\frac{f}{\pi}} \right)$, where f is the filling factor, here set to $f = 0.7$, and where a is the period of the 2D PnC structure. In the new samples, we wanted to avoid the removal of a whole column of holes to fabricate the SINIS device leads. That sets a condition $\Delta d \geq 100$ nm due to the lithographic width of the leads $\geq 100 nm$. Therefore, the period was first set as 4 μm and only one hole at the middle of the PnC structure was removed to fit the two SINIS junction pairs, see Figure 4.1 (a). Distance between the two SINIS junction pairs, i.e. the distance between the heater and the thermometer, was set to 4 μm and was never changed in any later designs. In the previous study [16], it was much longer, 20 μm. To have enough holes, the phononic crystal area was increased and kept at 200 μm $\times$ 200 μm for all samples, with total membrane area set as 300 μm $\times$ 300 μm. In the second design round, two

different periods, 4 and 8 μm, were fabricated for comparison. So an area of 4 μm × 8 μm was left unetched in the middle of the hole array, and the distance between two superconducting leads was set as 8 μm to fit one row of holes of 8 μm in between.

(a) First design 4 µm PnC (b) Second design, 4 µm PnC (c) Final design, 4µm PnC
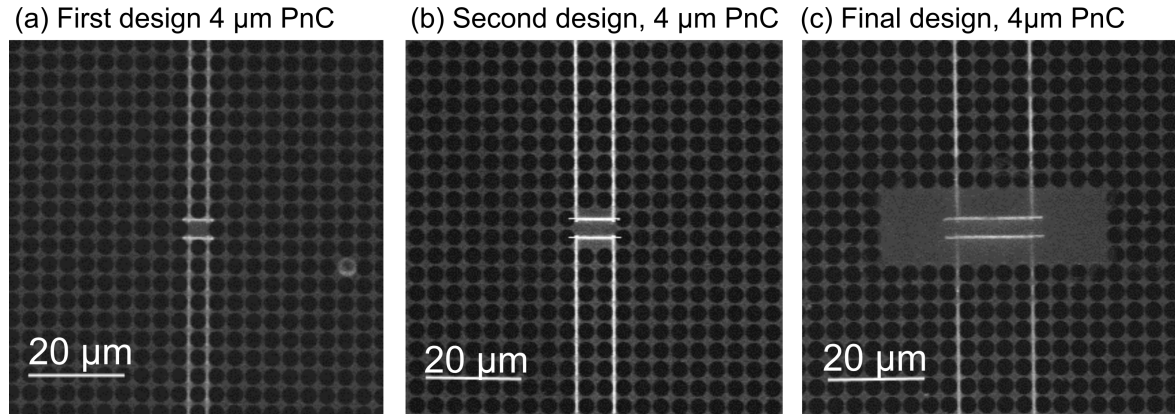
FIGURE 4.1 (a) First design of a 4 μm PnC structure and SINIS junctions. (b) Second design of a 4 μm PnC structure and SINIS junctions. (c) Final design of a 4 μm PnC structure and SINIS junctions. The normal metal island increased from 4 μm to 8 μm to 16 μm.

Finally, we decided that at least one more period was required for comparison. The distance between the two superconducting leads was set to 16 μm and the periods were chosen as 4, 8, 16 μm for convenience. The center area of 16 μm by 48 μm was not etched in the middle of hole array to allow the placement of SINIS junction pairs. Figure 4.2 shows the 8 μm and 16 μm period structures of the final design.

(a)Final design, 8 µm PnC (b)Final design, 16 µm PnC
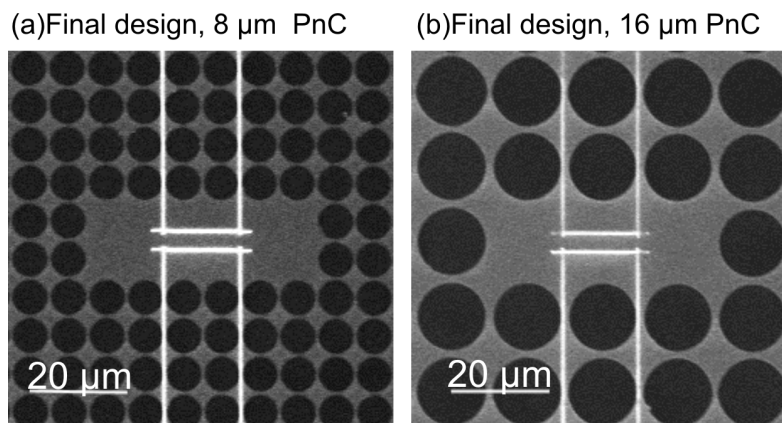
FIGURE 4.2 SEM images of 8 μm period and 16 μm period PnC samples.

The PnC samples with 4, 8 and 16 μm periods and one membrane sample of the final design were measured. Of the second designs, only one PnC sample with

a 4 μm period and one membrane sample were measured. No samples of the first design were measured.

4.2   Sample preparation

The 2D PnC samples were fabricated through three steps: membrane preparation, SINIS fabrication and hole etching. All samples were fabricated from commercially made 300 μm thick silicon wafer with double side 300 nm thick SiN$_x$ films. The fabrication recipe was modified from Tero Isotalo's earlier recipe [52].

Figure 4.3 shows a schematic of the 2D PnC structure fabrication process. The membrane needs to be prepared first, which was achieved by e-beam lithography (EBL), dry etching of an area of 670 μm $\times$ 670 μm SiN$_x$ at the back side, and wet KOH etching of silicon. The SINIS junction pairs were fabricated by EBL and the multi-angle metal deposition technique inside an ultra high vacuum chamber. The final 2D PnC structures were also obtained by EBL and plasma etching. In general, the fabrication of 2D PnC sample is quite a challenge.

4.2.1   Membrane preparation

There were always four membranes of the same size, 300 μm $\times$ 300 μm, made at the same time in the center of a 8 mm $\times$ 8 mm chip. The distance between the centers of two membranes was 2.2 mm. The chip was cleaned by hot acetone and isopropanol (IPA), and coated with 700 nm thick resist of 7% PMMA 950 in anisole, accomplished by spinning it twice at the speed of 3500 rpm. Soft bake was required after each spin, first on 160 °C hot plate for 1.5 mins and then for 3 mins. EBL was utilized to make four square openings on the resist. The sample was developed in a 1:2 solution of methyl-isobutyl ketone (MIBK), developer 1 (D1), for 45 second, rinsed in IPA for 30 seconds and dried by nitrogen(N$_2$) gas flow. Then SiN$_x$ was etched away by RIE with a built-in recipe (CHF$_3$/O$_2$ 10:1, 100 mTor, 100 W) for as long as 15 mins . The remaining resist was cleaned in hot acetone and rinsed in IPA. Finally, four SiN$_x$ membranes were released by wet etching silicon in 34% (wt/wt ratio) KOH at a bath temperature of 98 °C for about 3 hours, and cleaned by hot deionized water for several times.

4.2.2   SINIS junction pair deposition

All samples with the final design used TiAu bi-layer as the normal metal, as opposed to earlier samples which had Cu. An undercut technique [51] together with
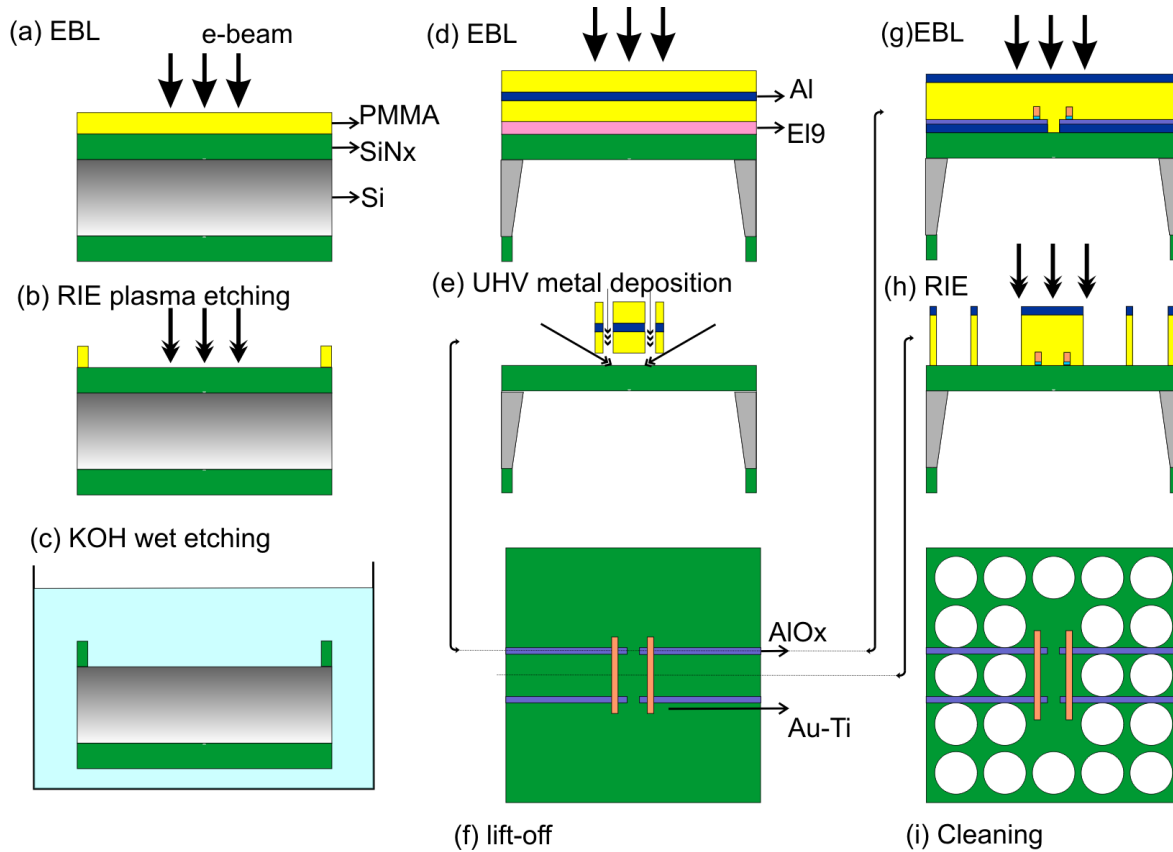
FIGURE 4.3 A schematic of the fabrication process for 2D PnC samples. (a) A clean sample with PMMA resist on top is patterned by e-beam into squares. (b) After the development, the sample is etched in RIE to remove the SiN_x in the square areas. (c) After cleaning in acetone, the sample is placed in 98 °C 34% KOH, for wet etching through the Si wafer. (d) After coating with one layer of co-polymer P(MMA-MAA), one layer of PMMA, one layer of Al, and one layer of PMMA, the sample is patterned by EBL into SINIS junction pairs. (e) After the developing, the etching in diluted NaOH, and the developing again, Al, Ti, Au are deposited in UHV by multi-angle technique. (f) Lift-off in hot acetone finally produces the SINIS junction pairs. (g) The sample is coated with PMMA, a thin layer of Al and patterned by e-beam into hole arrays. (h) The sample is etched in diluted NaOH and developed, then etched again in RIE to make the hole arrays. (i) After cleaning in warm acetone, the final sample of 2D PnC with SINIS junction pairs is produced.

multi-angle deposition were employed to make junctions (see Chapter 3). The under-cut layer was 9% co-polymer poly(methyl methacrylate-methacrylicacid) (P(MMA-MAA)) in Ethyl Lactate (EL 9), spun at the speed 2250 rpm for 60 seconds, followed by one layer of 4% PMMA 950 in anisole, spun at the speed of 1500 rpm for 60 seconds. The sample was baked on 160 °C hot plate for 1.5 minutes after each coating of the resist layer and then kept in a vacuum chamber for at least half an hour to evacuate possible air left inside resists. Before a final top PMMA layer, a 7 nm Al film was deposited on top of the two resist layers by UHV evaporation, aimed to reduce the charging effect, as well as to make clear points for focusing and alignment of the writing field (WF) when patterning. One more layer of 4% PMMA 950 in anisole was finally spun on it also at the speed of 1500 rpm, followed by 3 mins of 160 °C baking. The junction geometry was patterned by 20 kV e-beam at a WF of 100 μm, with a 30 μm aperture. The bonding pads were drew at a WF of 1000 μm, with a 120 μm aperture.

The sample was developed first in developer 1 for 45 seconds, rinsed in IPA for 30 seconds and dried by N_2 flow. Then the Al layer was removed by rising in diluted NaOH solution for 15 seconds and rinsed once by deionized water. A second development by developer 1 was then needed. After that, sample was developed in a 1:2 solution of 2-methoxyethanol and methanol (developer 2) for 8 seconds, rinsed in IPA for 30 seconds and dried by N_2 flow, after which an undercut appeared. Possible residual resist inside the pattern was removed in RIE with O_2 plasma of power 60 W, and 50 mTorr pressure for 30 seconds.

Multi-angle evaporation was used to deposited the metals. First Al was de-posited from two sides, along the lead directions, at angles changing in the series 70°, 65°, 60° (Figure 3.4). The total thickness of the deposition from each side was 27 nm. Then the sample was oxidized at 200 mbar of O_2 for a period of 5 mins, to form the tunnel barrier. Then the sample was rotated by 90° degrees around the surface normal and normal metal TiAu bi-layer was deposited by multi-angle evaporation. The Ti layer served as an adhesion layer for Au. Only one 10 nm layer Ti was de-posited from an angle of 70°. Au was also deposited from angle changing in series 70°, 65°, 60°. The total thickness was 74 nm. The resist was lifted-off by hot acetone, and cleaned by IPA. In addition, for a few membrane samples TiAu bi-layer was also deposited from an angle of 0° to the same thickness for comparison.

Cu was utilized as the normal metal in the first and second design round samples (see Figure 4.1 (a) and (b)). The angle evaporation in scheme was essentially the same with that described above, except that the thickness of Al and Cu were 60 nm and 90 nm, and the deposition angles were 64°, 62°, 60° for Al, and 46°, 44°, 42° for Cu. In addition, a 20 nm protection layer of Au was deposited on top of the Cu,

as Cu is easily destroyed when additional resist is spun on top.

The measurement results show that the total tunneling resistance of a SINIS junction pair using TiAu bi-layer as the normal metal is about 10 kΩ. In contrast, the total tunneling resistance of SINIS junction pair using Cu as a normal metal is about 200 kΩ, hugely increased after the plasma etching of holes. If the SINIS junctions were shorted, for example in bonding, the resulting SNS junctions had a room temperature resistance less than 1 kΩ.

4.2.3   2D PnC structure plasma etching

The Resist for EBL in this step used the same as in the membrane fabrication (Section 4.2.1). Additionally, a layer of 7 nm Al was deposited on top of the resist by UHV zero angle evaporation to reduce the charging effect. The patterning was performed by Eline at 20 kV with a 30 μm aperture. WF was 200 μm for both the 4 μm and 8 μm periods, and 250 μm for the 16 μm period. This way the hole arrays was exposed evenly by the electron beam. Before the development in developer 1, diluted NaOH was used to remove the Al layer as in Section 4.2.2. The patterned hole array was etched through the membrane by RIE using a low temperature nitride etching recipe (CHF$_3$/O$_2$ 10:1, 55 mTor, 100 W). the total etching time was 15 mins 20 s, however, divided into four periods of 6 mins, 6 mins, 6 mins and 3 mins 20 s to keep a relative low temperature. After the lift-off in hot acetone and cleaning in IPA, the sample was ready for bonding. The rms surface roughness of the hole side walls is < 10 nm, estimated from SEM images.

4.2.4   Bonding of samples

It is challenging to bond the sample to the stage, which connects the sample to the measurement set-up, i.e. cryostat (Figure 4.4). There is a high possibility that the junctions electrically break down in this process. That is why special care must be taken to avoid static electricity or excessive voltage drops across the junctions. Sometimes, a SINIS junction pair was electrically shorted to a SNS junction pair. If the other SINIS junction pair survived, such a sample was still measurable, by using the SNS junction pair as a heater.

4.3   Thermal model

The thermal conductance of sample was measured at sub-Kelvin temperatures. It is good to make clear how heat is transported inside the measurement set-up. There
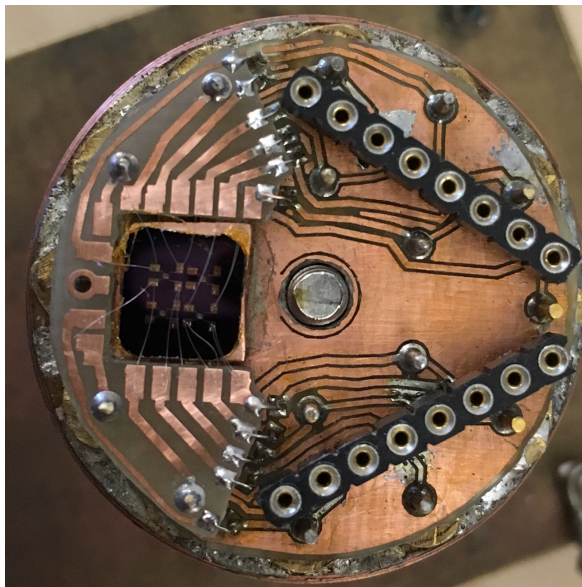
FIGURE 4.4 Example of a bonded sample on the stage.
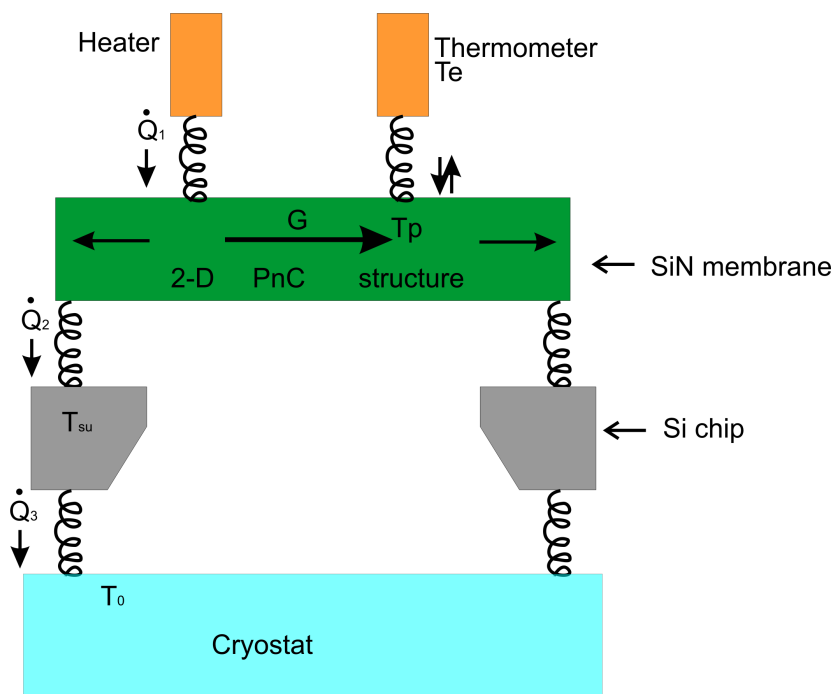

FIGURE 4.5 A simplified thermal model of the measurement set-up.

are two temperatures that are directly measured: the bath temperature (T_0) of the refrigerator measured by a separate Ge thermometer and the electron temperature (T_e) of the normal metal of the SINIS thermometer. The substrate, the Si chip, was always near equilibrium, i.e. the temperature of substrate T_{su} was always very close to the bath temperature T_0. This is because the large volume of the chip, and the good vanished thermal contact between the chip and the sample stage. On the other hand, the SINIS thermometer was always in quasi-equilibrium, meaning that all of the absorbed phonon power is also re-emitted into the structure. Thus, the electronic temperature T_e measured by the thermometer was always the same as local phonon temperature T_p, because minimal amount of heat could leak through the superconducting leads of the thermometer.

The thermometer was always calibrated against the Ge thermometer. In that measurement, no heat source was dissipated in the heater, and only the thermometer SINIS junction pair is current biased. The bias current is set such a way that it neither heats nor cools the normal metal. Thus, the membrane or PnC structure is in equilibrium with the substrate, and $T_e = T_p = T_{su} = T_0$.

When measuring the thermal conductance, T_0 is kept constant so that T_{su} is constant. The thermometer, on the other hand, is thermally isolated from the substrate, due to the weakness of thermal conductance of the membrane and PnC structure. The heater, a source of heat, is voltage biased, which emits phonons into the membrane following Equation 2.22. Neither the temperature of the heater normal metal nor the local phonon temperature at the exact location of the heater can be measured. However, if the thermometer is close to the heater, the thermal conductance between the heater and thermometer is much bigger than the total thermal conductance out of the membrane/PnC structure, and the thermometer will read a phonon temperature that depends on the total thermal conduction.

4.4   Measurement

All measurements were performed in a Nanoway PDR50 plastic dilution refrigerator [53]. The measurement was performed in three steps. The first two steps were the electrical characterization and calibration of the thermometer and the heater. The final step was to measure the thermal conductance, where the heater was biased by a sweeping voltage (increasing power) and the thermometer was biased by a constant current reading voltage that correspond to a temperature (see Figure 4.6 (a)).

The characteristic I-V curve of the thermometer was first measured at a bath temperature as low as possible. The applied voltage was swept from $-V_0$ to V_0 for at least two values. The absolute number of V_0 were chosen: one was relatively large
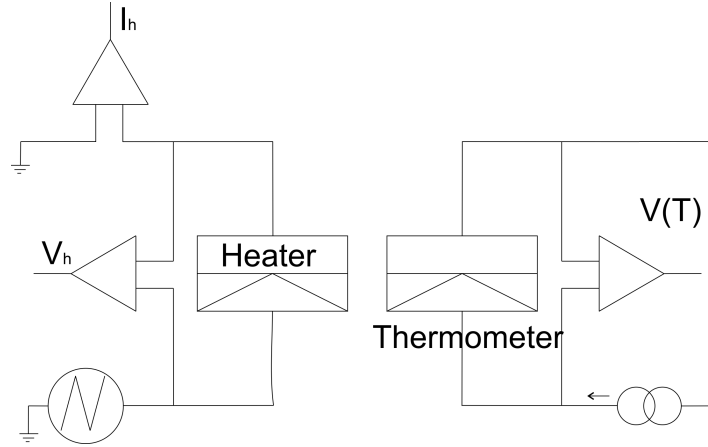
FIGURE 4.6 The circuit for measuring thermal conductance.

much beyond the gap 2Δ to confirm the asymptote of the tunneling resistance R_T and the other was set just above the gap, to get more accuracy of the data within the gap. Often, I-V curves were also measured at different bath temperatures, to help to choose a proper bias current for the other two steps. The bias current was chosen above the sub-gap, the level of current level carried by the Dynes parameter Γ, to retain maximum temperature sensitivity. Meanwhile, there should be no significant heating or cooling effect of the thermometer itself, otherwise the equilibrium between the phonons of the membrane or the PnC structure and the thermometer could be disturbed. This condition is best achieved by setting the bias current just above the sub-gap current level. Calibration, i.e. measurement of the voltage of thermometer by bath temperature, was done as slowly as possible, usually it took more than 12 hours. In this way, the sample and the stage were always in quasi-equilibrium so that the local temperature where the thermometer is localized was the same as the measured stage temperature. Once calibration was started, the measurement circuit was kept untouched, until thermal conductance measurement was performed.

Figure 4.7 (a) shows one example of measured I-V characteristics of a SINIS thermometer. In this plot, it is a thermometer on the PnC structure with 8 μm period. The green and red lines were the chosen bias currents. The 45 pA bias current was most sensitive for the low temperature range, and the 4 nA current was sensitive for higher temperature range. Figure 4.7 (b) shows the differential conductance as a function of the applied voltage of the same SINIS junction. It certifies that this is a SINIS junction pair, as the gap peak feature appears at 2Δ instead of Δ. Figure 4.8 shows the calibration V-T curve of the same junction with the bias current of 45 pA. It was fitted by BCS theory with a thermal model [43], showing very good agreement. Typical junction parameters observed for the TiAu samples are $R_T \sim 10$ KΩ, $\Delta \sim 0.2$
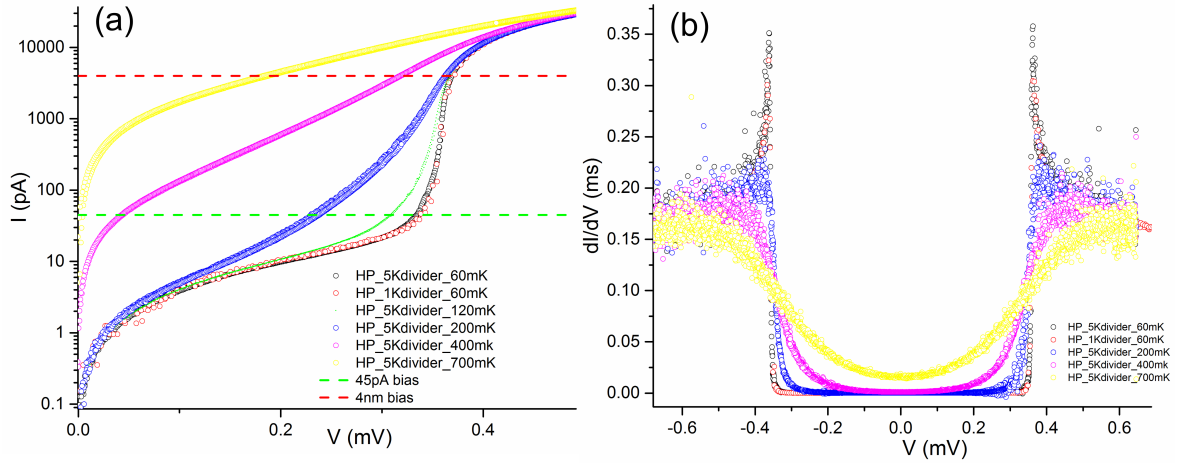
FIGURE 4.7 Characteristics of thermometer. (a) I-V curves at different bath temperature with $R_T \sim 8.6 \ k\Omega$. (b) dI/dV-V curve with $2\Delta \sim 0.38$ meV.

meV, $\Gamma_D/\Delta \sim 10^{-4}$.

This measured calibration curve can then be used to convert a measured thermometer voltage in the heating experiment (Figure 4.6) to temperature, i. e. local phonon temperature T_p. The emitted phonon power from the heater was measured by measuring the heater current I_h and voltage V_h in a four probe configuration, to give the power P_h

$$P_h = I_h V_h. \tag{4.1}$$

Here, we therefore assumed that all electrical power is converted into phonons, i.e. no heat leaks electrically out through the superconducting leads. This was estimated to be good approximation at the lowest temperatures < 0.5 K, where outdiffusion is strongly suppressed by the superconducting gap [54]. Finally, we can plot the heating power against the measured phonon temperature. The thermal conductance could then be defined as

$$G = P(T_p)/(T_p - T_{bath}). \tag{4.2}$$

With Al junctions, the maximum temperature is $\sim$ 1K, but if a higher gap superconductor such as Nb would be used for NIS thermometry [55] measurement could be extended to $\sim$ 7 K.
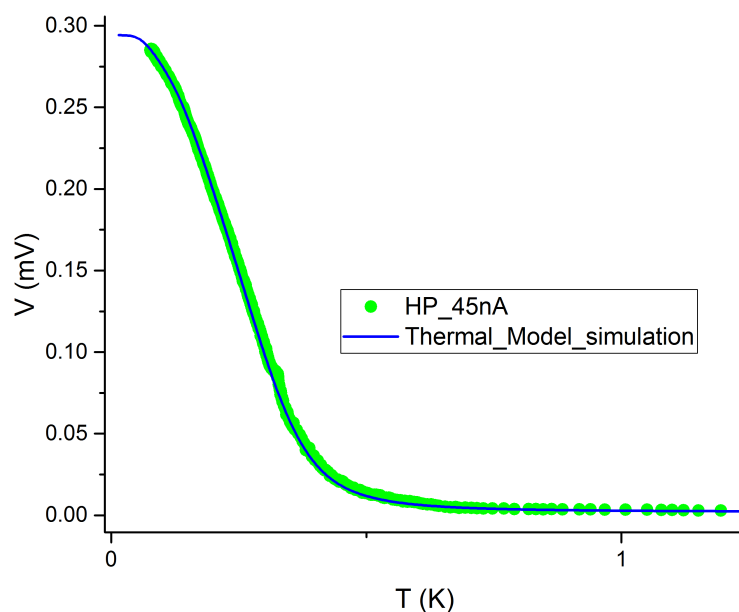
FIGURE 4.8 Calibration of voltage against temperature, the blue line is simulated by the BCS theory with a thermal model.

4.5 Results

4.5.1 Thermal conductance of PnC structures

Figure 4.9 shows a plot of the heating power vs. measured phonon temperature for several 2DPnC structures. All samples here were fabricated with TiAu without normal metal on top of the superconducting leads. The purple data was measured on an uncut membrane of 300 nm thickness. The black, blue and green plots are data from period of 4 μm, 8 μm and 16 μm, with the same membrane thickness. The bath temperature (T_0) was about 95 mK for the uncut membrane, 78 mK for periods of 4 and 8 μm, and 55 mK for the period of 16 μm structures. An observation for this experiment is that the observed reduction is less than what is predicted by ballistic theory, see theory curves in Figure 4.9, even for the 4 μm period. This is in contrast to data from 4 μm period PnC and membrane data with 8 μm long Cu as the normal metal, see Figure 4.10. There we observed the opposite effect of increased reduction as compared to the theory, up to a factor of 130. It is clear to see that the heat flow is blocked in all the PnC samples compared with the membrane sample. This effect is highest at 200 mK to 500 mK for all PnC samples, and is about one order of magnitude reduction. At 350 mK, the thermal conductance of the membrane is 128 pW/K, and 14.6, 7.8, 11.9 pW/K for 16, 8, and 4 μm period PnC, respectively. At 150 mK, the
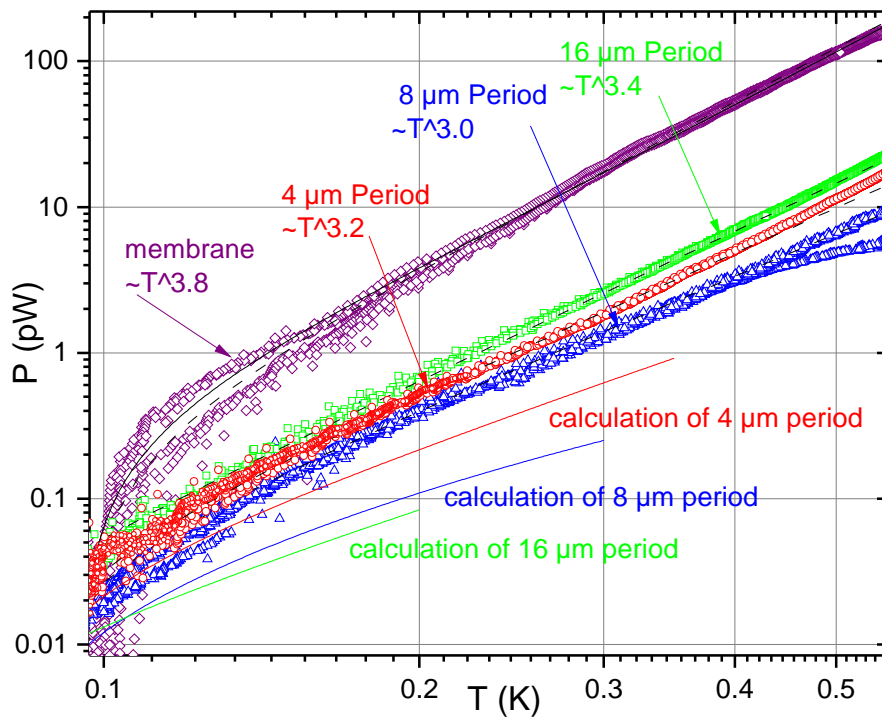
FIGURE 4.9 The measured power vs. temperature for 2DPnC structures and an uncut membrane. The red, blue and green plots are data of period of 4 μm, 8 μm and 16 μm. The purple plots are the uncut membrane data. Solid lines are the calculated theory, and dashed lines simple fits. The theoretical curves were computed by T. Puurtinen by solving the dispersion relation with finite element method and using Equation 2.22.
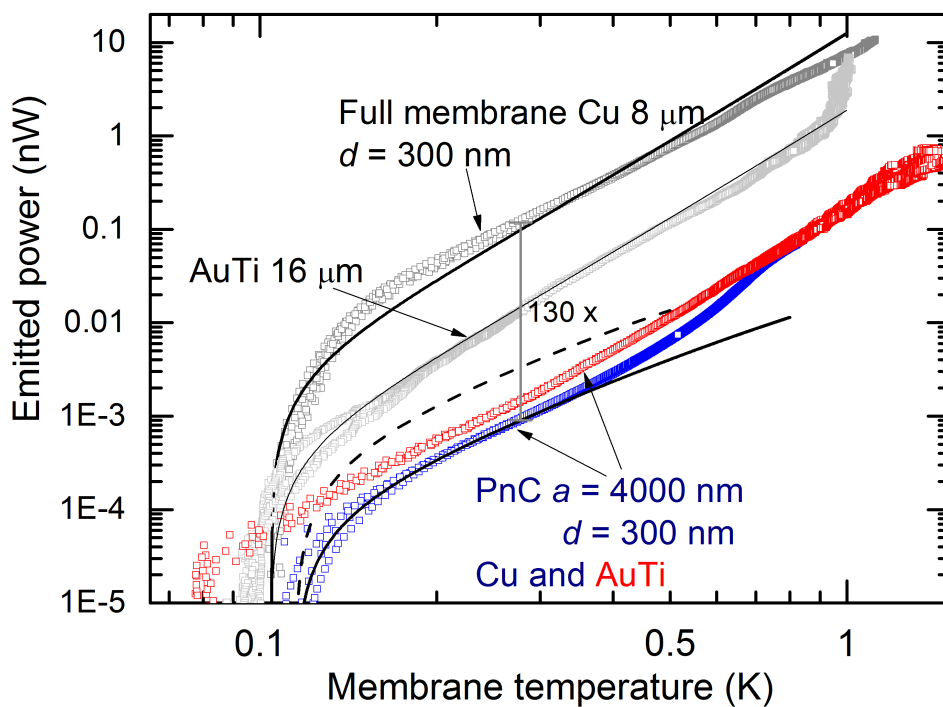
FIGURE 4.10 The measured power vs. temperature for 2D PnC structure of period 4 μm and an uncut membrane measured either by SINIS junctions with 16 μm long TiAu normal metal or by SINIS junctions with 8 μm long Cu normal metal.

measured thermal conductances, are 19, 2.5, 2.2 and 2.6 pW/K for the membrane, 16, 8, and 4 μm PnC structures, respectively. Apparently the lowest heat conductance of all these measured samples is with the PnC period of 8 μm, which indicates that there is a period between 4 and 16 μm giving a minimum thermal conductance. Clearly, the temperature dependence of thermal conductance is quite different between the uncut membrane and all the PnC samples at temperatures below 0.5 K. For the uncut membrane P$\propto$T$^{3.8}$ is consistent with the Rayleigh-Lamb theory [16]. In contrast, the power law exponent is 3.2, 3.0, and 3.4 for 2DPnC structures of 4, 8, and 16 μm period. These lower exponents are generally speaking consistent with previous results [16], as well.

Ballistic theory on PnCs [17], on the other hand, predicts no limit for the reduction of thermal conductance with increasing period, but our experimental observation of a minimum is hardly surprising. The explanation is that when the period of PnC is smaller than a mean free path for diffusive scattering, dominant phonons transport ballistically, and thermal conductance decreases as the period increases, as predicted by theory [16,17]. Once the period is larger than the mean free path, diffusive surface scattering starts to affect coherence, destroying it and thus leading to an increase as the period increases. Note that the counterintuitive possibility that diffusion increases conduction results from the increase of the group velocity, as opposed to the direct effect of scattering decreasing the conductance. Also, the effect of specular scattering off the hole side walls is an interesting question. Further work is required to understand these effects.

4.5.2 Difference caused by the material or the length of normal metal

The measured power against the measured local phonon temperature by SINIS junction pairs of either 8 μm or 16 μm with either Cu or TiAu normal metal length on membrane is plotted in Figure 4.11. The dark cyan symbols stand for the 8 μm Cu normal metal sample, the orange symbols stand for the 16 μm Cu normal metal junction pair, the dark yellow symbols stand for the 8 μm TiAu normal metal sample and the purple ones stand for the 16 μm TiAu normal metal junction pair, which is the same data as in Figure 4.9.

Fitting lines for the 8 μm and 16 μm Cu normal metal SINIS junctions are of the form $P = A(T^n - T_s^n)$ with $n = 2.8$ and $A = 5.2 \times 10^{-9} \frac{W}{K^{2.8}}$ for the length of 8 μm with $n = 3.8$ and $A = 3.6 \times 10^{-9} \frac{W}{K^{3.8}}$ for the 16 μm. Apparently, the power law of the temperature dependence is not the same, and shorter heater/thermometer pair gives a higher power law (lower temperature). In contrast, similar comparison with TiAu
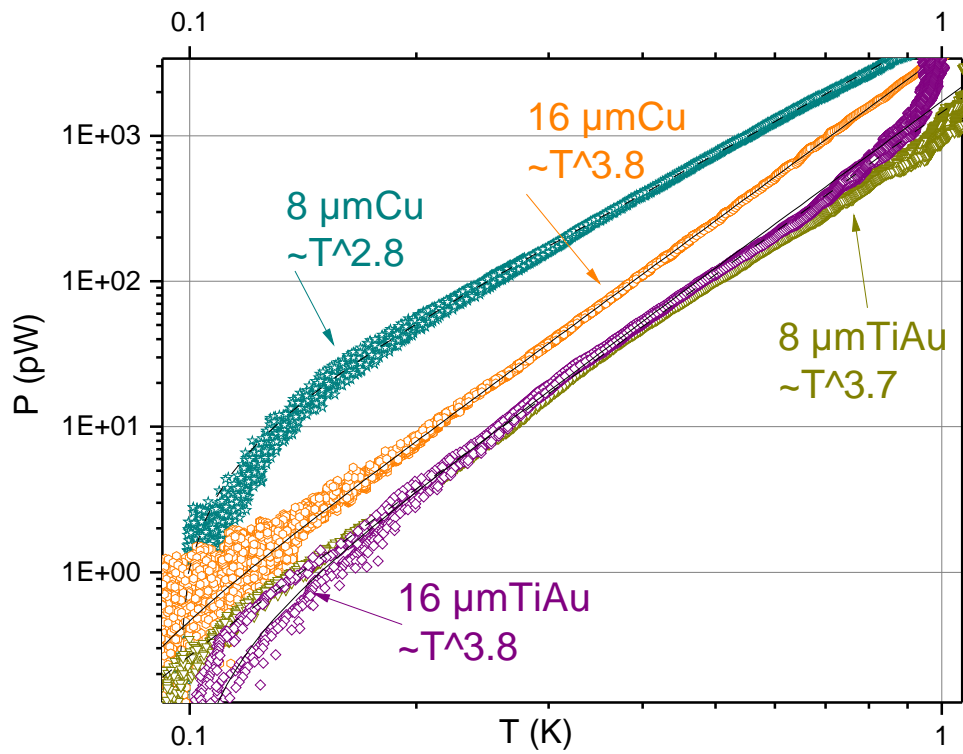
FIGURE 4.11 Membrane measurement using either Cu or TiAu as the normal metal, with heater and thermometer length either 8 μm or 16 μm. The dashed lines and the solid lines stand for simple fit curves of either 8 μm length of normal metal or 16 μm length of normal metal respectively.

as the normal metal shows no difference between 8 μm and 16 μm wire lengths in Figure 4.11. The understanding of these effects is not satisfactory and requires more experiment. Needless to say, to make comparisons, the length of the normal metal should be kept constant.

The plot also shows that the measurement depends on the normal metal material of the junction pair, which cannot be explained by the phonon physics alone. The temperature dependence of both 16 μm samples is $T^{3.8}$, and the ratio of absolute difference about a factor of two. One possible explanation is that the two materials have different electron-phonon coupling constant and Kapitza resistance [56]. This can affect how effectively the thermometer absorbs phonons and thus can lead to varying temperature with the same emitted power from the heater.However, this effect should not influence the relative reduction factor between membrane and PnC, as long as the same material is used in both.

4.5.3   Normal metal on the superconducting lead

(a) Normal metal deposited at zero angle 16 µm TiAu

(b) Normal metal deposited by multi-angle technique 16 µm TiAu
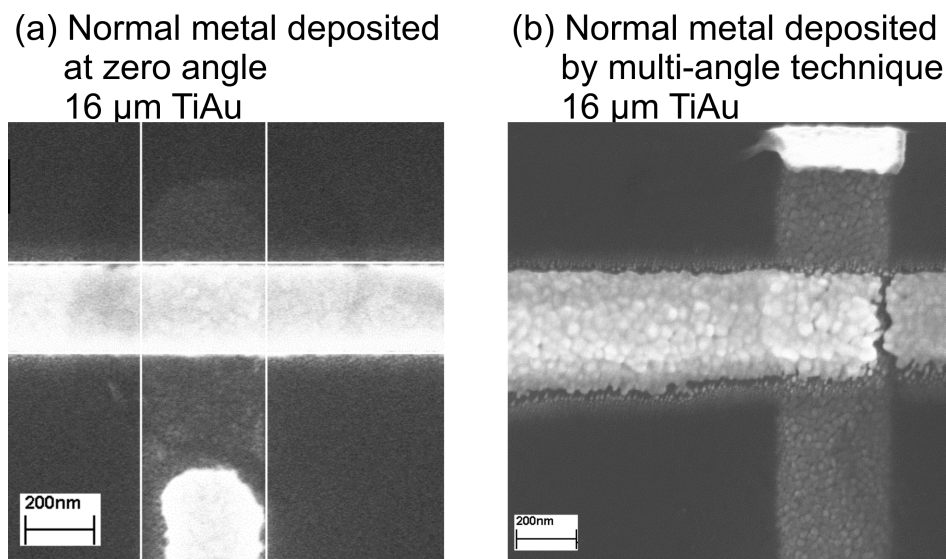
FIGURE 4.12 SEM images of two geometries of SINIS junction. (a) Geometry A, normal metal on top of leads. (b) Geometry B, normal metal not on top of the leads. The crack seen in (b) does not influence the device performance.

There are two ways to fabricate SINIS junction pairs. The normal metal will be deposited on the superconducting leads, if deposited from zero angle. We call this geometry A. When deposited by the multi-angle technique used in this study, called geometry B, it will not land on the superconductor. Figure 4.12 (a) shows a SEM image of the geometry A and (b) shows the geometry B, both are measured samples with data shown in Figure 4.13. Tunneling resistance of the first one is 8.17

$k\Omega$ and the second one is 13.7 $k\Omega$.

FIGURE 4.13 Thermal conductance measured by different geometries. Purple scatters stand for geometry B, and green scatters stand for geometry A.

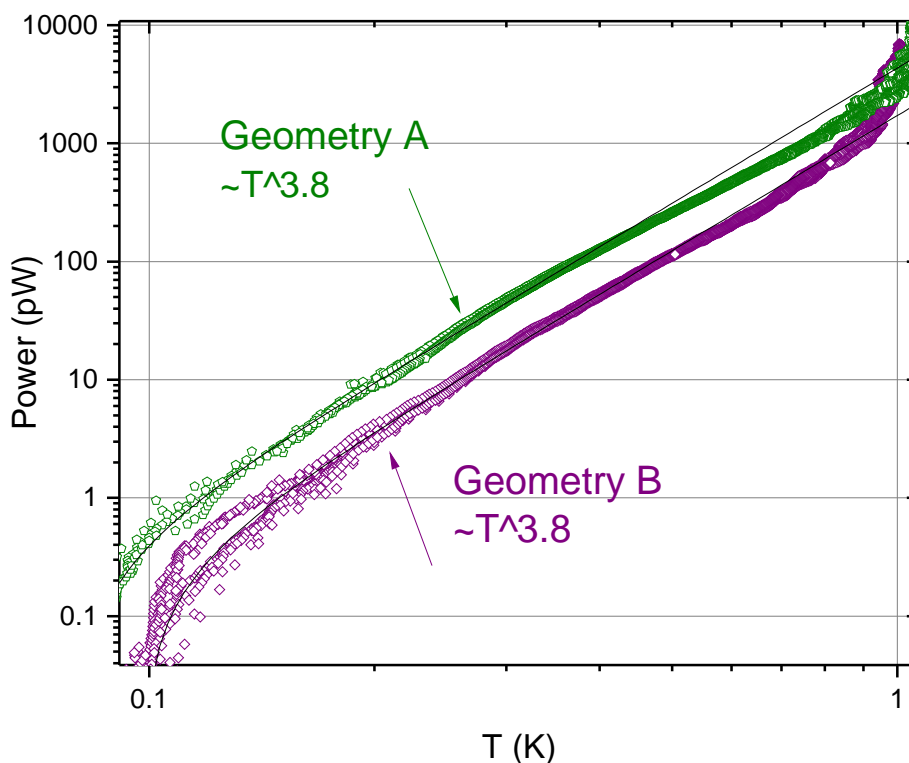Figure 4.13 shows the measured phonon temperature on a membrane measured by two the types of geometries of SINIS junction pairs of TiAu bi-layer as the normal metal. Green symbols stand for geometry A and purple symbols stand for geometry B, which is the same data as showed in Figure 4.9. Again, we see that even this detail can make a difference in the emitted power, but the power law of temperature dependance is the same for both, $n \approx 3.8$. By the fitted lines, the ratio of the power is $\approx \frac{2}{5}$. For type A geometry, emitted phonons can be absorbed by the normal metal, and part of the heat could perhaps diffuse out electrically along the leads. Therefore, part of the heat could be lost from the phonon system, and the measured temperature of phonons can then be lower for geometry A than geometry B for the same applied heating power. Note, however, that this explanation is not fully confirmed at the moment.
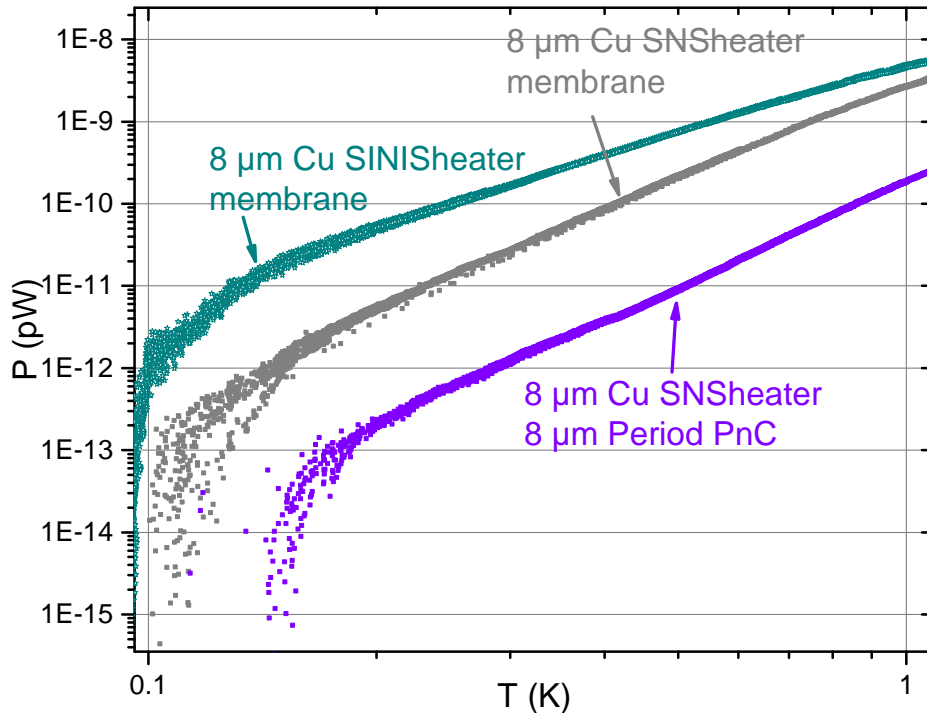
4.5.4 SNS as heater

FIGURE 4.14 Thermal conductance measured using SNS as heater. All samples were using Cu as normal metal high angle deposited.

In the old design of the samples (see Figure 4.1), the SINIS junctions are exposed to the unavoidable plasma etching, which has a high chance to short the junctions. Also, the tunneling resistance of the samples using Cu as the normal metal always increased a lot after the second EBL (hole array etching step). With tunneling resistances as large as 100 kΩ, there was a high possibility to short the SINIS junctions when bonding the sample to the measurement stage. Thus, a SNS junction could be formed and used as a heater. A surviving SINIS junction pair was then used as a thermometer. Measured phonon temperature against heating power was plotted in Figure 4.14, where all the junctions utilized a 8 μm long Cu as the normal metal. The violet symbols stand for a sample with a SNS heater on 8 μm period PnC structure, the gray symbols for a sample with a SNS heater on a membrane, and the dark cyan symbols for a sample with SINIS heater on a membrane, which is the same data as in Figure 4.11.

Comparing the two data measured with SNS junctions as a heater, it is clear that the thermal conductance was reduced by the PnC structures, by over an order of magnitude. The power law of the measured phonon temperature dependence on both the membrane and the PnC structure of periodicity of 8 μm are the same, $n \approx 3.8$, which is the same as measured by 16 μm TiAu SINIS heater on a membrane. In contrast, $n \approx 3.2$ for a 4 μm period sample measured by 16 μm TiAu SINIS heater, and $n \approx 2.8$ for a membrane sample measured by a 8 μm Cu SINIS heater. The reasons once again are not totally understood yet.

Chapter 5

Three-dimensional phononic crystal structures

This chapter is based on articles II, IV and V. Mono-disperse 260 nm diameter polystyrene (PS) nano-sphere solution was self-assembled to 3D PnC structures by a simple dipping method. It was first performed on plain Si chip, with a 10 nm thick TiO_x coating, using concentration of 0.02%, 0.2%, 2%, 5% and 10%, and the dipping speeds ranging from 0.01 mm/min to 0.05 mm/min with a step of 0.01 mm/min. Later, dipping was performed on silicon wafers with in-situ etched confinement boxes of sizes from 50 μm to 300 μm. PS nano-spheres self-assembled well inside boxes of size no larger than 200 μm without cracks, however there were always gaps between the edges of the box and the phononic domains. Finally, polymer boxes were fabricated using 3D lithography and used as a confinement box for the PS nano-sphere self-assembly. As a soft material, the phononic domains of PS nano-spheres were hardened by e-beam irradiation, and coated by an AlO_x layer before metal wiring was successfully fabricated on top of the phononic structures. This process will eventually allow thermal conductance measurement.

5.1 Self-assembly of PS nano-spheres on a plain substrate

Self-assembly is nowadays a common nano- and micro-fabrication technique. Here in this thesis, crystallization was observed by dipping chips in and out of colloidal suspensions of 260 nm diameter PS nano-spheres, purchased from Duke Scientific. In the withdrawal process, capillary forces, gravity and the water evaporation rate are the main factors affecting the assembly of the PnC structures [20, 23, 24]. Thus

we used the dipping angle, the withdrawal speed and the concentration of colloidal solution as control parameters.

5.1.1 Sample preparation and dipping method

All substrates were cut from a silicon wafer of 500 μm thickness with 300 nm SiN_x on both surface. Usually the 8 mm by 16 mm chip was coated with a 10 nm TiO_x to increase hydrophilicity. UHV evaporation was utilized to evaporate the Ti and to oxidize it with 200 mbar pure oxygen for 4 mins.
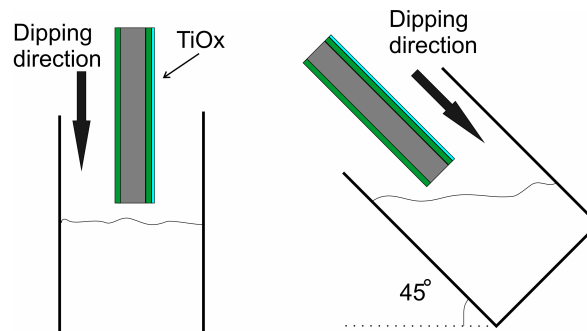

FIGURE 5.1 Schematic of the dipping set-up. Chips with TiO_x were dipped with an angle or vertically.

The dipping was controlled by the dipping set-up. The angle of dipping was set to be either 45° (angled) or 90° (vertical). The original bottle of PS nano-sphere solution is 10% weight to weight ratio. It was diluted to concentrations 0.02%, 0.2%, 2%, 5%, by adding deionized water. The withdrawal speed was set to be from 0.01 to 0.05 mm/min with a step of 0.01 mm/min. The speed was controlled by a gear box.

5.1.2 Dipping results on planar substrates

A top view of a typical colloidal crystal structure is shown in Figure 5.2 (a), with its corresponding Fourier transformed k-space image. A clear hexagonal symmetry is seen in both the real space and k-space data. Figure 5.2 (b) shows the side view of a thick multi-layer 3D PnC crystal. The 3D structure typically seen in these images is face-centered cubic (fcc). The self-assembled crystals typically consisted of many domains, separated by cracks. Domain size data was collected by taking several SEM images from each sample, and using the SEM scale bar as calibration length. All measurements take into account the direction of dipping, where measurements taken along the dipping direction were defined as vertical lengths, while those which are perpendicular along the surface of the substrate were defined as horizontal. Figure
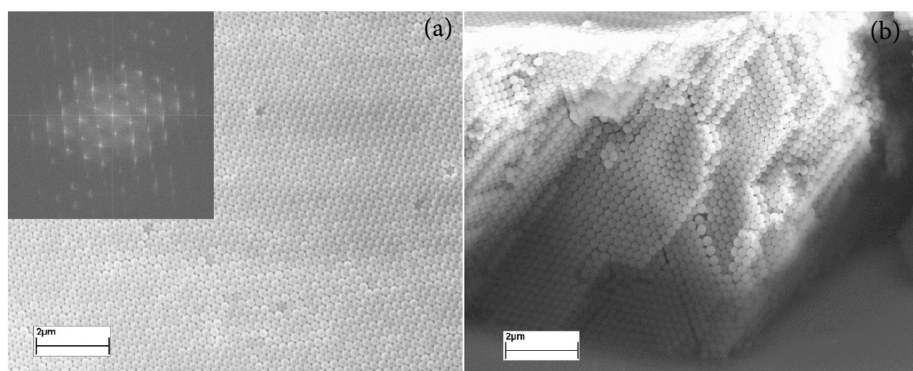
FIGURE 5.2 (a) A top view of a colloidal crystal structure with Fourier transformed image in the inset, (b) with a side-view showing the 3D multi-layer colloidal crystal structure. [IV]

5.3 shows a typical measurement of domain size from a SEM image, which was done at a few locations on each sample. Therefore a large data set was collected in order to improve the statistics.
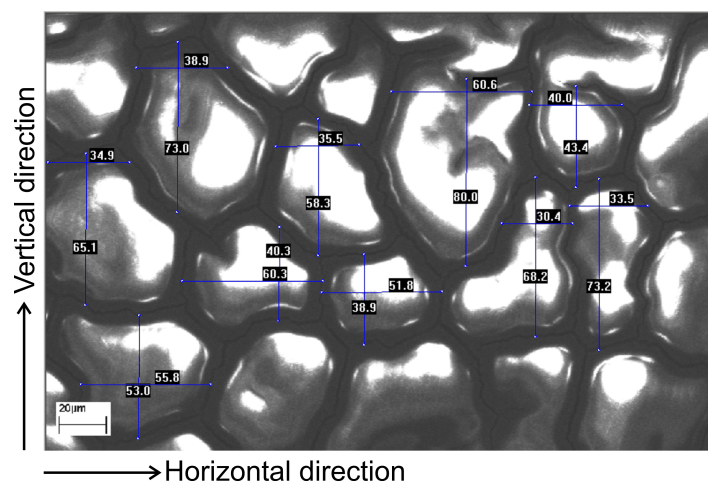
FIGURE 5.3 Example of a domain measurement image is shown, vertically dipped into 2% concentration with withdrawal speed of 0.02 mm/min.

No crystallization was observed for samples dipped into solutions of 0.02% and 0.2% concentration, therefore no data is shown for either of the two concentrations. For all the other concentrations, 3D PnC domains always formed at dipping speeds lower than 0.05 mm/min. Figure 5.4 (a) shows the average vertical domain size for vertical and angled dipping of 2%, 5% and 10% solutions, with dipping speed from 0.01 to 0.04 mm/min. The angled dipping was found to produce smaller domains on average than vertical dipping. It is possible that changes in the shape of the meniscus can alter the evaporation rate at the self-assembly region, which could lead to shorter

effective self-assembly times in the angled dipping cases. It is clear that increasing the concentration and decreasing the dipping withdrawal speed produces larger size PnC domains. However, there is some scatter. For example, for vertical dipping at speeds of 0.02 and 0.03 mm/min , the average domain size does not correlate perfectly with concentration; for angled dipping, the 5% concentration shows only a small change in the average domain size with increasing speed. Figure 5.4 (b) shows ratios of the vertical to horizontal length, giving an indication of directionality in domain growth. It is obvious that the average ratio increases as dipping speed increases. It also shows that the distribution of the ratios widens as dipping speed increases.
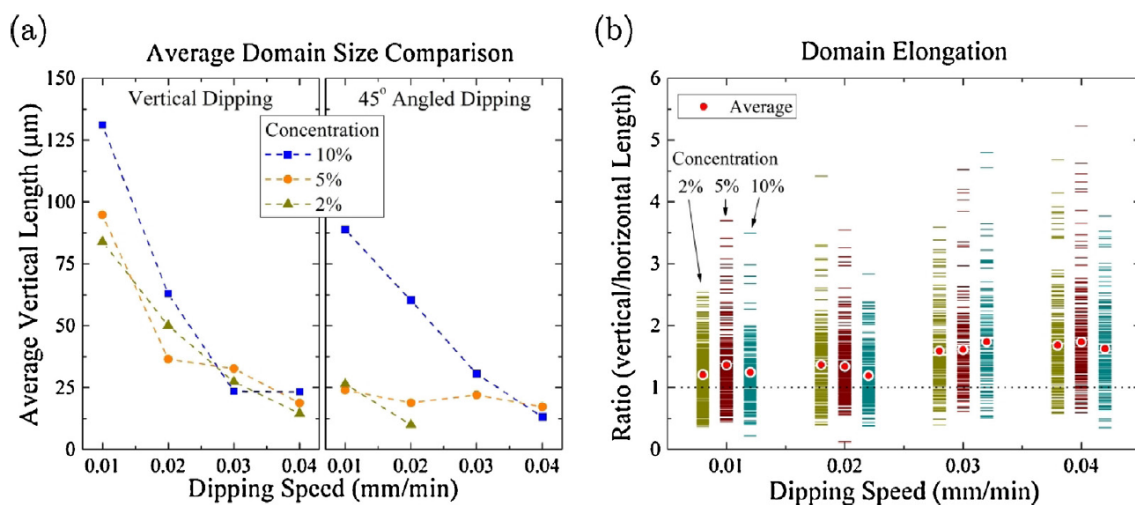
FIGURE 5.4 (a) Average vertical length of domains is plotted against dipping speed for vertical and angled dipping. Clear trends can be seen for dipping speed, concentration and angle. (b) Ratios of vertical to horizontal length of domains are plotted for vertical dipping. Vertical domain elongation and general spreading of domain sizes can be seen. [IV]

The thickness of the 3D PnC films self-assembled vertically from 2% and 10% PS nano-spheres colloidal solution was also investigated, as shown in Figure 5.5. There are several studies on the relation of crack spacing and layer thickness, and of crack patterns in desiccation processes of mud, clay and starch, with thicker layers forming cracks at greater spacing than thin layers [57--59]. The drying of our colloidal crystal structures could be similar to them, however, in a much smaller scale. Thicker films and larger domain sizes are correlated. It seems that this relation is linear for 2% concentration. In contrast, it is non-linear for the 10% concentration, which was expected from literature [57--59].

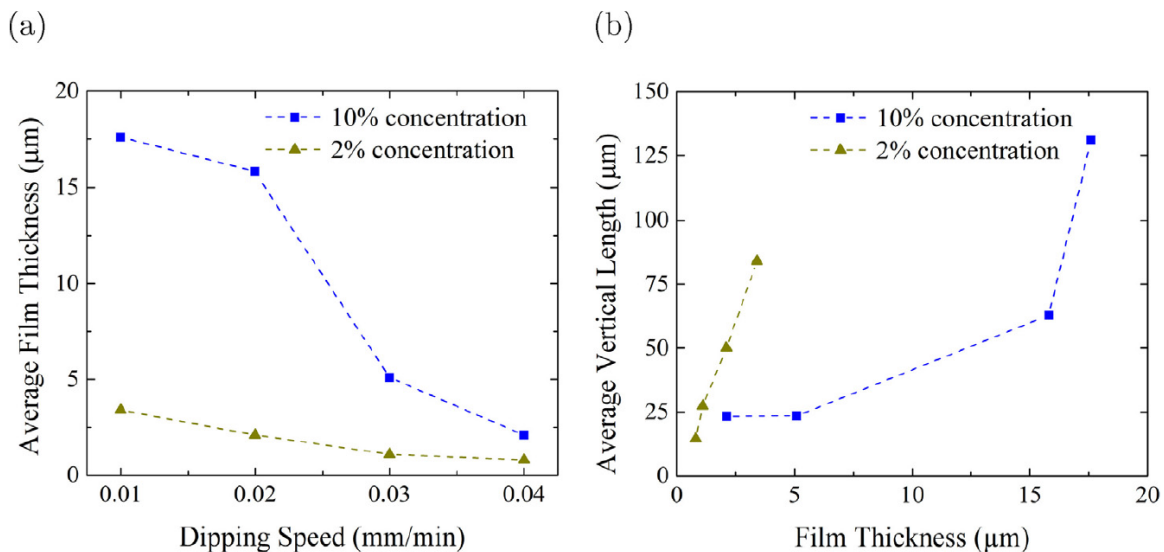(a)

(b)

FIGURE 5.5 (a) Average film thickness is shown for 10% and 2% concentrations as a function of dipping speed. (b) Average vertical domain size is plotted against average film thickness for 10% and 2% concentrations. [IV]

5.2 Self-assembly on in-situ silicon box

The vertical deposition was also carried out on lithographically patterned and etched substrates, to increase the size of single PnC domain and to reduce cracking.

5.2.1 Fabrication process of an in-situ box

Samples with in-situ boxes were made by a two-step e-beam lithography technique, shown schematically in Figure 5.6. The fabrication process of in-situ box was almost the same as the SiN_x membrane fabrication process in Chapter 4 Section 4.2.1. The sizes of squares vary from 50 μm to 300 μm and the etching time from 20 to 40 mins depending on the depth of box, which was either 10, 20 or 30 μm. With the Si crystal orientation of (1,0,0) , the wall of the etched box is not straight, instead there is a 54.74° angle between the wall and the surface of the silicon chip.

In the second time EBL process, the bottoms of the boxes were coated with a 10 nm TiO_x layer. It was not possible to coat the sidewalls of the box accurately enough. E-beam resist was the same as in Chapter 4 Section 4.2.1. The sizes of squares were a little smaller than that in first EBL step and aligned with the first pattern. The development was also done in D1 for 45 seconds, rinsed in IPA for 30 seconds and dried by N_2. The 10 nm thick Ti was deposited in the UHV evaporator with deposition rate of $\sim$ 0.10 nm/s. The TiO_x was grown also by in-situ oxidation by

pure O$_2$, with pressure of 100 mbar for 4 mins. The sample with an in-situ box was ready for dipping after the lift-off process.

(a) E-beam

(b) Developing

(c) Plasma etching

(d) Wet etching

(e) E-beam

(f) Developing

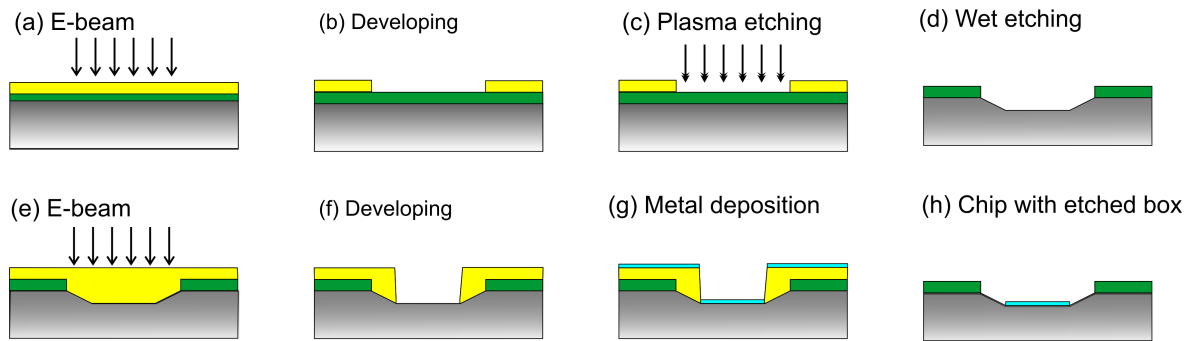**(g) Metal deposition**

(h) Chip with etched box

FIGURE 5.6 Schematic of in-situ box fabrication process. (a) E-beam pattern on chips coated with PMMA. (b) Sample developed in D1. (c) SiN$_x$ etched away by RIE. (d) Si etched in KOH solution. (e) Second EBL aligned with the first pattern. (f) Sample developed again in D1. (g) Ti evaporated and oxidized in UHV. (h) Lift-off.

5.2.2 Dipping results of samples with in-situ boxes

Samples of in-situ boxes were vertically dipped into 2%, 5% and 10% PS nano-sphere colloidal solutions at the speeds varying from 0.01 to 0.04 mm/min. For boxes of 10 μm depth, there was hardly any change in domain sizes compared to areas outside boxes; while for boxes of 30 μm depth, the PS nano-spheres were not able to fill boxes fully. For boxes of 20 μm depth, phononic domains inside boxes showed more consistent order in general than areas outside boxes. There was little or no difference in domain size for boxes smaller than 70 μm compared with areas outside boxes. There were always more than one domain formed inside the box for boxes larger than 200 μm. The results were reproducible. Figure 5.7 (a) shows clearly the increase of domain size within boxes compared to the areas outside boxes. The domain sizes outside the boxes are approximately 30 - 70 μm, while inside the box it is the same as the size of the box, which indicates that a confinement box on chip can be used to suppress the domain size distribution. Figure 5.7 (b) shows a zoom in view of the largest box.

The thickness of 3D PnC domains within the boxes are higher than in the surrounding areas, which could be a possible reason for the larger domain size formed inside the boxes consistent with the correlation in Figure 5.5 (a). The result that there are no small domains inside the boxes indicates that the in-situ box produces the large domains directly. For all domains inside the boxes, they have a polycrystalline order with differing crystal orientations, and single crystal domains size up 10 μm.
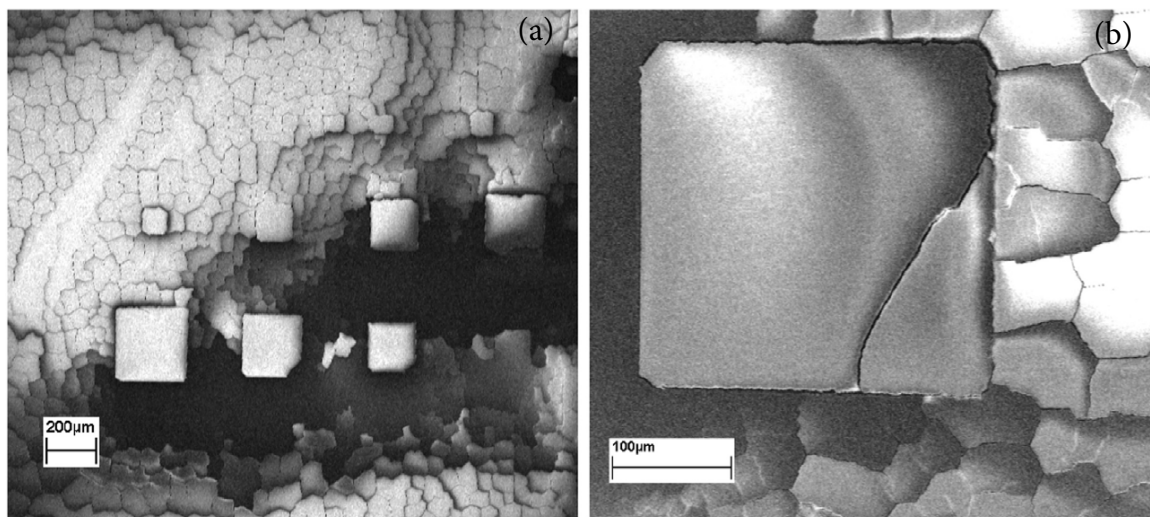
FIGURE 5.7 (a) SEM image of a sample with a range of etch box sizes, after dipped in 10% solution with speed 0.02 mm/min. Areas outside the boxes have domains ranging from 30 to 70 μm, while the etched boxes show significantly larger domains. (b) Close up view of a 250 μm by 250 μm box, seen with a continuous crystalline region several times larger than the surrounding domains. [IV]

However, the gaps between the PnCs and the inside walls of the boxes make it is impossible to fabricate metal wires that cross the gap. There is a material mismatch between the PS nano-spheres as polymer and the silicon wall, which could be a reason for the wide gaps. Therefore, as a next step, polymer boxes were developed and used for the confined self-assembly of 3D PnC structures, to minimizing those gaps.

5.3 Polymer box for PS nano-sphere self-assembly

Polymer boxes were fabricated and used as the confinement box for PS nano-sphere self-assembly. The fabrication process was a 3D process, and 3DL was utilized here. Two operational modes of the Nanoscribe Instrument were utilized here, the normal mode and the DILL mode (see Chapter 3 Section 3.2). The normal mode is easy to operate using a standard glass slide as substrate. However, glass is a bad thermal conductor at temperatures below 1 K. Therefore a polymer box was later fabricated on a substrate of 500 μm thick silicon chip with double-sided 300 nm SiN$_x$, by the DILL mode. Both types of boxes were dipped into 260 nm diameter PS colloidal solutions. 3D PnC structures were obtained
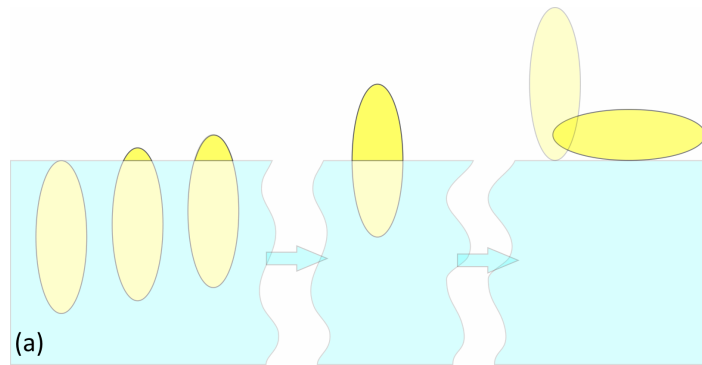
5.3.1 Dose Tests

FIGURE 5.8 Ascending method to do a dose test.

Since the 3DL is a relatively new piece of equipment, a voxel dose test is required to confirm basic parameters for the design of patterned structures. The ascending method is a good way to do a dose test [60]. In it, the focus is moved out of the substrate in steps, until finally a full voxel is exposed, which typically falls on its side (Figure 5.8). The two resists supplied by Nanoscribe GmbH, IPDIP for the DILL mode and IPL780 for the normal mode, were used. The voxel width and length, dependent on the laser power and exposure time, were accurately measured. It is common to have charging effects when imaging non-conductive resists in a SEM, including the resists of IPL780 and IPDIP. Therefore a layer of 15 nm Au was coated on all samples before SEM imaging. The coating was performed by Fine Coat, Ion sputter JFC-1100. The laser beam has a Gaussian wave profile, thus the patterning of resist IPL780 gave a rice shaped voxel (see Figure 5.9 (a) (b) (c)). However, the patterning of resist IPDIP leads to a more complicated shape (see Figure 5.9 (d) (e) (f)). Interference of the reflected laser beam from the substrate surface with the original laser beam is the main reason for this phenomenon.

The maximum input laser power was kept constant at 200 mW, and laser power for each pattern was chosen as a percentage of it. For example, Power 50 means 50% of total power. The power varied from 20, 25, 30, 40, 50, 70 to 80 with different exposure times. The exposure time was set as 1, 2, 5, 10, 20, and 50 ms. The voxel width and length were measured as in Figure 5.9. A voxel was not obtained with power 20 of exposure time less than 10 ms, in contrast, power 80 was too high to make a good shaped voxel. Thus only power levels from 25 to 70 are shown in the result of the dose test (see Figure 5.10). An expose time longer than 10 ms did not help to improve anything, it just consumed time, so exposure times up to 10 ms are shown.

| Power 30, ET 1 ms | Power 40, ET 1 ms | Power 25, ET 10 ms |

Resist IP L780

(a)

length 290 nm
width 115 nm

(b)

length 628 nm
width 178 nm

length 444 nm
width 155 nm

Resist IP DIP

Width1 207 nm
width2 188 nm

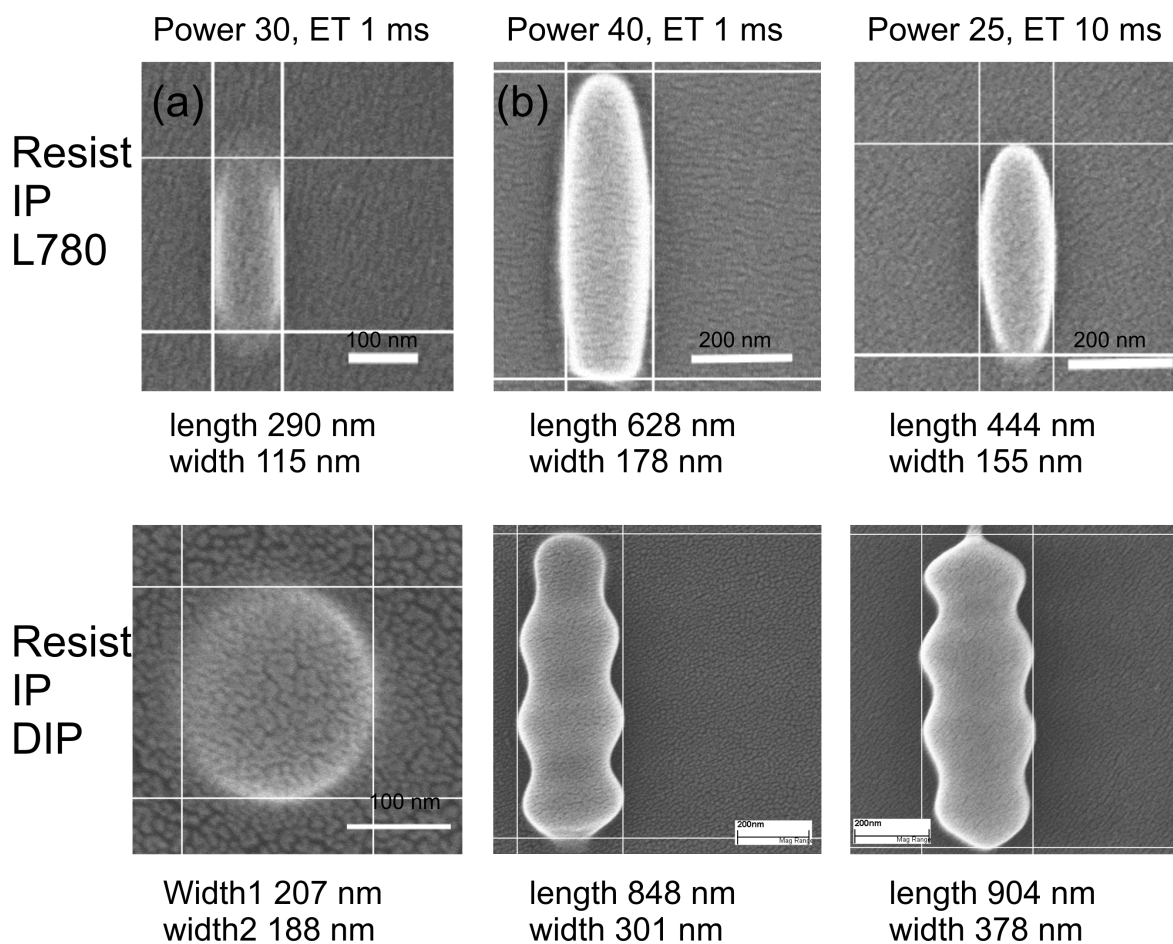length 848 nm
width 301 nm

length 904 nm
width 378 nm

FIGURE 5.9 Examples of voxel dose tests. (a) (b) and (c) are in resist IPL780, (e)(f) and (g) are in resist IPDIP. For both resists, power 30% and exposure time 1 ms did not give a clean voxel, power 25% and exposure time 10 ms resulted in a clear voxel, however it is about the same size as that patterned by power 40% and exposure time 1 ms.
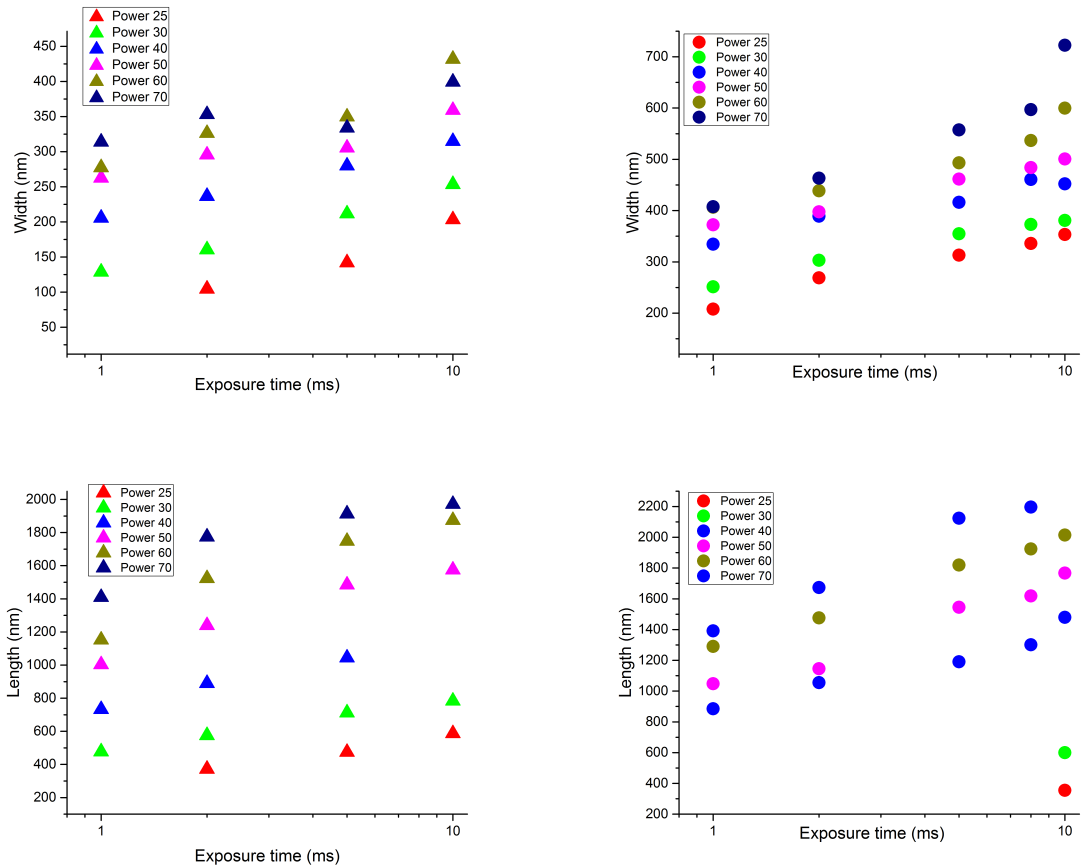
FIGURE 5.10 Voxel dose test results. Voxel width and length vs. exposure time are shown for both IPL780 and IPDIP resists for powers from 25 to 70. Triangle symbols stand for IPL780 resist, and dot symbols stand for IPDIP resist.

Generally, for both resists, the width and length of the voxel increase, as power and exposure time increase. The resist IPL780 gave a voxel width varying from 100 to 500 nm, and length varying from 370 nm to 1970 nm. Power 25 did not give a voxel at exposure time of 1 ms, which means power 25 is too low. For power 40 with exposure time 10 ms, no voxel was observed because apparently it was washed away in development. At an exposure time of 5 ms and 10 ms, the length of the voxel patterned at power 70 is smaller than that patterned by power 60. Power 40 is a good choice, consistent with parameters given by Nanoscribe GmbH. The resist IPDIP gave voxel width varying from 200 to 720 nm, and length varying from 355 nm to 2200 nm. Power 25 and 30 only gave dots at exposure time of 10 ms. Apparently, power 25 and 30 are too low power. Power 70 did not give a voxel at exposure time of 10 ms. It boiled the resist and only gave a dot. So power 70 is too high with exposure time above 5 ms.

Based on the voxel dose tests, linewidth was also studied using the ascending method for the resist IPDIP. One critical parameter for the quality of a line is its scan speed, which corresponds to the exposure time when the using continuous drawing mode. The linewidth against the scan speed was plotted in Figure 5.11. The linewidth decreases as scan speed increases.The patterning time is both decided by the scan speed and the line distances that are proportional to linewidth. So there is a compromise between the scan speed and the line spacing. Figure 5.12 shows that lines drawn at a speed of 400 μm/s were bent too much, and lines drawn at a speed of 300 μm/s were ok. Therefore, scan speed was chosen to be 300 μm/s, and the line distance was set 0.2 μm for test.

The basic pattern parameters for the resist IPL780 was supported by manufacturer. They were power 40, line distance 0.2 μm and a scan speed 300 μm/s. So for fabrication of a box, the line distance was chosen to be 0.2 μm as suggested by manufacturer and the scan speed 300 μm/s.

5.3.2 Polymer box fabrication

Considering the dipping results of the in-situ Si box, and that 3D laser drawing is indeed time consuming, the size of polymer box in IPL780 resist was chosen as 100 μm $\times$ 100 μm with height 20 μm. The height was first set to be 10 μm for comparison, increased to 20 μm later.

At the beginning, we made trials with a small solid volume of 30 μm $\times$ 30 μm with 10 μm high. Parameters were set as power 40, vertical spacing 0.2 μm, line spacing 0.2 μm and scan speed 300 μm/s. The result showed that there was always significant shrinkage of the box after the development. This was an unavoidable result
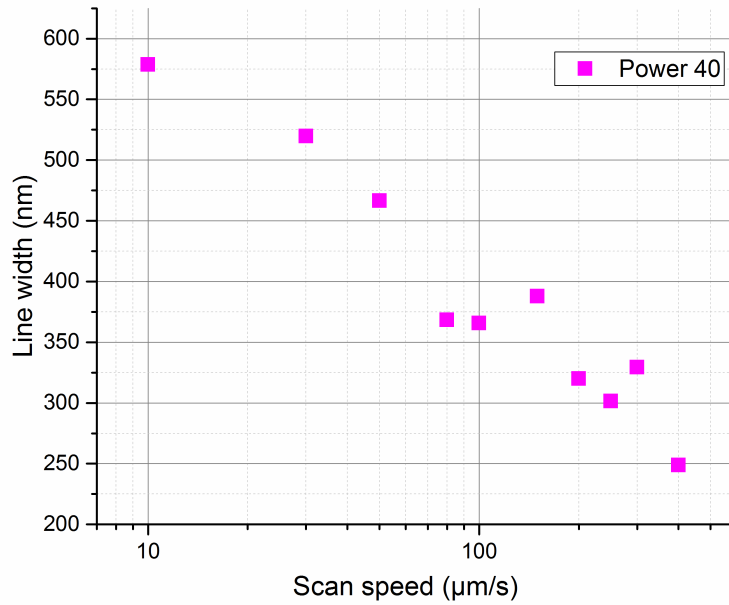
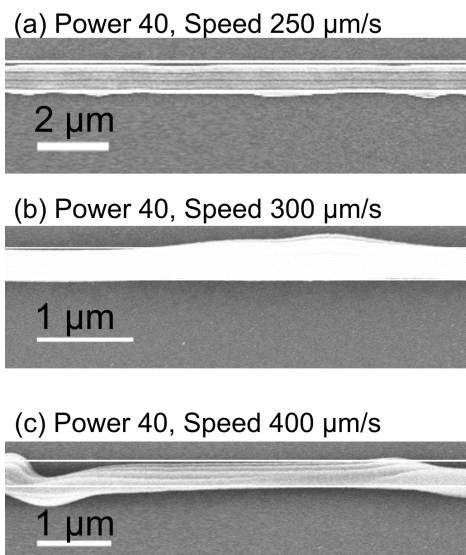**FIGURE 5.11** Linewidth against scan speed at power 40 for IPDIP.

FIGURE 5.12 Lines draw with power 40 at scan speed of 250, 300 and 400 μm/s.
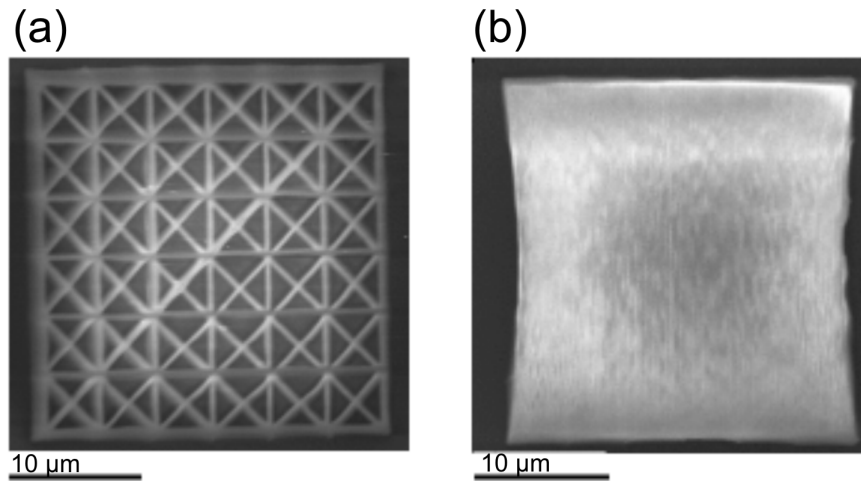
FIGURE 5.13 Box fabricated by IPL780 resist. (a) A frame and (b) a frame with cover.

of the process of the development. A straightforward improvement of the design was to make the box partially hollow. So a box design was developed consisting of a frame and cover layers. The frame was set to be built from triangles (see Figure 5.13 (a)) to maximize stability. Unexposed liquid resist was drained through holes in the frame. In addition, the total volume needed for patterning was less than half of the volume of the box, and thus the total process time was halved. Figure 5.13 (a) shows that there was almost no shrinkage with only the frame in place, however the shrinkage appeared again as soon as cover layer was added on top (see Figure 5.13 (b)).
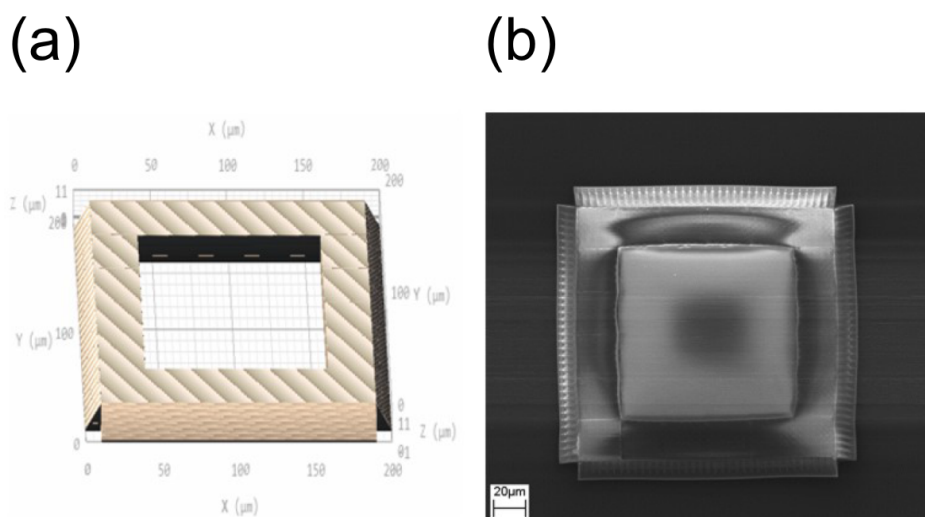

FIGURE 5.14 The design of the 3D resist box. (a) Schematic design, with walls and slopes surrounding outside walls. (b) SEM micrograph of a fabricated structure from top view.

Side-supporting structures (Figure 5.14 (b)) were added to the final box. Shrinkage was then reduced to within acceptable range.
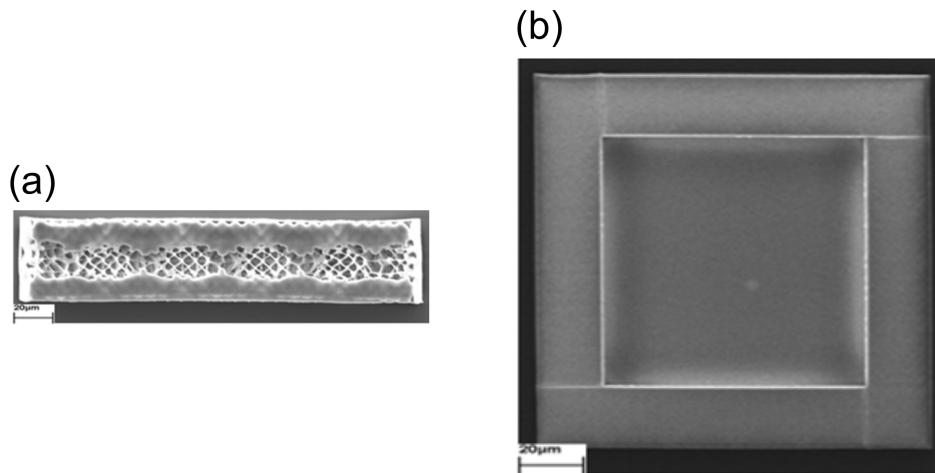
(b)

(a)

FIGURE 5.15 (a) One side wall with constant power for all layers. (b) Box successfully draw by increasing the power as height is increasing.

A box as high as 20 μm was harder to obtain using the same patterning parameters as those used in fabrication box of 10 μm height. It seemed that the top layers were always underexposed (see Figure 5.15 (a)). The reason is that the structure was drawn from the bottom to the top, using the normal mode patterning. Thus, the laser beam had to go through an already patterned layer to draw the next layer. Thus, laser power can then be weakened by having to go through solid resist. A possible reason is that the exposed resist has a higher refractive index than unexposed resist. This effect was always there, however, it was not noticeable until the designed structure was higher. Therefore, laser power had to be adjusted as a function of the height, with higher layers drawn with larger power, and a few top layers were using power 70. Thus, box as high as 20 μm was obtained (see Figure 5.15 (b)).

Later, polymer box using IPDIP resist was also fabricated. There was also a shrinkage problem, and a similar design as was used as above. In this case, there was no attenuation of the laser power, because for this resist as the drawing starts from the bottom of the substrate to the top of the substrate, the focus moves upwards instead of through the exposed resist. All boxes fabricated in IPDIP were 20 μm high. The size of the boxes was 70 μm $\times$ 70μm $\times$ 20μm, and the hollow area was about 50 μm $\times$ 50μm. Some boxes with middle slopes aimed at supporting leads for mounting the measuring event devices for thermal transport were fabricated (see Figure 5.16 (a)); some boxes with extending supports at the corner were fabricated (see Figure 5.16 (b)). It is clear that the box with corner supports produced more straight walls. The box without Au coating (see Figure 5.16 (b)) by optical microscope was dipped
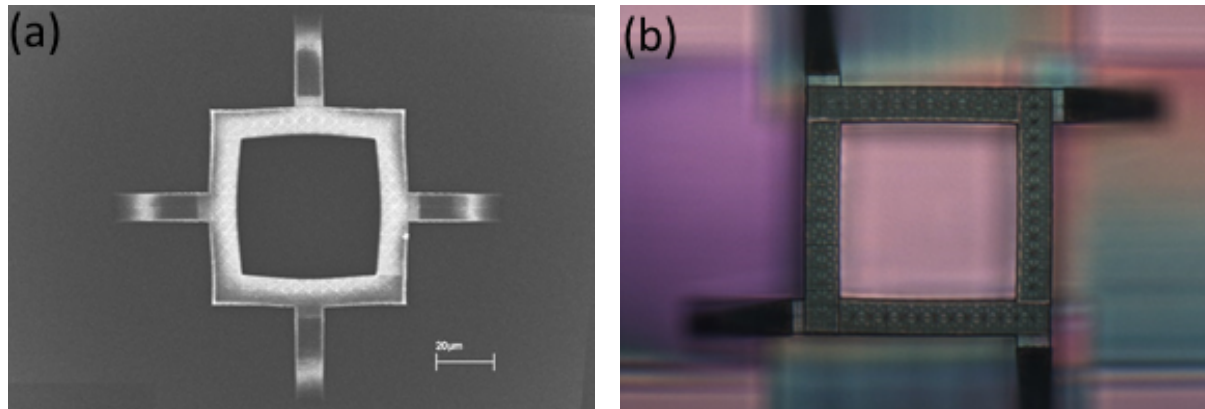
FIGURE 5.16 Box fabricated by IPLDIP resist. (a) A SEM image of a box with slopes for metal wiring. (b) A optical microscope image of box with corner supporting slopes.

into PS nano-spheres solution.

5.3.3 Dipping of polymer boxes

Boxes made from IPL780 of 10 μm height were vertically dipped into 260 nm diameter PS nano-sphere colloid solutions. Concentrations were 0.2%, 1% and 2%, diluted from the 10% original bottle. Withdrawal speeds were 0.01 mm/min and 0.02 mm/min. Only chips dipped into 1% PS nano-sphere colloid solution at speed of 0.01 mm/min gave good crystal structure inside boxes. The withdrawal speed of 0.02 mm/min was too high for all concentrations used. The 0.2% concentration was too diluted and the 2% concentration was too dense at both dipping speeds.

It is obvious from Figure 5.17 that there were almost no spheres deposited on top of the boxes. There were also no PS nano-spheres on the side supporting walls except on the top one, and there were even no PS nano-spheres under the box. In contrast, there were PS nano-spheres everywhere except on top of the box if the box did not have supporting walls. It seems that the exposed IPL780 resist layer on bottom protected the substrate from the self-assembly of the nano-spheres. This result is promising for integrating metal wires of the measurement set-up onto 3D phononic crystal structures. The gaps between the walls of the box and the phononic crystals did not totally disappear, but got much better as compared to etched Si boxes. One possible reason is that the domain size was smaller than the hollow area of the box. A single domain covering the whole box can be obtained by reducing the box area or increasing the box height.

A box made from IPDIP was studied after the above box dipping was done. Therefore, the size of box made from IPDIP on silicon wafer was set to 50 μm
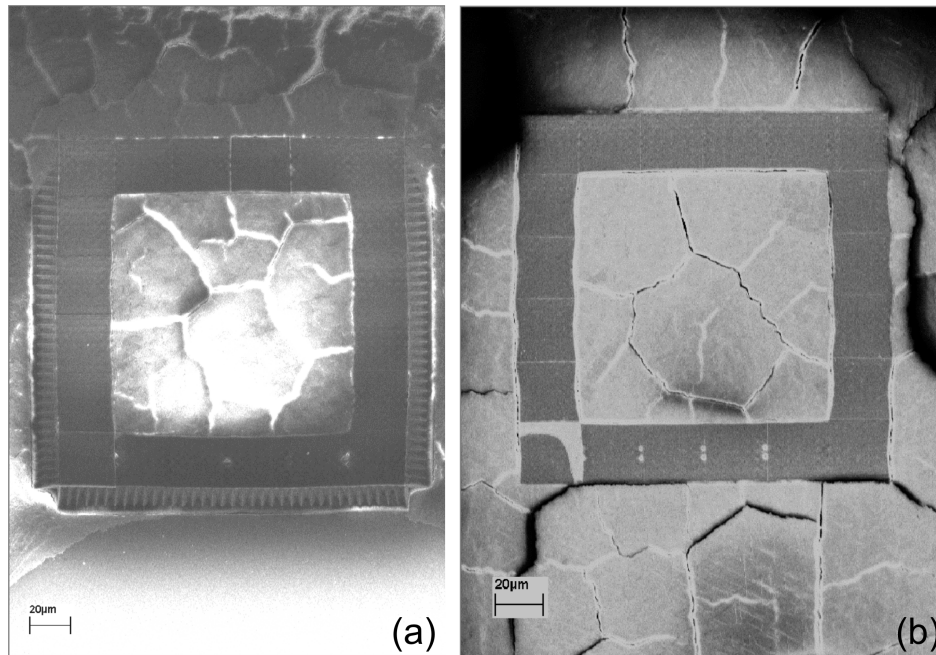
FIGURE 5.17 A sample with a box made of IPL780 dipped into 1% concentration PS nano-sphere solution at a speed of 0.01 mm/min. (a) shows box with side supporting wall and (b) shows box without side supporting wall. The top of the images were lifted out of the solutions first.

$\times$ 50 μm $\times$ 20 μm. Samples were dipped into polystyrene colloid solutions with concentrations of 5%, 2% and 1% at withdrawal speed of 0.01 mm/min. The dipping results show that 5% and 2% solutions formed too thick crystals. The dipping from the 1% concentration solution gave the optimal self-assembling crystals, which have close packed crystal structures. This dipping result was almost the same as that for the in-situ silicon boxes. As expected, there was one single domain as large as the hollow area of the box formed. Unexpectedly, there were also gaps between the domain and box walls in some regions, and there were PS spheres everywhere even on top of the box walls. This indicates that there is difference between the two resists. Resist IPL780 seems to be more hydrophilic than the resist IPDIP.

In the future, it is worth fabricating a box of IPL780 with a hollow area of 50 μm $\times$50 μm $\times$ 20 μm and dipping into 1% concentration 260 nm diameter PS solution at a withdrawal speed of 0.01 mm/min. It is expected that hollow area of the box then fully covered by PS nano-spheres, meanwhile there should be no PS nano-spheres on the top of the box. Hexagonally shaped box, which is harder to fabricate by wet etching for the in-situ Si box than by 3DL, is an option to help to possibly remove the gaps. In addition, sapphire could be finally used as a transparent substrate for measurements at low temperature.
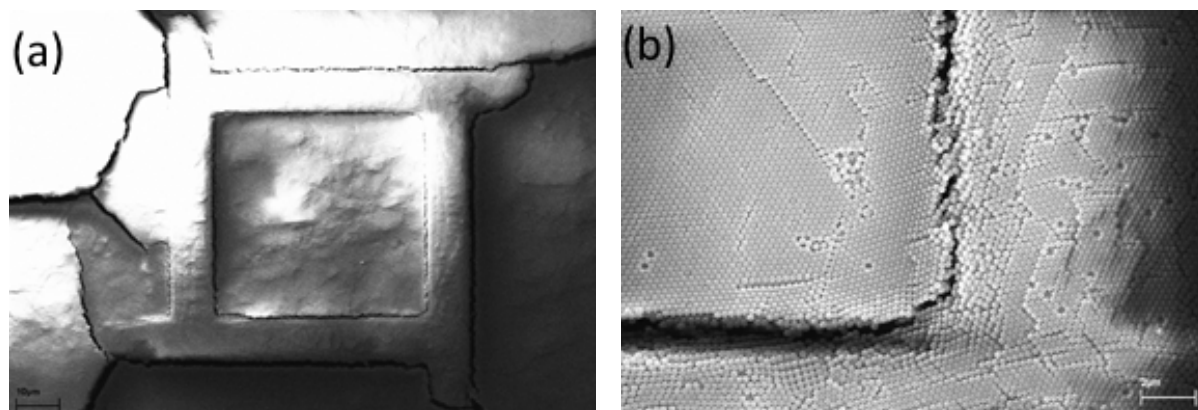
FIGURE 5.18 A Box fabricated by IPLDIP resist. (a) A SEM image of box with cover and slops for metal wiring. (b) SEM image of a corner of the box, where gap is not wide.

5.4 Treatment of 3D PnC crystals

The measurement of thermal conductance on our self-assembled 3D PnC structures requires mounting metallic thermometers and heaters, such as SINIS junction pairs (see Chapter 4), on top of it. EBL is involved for metal deposition and many processes used in standard EBL techniques are known to damage the PS nano-spheres. For example, baking of e-beam resist at 160°C is above the normal glass transition of polystyrene, destroying the spherical shape of PS nano-spheres, and acetone used in standard lift-off process will dissolve polystyrene. To protect the PS nano-spheres from those damages, e-beam irradiation was used to harden the PS nano-spheres by cross-linking the polymers [61]. The irradiation is performed by SEM, thus the irradiation area can be controlled to be a rectangle shape. With help of an AlO_x capping layer, Al wires were successfully deposited on top of self-assembled PS 3D PnC structures.

5.4.1 Metal wire deposition process

The schematic of the evaporation Al metal on top of a colloidal 3D PnC structure is shown in Figure 5.19. Dipped colloidal 3D PnC plain samples were irradiated inside a vacuum chamber of SEM, carried out by a JEOL JSM-840A scanning electron microscope, operated at a higher 30 kV accelerating voltage. All exposures were performed at 600 X magnification, giving an exposed area of 230 μm $\times$ 160 μm. The beam current was varied from 75 pA to 0.4 nA, with a constant exposure time of 5 mins. Therefore, the area dose ranged from 60 nC/cm^2 to 326 mC/cm^2. Irradiated samples were immersed in acetone for several minutes. For high enough doses

(a) PnC structures
on plain chip

(b) ebeam irradiation

(c) Merged into,
out of acetone

(d) AlOx deposition

(e) Spinned resist on

PMMA

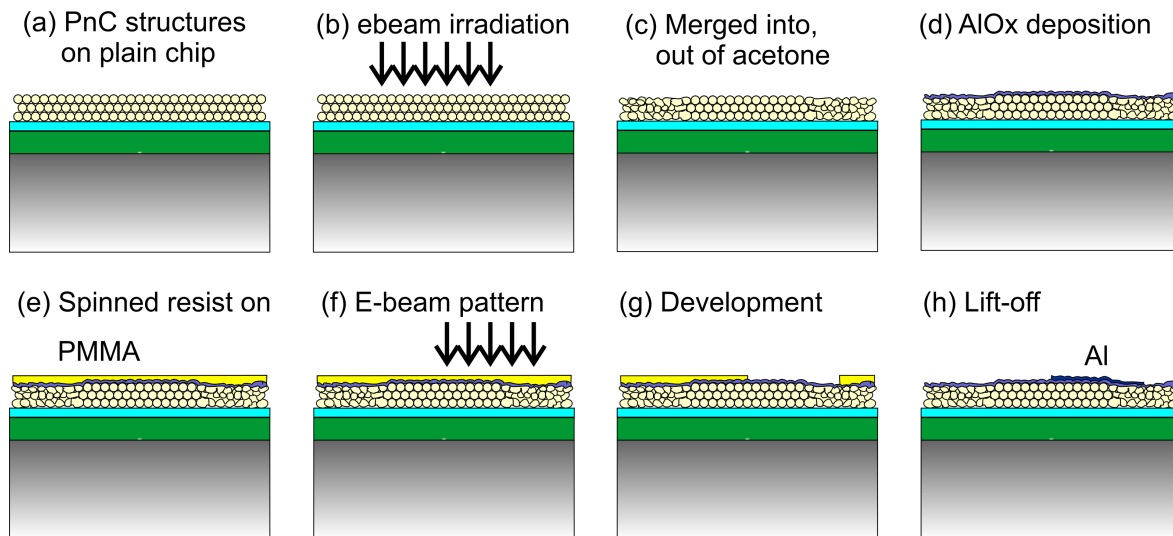(f) E-beam pattern

(g) Development

(h) Lift-off

Al

FIGURE 5.19 Schematic of evaporation Al wire on top of 3D PnC structures. (a) Plain Si chip with a thin layer of TiO_x with 3D PnC structures on top. (b) E-beam irradiation. (c) Sample was immersed into room temperature acetone. (d) Deposition of AlO_x on sample. (e) E-beam lithography resist was spun normally on top of sample. (f) E-beam patterning. (g) Development. (h) Lift-off, removing unnecessary parts by acetone.

above $\sim 2200 \ \mu C/cm^2$, the exposed areas were not dissolved in acetone while the surrounding unexposed areas were dissolved (see Figure 5.20).

As the irradiated sample did not have a smooth surface for further EBL, an AlO_x layer of thickness 100 nm was deposited on top of it before spinning the PMMA resist, which was performed by Balzers BAL-TEC BAE 250 evaporator using a rotatable sample stage and angle evaporation from 70 degrees. A layer of co-polymer P(MMA-MAA) and two PMMA layers of thicknesses of 400 nm and 200 nm $\times$ 2 respectively were spun. The coated sample was then patterned by Raith e-LiNE with a 20 kV accelerating voltage, developed in D1 solution for 60 seconds, rinsed in IPA for about 30 seconds and dried by N_2. On the sample, Al lines of 40 nm to 80 nm thickness were fabricated in UHV evaporator. Finally, the sample was lifted-off in room temperature acetone for 30 minutes, applying a mildly turbulent flow from a syringe, and dried by N_2 gas.

5.4.2   Metal wire deposited on top of 3D PnC domains

Conducting metal wires of a few hundred μm in length and as narrow as a few μm were fabricated cross a irradiated and its surrounding areas. The roughness at the edge of wires (see Figure 5.21 (b)), was found to be low enough indicating there is possibility of producing wires approaching the diameter of the PS spheres. However,
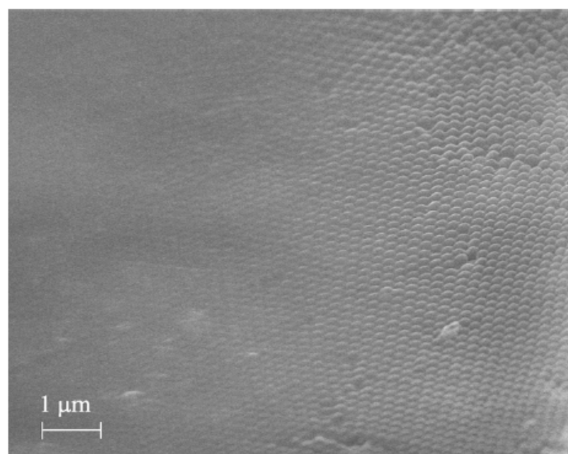
FIGURE 5.20 The edge of an e-beam exposure area, showing a gradient of dissolution after immersion in acetone.
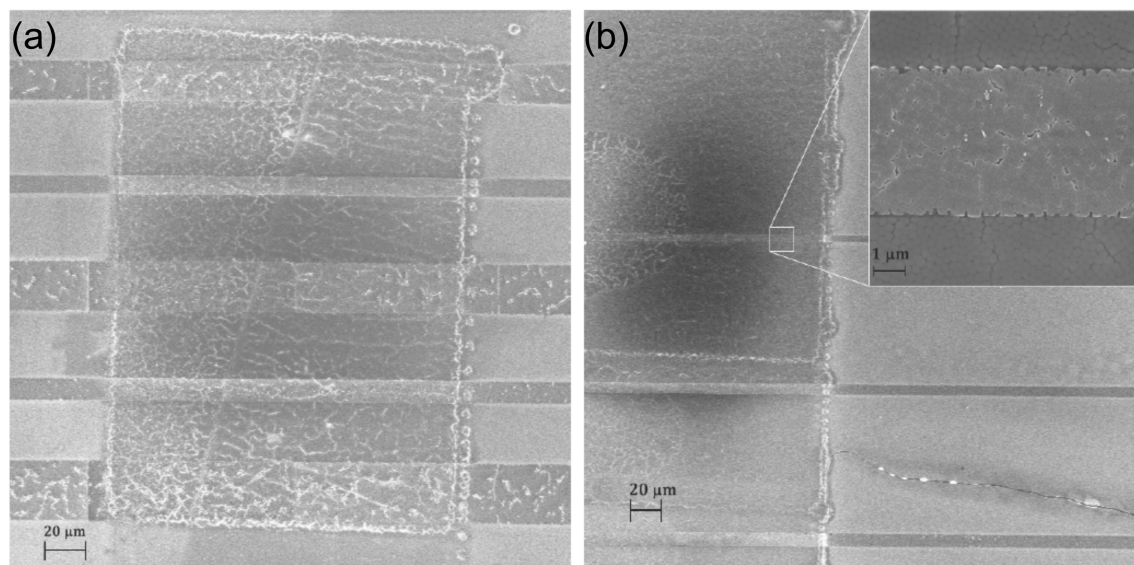
FIGURE 5.21 (a) Al wires of varying width deposited on colloidal crystal surface with AlO_x capping layer. Scale bar is 20 μm. (b) Thinnest Al wires were a few micrometers. The roughness of the metal wire edge (inset) is on the order of the sphere size.

there can still be problem with continuity and electrical conductivity for longer wires. Further development of lithographic processing is expected to enable the fabrication of about 500 nm wide conducting metal wires on top of the 3D PnC structure.

Chapter 6

Summary

In this thesis, two-dimensional microscale periodic structures were fabricated on 300 nm thickness SiN_x membrane, using electron-beam lithography. Three-dimensional periodic structure were fabricated by self-assembling polystyrene nano-spheres either on a plain chip with TiO_x on surface, or on patterned chips with etched boxes with TiO_x on the bottom, or on samples with polymer boxes patterned by three-dimensional laser lithography. PS nano-spheres were protected from deformation for their spherical shape and dissolution into acetone by e-beam irradiation hardening. Using an AlO_x capping layer, metal wires were successfully deposited on 3D PnC structures.

Three simple 2D square arrays of holes of periods 4, 8, 16 μm were fabricated, with a filling factor of the holes of 0.7. Thermal conductance was measured on all three different periodic structures, and compared with membranes at temperatures from 50 mK to 1.2 K using SINIS thermometry. All PnC structures gave a much lower thermal conductance than the membrane. The thermal conductance of the 8 μm periodic structure was the lowest, which indicates that there is a period between 4 and 16 μm giving a minimum thermal conductance for 300 nm thick SiN_x. More theoretical work is required to explain this result.

Statistics of 3D colloidal crystal domain sizes were collected by varying the dipping withdrawal speed, the concentration of PS nano-sphere colloidal solution, and the dipping angle on plain chips. It turned out that lower speed, higher concentration and vertical dipping produces larger and thicker 3D PnC domains. The relation is not necessary linear. Samples with etched in-situ silicon boxes were vertically dipped. Single 3D PnC domain was self-assembled in 20 μm deep boxes of length no larger than 300 μm. Depth and size of the boxes directly affect the self-assembly of PS nano-spheres. Unfortunately, it is still challenging to fabricate a thermal conductance measurement device, because of gaps between the domains inside the confinement box and the wall of the confinement box were large. To study the effect

of box material, samples with boxes made from polymers of two types were utilized for self-assembling 3D PnC structures by vertical dipping. It seems that the IPL780 polymer resist is more hydrophilic than the IPDIP polymer resist. The height and the size of the box are two main factors affecting the self-assembly, consistent with previous results. In the future, IPL780 photoresist with hollow area of 50 μm $\times$ 50 μm to 100 μm $\times$ 100 μm and as high as 20 μm should be fabricated and dipped to fabricate a crack-free and gap-free domains inside the polymer box. It is also possibly interesting to use a sample with both an in-situ silicon box and a polymer box, by aligning two fabrication steps. Even though Al wire as narrow as a few μm with side edge roughness of hundreds nanometers were successfully fabricated on top of 3D PnC domains with the help of irradiated polystyrene and a capping layer of 100 nm thick AlO$_x$, it is still somewhat challenging to deposit long wires with good continuity and electrical conductivity. As soon as both longer conductive metal wires and crack-free and gap-free domains are observed inside the confinement boxes, the thermal conductance of 3D PnC structures can be measured.

Bibliography

[I]   This thesis article **A.I.**

[II]   This thesis article **A.II.**

[III]   This thesis article **A.III.**

[IV]   This thesis article **A.IV.**

[V]   This thesis article **A.V.**

[1] M.S. KUSHWALA, P. HALEVI, L. DOBRZYNSKI, B. DJAFAR-ROUHANI, *Acoustic Band Structure of Periodic Elastic Composites*. Phys. Rev. Lett. **71**, 2022-2025 (1993)

[2] M. SIGALAS, E.N. ECONOMOU, *Band Structure of Elastic Waves in Two Dimensional Systems*. Solid. State. Com. **86**, 141-143 (1993)

[3] S. YANG, ET AL., *Focusing of Sound in a 3D Phononic Crystal*. Phys. Rev. Lett.**93**, 024301 (2004)

[4] Y. PENNEC, J.O. VASSEUR, B. DJAFARI-ROUHANI, L. DOBRZYNSKI, P. DEYMIER, *Two-Dimensional Phononic Crystals: Examples and Applications*. Surf. Sci. Rep. **65**, 229-291 (2010)

[5] T. GORISHNYY, C.K. ULLAL, M. MALDOVAN, G. FYTAS, E.L. THOMAS, *Hypersonic Phononic Crystals*. Phys. Rev. Lett.**94**, 115501 (2005)

[6] W. CHENG, J. WANG, U. JONAS, G. FYTAS, N. STEFANOU, *Observation and Tuning of Hypersonic Band Gaps in Colloidal Crystals*. Nat. Mater. **5**, 830-836 (2006)

[7] III R.H. OLSSON, I. EL-KADY, *Micro-Fabricated Phononic Crystal Devices and Applications*. Meas. Sci. Tech.**20**, 012002 (2009)

[8] J. WEI, D. OLAYA, ET AL, *Ultrasensitive Hot-Electron Nanobolometers for Terahertz Astrophysics*. Nat. Nanotech. **3**, 496 - 500 (2008)

[9] W. Kim, J. Zide, A. Gossard, D. Klenov, S. Stemmer, A. Shakouri, A. Majumdar, *Thermal Conductivity Reduction and Thermoelectric Figure of Merit Increase by Embedding Nanoparticles in Crystalline Semiconductors*. Phys. Rev. Lett. **93**, 045901 (2006)

[10] B.S. Lee, J.S. Lee, *Thermal Conductivity Reduction in Graphene with Silicon Impurity*. App. Phys. A **121**, 1193-1202 (2015)

[11] P.R. Hopkins, C.M. Reinke, M.F. Su, et al., *Reduction in the Thermal Conductivity of Single Crystalline Silicon by Phononic Crystal Patterning*. Nano. Lett. **11**, 107-112 (2011)

[12] R. Anufriev, J. Maire and M. Nomura, *Reduction in the Thermal Conductivity by Surface Scattering of Phonons in Periodic Silicon Nanostructures*. Phys. Rev. B **93**, 045411 (2016)

[13] J. Tang, H.-T. Wang, D.H. Lee, M. Fardy, Z. Huo, T. P.Russell, and P. Yang, *Holey Silicon as An Efficient Thermoelectric Material*. Nano Lett. **10**, 4279 (2010)

[14] J.-K. Yu, S. Mitrovic, D. Tham, J. Varghese, and J.R. Heath,, *Reduction of thermal conductivity in phononic nanomesh structures*. Nat. Nanotech. **5**, 718 (2010)

[15] M.R. Wagner, B. Graczykowski, J.S. Reparaz, A.E. Sachat, M. Sledzinska, F. Alzina, and C.M.S. Torres, *2D Phononic Crystals: Disorder Matters*. arXiv:1511.07398 (2016)

[16] N. Zen, T. A. Puurtinen, T. J. Isotalo, S. Chaudhuri, I. J. Maasilta, *Engineering Thermal Conductance Using a Two-Dimensional Phononic Crystal*. Nat. Commun. **5**, 4435 (2014)

[17] T.A. Puurtinen and I.J. Maasilta, *Low-Temperature Coherent Thermal Conduction in Thin Phononic Crystal Membranes*. Crystals **6**, 72 (2016)

[18] P. Jiang, J.F. Bertone, K.S. Hwang, and V.L. Colvin, *Single-Crystal Colloidal Multilayers of Controlled Thickness*. Chem. Mater. **1**, 2132 (1999)

[19] Y.A. Vlasov, X.-Z. Bo, J.C. Sturm, D.J. Norris, *On-Chip Natural Assembly of Silicon Photonic Bandgap Crystals*. Nat. **414**, 289 (2001)

[20] E. Adachi, A.S. Dimitrov, and K. Nagayama, *Stripe Patterns Formed on a Glass Surface during Droplet Evaporation*. Langmuir **11**, 1057 (1995)

[21] D. Hatanaka, I. Mahboob, K. Onomitsu, H. Yamaguchi, *Phonon Wageguides for Electromechanical Circuits*. Nat. Nanotech. **9**, 520-524 (2006)

[22] Z.-Z. Gu, A. Fujishima, O. Sato, *Fabrication of High-Quality Opal Films with Controllable Thickness*. Chem. Mater. **14**, 760-765 (2013)

[23] C.A. Fustin, G. Glasser, H.W. Spiess, U. Jonas, *Parameters Influencing the Templated Growth of Colloidal Crystals on Chemically Patterned Surfaces*. Langmuir. **20**, 9114-9123 (2004)

[24] R.G. Shimmin, A.J. Dimauro, P.V. Braun, *Slow Vertical Deposition of Colloidal Crystals: A Langmuir-Blodgett Process?* Langmuir **22**, 6507-6513 (2006)

[25] F. Fiazotto, T. Heikkilä, A. Luukanen, A.M. Savin, J. Pekola, *Opportunities for Mesoscopics in Thermometry and Refrigeration: Physics and Applications*. Rev. of Mod. Phys.**78**, 217-274 (2006)

[26] James S. Trefil, *The Nature of Science: An A-Z guide to the Laws and Principles Governing Our Universe* (Houghton Mifflin Harcourt, 2003).

[27] M. Bailyn, *A Survey of Thermodynamics* (American Institute of Physics, New York, 1994).

[28] James P. Wolfe, *Imaging Phonons: Acoustic Wave Propagation in Solids* (Cambridge University press, 1998).

[29] Andrew N. Cleland, *Foundations of Nanomechanics* (Springer-Verlag, Berlin, 2003).

[30] F.K. Graff, *Wave Motion in Elastic Solids* (Oxford University Press, 1975).

[31] T.Kuhn, D.V. Anghel, J.P. Pekola, M. Manninen, and Y.M. Galperin, *Heat Transport in Ultrathin Dielectric Membranes and Bridges*. Phys. Rev. Lett. **70**, 125425 (2004)

[32] M.L. Roukes, M.R. Freeman, R.S. Germain, R.C. Richardson, M.B. Ketchen, *Hot Electrons and Energy Transport in Metals at Millikelvin temperatures*. Phys. Rev. Lett. **55**, 422-425 (1985)

[33] Rudolf de Bruyn Ouboter, *Heike Kamerlingh Onnes's Discovery of Superconductivity*. Sci. Amer. **276**, 98-103 (1997)

[34] W. Meissner, R. Ochsenfeld, *Ein neuer Effekt bei Eintritt der Supraleitfähigkeit*. Kurze Originalmitteilungen. **21**, 787-788 (1933)

[35] J. BARDEEN, L. COOPER, J.R. SCHRIFFER, *Theory of Superconductivity*. Phys. Rev. **8**, 1178 (1957)

[36] M. TINKHAM, *Introduction to Superconductivity*. (McGraw Hill, New York, 1996), 2nd ed.

[37] BERNHARD M UHLSCHLEGEL, *Die Thermodynamischen Funktionen des Supraleiters*. Zeitschrift f ur Physik A Hadrons and Nuclei, **155**, 313-327 (1959)

[38] T.V. DUZER, *Principle of Superconductivitive Devices and Circuits*. (Prentice Hall, 1998).

[39] J.C. FISHER AND I. GIAEVER, *Tunneling Through Thin Insulating Layers*. J. App. Phys. **32**, 172 (1961)

[40] M. NAHUM, J.M. MARTINIS, *Ultrasensitive Hot Electron Microbolometer*. App. Phys. Lett. **63**, 3075 (1993)

[41] P.J. KOPPINEN, I.J. MAASILTA, *Phonon Cooling of Nanomechanical Beams with Tunnel Junctions*. Phys. Rev. Lett. **102**, 165502 (2009)

[42] V. AMBEGAOKAR, A. BARATOFF, *Tunneling between Superconductors*. Phys. Rev. Lett. **10**, 486 (1963)

[43] S. CHAUDHURI, I.J. MAASILTA, *Cooling, Conductance and Thermometric Performance of Nonideal Normal Metal-Ssuperconductor Tunnel Junction Pairs*. Phys. Rev. B **85**, 014519 (2012)

[44] J.P. PEKOLA, V.F. MAISI, S. KAFANOV, N. CHEKUROV, A. KEMPPINEN, Y.A. PASHKIN, O.-P. SAIRA, M. MÖTTÖNEN, AND J.S. TSAI, *Environment-Assisted Tunneling as an Origin of the Dynes Density of States*. Phys. Rev. Lett. **105**, 026803 (2010)

[45] P. J. KOPPINEN, T. KÜHN, I. J. MAASILTA, *Effects of Charging Energy on SINIS Tunnel Junction Thermometry*. **154**, 179-189 (2009)

[46] RAYLEIGH, LORD, *On the influence of obstacles arranged in rectangular order upon the properties of a medium*. Phil. Mag. **34**, 481-502 (1892)

[47] F. BASSANI, J.J. FORNEY AND A. QUATTROPANI, *Choice of Gauge in Two-Photon Transitions: 1s-2s Transition in Atomic Hydrogen*. Phys. Rev. B **39**, 1070 (1977)

[48] F. Schmidt-Kaler, D. Leibfried, M. Weitz, and T.W. Hänsch, *Precision Measurement of the Isotope Shift of the 1S-2S Transition of Atomic Hydrogen and Deuterium.* Phys. Rev. Lett. **39**, 1070 (1977)

[49] N. Fatkullin, T. Ikehara, H. Jinnai, S. Kawata, R. Kimmich, T. Nishi, Y. Nishikawa, H.-B. Sun, *NMR ● 3D Analysis ● Photopolymerization* (Springer-Verlag, 2004).

[50] Donald M. Mattox, *Handbook of Physical Vapor Deposition (PVD) Processing* (Noyes Publications, Westwood, NJ, 1998).

[51] Sami Franssila, *Introduction to Microfabrication* (John Wiley & Sons, Great Britain, 2004).

[52] T. Isotalo, *Periodic Nanostructures for Thermal Engineering Applications.* (Nanoscience Center, University of Jyvaskyla, 2014).

[53] Z. Geng, *Development of an Inductive NIS Thermometer.* (Nanoscience Center, University of Jyvaskyla, 2012).

[54] J.T. Peltonen, P. Virtanen, M. Meschke, J.V. Koski, T.T. Heikkil a, and J.P. Pekola, *Thermal Conductance by the Inverse Proximity Effect in a Superconductor.* Phys. Rev. Lett. **105**, 097004 (2010)

[55] J. Julin and I.J Maasilta, *Applications and non-idealities of submicron Al-AlO$_x$-Nb tunnel junctions.* Supercond. Sci. Technol, in press (2016)

[56] E.T. Swartz, R.O. Pohl, *Thermal Boundary Resistance.* Rev. Mod. Phys. **61**, 605 (1989)

[57] A. Groisman, E. Kaplan, *Experimental Model of Cracking Induced by Drying Shrinkage .* Europhys. Lett. **25**, 415-420 (1994)

[58] H. Colina, S. Roux, *An Experimental Study of Cracking Induced by Desiccation.* Eur. Phys. J. E **1**, 189-194 (2000)

[59] S. Bohn, J. Platkiewicz, B. Andreotti, M. Adda-Bedia, Y. Couder, *Hierarchical Crack Pattern as Formed by Successive Domain Divisions. II. From Disordered to Deterministic Behavior .* Phys. Rev. E **71**, 046215 (2006)

[60] K.-S Lee, R.H. Kim, D.-Y. Yang, S.H. Park, *Advances in 3D Nano/Microfabrication Using Two-Photon Initiated Polymerlaiztion.* Pro. Poly. Sci. **33**, 631-681 (2008)

[61] R.L. CLOUGH, *High-energy radiation and polymer: A Review of Commerical Processes and Emerging Applications*. Nuclear Instruments and Methods in Physics Research B **185**, 8-33 (2001)