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Computation of lock-in range for classic PLL with lead-lag filter and impulse signals

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Abstract: For a classic PLL with square waveform signals and lead-lag filter for all possible parameters lock-in range is computed and corresponding diagrams are given.

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Keywords: Phase-locked loop, nonlinear analysis, analog PLL, cycle slipping, hold-in range, pull-in range, lock-in range, definition, lead-lag filter.

1. INTRODUCTION

The phase-locked loop (PLL) is an electric circuit extensively used in various applications in computer architectures and telecommunications (see, e.g. Kroupa (2003); Bianchi (2005); Gardner (2005); Best (2007); Shakhtarin et al. (2009)). A PLL is essentially a nonlinear control system, which allows one to tune frequency (phase) of the controlled oscillator to the frequency (phase) of the reference oscillation (reference signal). One of the main characteristics of PLL is the *lock-in range* (Gardner, 1966; Best, 2007): the range of frequencies of the reference signal for which fast synchronization without cycle sipping is guaranteed.

In this work for a classic PLL with square waveform signals and lead-lag filter for all possible parameters the lock-in range is computed and corresponding diagrams are given. The computed lock-in range is compared with estimates in (Best, 2007).

2. MATHEMATICAL MODEL OF PLL WITH LEAD-LAG FILTER

Consider signal's phase space model of classic PLL circuit (see Fig. 1). Here the phase detector (PD) is a nonlinear block and the phases $\theta_{1,2}(t)$ of the input (reference) and VCO signals are PD block inputs and the output is a function $\varphi(\theta_e(t)) = \varphi(\theta_1(t) - \theta_2(t))$ named a phase detector characteristic, where

$$\theta_e(t) = \theta_1(t) - \theta_2(t),\tag{1}$$

named the phase error. Consider triangular PD characteristic (see Fig. 2):

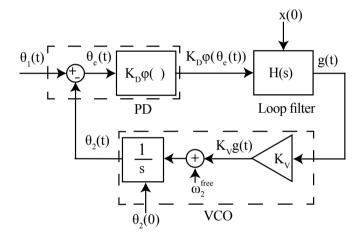


Fig. 1. PLL-based circuit in a signal's phase space.

$$\varphi(\theta_e) = \begin{cases} \frac{2}{\pi} \theta_e, & \text{for } \theta_e \in [-\frac{\pi}{2}, \frac{\pi}{2}], \\ 2 - \frac{2}{\pi} \theta_e, & \text{for } \theta_e \in [\frac{\pi}{2}, \frac{3}{2}\pi]. \end{cases}$$
 (2)

This characteristic appears for the case of classical multiplier/mixer and impulse signal waveforms of VCO and reference. For exclusive-or (EXOR) the phase detector characteristic is also triangular. The output of the PD is connected to the input of the passive lead-lag filter with the transfer function

$$F(s) = \frac{1 + \tau_2 s}{1 + \tau_1 s},\tag{3}$$

where $0 < \tau_2 < \tau_1$. Loop filter dynamics can be described by the following differential equations

$$\dot{x} = -\frac{1}{\tau_1} x + \frac{1}{\tau_1} \varphi(\theta_e(t)),
g = (1 - \frac{\tau_2}{\tau_1}) x + \frac{\tau_2}{\tau_1} v_e(\theta_e(t)).$$
(4)

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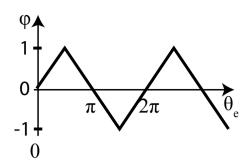


Fig. 2. Triangular PD characteristic

where x(t) is a state of the loop filter, $K_D\varphi(t)$ is the PD output, and q(t) is a filter output.

The output of the filter g(t) adjusts the frequency of the VCO to the frequency of the input signal:

$$\dot{\theta}_2(t) = \omega_2(t) = \omega_2^{\text{free}} + K_V g(t), \tag{5}$$

where ω_2^{free} is called free-running frequency (i.e. for $g(t) \equiv$ 0) and \tilde{K}_V is the VCO gain. Nonlinear VCO models can be studied similarly (see, e.g. Margaris (2004); Suarez (2009)).

The frequency of the input signal (reference frequency) is usually assumed to be constant:

$$\dot{\theta}_1(t) = \omega_1(t) \equiv \omega_1. \tag{6}$$

The difference between the reference frequency and the VCO free-running frequency is denoted as ω_e^{free} :

$$\omega_e^{\text{free}} \equiv \omega_1 - \omega_2^{\text{free}}.\tag{7}$$

Combining (4) - (6), one obtains the following equations:

$$\dot{x} = -\frac{1}{\tau_1}x + \frac{1}{\tau_1}\varphi(\theta_e(t)),$$

$$\dot{\theta}_e = \omega_e^{free} - K_V \left((1 - \frac{\tau_2}{\tau_1})x + \frac{\tau_2}{\tau_1}v_e(\theta_e(t)) \right).$$
(8)

System (8) is periodic in θ_e , therefore the analysis is restricted to the range $\theta_e \in [-\pi, \pi)$. The equilibria of (8) are denoted by (x_{eq}, θ_{eq}) :

$$\theta_{eq} = \frac{\pi}{2} \frac{\omega_e^{\text{free}}}{K_{VCO} K_D},$$

$$x_{eq} = \frac{\omega_e^{\text{free}}}{K_{VCO} K_D}.$$
(9)

Stable equilibria correspond to the locked states of the loop. Since PD characteristic (2) is an odd function $(\varphi(-\theta_e) = -\varphi(\theta_e))$, system is not changed by the trans-

$$\left(\omega_e^{\rm free}, x(t), \theta_e(t)\right) \to \left(-\omega_e^{\rm free}, -x(t), -\theta_e(t)\right). \tag{10}$$

This symmetric property of PD allows one the analysis of system (8) with only $\omega_e^{\text{free}} \geq 0$ and introduces the concept of frequency deviation

$$|\omega_e^{\rm free}| = |\omega_1 - \omega_2^{\rm free}|.$$

3. LOCK-IN RANGE DEFINITION

The concepts of lock-in frequency and lock-in range were intended to describe the set of frequency deviations for which the loop can acquire lock within one beat without cycle slipping. Next we use the definitions of the cycle slipping and lock-in range from (Kuznetsov et al., 2015; Leonov et al., 2015). If

$$\lim_{t \to +\infty} \sup_{t \to +\infty} |\theta_e(0) - \theta_e(t)| > 2\pi, \tag{11}$$

we say that cycle slipping occurs. The lock-in range may be define as follows: if the model is in an equilibrium state, then after an abrupt change of $\omega_{\rm ref}$ within a lock-in range $|\omega_e^{\rm free}| < \omega_{
m lock-in}$, the model locks without cycle slipping. Here $\omega_{\text{lock-in}}$ is called lock-in frequency.

Thus, the lock-in domain (i.e. a domain of the model states, where fast acquisition without cycle slipping is possible) contains both symmetric locked states (i.e. stable equilibrium points for the positive and negative value of the difference between the reference frequency and the VCO free-running frequency).

3.1 Lock-in range computation

System (8) depends on 5 parameters: $\tau_1, \tau_2, K_V, K_D, \omega_e^{\text{free}}$. Introduce parameter $\tau = t\sqrt{K_V K_D/\tau_1}$ and reduce (8) to the following equation

$$\ddot{\theta}_e = \frac{\omega_e}{K_V K_D} - \frac{\dot{\theta}_e}{\sqrt{K_V K_D \tau_1}} - \frac{\tau_2}{\tau_1} \sqrt{K_V K_D \tau_1} \frac{d\varphi}{d\theta_e} \dot{\theta}_e - \varphi(\theta_e).$$
(12)

This equation contains only three parameters. The first one is the normalized frequency deviation $\frac{\omega_e}{K_V K_D}$, and two others are the normalized loop filter parameters: $\frac{\tau_2}{\tau_1}$ and $K_V K_D \tau_1$.

Consider now simple numerical algorithm for computation

of the lock-in range. For each pair $\left(\frac{\tau_2}{\tau_1}, K_V K_D \tau_1\right)$ the normalized frequency deviation $\frac{\omega_e^{\text{free}}}{K_V K_D}$ is increased starting from zero. The largest possible value of frequency deviation is $\frac{\omega_e^{\text{free}}}{K_V K_D} = 1$ since there are no equilibrium points for bigger values. Taking into account that aguilibria are for bigger values. Taking into account that equilibria are proportional to the frequency deviation and using the symmetry $(x_{eq}(\omega_l), \theta_{eq}(\omega_l)) = -(x_{eq}(-\omega_l), \theta_{eq}(-\omega_l))$, one can effectively determine the lock-in range. We have to increase the frequency deviation $|\omega_e^{\text{free}}|$ step by step and at each step, after the loop achieves a locked state, to change $\omega_e^{\rm free}=\widetilde{\widetilde{\omega}}$ abruptly to $\omega_e^{\rm free}=-\widetilde{\omega}$ and to check if the loop can achieve a new locked state without cycle slipping. If so, then the considered value belongs to the lock-in range.

Consider example in Fig. 3. Here filter parameters τ_1 = $0.02, \tau_2 = 0.008$ correspond to a curve $\frac{\tau_2}{\tau_1} = 0.4$ (see the right-hand side axis). By substituting PD gain K_D and VCO gain K_V into $K_V K_D \tau_1$ one determines a point on the curve (see horizontal axis). The corresponding lockin frequency ω_l is then computed from the corresponding value of the normalized value of the lock-in frequency $\frac{\omega_e^{-\tau}}{K_V K_D}$ on the left-hand side of vertical axis. Note that the same diagram may be used for any filter as long as $\frac{\tau_2}{\tau_1} = 0.4$. Lock-in frequencies for other loop filter parameters are in Fig. 4. Lock-in range for considered the case is estimated in (Best (2007)) for the case of small $\frac{\tau_2}{\tau_1}$ and large loop gain K_DK_V :

$$\omega_l \approx K_D K_V \left(\frac{\tau_2}{\tau_1} + \frac{1}{K_D K_V \tau_1}\right). \tag{13}$$

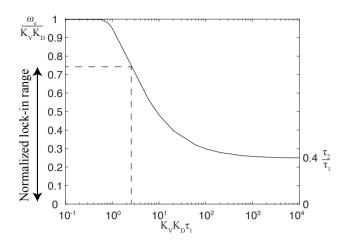


Fig. 3. Lock-in range for parameters $\tau_1=0.02,\,\tau_2=0.008.$ For $\frac{\tau_2}{\tau_1}=0.01$ lock-in diagrams are in Fig. 5. These diagrams were constructed numerically in Matlab, by integrating system (8) with "ode15s".

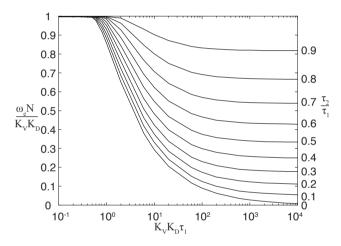


Fig. 4. Lock-in range lead-lag filter, triangular PD.

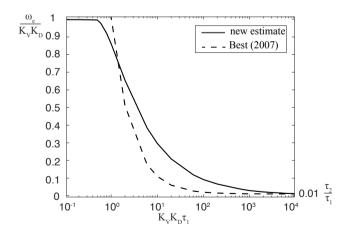


Fig. 5. Lock-in range estimates.

REFERENCES

Best, R. (2007). Phase-Lock Loops: Design, Simulation and Application. McGraw-Hill, 6th edition. Bianchi, G. (2005). Phase-Locked Loop Synthesizer Simulation. McGraw-Hill. Gardner, F. (1966). *Phase-lock techniques*. John Wiley & Sons, New York.

Gardner, F. (2005). Phaselock Techniques. Wiley, 3rd edition.

Kroupa, V. (2003). Phase Lock Loops and Frequency Synthesis. John Wiley & Sons.

Kuznetsov, N., Leonov, G., Yuldashev, M., and Yuldashev, R. (2015). Rigorous mathematical definitions of the hold-in and pull-in ranges for phase-locked loops. *IFAC-PapersOnLine*, 48(11), 710–713. doi: http://dx.doi.org/10.1016/j.ifacol.2015.09.272.

Leonov, G., Kuznetsov, N., Yuldashev, M., and Yuldashev, R. (2015). Hold-in, pull-in, and lock-in ranges of PLL circuits: rigorous mathematical definitions and limitations of classical theory. *IEEE Transactions on Circuits and Systems-I: Regular Papers*, 62(10), 2454–2464. doi: http://dx.doi.org/10.1109/TCSI.2015.2476295.

Margaris, N. (2004). Theory of the Non-Linear Analog Phase Locked Loop. Springer Verlag, New Jersey.

Shakhtarin, B., Andrianov, M., and Andrianov, I. (2009). Application of discontinuous communications in channels with random parameters to transmit narrowband signals and signals with orthogonal frequency-division multiplexing. *Journal of communications technology and electronics*, 54(10), 1175–1182.

Suarez, A. (2009). Analysis and Design of Autonomous Microwave Circuits. Wiley Series in Microwave and Optical Engineering. Wiley-IEEE Press.