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# SIZE SENSITIVE PHENOMENA IN SUPERCONDUCTING WIRES AND SINGLE CHARGE DEVICES

**BY**
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Academic Dissertation
for the Degree of
Doctor of Philosophy

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# Preface

The work reviewed in this thesis has been carried out at the Department of Physics, University of Jyväskylä during the years 1998-2004 including a half-year visit to Technical University of Denmark (DTU) in 2001.

First of all, I thank my supervisor Academy Prof. Jukka Pekola for introducing me to the field of nanoscience and for giving excellent guidance in SQUBIT-project. I thank Prof. Jesper Mygind for a possibility to visit his laboratory at DTU and give a contribution to his project. I thank my other supervisor Docent Konstantin Arutyunov for guiding me during the last part of my thesis work and giving me a deeper insight in superconductivity.

The Department of Physics has been a great place to study and the applied physics group has given excellent conditions for research work. First of all, I thank Dr. Jussi Toppari, with whom I have spent countless of hours making measurements from the very beginning. I also thank Mr. Ari Halvari, Dr. Klavs Hansen, Mr. Pasi Keinänen, Dr. Nam Kim, Mr. Kimmo Kinnunen, Mr. Panu Koppinen, Dr. Anssi Lindell, Mr Antti Nuottajärvi, Mr. Kari-Pekka Riikonen, Mr. Lasse Taskinen and Dr. Vladimir Touboltsev for co-operation. Also the teaching personnel and departmental staff are to thank. From DTU, I thank Dr. Mikkel Ejrnæs, Dr. Martin Manscher, Dr. Andrey Moskalenko, Mr Carsten Mahaini and Mr. Benjamin Thomsen for co-operation and making my stay pleasant.

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And finally, I thank my parents for support and my future wife Outi for standing beside me.

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# Abstract

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diss.

In studying micro- or nanoscale phenomena, it is important to be able to routinely fabricate nanostructures, and particularly in statistical studies to fabricate a batch of similar structures. The main part of this thesis presents first results obtained by applying a novel ion beam sputtering method developed in this work to decrease dimensions of prefabricated nanostructures. The material is removed from the sample surface by bombarding it with energetic argon ion beam. The applicability of the method was tested with aluminium nanowires and single electron transistors and the promising results are presented in this thesis. An interesting feature of the method is that it can be applied multiple times so that dimensions are reduced gradually. This enables in general measurements of size-sensitive phenomena without fabricating numerous samples. This helps in ruling out circumstantial factors in fabrication.

Also transport phenomena in single charge devices are discussed. Single electron transistors were used as electrometers in detecting tunnelling of electrons and Cooper pairs to an isolated piece of metal. For this purpose, special multilayer technique was applied in order to capacitively couple the systems. The effect of externally applied microwave signal to the current through single electron transistor was measured and compared with the theory. Also measurements and theoretical aspects of Cooper pair pumps are discussed.

**Keywords** Sputtering, nanowires, single electron transistor, Cooper pair box, Cooper pair pump, electrometer, superconductivity, cotunnelling

# List of Publications

**A.I.** SAVOLAINEN, M.T., TOUBOLTSEV, V., KOPPINEN, P., RIIKONEN, K.-P., AND ARUTYUNOV, K., *Ion beam sputtering for progressive reduction of nanostructures dimensions*. Appl. Phys. A **79** (2004) 1769.

**A.II.** SAVOLAINEN, M.T., TOPPARI, J.J., TASKINEN, L., KIM, N., HANSEN, K., AND PEKOLA,J.P., *Characterization of Cooper pair boxes for quantum bits*. Proceedings of 'Macroscopic Quantum Coherence 2', Napoli, 2000: Macroscopic Quantum Coherence and Quantum Computing, D. Averin, B. Ruggiero, and P. Silvestrini (eds.) Plenum Publishers, New York (2001) 145.

**A.III.** EJRNÆS, M., SAVOLAINEN, M., AND MYGIND, J., *Noise and Microwave properties of SET-transistors*. Proceedings of 'International workshop on Superconducting Nano-Electronics Devices', Napoli 2001, J. Pekola, B. Ruggiero and P. Silvestrini (eds.), Plenum publishers, New York (2002) 53.

**A.IV.** EJRNÆS, M., SAVOLAINEN, M.T., MANSCHER, M., AND MYGIND, J., *Microwave induced co-tunneling in single electron tunneling transistors*. Physica C **372-376** (2002) 1353.

**A.V.** PEKOLA, J.P., TOPPARI, J.J., AUNOLA, M., SAVOLAINEN, M.T., AND AVERIN, D.V., *Adiabatic transport of Cooper pairs in arrays of Josephson junctions*. Phys. Rev. B **60** (1999) 9931.

**A.VI.** TOPPARI, J.J., KIVIOJA, J.M., PEKOLA, J.P., AND SAVOLAINEN, M.T., *Turnstile Behaviour of the Cooper-Pair pump*. J. Low Temp. Phys. **136** (2004) 57.

**A.VII.** MANSCHER, M.H., SAVOLAINEN, M.T., AND MYGIND, J., *Microwave Enhanced Cotunneling in SET Transistors*. IEEE Trans. Appl. Supercond. **13** (2003) 1107.

**A.VIII.** ZGIRSKI, M., RIIKONEN, K.-P., HOLMQVIST, T., SAVOLAINEN, M., TOUBOLTSEV, V., AND ARUTYUNOV, K., *Quantum tunneling phenomena in ultra-thin superconducting wires*. Abstracts of IV International workshop on "Macroscopic Quantum Coherence and Computing", Napoli, 7-10 June, 2004.

## Author's contribution

The author carried out most of the development work related to the ion beam sputtering method presented in this thesis. The author has written the publications A.I and A.II. Related to publication A.I, the author fabricated all SET samples and part of the nanowire samples. All SET measurements and their analysis was performed by the author. The author participated in measurements of nanowires and made all fittings to the LAMH-theory presented in this work. The results presented in publication A.VIII were obtained side by side with the measurements relating to A.I, by using the same samples partly fabricated by the author, and with the partial contribution of the author to measurements and analysis.

In work related to A.II, the multilayer technique needed in fabrication process of the samples was mainly studied by the author and he fabricated part of the samples. The measurements and analysis were partly done by the author. The author contributed to the preliminary calculations leading into publication A.V. Related to A.VI, the author participated in measurements needed to map out the honeycomb structure of the Cooper pair pump.

The experimental work related to A.III, A.IV and A.VII was done during the author's visit to Technical University of Denmark (DTU). Related to publications A.III and A.IV, the author contributed on preparing the cryostat for the measurements and participated in the measurements. The author fabricated the samples and participated in measurements of publication A.VII.

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# Chapter 1

# Introduction

"Why cannot we write the entire 24 volumes of the Encyclopædia Britannica on the head of a pin?", asked Richard Feynman in his classic talk "There's plenty of room at the bottom" held on December 29th 1959 at the annual meeting of the American Physical Society. Finding the size limits of metallic wires is important for both the fundamental research and computer industry. The development of the fabrication processes has resulted in faster computers, since the processor speed increases as the distances between the transistors are reduced. In the year 1965, Gordon Moore noticed that the number of transistors per square inch on integrated circuits had doubled once every 18 months since the integrated circuit was invented. He also predicted this to continue in the future. The pace has slowed a bit, but still *the Moore's law* has held surprisingly well during the years. Moore himself has estimated, that the physical limitations will hit the industry around 2017 [1].

The fabrication techniques used at present in obtaining ultrasmall structures, for instance nanoelectronic circuits, have their limits, and researchers try constantly to push these limits further. It is not difficult to produce narrower metallic wires than the existing ones in microprocessors. These techniques include for example fabrication by using electron beam (electron beam lithography, EBL) and atomic force microscope in patterning. However, these methods cannot be used in mass production as they are too slow and expensive.

## 1.1 Size effects in solids

As it has become possible to fabricate small enough systems, many interesting new phenomena have been observed. These include quantised conductance, universal conductance fluctuations, Aharonov-Bohm oscillations, and single charge effects, just to mention few.

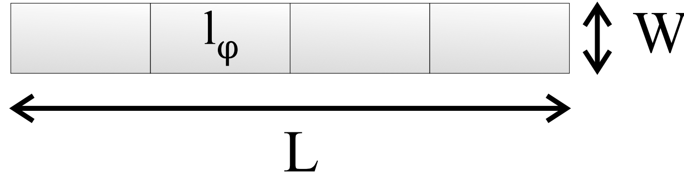


**FIGURE 1.1** *Schematic image of a macroscopic conductor, where $L > l_\varphi > W$.*

For the disordered two-dimensional electron gas (2DEG), the classical Drude conductance is written as

$$G_{\text{Drude}} = \frac{e n_{\text{s}} \mu W}{L}, \tag{1.1}$$

where $n_{\text{s}}$ is the electron density, $\mu$ is the mobility, $W$ is the width and $L$ the length of the device, respectively. This conductance does not depend on the arrangement of impurities in metal. However, when the phase-breaking length $l_\varphi$ becomes comparable to the characteristic size of the system, the electrons are considered as waves scattering from the impurities, which can be treated as sources of new waves in spirit of the Huygens principle. The waves sourcing from the different impurities form interference pattern resulting in sample specific conductance around the 'classical value'. The RMS magnitude of this conductivity contribution is of order $e^2/h$, not depending on the degree of disorder or device size, and the corresponding oscillation is called Universal Conductance Fluctuation (UCF). A macroscopic conductor, where $L > l_\varphi > W$, contains several phase coherent sections in series, each giving a contribution of about $e^2/h$ to the conductance fluctuations. The RMS magnitude of the conductance fluctuations, rms($G$)=rms($R$)/$R^2$ is proportional to $[(l_\varphi/L)^{3/2}]$, thus a short wire has more conductance fluctuations than a long wire.

Let us consider a small metallic ring in magnetic field. Small in a sense that the electron states are not altered by inelastic or magnetic scattering when travelling in the arm of the ring. The magnetoresistance of the device should show an interference pattern [15, 27, 14]: Electron wave packets circling a magnetic flux exhibit a phase shift introduced by a magnetic vector potential $\mathbf{A}$ [9]. The phase of the electrons travelling along one arm of the ring will change by an amount $\delta_1$, and electrons of the other arm in general have a different phase shift $\delta_2$. By tuning the magnetic flux the phase along one arm will change by $\delta_{\text{B}} = (e/\hbar)\int \mathbf{A} \cdot \mathbf{dl}$ and by $-\delta_{\text{B}}$ along the other arm. This tuning will emerge as cycles of constructive and destructive interference of the wave packets and reflect in the transport properties of the ring with a period $\Phi_0 = h/e$. These predicted $h/e$ Aharonov-Bohm oscillations have been observed by Webb *et al.* [64] and later by other groups.

In superconductors, interesting size effects become observable, when the di-

mensions of the superconductor are comparable to the temperature dependent coherence length $\xi(T)$, which sets the smallest volume of the superconductor order parameter to be altered by any means. The superconductor is said to be zero-dimensional, when all dimensions of the superconductor are smaller than the coherence length. One-dimensionality in turn is obtained when one dimension is larger than the coherence length. In this case the system is very sensitive to fluctuations, since even one section of length $\xi(T)$ of the wire switching into normal state will destroy superconductivity of the whole superconductor. This switching can occur by means of thermally activated phase slip or quantum phase slip. The corresponding competing energies are the condensation energy vs. thermal energy $k_{\mathrm{B}}T$, and condensation energy vs. quantum-originated energy $h\omega$, respectively.

In many nanoelectronic components, especially in those that contain tunnel junctions, the reduction of size usually corresponds to higher operational temperatures. This is because the characteristic energy $E_{\mathrm{C}}$ related to charging the system with one unit charge increases and the system is not so easily disturbed by the competing thermal energy $k_{\mathrm{B}}T$.

## 1.2 Objectives of the work

The main part of this thesis describes miniaturization of nanostructures, metallic nanowires and tunnel junctions, from a new point of view. The objective was to study the possibility to progressively reduce dimensions of prefabricated nanostructures by bombarding (sputtering) with energetic argon ions. This included the determination of etching rates for various materials and testing the applicability of the method with aluminium nanowires and single electron transistors, which are basic components of many nanoelectronic devices. Furthermore, relating to the size reduction of one-dimensional superconducting aluminium nanowires, there was an ambitious objective to observe finite resistance due to quantum phase slips (QPS).

This thesis also reviews other projects where the author has had contributions during the years 1998-2003. These include measurements and theory of mesoscopic systems: single electron transistor (SET), Cooper pair box (SCB) and Cooper pair pump (CPP). The use of superconducting SET as an electrometer measuring the charge of the Cooper pair box was studied. A fundamental inaccuracy of Cooper pair transfer was calculated and the transfer of Cooper pairs was studied also experimentally. Cotunnelling measurements were carried out in co-operation with the Department of Physics, Technical University of Denmark (DTU), where the effect of microwaves on cotunnelling was studied.

# Chapter 2

# Theoretical background

## 2.1 Superconductivity

*"A property of many metals, alloys, and chemical compounds at temperatures near absolute zero by virtue of which their electrical resistivity vanishes and they become strongly diamagnetic"* [51].

This is a basic definition of superconductivity by Dictionary of Physics providing two important aspects of this interesting phenomenon first observed by Kamerlingh Onnes and his student in 1911 [49, 47, 48]. Perhaps the most famous property of superconductors is the disappearance of resistance below critical temperature $T_C$. The perfect diamagnetism of superconductors was observed by Meissner and Ochsenfeld in 1933 [42]. They noticed that the external magnetic field is expelled out inside the superconductors by opposing magnetic field formed by supercurrent. It was also predicted that the magnetic field stronger than a critical magnetic field, $H_{\mathrm{C}}$, will destroy superconductivity. The empirical formula describing this as function of temperature in *type I* superconductors is [62]

$$H_{\mathrm{C}}(T) \approx H_{\mathrm{C}}(0)[1-(T/T_{\mathrm{C}})^2]. \tag{2.1}$$

In *type II* superconductors (e.g. niobium, most intermetallic alloys and high temperature superconductors) there are two critical magnetic fields, $H_{\mathrm{C1}}$ and $H_{\mathrm{C2}}$. With magnetic fields higher than $H_{\mathrm{C1}}$ but smaller than $H_{\mathrm{C2}}$, the field can penetrate through the superconductor via vortices each able to carry a magnetic flux quantum $\Phi_0 = h/(2e)$. The vortices have been observed also experimentally [23]. When applying higher magnetic field than $H_{\mathrm{C2}}$, the superconductivity is destroyed in bulk.

Since the discovery of superconductivity, several theoretical approaches have been developed to describe this phenomenon. The Ginzburg-Landau theory [28] proposed in 1950, is a phenomenological theory based on the Landau's theory of

second order phase transitions. The superconductor is described by a macroscopic wave function $\psi = |\psi|e^{-i\varphi}$, stating that the superconductor is macroscopically phase coherent. The microscopic BCS-theory was published in 1957 by Bardeen, Cooper and Schrieffer [12] almost 50 years after superconductivity was first observed.

The essence of BCS-theory is that in superconductors even a very weak attractive interaction between electrons, e.g. via lattice phonons, makes the electrons to form pairs, which are called Cooper pairs. These pairs act like bosons and condense to Fermi level $E_\mathrm{F}$. The theory predicts the minimum energy needed to break a Cooper pair, $2\Delta(T)$, where $\Delta$ is the energy gap formed around Fermi energy as consequence of the pairing. The energy gap is largest at zero-temperature, $2\Delta(0) = 3.528 k_\mathrm{B} T_\mathrm{C}$, and decreases as the temperature increases. Finally the gap disappears at $T_\mathrm{C}$.

**TABLE 2.1** *Clean limit parameters of various superconducting materials [20].*

| | Al | In | Sn | Pb | Nb |
|---|---|---|---|---|---|
| $T_\mathrm{C}[\mathrm{K}]$ | 1.175 | 3.408 | 3.722 | 7.196 | 9.25 |
| $\lambda_\mathrm{L}(0)[\mathrm{nm}]$ | 16 | 21 | 36 | 37 | 39 |
| $\xi_\mathrm{BCS}(0)[\mathrm{nm}]$ | 1600 | 440 | 230 | 83 | 38 |

There are two characteristic length scales in superconductors: the magnetic field penetration length $\lambda_\mathrm{L}$ and the coherence length $\xi$, which defines the effective size of a Cooper pair. Type-I superconductors are characterized by $\lambda_\mathrm{L} < \xi$ and type-II materials with $\lambda_\mathrm{L} > \xi$. Both parameters $\lambda_\mathrm{L}(T)$ and $\xi(T)$ are temperature dependent, diverging at critical temperature $T_\mathrm{C}$ and should be recalculated for the 'dirty limit' case. That is when the mean free path $l < \lambda_\mathrm{L}, \xi$. In this limit, the coherence length is written as [62]

$$\xi(T) = 0.85\sqrt{l\xi_\mathrm{BCS}(T)}. \tag{2.2}$$

The corresponding penetration depth is

$$\lambda_\mathrm{L} = \sqrt{\frac{m^*}{4\pi n_\mathrm{s} e^2}}, \tag{2.3}$$

where $n_\mathrm{s}$ is the density of the superconducting electrons and $m^*$ the mass in the two-fluid model[1]. Table 2.1 presents parameters of common superconducting materials.

It is not difficult to reach the limit of one-dimensionality in superconductors. The coherence length is function of temperature as depicted in Fig. 2.1. Note that the coherence length increases rapidly as temperature approaches the critical temperature $T_\mathrm{C}$. Thus near the critical temperature even very wide wires can be considered

[1]In two-fluid model all the free electrons of a superconductor are divided into two groups, superconducting and normal electrons

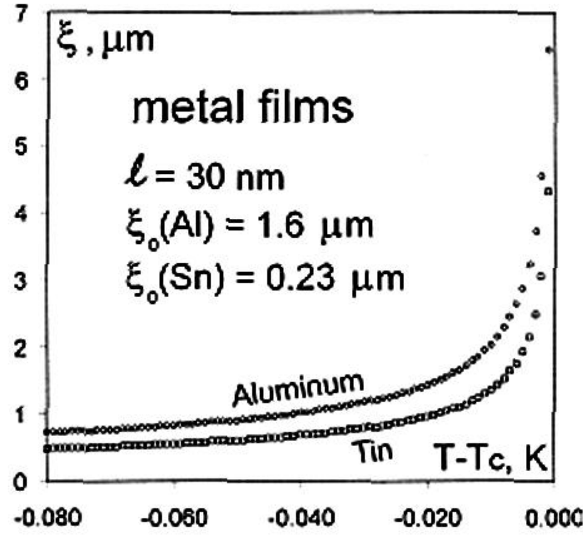


**FIGURE 2.1** *Calculated coherence length of aluminium and tin as a function of temperature plotted by using Eq. 2.2. $l$ is the mean free path and $\xi_0$ the coherence length at zero temperature.*

as one-dimensional. If to consider reasonably 'dirty' samples ($l \sim$ 10-30 nm), one can consider an aluminium wire with the effective diameter $\sqrt{\sigma} < 100$ nm ($\sigma$ being the cross-section of wire) as one-dimensional. All the measured aluminium wires discussed in this thesis have been below 100 nm in width.

In case of a thin wire or film, the current density can be written according to the Ginzburg-Landau theory as

$$J_\mathrm{S} = \frac{2e}{m^*}|\psi|^2 \left(\hbar\nabla\varphi - \frac{2e}{c}A\right) = 2e|\psi|^2 v_\mathrm{s}, \tag{2.4}$$

where $A$ is the vector potential and $v_\mathrm{s}$ is the supercurrent velocity. The free energy in this case is written as

$$f = f_{n0} + \alpha|\psi|^2 + \frac{\beta}{2}|\psi|^4 + |\psi|^2\frac{1}{2}m^* v_\mathrm{s}^2 + \frac{h^2}{8\pi}, \tag{2.5}$$

where $\alpha$ and $\beta$ are phenomenological parameters and $h$ is the magnetic energy. These equations will give interesting results when applied to the case of an uniform current density through a wire. The maximum possible current in supercurrent, critical current density $J_\mathrm{C}$, will get a form [62]

$$J_C = 2e\psi_\mathrm{inf}^2 \frac{2}{3}\left(\frac{2|\alpha|}{3m^*}\right)^{1/2} = \frac{cH_\mathrm{C}(T)}{3\sqrt{6}\lambda(T)} \propto (T_\mathrm{C} - T)^{3/2}, \tag{2.6}$$

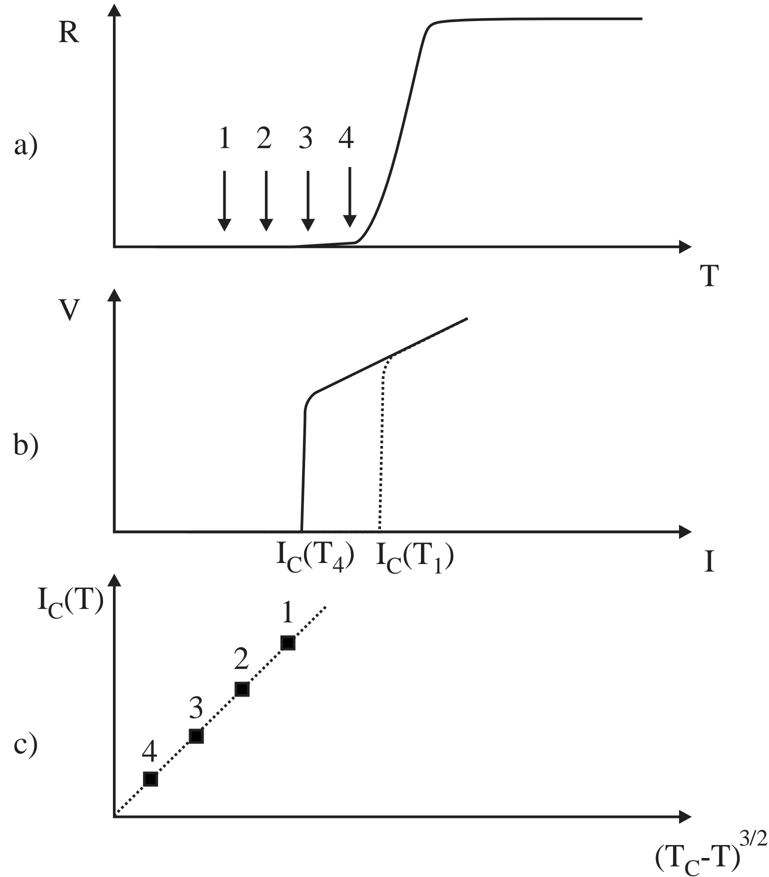


**FIGURE 2.2** *Schematic representation of results expected when measuring one-dimensional superconductor. a) resistance vs. temperature. b) current-voltage characteristics at two temperatures below the critical one. c) temperature dependence of the critical current. The linear dependency in Fig. c) is an indication that the sample is one-dimensional.*

where $\psi_{\text{inf}}$ is the order parameter.

Thus, the critical current density of a one-dimensional wire depends on temperature, being proportional to $(T_C - T)^{3/2}$.

Figure 2.2a) shows a schematic image of a superconducting transition with fictitious four points of interest. In Fig. 2.2b), I-V measurement has been done at temperatures $T_1$ and $T_4$, where the current has been increased until the critical current $I_C(T)$ has been reached[2]. This is repeated at several temperatures and in Fig. 2.2c) the corresponding critical currents are plotted as function of $(T_C - T)^{3/2}$. The linear dependence suggests that the wire is one-dimensional.

[2]The definition of the critical current in measurements is up to an experimentalist, who can as an example decide that critical current corresponds to voltage exceeding some predefined small value.

## 2.2 One-dimensional superconductors

### 2.2.1 Shape of R(T)

The effects of thermodynamic fluctuations on electric currents in bulk superconductors are difficult to observe as they exist in an extremely narrow temperature range near the critical temperature: $\Delta t = |T_\mathrm{C} - T|/T_\mathrm{C} < 10^{-12}$ [63][3]. The temperature range can be extended by restricting the fluctuation volume. The range is largest in one-dimensional superconductors, where the diameter of the superconductor is assumed to be much smaller than the temperature-dependent coherence length: $d \ll \xi(T)$. For the 'dirty limit' superconductors, where mean free path $l$ is smaller than $\xi$, the effective coherence length is given by Eq. 2.2. The coherence length sets the minimum size of a superconducting domain that can become normal. If this happens in an one-dimensional wire, the effect is large, since a single normal domain blocks the supercurrent and induces finite resistance.

The form of the superconducting transition is explained by two mechanisms. If to consider one-dimensional nanowires of width somewhat larger than 10 nm, the finite resistance below the critical temperature $T_\mathrm{C}$ is explained essentially by thermally activated phase slips, the process corresponding to local destruction of superconductivity by thermal fluctuations [33, 41, 38, 46]. During this momentary process, the superconducting phase is allowed to slip by the amount $2\pi$. It can be seen from the Josephson relation

$$\hbar\frac{\partial\varphi}{\partial t} = 2eV, \tag{2.7}$$

that the phase slip corresponds to a voltage drop $V$ and thus produces resistance. The rate of activation of thermally activated phase slips decreases exponentially with temperature and in practice becomes immeasurably small relatively close to critical temperature.

If the diameter of the wire is reduced close to $\sim$10 nm or below, the phase slips due to quantum fluctuations of the order parameter (quantum phase slips) become possible and cause resistance below the threshold temperature of the thermally activated phase slips [67, 29].

The motivation for the use of term 'phase slip' is the following. The free energy of a current biased superconducting wire as function of the phase $\varphi$ of the Ginzburg-Landau wave function $\psi_\mathrm{GL}$ is depicted in Fig. 2.3. The tilting of the energy function of Fig. 2.3 is directly proportional to the biasing current. The system can lower its

[3]It would be very difficult to keep the temperature stable enough to observe the effects.

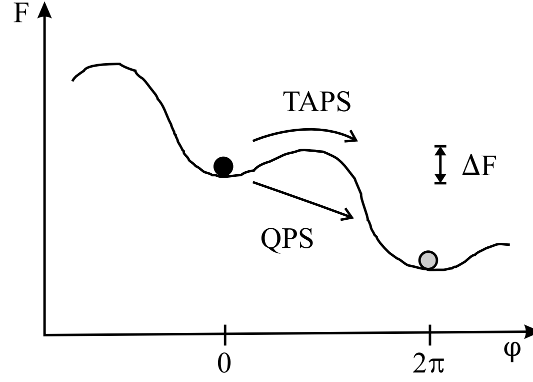


**FIGURE 2.3** *Free energy of a current biased superconducting wire as function of the phase $\varphi$. There exist two mechanisms to overcome the energy barrier $\Delta F$: thermally activated phase slip (TAPS) and quantum phase slip (QPS).*

energy by choosing a phase giving a lower energy to the system. However, there is a barrier of height $\Delta F$ to overcome. If there is enough thermal energy available, the system can change its state 'classically' by jumping over the barrier. Other possibility is the quantum mechanical tunnelling of the order parameter through the barrier. The energy minima are separated by phase shifts of $2\pi$, and it is said that during the thermal activation or quantum tunnelling the phase 'slips' by the amount $2\pi$.

Each thermally activated phase slip generates a voltage pulse on the wire, that can be written according to LAMH[4] model [33,41] as:

$$V_{\mathrm{S}} = 2\Phi_0\Omega(T)\sinh\left(\frac{I_{\mathrm{S}}}{2I_1}\right)\exp\left[\frac{-\Delta F}{k_{\mathrm{B}}T} - \sqrt{\frac{2}{3}\frac{I_{\mathrm{S}}^2}{3\pi I_1 I_{\mathrm{C}}}}\right], \tag{2.8}$$

where $I_{\mathrm{S}}$ is the applied current and $I_{\mathrm{C}}$ is the critical current. The formula is valid when $I_{\mathrm{S}} \ll I_{\mathrm{C}}$, but $I_{\mathrm{S}}$ does not have to be small compared to $I_1$ defined by

$$I_1 = k_{\mathrm{B}}T_{\mathrm{C}}/\Phi_0, \tag{2.9}$$

where $\Phi_0 = h/2e$ is the flux quantum. The attempt frequency $\Omega(T)$ is defined as

$$\Omega(T) = \frac{L}{2\pi^2\xi(T)\tau_{\mathrm{GL}}}\sqrt{\frac{3\pi\Delta F}{k_{\mathrm{B}}T}}, \tag{2.10}$$

where $\tau_{\mathrm{GL}} = h/[16k_{\mathrm{B}}(T_{\mathrm{C}} - T)]$ is the Ginzburg-Landau relaxation time, and energy barrier

$$\Delta F = \frac{8}{3}\sqrt{2}[\sigma H_{\mathrm{C}}^2(T)\xi(T)/8\pi], \tag{2.11}$$

[4]Abbreviation from the names of Langer, Ambegaokar, McCumber and Halperin, the ones who derived and developed the theory

where $\sigma$ is the cross-sectional area of the wire.

The effective resistance depends exponentially on the ratio of the condensation energy of a minimum size superconducting domain of $\sim \sigma\xi$ and the thermal energy $k_{\mathrm{B}}T$ [33,41]:

$$R_{\mathrm{eff}}(T) \propto R_{\mathrm{N}}\frac{L}{\xi}\exp\left(-\frac{B_C^2 K\xi\sigma}{k_{\mathrm{B}}T}\right), \tag{2.12}$$

where $R_{\mathrm{N}}$ is the normal state resistance, $L$ is the length of the wire, $B_{\mathrm{C}}(T)$ is the critical magnetic field, and $K\xi\sigma$ is the effective volume of the phase-slip center (minimum size of a superconductor to be driven normal). Coefficient $K$ should be of the order of one: $K \sim 1$, relating the geometrical size to the effective one. The complete expression for the effective resistance includes other terms [33,41] being dependent, for example, on the ratio between the measuring current and the critical current (see Eq. 2.8). However, as the used measuring currents in experiments described in chapter 4 ($\sim$ 10 nA) were much smaller than the critical value, these terms do not contribute quantitatively and are skipped in Eq. (2.12) for simplicity.

The validity of the expression (2.12) has been verified experimentally using tin whiskers [38,46].

### 2.2.2 Resistance due to quantum phase slips

As described in previous section, part of the resistance of one-dimensional superconductors is caused by thermally activated phase slips. A competing mechanism is macroscopic quantum tunnelling of the phase of superconductor, often called quantum phase slip (QPS). Zaikin and Golubev have presented a detailed microscopic theory of quantum phase slips [29,68] (GZ model). Their starting point was a Hamiltonian including short range attractive BCS and long range repulsive Coulomb interaction. With sophisticated theoretical treatment they were able to calculate the quantum phase slip rate as

$$\Gamma_{\mathrm{QPS}} = B\exp(-S_{\mathrm{QPS}}), \tag{2.13}$$

where

$$S_{\mathrm{QPS}} = A\frac{R_{\mathrm{Q}}}{R_{\mathrm{N}}}\frac{L}{\xi(\mathrm{T})} \tag{2.14}$$

and the prefactor

$$B \approx \frac{S_{\mathrm{QPS}}L}{\tau_0 x_0}, \tag{2.15}$$

where $x_0$ is the size of the QPS core $x_0 \approx \xi_0$ and $\tau_0$ is duration of the QPS. $L$ is the length of the wire and $A = 2(\sqrt{a_2a_3} + \sqrt{a_4a_5})\pi$, where $a_{\mathrm{j}}$ are numerical factors of

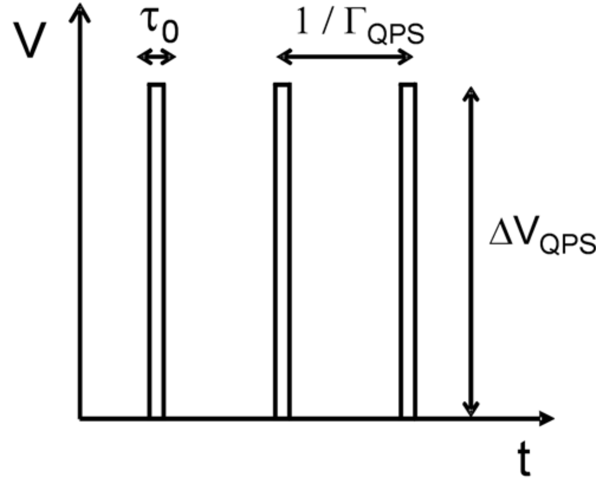


**FIGURE 2.4** *Schematic representation of the phase slip events in time domain. While each phase slip of duration* $\tau_0$ *the voltage jumps by* $\Delta V_{\mathrm{QPS}}$.

order one depending on the precise form of the trial functions $\varphi(x,\tau)$ used in their calculations. The results presented here are valid in case of short wire, when only one QPS may occure at a time:

$$L \ll C_0 \frac{h}{k_{\mathrm{B}}T}, \tag{2.16}$$

where $C_0$ is the velocity of the Mooij-Schoen mode, which depends on the kinetic inductance and capacitance of the wire.

In a short wire, not much longer than the coherence length, only single phase slip can be activated at a time. Each slip generates a voltage jump, represented in Fig. 2.4,

$$\Delta V_{\mathrm{QPS}} = \frac{IR_{\mathrm{N}}\xi}{L}, \tag{2.17}$$

where $I$ is the measuring current. Time averaged voltage is

$$< V >= \Delta V_{\mathrm{QPS}}\tau_0\Gamma_{\mathrm{QPS}}. \tag{2.18}$$

Defining the effective resistance $R(T) \equiv R_{\mathrm{eff}} =< V > /I$, one gets

$$\frac{R_{\mathrm{eff}}}{R_N} = \frac{\xi_0\tau_0}{L\Gamma_{\mathrm{QPS}}}. \tag{2.19}$$

Zaikin and Golubev compared the theory to the experiments made by Bezryadin *et al.* [13,34]. In the experiments, some of the measured $Mo_{79}Ge_{21}$ nanowires showed no traces of superconductivity well below the bulk critical value. The theory

gives high QPS rates to the samples that in experiments turned out to be 'insulating'. This speaks strongly for the observation of the QPS phenomenon in mentioned experiments.

## 2.3 Single charge tunnelling devices

In this section, an introduction to the charging effects is presented and some systems capable of manipulating single charges are introduced. These are single electron box (SEB), single electron transistor (SET) and single electron pump (SEP). In superconducting case the unit charge is 2e corresponding to a Cooper pair, and the systems are called Cooper pair box (CPB), superconducting single electron transistor (SSET) and Cooper pair pump (CPP), respectively. Also cotunnelling, a possible error source in applications is discussed.

There are several components in nanoelectronics capable of manipulating single charges. Let us consider a tiny piece of metal isolated from its environment through capacitances $C_\mathrm{i}$ (Fig. 2.5). These capacitances introduce an energy scale, charging energy, that corresponds to a single electron charge $e$ in the metallic *island* defined by

$$E_C = \frac{e^2}{2C_\Sigma}, \tag{2.20}$$

where $C_\Sigma = C_1 + C_2 + C_3$ in the case of Fig. 2.5. It is seen from Eq. 2.20, that the charging energy increases as the total capacitance decreases.

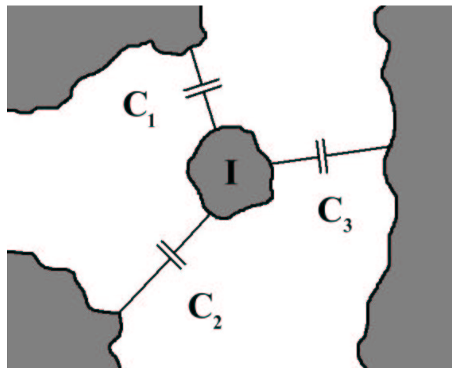


**FIGURE 2.5** *A tiny metallic island isolated from its environment via capacitors.*

The charging energy $E_\mathrm{C} = e^2/2C_\Sigma$ is inversely proportional to the area of the capacitors. This can be seen by substituting the expression for the plate capacitor $C = \varepsilon\varepsilon_0 A/d$ to Eq. (2.25), where $A$ is the junction area, $d$ is the thickness and $\varepsilon$ the dielectric constant of an insulating barrier. This feature is used in section 5 in order to detect the change in tunnel junction areas after ion beam sputtering.

When the capacitance of the system is very small, of the order of femtofarads, the corresponding temperature calculated as $T = E_\mathrm{C}/k_\mathrm{B}$ is around 1 K. To be able to see the interesting consequences of the high charging energy in measurements, the

charging energy should be larger than the thermal energy,

$$E_{\mathrm{C}} \gg k_{\mathrm{B}}T. \tag{2.21}$$

The large charging energy enables the manipulation of single charges, since even the transfer of a single charge to a small metallic island requires noticeable energy. The systems realizing this condition usually include tunnel junctions, which are essentially very small capacitors. In these junctions the insulating layer is very thin, typically 1-2 nm, and the electrons are able to tunnel quantum mechanically through the junction [2]. Fig. 2.6 shows a typical design of tunnel junction consisting of thin oxide layer between two metallic electrodes.

**FIGURE 2.6** *Typical realization of tunnel junction consisting of a thin oxide layer between metal electrodes.*

The tunnelling of electrons occur with a finite probability only if there is enough energy available for the tunnelling event. In single electron tunnelling devices this energy can be tuned with external voltage. In the following, three different kind of single electron tunnelling devices used in charge manipulation are introduced: single electron box, single electron transistor, and single electron pump.

### 2.3.1 Single electron box

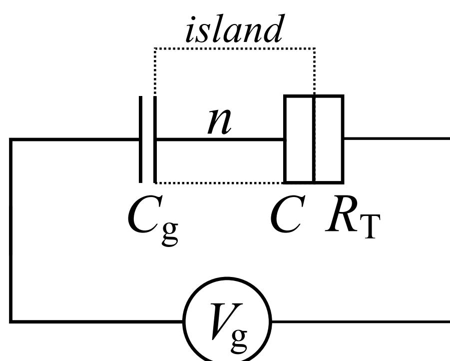


**FIGURE 2.7** *Schematics of a single electron box. $C$ is a capacitance and $R_{\mathrm{T}}$ the tunnelling resistance of the junction.*

In single electron box, a tiny island isolated from the environment is formed between tunnel junction and capacitor (Fig. 2.7). The number of charges in the box can change by tunnelling through the tunnel junction. Let us divide the total number of electrons in the island as

$$n_{\mathrm{Total}} = n_0 + n, \tag{2.22}$$

where $n_0$ represents the charge compensating the charge of the positive ion background and $n$ is the number of additional tuneable *excess* electrons on the island.

The voltage $V_{\mathrm{g}}$ applied to the system changes the effective charge on the island. Considering a situation where the island contains $n$ excess electrons, the charging energy of the whole circuit can be written as [60]

$$E_{\mathrm{ch}}(n, V_{\mathrm{g}}) = \frac{(ne - C_{\mathrm{g}}V_{\mathrm{g}})^2}{2C_{\Sigma}}, \tag{2.23}$$

where $C_{\Sigma} = C + C_{\mathrm{g}} + C_0$, $C_{\mathrm{g}}$ being the gate capacitance and last term the ground capacitance. In Fig. 2.8 this charging energy is plotted as function of the normalized

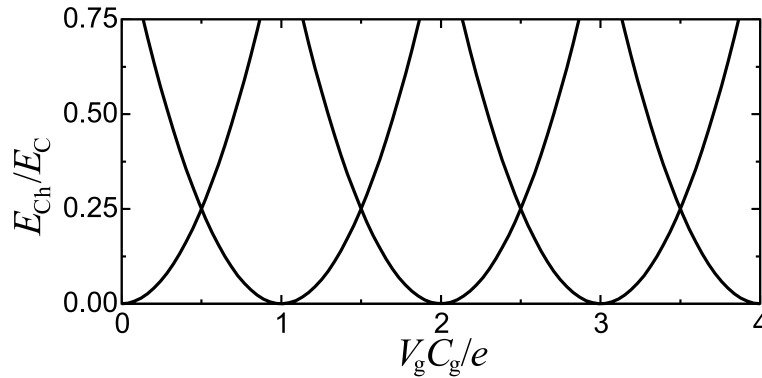


**FIGURE 2.8** *The charging energy of single electron box as function of the normalized gate charge for different numbers of excess electrons $n$.*

gate charge $C_{\mathrm{g}}V_{\mathrm{g}}/e$ for different numbers of excess electrons $n$. As an example, let us consider an initial state of the system with gate voltage $V_{\mathrm{g}} = 0$. When increasing the gate voltage, the system follows the energy parabola calculated from Eq. 2.23 with $n = 0$ as long as it gives the minimum energy to the system. When the degeneracy point at $C_{\mathrm{g}}V_{\mathrm{g}}/e = 1/2$ is passed, the parabola corresponding to $n = 1$ gives the energy minimum to the system and one extra electron tunnels to the island through the tunnel junction. The next tunnelling occurs when the next degeneracy point is reached and so on. Thus the number of electrons in the island is a step-like function of the external voltage $V_{\mathrm{g}}$, as depicted in Fig. 2.9.

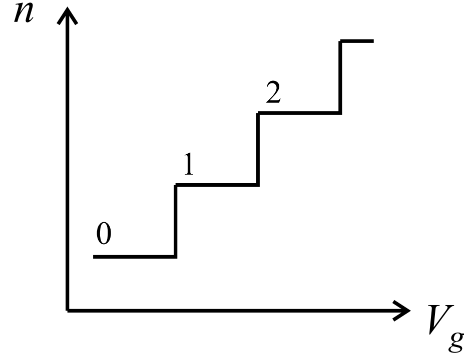


**FIGURE 2.9** *Excess charge in single electron box as a function of external voltage.*

### 2.3.2 Single electron transistor

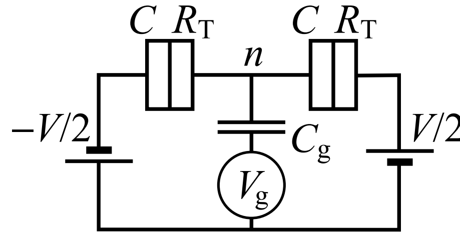


**FIGURE 2.10** *Schematics of a single electron transistor.*

A single electron transistor consists of an island isolated from the environment via two tunnel junctions, and a gate electrode (Fig. 2.10). The single electron transistor differs from the box in a way that it is 'open' from both sides and the tunnelling of electrons is possible in both junctions. When the bias voltage $V$ is applied, the tunnelling probability is much higher in the direction set by the voltage and there is a net current on that direction. Like in the case of a SEB, the number of excess electrons in the island is function of the gate voltage $V_{\mathrm{g}}$, and the charge on the island is a step-like function of the gate voltage. In this sense the single electron transistor is much like a single electron box, but the extended structure gives more functionality and enables for instance its use as an electrometer as described in section 6.

The Hamiltonian of the single electron transistor in the general case (including the superconducting case) is written as

$$H = H_{\mathrm{Ch}}(q) - \Sigma_{\mathrm{i}=1}^{2} E_{\mathrm{Ji}} \cos(\varphi_{\mathrm{i}}), \tag{2.24}$$

where the first term represents the charging effects and $q = V_{\mathrm{g}}C_{\mathrm{g}}$. The second term describes Josephson coupling, $\varphi_{\mathrm{i}}$ is the superconducting phase difference over the junction $i$ and $E_{\mathrm{J}}$ is the Josephson coupling energy (zero in case of normal state SET). The effect of the nonzero Josephson energy can be seen from Fig. 2.11, where the en-

ergy of the transistor is plotted as function of the normalized gate charge in superconducting state (dashed line, $E_J$ is set to zero in Eq. 2.24; solid line, $E_J/E_C = 0.1$ and $\varphi = 0$). An energy gap of 2 $E_J/E_C|\cos\varphi|$ is formed in the degeneracy points. This is a key feature in many superconducting two-state systems suggested as quantum bits (qubits) as the state of the system biased to the gap area is a superposition of the charge states 0 and 1[5].

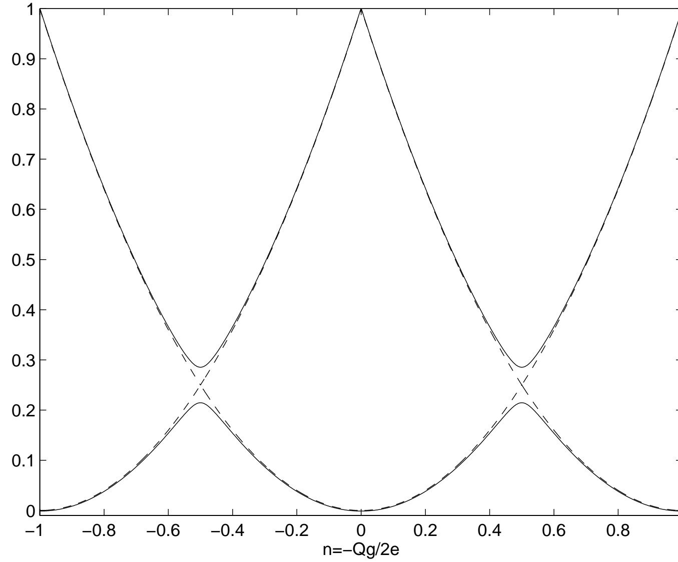


**FIGURE 2.11** *Energy (normalized with the charging energy) of SSET with $\varphi = 0$. The Josephson energy $E_J = 0$ (dashed line ) and $E_J/E_C = 0.1$ (solid line).*

The total charging energy of the SET can be written as

$$H_{Ch} = E_C(u^2 + 2CV/e) - keV, \tag{2.25}$$

where $k$ is the number of electrons passed through the system, $E_C = e^2/2C_\Sigma$ is the unit of the charging energy, $C_\Sigma = C_1 + C_2 + C_g + C_0$ is the sum of the capacitances of the junctions and the gate and the capacitance of the central island to the ground, and $u = V_g C_g/e - n$. Usually it is assumed that the ground capacitance $C_0$ is negligible and the capacitances of the junctions are equal, $C_1 = C_2 \equiv C$.

Top graph of Fig. 2.12 shows typical current-voltage (I-V) characteristics of an aluminium single electron transistor in normal state. The different curves correspond to different gate voltages. It is seen that with certain gate voltage the I-V curve is linear and other curves have flat region. This effect is called Coulomb blockade, and it originates from the fact that tunnelling does not happen if it is not

[5]However this superposition is suppressed quickly by a decoherence due to coupling of the system to its environment.

energetically favourable. At zero temperature and with gate voltage $V_{\rm g} = 0$, an energy $E_{\rm C} - eV/2$ is required to add one electron to the island. The bias voltage is the only source of energy at zero temperature and as a consequence there is no current through the SET below a threshold voltage, that is if $|V| < e/C_{\Sigma}$.

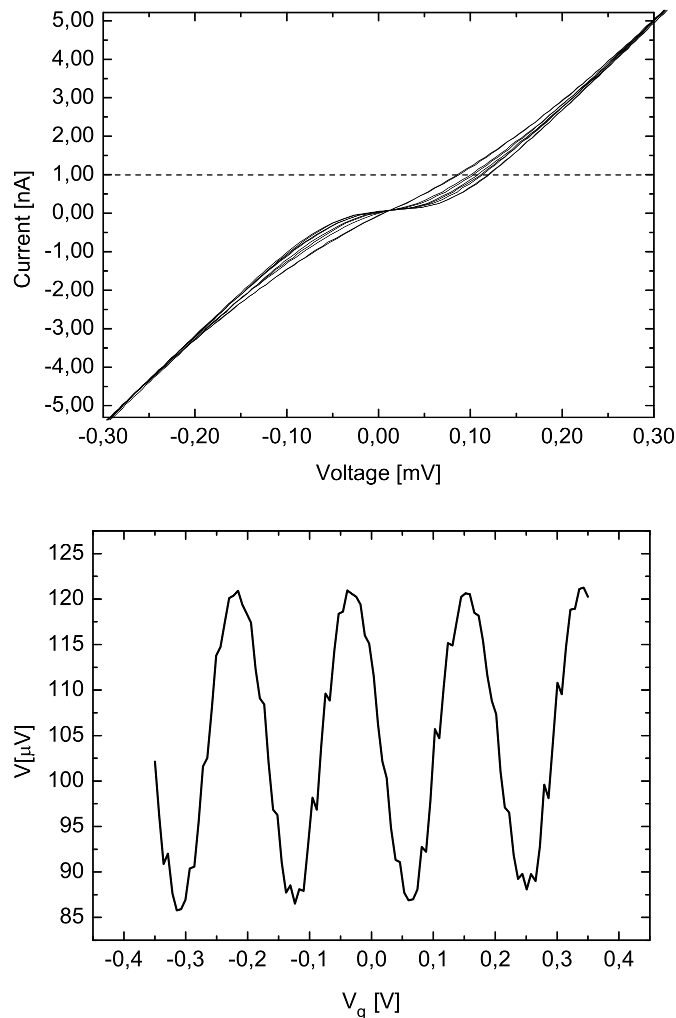


**FIGURE 2.12** *(Top): Typical I-V characteristics of an Al-based SET in normal state me asured at 55 mK (with 1 T magnetic field on in order to keep the sample in normal state). Different curves correspond to different gate voltages. (Bottom): current modulation curves as function of the gate voltage. The sample is current biased to 1 nA (indicated by dashed line in top graph).*

Current modulation curve in bottom graph of Fig. 2.12 is obtained by biasing the SET to a 'sensitive operating point', as an example to 1 nA current indicated with dashed line in the I-V graph and measuring the voltage across the SET as function of the gate voltage. The period of the modulation $\Delta V_g = Q/C_{\rm g}$, where Q is the unit charge. In the normal state unit charge $Q = e$ and the gate capacitance can be deter-

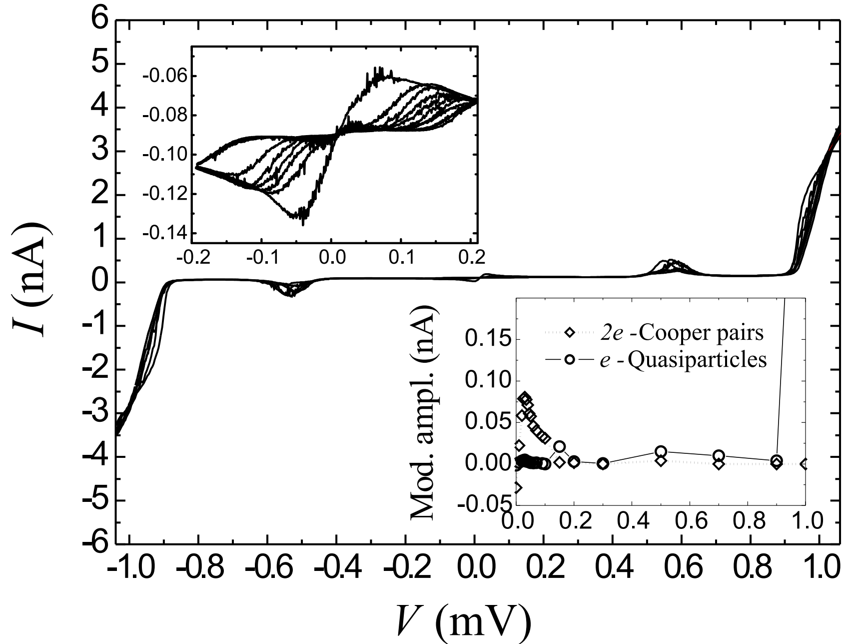


**FIGURE 2.13** *I-V characteristics of superconducting SET. The left-top inset shows a supercurrent region magnified. Right-bottom inset shows amplitude of the gate current modulation for quasiparticles and Cooper pairs as function of the positive subgap voltage.*

mined by measuring the period of the modulation. In the superconducting state the period of the modulation is twice the period of the normal state, since charge carriers in superconductors are Cooper pairs. It is known however, that the observation of this 2e-periodic signal usually requires the fabrication of normal metal electrodes close to the junctions to act as 'quasiparticle traps' [30,32].

This was also seen in our measurements conducted at Jyväskylä. We tried to observe the $2e$-periodicity by measuring the gate current modulation from supercurrent region located near the zero-voltage. This region is depicted in the left-top inset of Fig. 2.13, which shows a typical I-V curve of the voltage biased superconducting SET. The period of this modulation was compared to the period measured from the modulation outside the gap voltage, where the current is carried out by quasiparticles. Before fabricating the normal metal traps, all samples showed $e$-periodicity even when measured from the supercurrent. The samples that had the quasiparticle traps showed $2e$-periodicity. Figure 2.14 shows the current modulations measured at three different gate voltages. The curve measured at $V$=1 mV shows a clear $e$-periodicity as the curve at $V$=70 $\mu$V clear 2e-periodicity. The third curve measured at $V$=0.15 mV is a combination of these two.

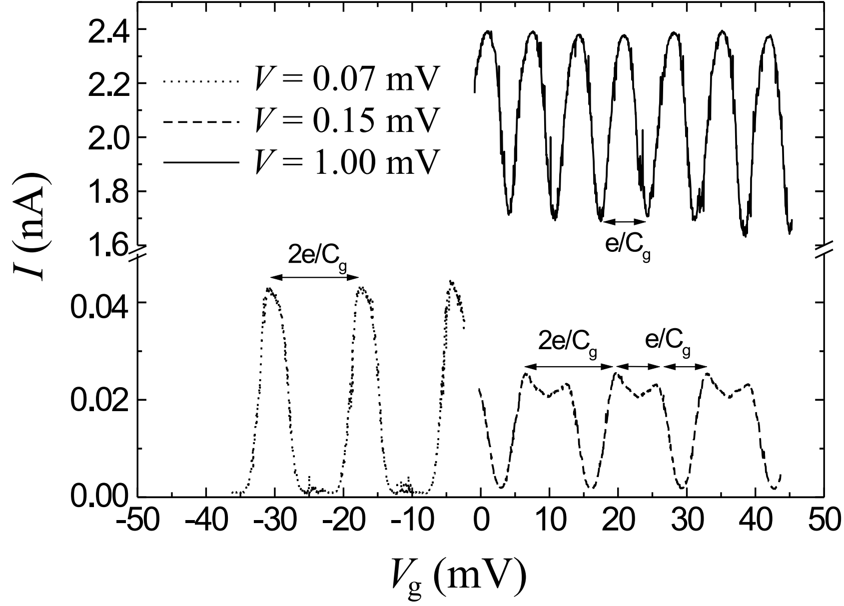


**FIGURE 2.14** *Current modulation curves from superconducting SET measured with different bias voltages. The left-bottom one shows clear 2$e$-periodic signal.*

**Single electron transistor at weak Coulomb blockade regime**

When charging effects were first studied, the attention was focused at the region $k_\mathrm{B}T \ll E_\mathrm{C}$, where the studied systems exhibited 'extreme Coulomb blockade'. However, it was pointed out by Pekola *et al.* [55], that the other limit $k_\mathrm{B}T > E_\mathrm{C}$ is also interesting. It was shown that the tunnel junction arrays can be used in primary thermometry, since the half width of the dip in measured differential conductance is proportional to temperature as

$$V_{1/2} = 5.439 N k_\mathrm{B} T/e, \tag{2.26}$$

where $N$ is the number of tunnel junctions in the array. In the study described in Chapter 5 the parameter of interest is particularly the relative height of the dip in conductance curve (Fig. 2.15), which is shown to be proportional to the charging energy [55] as

$$\Delta G/G_\mathrm{T} = \frac{E_\mathrm{C}}{6 k_\mathrm{B} T}, \tag{2.27}$$

where $\Delta G$ is the height of the conductance dip and $G_\mathrm{T}$ is the conductance value far from zero voltage. This formula can be used for example in secondary thermometry or if the temperature is known, in determining the charging energies of systems, as it is done in Chapter 5.

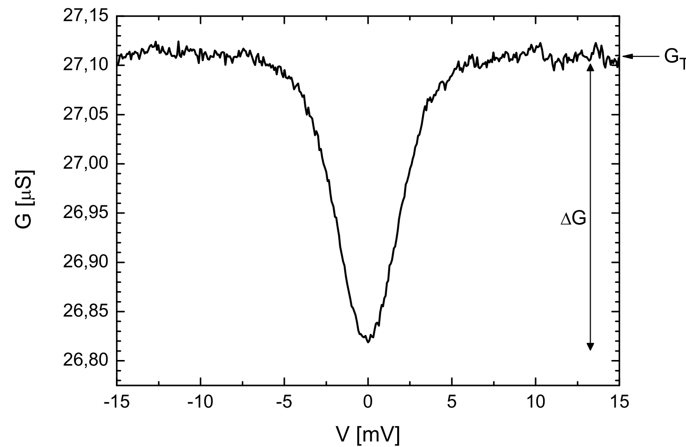


**FIGURE 2.15** *Typical dependence of the conductance $G$ vs. voltage $V$ of a SET at liquid helium temperature 4.2 K.*

### 2.3.3 Single electron and single Cooper pair pump

Even more functionality is obtained by adding a third tunnel junction in series. The system is now called single electron pump, consisting of two islands and gate electrodes to change the potential of the corresponding island. The operation as a pump

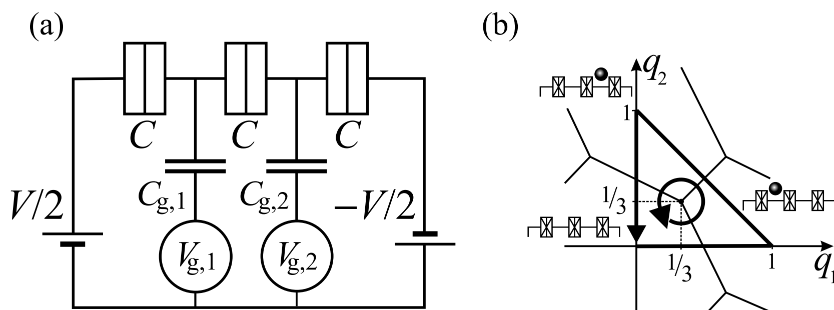


**FIGURE 2.16** *a) Schematics of a single electron pump. b) Cycle in gate charge plane used in pumping Cooper pairs through the system.*

can be understood as follows. The energy of the system can be calculated by using model Hamiltonian

$$H = H_{\mathrm{Ch}}(q_1, q_2), \tag{2.28}$$

depending on the gate charges $q_{\mathrm{i}} = V_{\mathrm{g,i}}C_{\mathrm{g,i}}$. In superconducting case the Hamiltonian also includes term representing Josephson coupling[6]. Figure 2.17 shows the

[6] $H_{\mathrm{J}} = -\Sigma_{i=1}^{3} E_{\mathrm{Ji}} \cos(\varphi_{\mathrm{i}})$, where $i$ is a sum over the junctions and $\varphi_{\mathrm{i}}$ is a phase over the corresponding junction. Note that scaling of charges changes also from $e$ to $2e$.

energy of the single electron pump as function of the normalized gate charges. The energies of the ground states form a honeycomb-like structure.

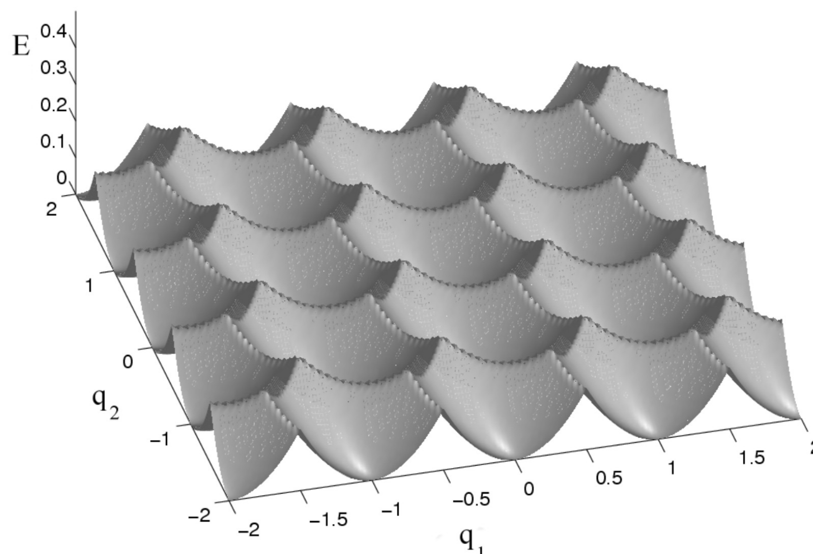


**FIGURE 2.17** *Energy (normalized with the charging energy) of the single electron pump as function of the normalized gate charges.*

Figure 2.18 shows the energy of the system in the superconducting case with phase $\varphi = 0$ with vanishing Josephson coupling. By comparing this to Fig. 2.19 where $E_{\mathrm{J}}/E_{\mathrm{C}} = 0.1$, the effect of the Josephson coupling is seen to decrease the energy near the degeneracy points. What happens is that an energy gap is formed in between the ground state (shown) and the excited states (compare with Fig. 2.11).

Figure 2.20 shows a contour plot of the honeycomb structure. Each honeycomb represents the area where certain charge configuration of the pump is stable. As an example, inside the area $|10\rangle$, there is one excess unit charge in the left island and zero in the right. It is seen from Fig. 2.20 that when manipulating the gates so that the system goes through a path depicted in Fig. 2.16b), one electron is transferred through the system. If the path is circulated in the opposite direction, the direction of the pumped charge changes also. The pumping is possible with a very high accuracy if more junctions and also more gates are added to the system. In future one might expect a current standard achieved this way. At the moment approximately $10^8$ electrons can be pumped with the single electron pump before first error in pumping. This means also that one can charge capacitors with very good accuracy with these pumps because the exact amount of electrons in the capacitor is known. It has been shown though, that when operating pumps in superconducting state there is a fundamental limit of the pumping accuracy [3]. However, it has been suggested, that

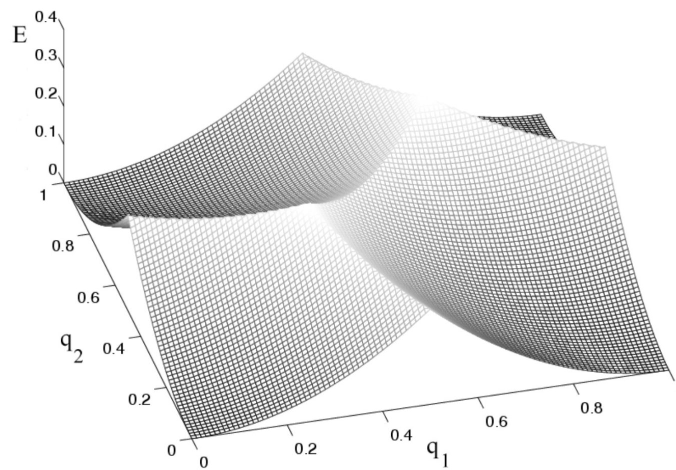


**FIGURE 2.18** *Energy of the Cooper pair pump with phase $\varphi = 0$ and vanishing Josephson coupling.*

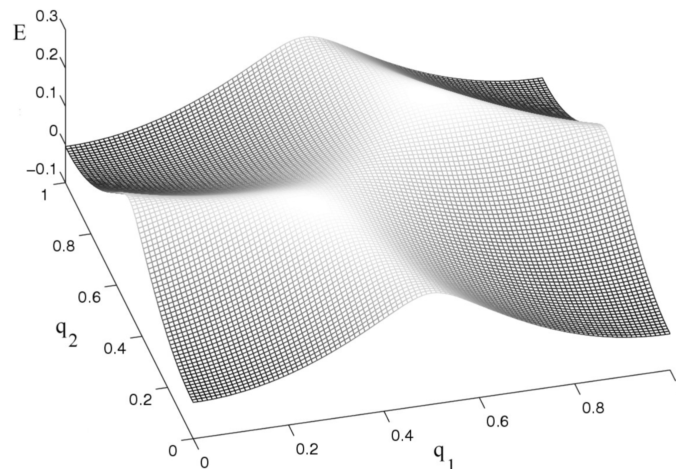


**FIGURE 2.19** *Energy of the Cooper pair pump with phase $\varphi = 0$ and $E_\mathrm{J}/E_\mathrm{C} = 0.1$*

these problems can be solved with the so-called R-pump [71,37,70].

One should keep in mind, that as the number of the gate electrodes increase, the systems become much more difficult to operate. This is partly because the voltage applied to certain gate electrode does not change only the potential of the corresponding island, but affects also the others. This cross-coupling can be as high as 80 % and has to be compensated away to be able to operate the system properly. The compensation circuit electronics become more and more complicated as the size of the system increases.

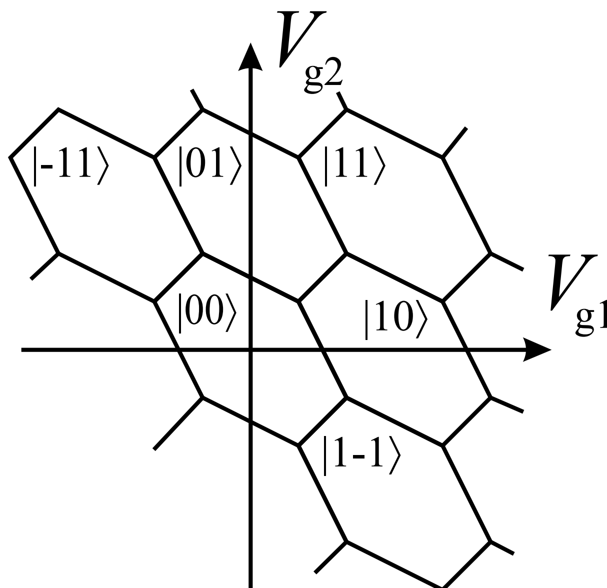


**FIGURE 2.20** *Diagram of lowest energy charge states of single electron pump as a function of the gate voltages.*

**Effect of the quasiparticles to the honeycomb structure**

In the superconducting case the measurement of the clear $2e$-honeycomb structure (supercurrent as a function of the gate voltages) requires system with no quasiparticles. This became clear in our measurements [4], where we obtained a honeycomb represented in Figure 2.21. The resulted graph contained several honeycomb structures separated by period of $e$. We attributed this to quasiparticles tunnelling in and out of the islands which has the same effect as changing the gate charge by one electron thus introducing the shifts of the $2e$-honeycomb structures. Despite of this usually undesired effect, the pump has been used for turnstile-like current transfer with the 3 % error in transfer. The operation takes advantage of coherent tunnelling, cotunnelling and relaxation processes and is discussed in detail in ref. [4].

### 2.3.4 Cotunnelling in single electron transistor

In the coulomb blockade regime of the SET transistor, the sequential tunnelling of electrons is blocked at low temperatures. However, a cotunnelling channel is open for charge transport and carries out a significant part of the current in this regime. In a cotunnelling event two electrons tunnel simultaneously through the two tunnel junctions of the transistor by using a virtual charge state on the island.

The theory for cotunnelling in SET at small bias and low temperature limit has been developed by Averin and Nazarov [11] and verified experimentally in metallic systems by several researchers [26,21,53].

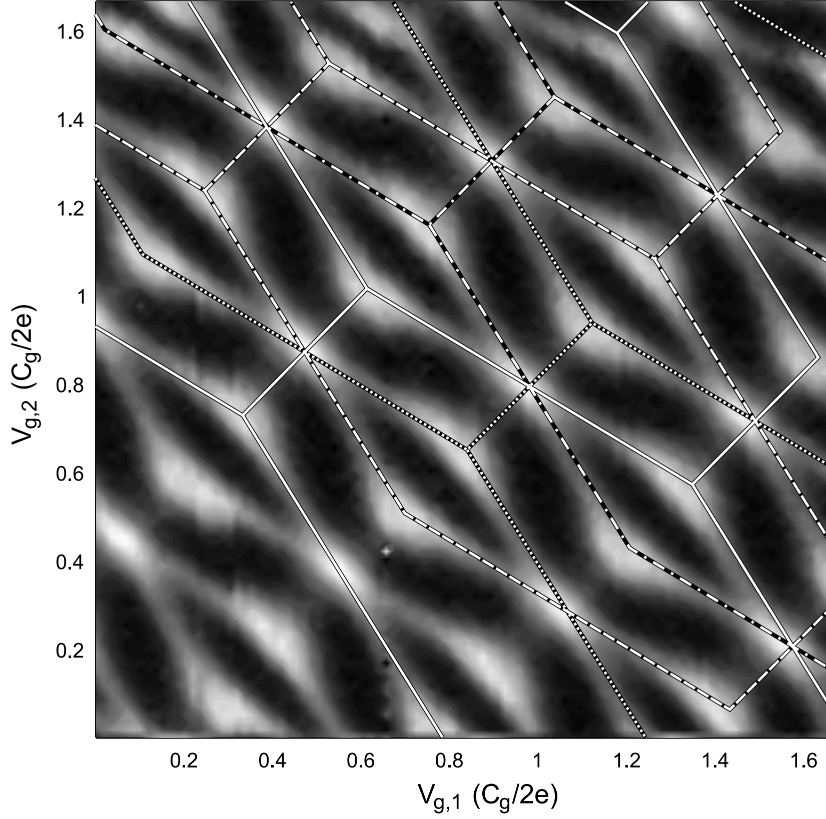


**FIGURE 2.21** *Supercurrent of the Cooper pair pump as function of the gate voltages. The quasiparticle tunnelling has induced many honeycomb structures separated by period of* $e$.

The inelastic cotunnelling current in transistor for small bias voltage ($eV_{\mathrm{DC}} \ll \Delta^{\pm}$) and low temperature ($k_{\mathrm{B}}T_{\mathrm{e}} \ll \Delta^{\pm}$) was derived by Averin and Nazarov [11] as

$$I_{\mathrm{DC}} = \frac{R_{\mathrm{K}}}{24\pi^2 R_1 R_2}\left(\frac{1}{\Delta^+} + \frac{1}{\Delta^-}\right)^2 \left[(2\pi k_{\mathrm{B}}T_{\mathrm{e}})^2 + (eV_{\mathrm{DC}})^2\right] V_{\mathrm{DC}}, \qquad (2.29)$$

where $R_{1,2}$ are the tunnelling resistances of the tunnel junctions, at zero bias $\Delta^{\pm} = (e/C_{\Sigma})(e/2 \mp C_{\mathrm{G}}V_{\mathrm{G}}) \pmod{(e^2/C_{\Sigma})}$ are the energies needed to add/remove one electron to/from the island, $T_{\mathrm{e}}$ is the temperature of the electron system, and $R_{\mathrm{K}} = h/e^2$. In the maximum blockade state, $\Delta^{\pm}$ reduces to the charging energy $E_{\mathrm{C}} = e^2/2C_{\Sigma}$, where $C_{\Sigma} = C_1 + C_2 + C_{\mathrm{G}}$ is the total capacitance of the island assuming the ground capacitance negligible.

Let us now assume, that a high frequency signal is added to the bias voltage $V$ and calculate the cotunnelling current in this case by substituting $V_{\mathrm{DC}} \rightarrow V_{\mathrm{DC}} +$

$V_{\mathrm{AC}} \cos(2\pi f t)$ to Eg. 2.29 and average over time:

$$
\begin{aligned}
I_{\mathrm{DC}}^{(1)} &= f \int_0^{1/f} \left[ \frac{R_{\mathrm{K}}}{24\pi^2 R_1 R_2} \left( \frac{1}{\Delta^+} + \frac{1}{\Delta^-} \right)^2 \right] \times \\
&\times \left\{ (2\pi k_{\mathrm{B}} T_{\mathrm{e}})^2 + [eV_{\mathrm{DC}} + eV_{\mathrm{AC}} \cos(2\pi f t)]^2 \right\} \{ (V_{\mathrm{DC}} + V_{\mathrm{AC}} \cos(2\pi f t) \} dt \\
&= \frac{R_{\mathrm{K}}}{24\pi^2 R_1 R_2} \left( \frac{1}{\Delta^+} + \frac{1}{\Delta^-} \right)^2 \left[ (2\pi k_{\mathrm{B}} T_{\mathrm{e}})^2 + (eV_{\mathrm{DC}})^2 + \tfrac{3}{2} (eV_{\mathrm{AC}})^2 \right] V_{\mathrm{DC}}.
\end{aligned}
\tag{2.30}
$$

This formula is valid in the adiabatic limit, where all frequency, temperature and amplitude of the signal are small.

It has to be noted, that taking into account the 'photon assisted cotunnelling' derived by Flensberg [25] there is an additional term to be included in the cotunnelling current (Eq. 2.30):

$$
I_{\mathrm{DC}}^{(2)} = \frac{R_{\mathrm{K}}}{48\pi^2 R_1 R_2} \left( \frac{1}{\Delta^+} + \frac{1}{\Delta^-} \right)^2 \left( \frac{1}{\Delta^-} - \frac{1}{\Delta^+} \right) \times \left[ (2\pi k_{\mathrm{B}} T_{\mathrm{e}})^2 + \tfrac{3}{4} (eV_{\mathrm{AC}})^2 + (hf)^2 \right] (eV_{\mathrm{AC}})^2 . \tag{2.31}
$$

In case of maximum Coulomb blockade, this term vanishes, since then $\Delta^{\pm} = E_{\mathrm{C}}$. Thus current predicted by Eq. 2.30 can be studied experimentally by using a gate voltage corresponding to maximum Coulomb blockade.

Cotunnelling is an important error process in devices based on single electron tunnelling. We have studied the effect of externally applied high-frequency field to cotunnelling in SET and the results are presented in chapter 7. There the measured quantity is zero-bias differential conductance, and the comparison to the theory has been made by taking the derivative from Eq. 2.30 at $V$=0,

$$
\frac{dI}{dV_{\mathrm{DC}}}_{(V_{\mathrm{DC}}=0)} \propto T^2, V_{\mathrm{AC}}^2. \tag{2.32}
$$

One might wonder why the use of maximum Coulomb blockade is needed in eliminating the effect of photon assisted cotunnelling, as the dynamical conductance calculated by using Eq. 2.32 from equation 2.31 is zero. However, the lock-in amplifier applies a small current exitation around zero-current and measures its effect to the voltage and in this way determines the dynamical conductance. This exitation is chosen to be as small as possible, but the essential thing is that the measurement is not done at zero-current but around zero-current and so photon assisted cotunnelling might have an effect if not using the maximum blockade.

### 2.3.5 Single charge devices as potential building blocks of a quantum computer

In the early days of quantum mechanics it was believed, that there is a fundamental difference between microscopic and macroscopic systems, the former behaving quantum mechanically and the latter 'classically'. However, in last twenty years it has become clear, that also macroscopic systems can behave quantum mechanically. One proof has been the direct observation of coherent oscillation between two macroscopically distinct charge states of Cooper pair box by Nakamura *et al.* [45]. This observation opened new scenarios in realising a quantum computer [19], which requires quantum bits, or *qubits*, elementary building blocks of quantum computer. In principle any system capable of macroscopic quantum coherence between two of its distinguished states (without the other states disturbing) can be used as a qubit, but one problem has been the scaling of the number of qubits to large enough. By using solid state qubits it is possible to fabricate large number of qubits on silicon chip, but the problem is the required controlled couplings between the qubits; it is necessary to be able to perform unitary transformations to pairs of qubits within a small collection of qubits without affecting the others. To compare this to the progress made with ion traps, the situation is somewhat opposite. In ion traps few ions can be trapped and excited to form qubits and the couplings between these can be realised with laser radiation. The problem is the trapping of large number of ions and also the quantum decoherence due to coupling between the ion motion and the environment. The maximum number of ions that have ever been trapped is about 40, but the manipulation of ions fulfilling all the requirements for quantum computing listed for example by Divincenzo [19] has been successful just for a system of two ions [43].

There are two main ideas how to realise a solid state charge qubit both of them including tunnel junctions. The use of Josephson junction array [10] and single Josephson junction [58,57,39] has been proposed. In Averin's proposal including arrays an important aspect is that one should be able to transfer Cooper pairs in these arrays in a controlled way. Transferring electrons one by one in tunnel junction arrays has been demonstrated with high accuracy by using single electron pumps. The limiting factor in the case of Cooper pair pumping is the accuracy of pumping. It has been shown that there is a fundamental inaccuracy in pumping of Cooper pairs [3]. Later Zorin et. al suggested, that this problem can be avoided by using the R-pump [71,37,70].

The manipulation of qubits in controllable way should be accompanied with the ability of performing a strong measurement of the state of the system after the

calculations. The strong here means the textbook-type quantum measurement that determines in which orthogonal eigenstate of the system the state belongs to. In charge qubits the readout device suggested is usually single electron transistor used as an electrometer to detect if the qubit has zero or one excess Cooper pair, i.e. if it collapsed into the charge eigenstate $|0\rangle$ or $|1\rangle$. The problem is that the measurement device cannot be considered as a separate system but is has to be taken into account when calculating the time evolution of the quantum system (see for example Ref. [57] as an example of this kind of treatment).

# Chapter 3

# Ion beam sputtering method for progressive reduction of nanostructures dimensions

## 3.1 Introduction

There is a variety of different techniques available for fabrication of nano- or micron-sized structures. Ultraviolet (UV) lithography is widely used in microelectronic industry to fabricate large-scale integrated circuits with vast amount of functional elements at once. However, the minimum lateral dimensions attainable with this technique is around 250 nm. By using deep UV light the limit was put to 90 nm by Intel in 2003. More advanced methods based on use of electron beam lithography (EBL) are capable to provide even smaller dimensions and has been applied, e.g., to fabrication of 5-7 nm wide etched lines on a silicon substrate [16]. However, when evaporating metallic structures through masks made with EBL the limit is higher, around 20-50 nm, depending on the properties of the resist material and the performance of the used equipment. The disadvantage of EBL is that it is very slow compared to UV-techniques. X-ray lithography can in principle be used for patterning, but this requires significantly more efforts and complicated masks [65]. It is also possible to use the sharp tip of an atomic force microscope (AFM) to transfer single particles on a substrate to form a nanopattern [36]. Alternatively, one can oxidize patterns on a hydrogen-passivated surface with the tip or scratch the pattern on a thin resist layer (see Ref. [35] and references therein for detailed description of the AFM based methods). The difficulty in using AFM in patterning is in removal of the mask material (lift-off) after metal evaporation. As a result, AFM based nanofabrication at present has rather limited range of applications.

We have studied a different kind of approach where the dimensions of the prefabricated nanostructures are reduced by ion beam sputtering in controllable and reproducible way. Aluminium nanowires (chapter 4) and single electron transistors (chapter 5) have been used to test applicability of the sputtering method. The change in the dimensions of the tunnel junctions was detected by electrical measurements of the charging energy $E_C$ at liquid helium temperature 4.2 K (see section 2.3.2). In case of nanowires, the decrease of the diameter was determined from the normal state resistance of the wire and from the change in slope of superconducting transition $R(T)$.

### 3.1.1 Other studies concerning miniaturization of nanostructures and increasing the operational temperatures of devices

To our knowledge, an application of the ion gun etching (sputtering) for reducing the size of nanostructures has not been reported elsewhere. However, some other techniques have been tested for the same purpose. One possible approach is wet etching, where the structure is inserted into etching solution which removes material from the surface with high selectivity. There are problems in etching of narrow structures, for instance thin wires, as etching is not homogenous and breaks are formed very easily. Chemical etching can give satisfactory results at scales $\geq 100$ nm.

Nakamura *et al.* have developed a successful method to reduce dimensions of metal-oxide-metal tunnel junctions. They have studied the reduction of the tunnel junction areas and capacitances of $Al/Al_2O_3/Al$ single electron transistors by using "anodization controlled miniaturization enhancement" (ACME) [44]. The method has been reported very efficient and operation temperatures as high as 30 K has been reached (the current modulations by gate voltage was observable at this temperature). This method has been proved to work nicely in case of tunnel junctions, but as far as we understand it cannot be used to decrease cross-sectional area of nanowires and moreover the method cannot be used to push the operation temperatures of single electron devices up to room temperature.

One does not necessarily need special methods to reduce dimensions of prefabricated structures to obtain high operation temperatures of single electron devices. For instance Chen *et al.* have observed Coulomb blockade effects at 77 K by introducing AuPd islands of sizes between 2 and 3 nm in between source and drain electrodes separated by a gap of 20 nm [17]. A problem in this approach is that it is difficult to control the distribution of the grains in the devices. Similar kind of approach has been studied by others also (see e.g. [66, 54, 56]). A breakthrough in

nanofabrication has been the single electron transistors operating at room temperature fabricated with conventional electron beam lithography and shadow evaporation method [52].

## 3.2 Description of the method

The samples are three-dimensionally dry etched by ion beam sputtering in a set-up consisting of a high vacuum (p$\sim 10^{-5}$ mbar) experimental chamber equipped with a sample manipulator and TECTRA Electron Cyclotron Resonance (ECR) plasma ion source capable of delivering wide and homogeneous high current ion beams (see Fig. 3.4). Before sputtering, the samples are cleaned with acetone in an ultrasonic bath and subsequently rinsed in isopropanol. Prior to sputtering the surface of the structures is checked by profiler Tencor P15 which is capable to provide a vertical step height repeatability of $\sim$6-7 Å. For dry etching, the samples are bombarded by 1 keV $Ar^+$ ions to a certain fluence using an ion beam current density of about 0.014 mA/cm$^2$. In order to ensure uniform etching over the whole sputtered area, the ions incidence is 60$^\circ$ off the surface normal and the samples are rotated while sputtering (see Fig. 3.1). To avoid overheating of the samples exposed to high current ion beam, the sample holder made of copper was cooled with water and the temperature was estimated to be close to room temperature. Part of the sample surface can be protected against sputtering to form a step on the surface between exposed and non-exposed areas that could be subsequently used for profiling and etching rate calibration.

$Ar^+$ ions of energy 1 keV impinging on the surface at an angle of 60 degrees with respect to the surface normal practically do not penetrate into the subsurface layers. The range of the ions in Al matrix was calculated by SRIM (Stopping and Ranges of Ions Matter) program [69] for the selected geometry: SRIM is a group of programs [5] which can be used in calculating stopping and range of ions of energy between 10 eV and 2 GeV into matter by using full quantum mechanical treatment of ion-atom collisions. The calculation includes statistical algorithms allowing the ion to make jumps between calculated collisions and then averaging the collision results over the intervening gap. The program also takes into account the fact that during the collision the ion and atom have a screened Coulomb collision which include exchange and correlation interactions between the overlapping electron shells. The long-range interactions of ions creating electron excitations and plasmons are also included. The program has become a standard tool in the fields including ion collisions with matter. The full description of the calculational methods can be found from ref. [69].

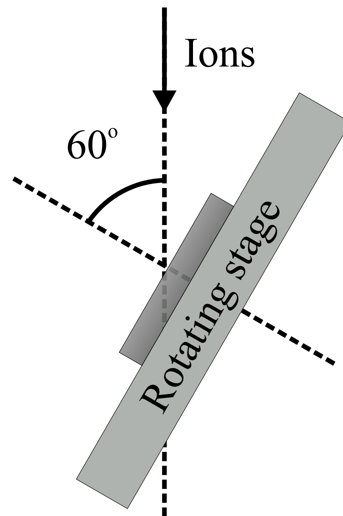


**FIGURE 3.1** *Rotating sample holder of the ion gun.*

**TABLE 3.1** *Sputtering rates of various materials [nm/min] by 1 keV $Ar^+$ ions at the current density of 0.014 mA/cm$^2$.*

| Aluminium | $SiO_x/Si$ | Sapphire |
|---|---|---|
| 1.1 | 3.9 | 0.75 |

The stopping range of 1 keV argon ions used in our study in aluminium has been calculated with the SRIM program and the result was that the longitudinal straggling was 15 Å and the lateral 11 Å. So only the surface of the sample is altered during the sputtering.

Taking into account the high rate of the surface sputtering due to high density of the ion current and the glancing incidence, the ion beam etching can be considered as "a gentle cut" of the up-most surface atoms without appreciable influence on the underlying layers. The sputtering conditions were assured by AFM and profilometer to result in polishing of the surface and cause no destruction to nanostructures. In addition, argon is a nobel gas and does not form compounds with the surface material.

## 3.3 Benefits of the method

The conventional nanofabrication techniques have their limitations, as described in section 3.1. An important benefit of the ion beam sputtering method is that it can be applied to overcome the existing limitations. For instance it is difficult to obtain line widths smaller than 50 nm by using the conventional EBL technique. However, we

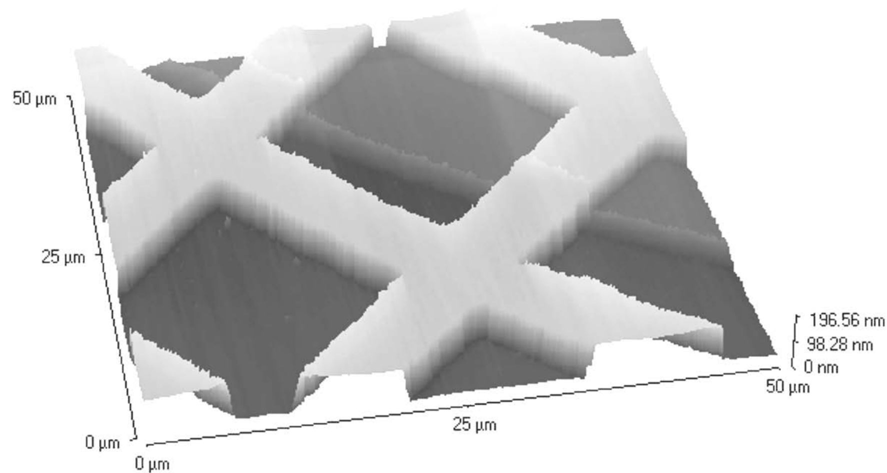


**FIGURE 3.2** *An atomic force microscope image of a step on silicon obtained by covering part of the chip with protective glue for sputtering. The light mesh is an aluminium pad used to make electrical contacts by bonding.*

have been able to reduce the line widths of our aluminium samples from about 70 nm to 30 nm.

The range of applicability of the method is wide. Also tunnel junctions, which are the basic components of many nanoelectronics circuits survive and are size-reduced after sputtering session. Part of the chip can be covered with protective glue that can be completely removed afterwards with acetone and isopropanol. This can be used to protect some of the components on chip from etching and the step formed during a sputtering session can be used in determining how much material was removed. Fig. 3.2 shows an example of a step formed this way. The difference of etching rates between aluminium and silicon is clearly visible as the step on aluminium is barely noticeable compared to the huge step of silicon. Measured sputtering rates for various materials are listed in Table 3.1.

Generally speaking, it is common to study some properties of the system of interest as a function of some characteristic dimension. Traditionally many samples of different sizes are fabricated for this purpose. With the ion beam sputtering method, the measurements can be performed by using the same sample, whose dimensions are progressively decreased between the measurements. This way the inner structure of the system stays the same and thus there are less possibilities of having statistical errors due to circumstantial factors in fabrication.

As an example, in tunnel junction the tunnelling current depends exponentially on the thickness of the oxide layer (typically around 10 Å). Let us assume a

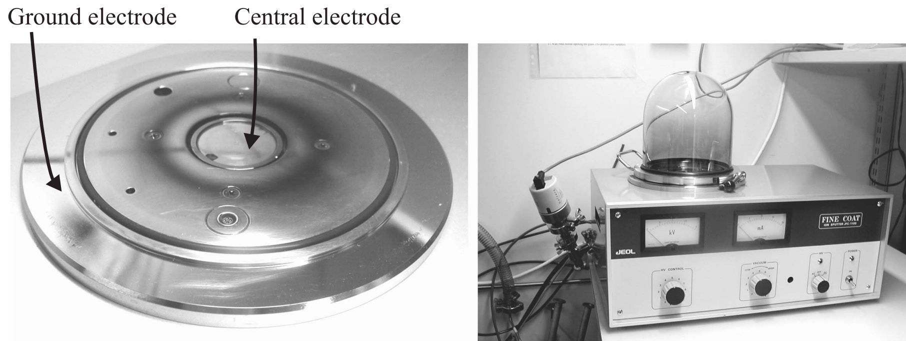


**FIGURE 3.3** *Electrodes of the JEOL JFC-1100 Plasma Ion Sputter (left). The sample is inserted to the central electrode and the outer electrode is grounded. Right image shows the whole system with glass chamber on.*

situation, where a researcher would like to measure some quantity of the junction as function of the surface area of the junction. Traditionally this would be done by fabricating several SETs of different sizes. It is very important that the only thing different in these samples is the area of tunnel junction. The thickness of the tunnel barrier, defects and impurity concentration should be the same. If the samples are on the same chip and thus evaporated in the same chamber with same conditions, one might expect that they are equal. However, there are still chances for statistical differences. When using the sputtering method, only the surface layers are altered and the inner structure stays the same. One can be sure, that the only changed parameter is the area of the junction. If the sample had defects of any kind after fabrication, exactly the same defects are still there when measuring junction having a smaller area.

## 3.4 About the development work of the sputtering method

### 3.4.1 Etching by using argon plasma sputterer JEOL JFC-1100

The development of the method started with JEOL JFC-1100 Plasma Ion Sputter (Fig. 3.3). After some time we decided to use the ion gun instead, but the tests with plasma sputterer gave us important knowledge about the sputtering of nanostructures. The sample is put on the central electrode, where the electric field accelerates the argon ions of the surrounded plasma. Argon gas of purity 99,998 % is flowing into the chamber. The plasma is formed by applying AC or DC voltage between the electrodes. We used ∼500 V voltage in our experiments. First we tried the sput-

tering with aluminium nanowires that were not grounded. We saw some signs of the reduction of dimensions, but there were also broken samples and changing parameters. We concluded that perhaps the argon ions bring too much charge to the metallic wires on the substrate, causing damaging discharge (we tested both Si and SiO substrates). The next step tried was to ground the samples. However, this did not bring solution to the problem. Then we decided to neutralize the incoming argon ions by applying a platinum grid $\sim$2 mm above the chip. Having a low work-out energy, platinum grid is surrounded by a 'cloud' of negatively charged electrons, which neutralize the positive charge of argon ions passing by. This should not affect significantly the kinetic energy of the argon atoms that finally hit the surface of the sample. In addition we improved the vacuum and purity of the chamber in many ways, for example by renewing the argon line and valves and by inserting a liquid nitrogen trap to the pumping line. After this less breakage occurred. However, etching was considerably slower and the sputtering conditions were still difficult to keep under control. At this stage we had started tests with the ion gun and concluded that it is more efficient and reliable than the plasma etching system for our purposes. Despite of this, it is possible that the plasma etching would have worked after some additional work. This would mean that the method does not necessarily need big and expensive equipment. The principal comparison in section 3.4.3 between plasma etching and ion gun etching speaks for the ion gun.

### 3.4.2 Sputtering using ion gun

The sputtering of nanostructures with ion gun showed promising results from the very beginning. The first promising result naturally was that the samples survived the ion bombardment without any noticeable macroscopic degradation. The next step was to find out the sputtering rates for the materials used in our samples: aluminium, aluminium oxide (sapphire) and silicon. For this purpose we used aluminium film evaporated on silicon substrate, bulk sapphire and silicon chip, respectively. A step was formed on these films by covering part of the chip with protective glue that was removed after ion beam etching. The height of this step was measured with profilometer and the etching rate was then calculated. Fig. 3.5 shows a step on sputtered aluminium film measured with profilometer. The sample was fabricated by evaporating 45 nm of aluminium on silicon substrate followed by evaporation of 11 nm of gold as a protective layer against oxidation. The gold is etched away very fast compared to aluminium and should not affect the calculation of the rate too much. As it can be seen from Fig. 3.5, the step is 50 nm high. The sputtering time was 10 minutes so approximately 5 nm of aluminium was removed in one minute.

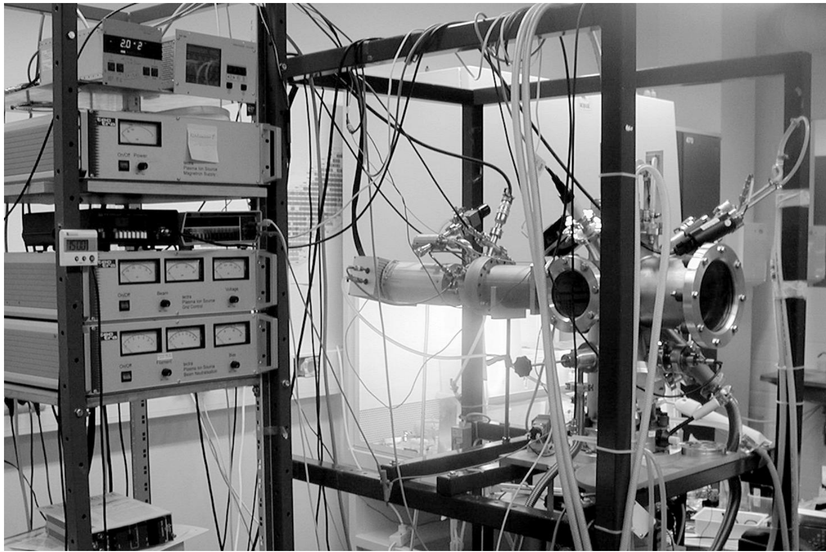

**FIGURE 3.4** *Ion gun used in sputtering nanostructures*

In the actual sputtering sessions of nanostructures the etching rates were used to estimate the time needed to remove certain amount of aluminium. Part of the contact pad was covered with the protective glue to check the rate after sputtering session.

One problem in the whole process including the sputtering and measurements was the making of electrical contacts. At first, there were separate sample holders to be used in measurements and sputtering sessions. The electrical contacts made by bonding aluminium wires to the pads had to be removed from the sample before the sputtering sessions and had to be redone after. This caused additional risk to the samples and many were damaged during bondings. The solution was a common sample holder for etching and measurements. This way the same electrical contacts could be used during the whole process depicted in Fig. 4.1.

### 3.4.3 Qualitative comparison of the used systems

There are principal differences in using AC/DC-plasma etching (section 3.4.1) and the ion gun etching that are affecting the result. First of all, in plasma system the sample is placed on the central electrode that is used to form the plasma and also to accelerate the ions of the plasma. This means that the sample itself is actually a part of the electrode and the sample structure defines the electric field just over the surface to be etched and hence, may deflect the ions. The local electric field strongly depends on the sample shape. This makes the etching inhomogeneous. Ion gun does not have this problem as the ions are accelerated relatively far from the

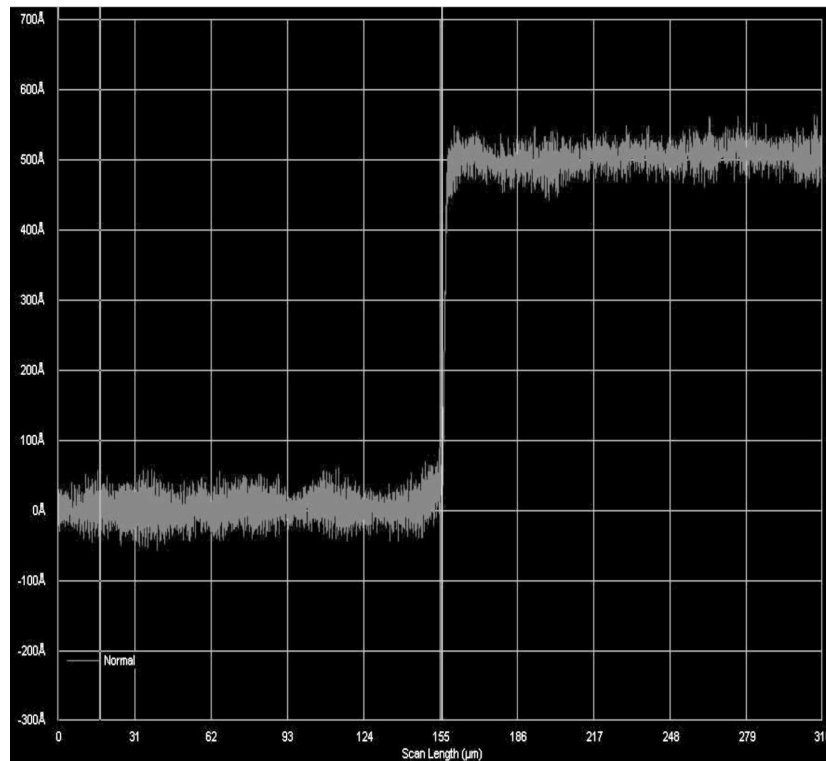


**FIGURE 3.5** *Step on evaporated aluminium film after sputtering 10 minutes by 1 keV $Ar^+$ ions (0.042 mA/cm$^2$). The aluminium film was covered with 11 nm of gold to protect the surface from oxidizing.*

sample holder and the sample holder is not an electrode for the acceleration voltage. So the sample geometry does not affect the etching rate.

## 3.5 Visualization of samples

The sample visualization was done with optical microscope (maximum magnification x1000), SEM and AFM. Quite good resolution images were taken, but the analysis was nontrivial though. In case of AFM, the main problem was to distinguish between silicon and metal. Silicon is etched faster, so eventually aluminium wires are on top of 'pillars' of silicon. Figure 3.6 shows a typical AFM-image after etching of aluminium nanowire. Another difficulty in analysis is the apparent height difference along the wire, possibly due to resist leftovers in the vicinity of the wire. The cutaway profile plotted directly from the AFM data (Fig. 3.7) is quite smooth and it is difficult to say much about the width of the wire or which part is metallic. The SEM is able to distinguish between aluminium and silicon, but the problem is the contrast. The sample is thinner after ion etching so more contrast and brightness

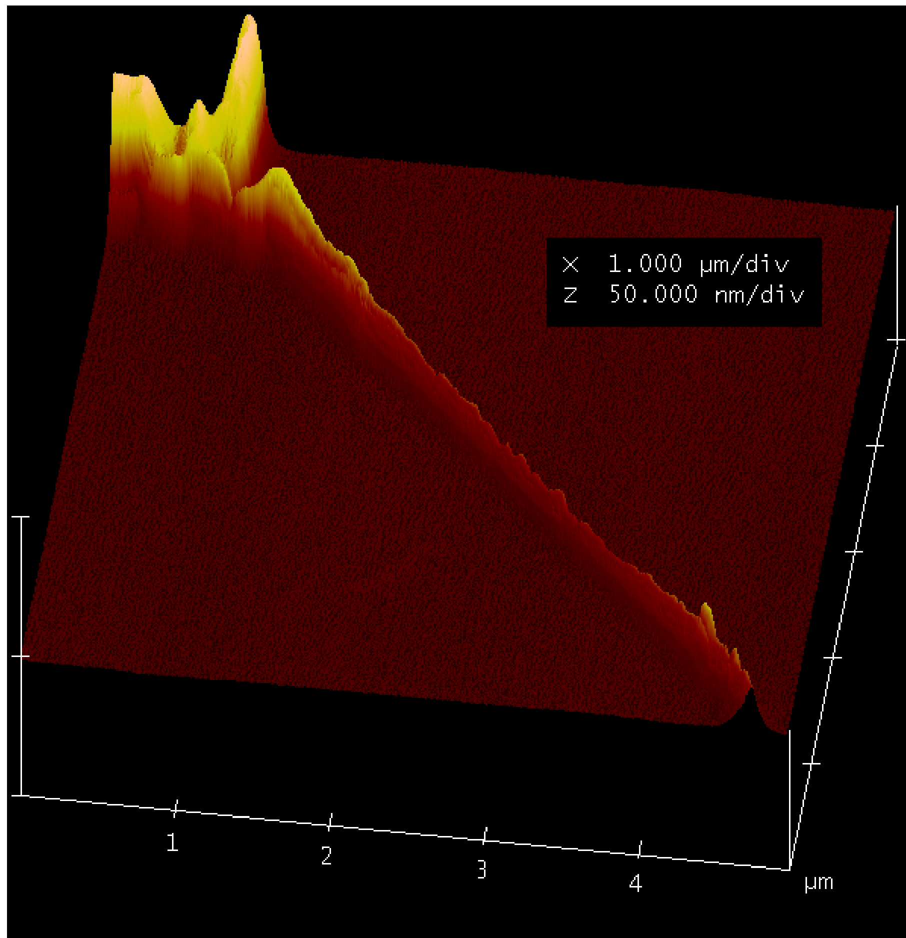


**FIGURE 3.6** *AFM-image of etched aluminium nanowire. Silicon is etched faster than aluminium and eventually nanowire is on top of a silicon 'pilar'.*

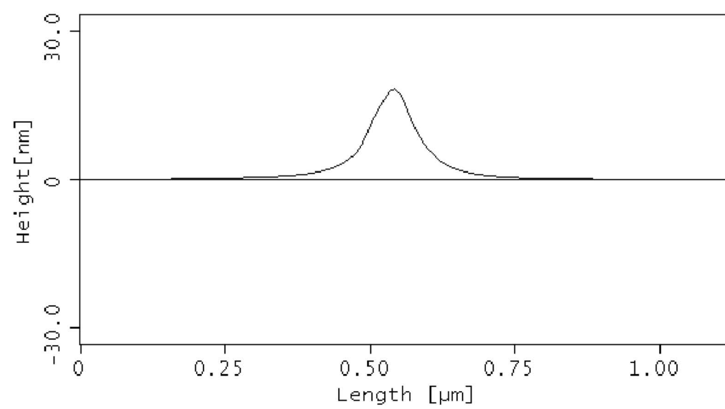


**FIGURE 3.7** *Cross-sectional AFM image of etched aluminium nanowire.*

should be used in SEM than before etching to be able to get a good image. The problem arise because the measured line widths are affected too much by the contrast and brightness, and the operation of SEM changes in between the image taking sessions. Finally, the conclusion about the actual dimensions (mainly cross-section) of the nanostructures was made taking into consideration both SEM and AFM analysis and electric measurements of the resistance (for nanowires).

Despite of these problems in determining the accurate line widths of wires (and also areas of tunnel junctions), the visualisation has a great importance in the study. It can be seen from the images, that the surfaces stay smooth. It is very important to check that the samples do not have constrictions after the fabrication or sputtering sessions. By doing this we conclude, that the etching of nanostructures with ion gun is very gentle to the structures. In the same way we have been able to detect the problems when using the plasma ion sputterer (see section 3.4.1). Figure 3.8 shows some examples of those. Note, that more damage occurred when the sample was grounded than without grounding (image a). However, the sample without grounding had also breakages (image b).

Comparing AFM images of the same sample before and after fabrication, one can come to a conclusion that the ion bombardment removes the inevitable inhomogeneties left from the lift-off process. The ion beam sputtering makes the surface of nanowires smoother.

## 3.6 Conclusions

The ion been sputtering method has been developed and proved to be very 'gentle' in a sense that it allows to decrease the dimensions of delicate nanostructures by gradually removing the surface layers without introducing changes into the interior. Reproducibility and controllability provided by the method imply that ion sputtering is in general applicable to nanoelectronic components and circuits containing nanosized wires and tunnel junctions (see details of the conducted measurements in Chapters 4 and 5). It is believed, that bombardment with low energy inert argon gas ions causes no chemical reactions. Based on measurements and sample imaging the method is envisaged to be applicable to circuits based on any kind of metals, semiconductors, insulators and their combinations, regardless of the chemical composition and morphology. Since the method can be applied repeatedly to the same sample, gradual reduction of dimensions is achievable in those applications where the size effect is studied or employed. Instead of fabricating a number of samples of different sizes and comparing their properties and performance, the sputtering method allows working only with a single sample, thereby, avoiding uncertainties

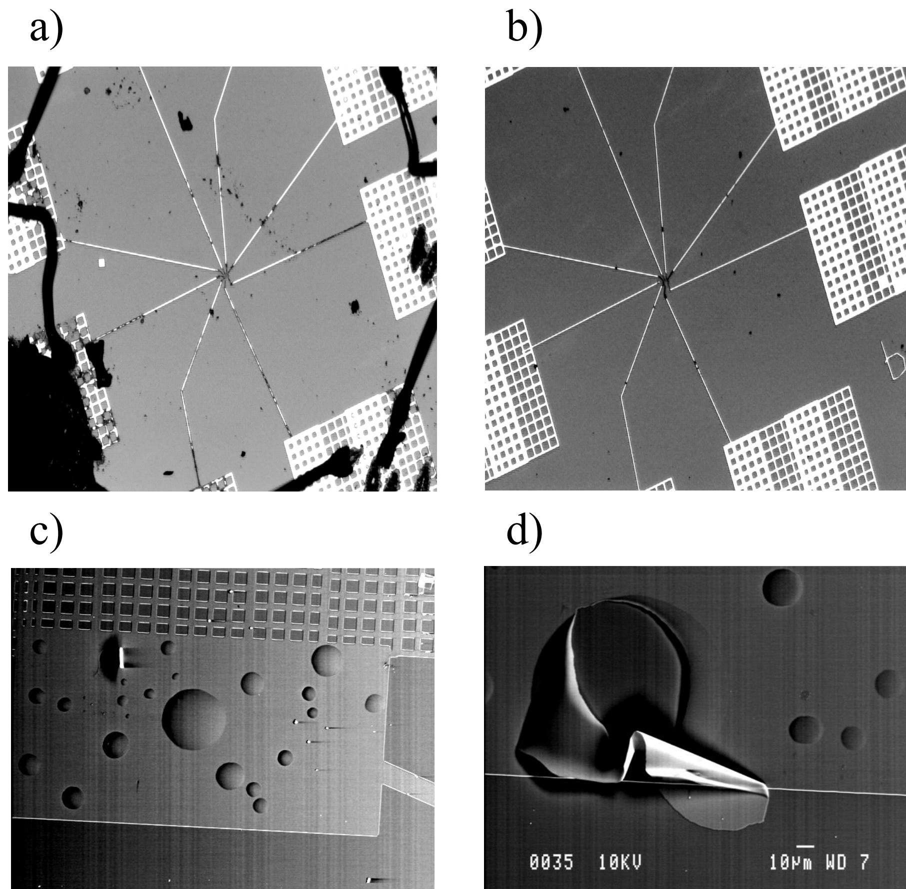


**FIGURE 3.8** *a-b) Optical microscope images of samples etched with JEOL plasma ion sputterer. The sample of left picture was grounded and the pads were also shorted with aluminium bonding wires. The sample of the right image was etched at the same time as the left one, the only difference being that it was not grounded or shorted. The scale of the images a-b) is approximately 2 mm. c-d) Topographic SEM images of 'blisters' formed on the contact pads after etching.*

due to the circumstantial factors in fabrication.

# Chapter 4

# Measurements of the sputtered nanowires

## 4.1 Introduction

This chapter describes the electrical measurements of aluminium nanowires conducted in order to test the applicability of the ion beam sputtering method to decrease cross-section areas of nanowires. The corresponding measurements with single electron transistors are presented in the next chapter. The promising results of detecting quantum phase slip phenomenon are also presented in this chapter.

As it is sometimes difficult to compare SEM or AFM images taken before and after ion etching, it is good to have some independent way of detecting the decrease of dimensions. There were two independent methods to confirm the effects of ion beam etching: sample imaging by using SEM, AFM and profilometer, and electrical measurements. These both were used in testing the applicability of the sputtering method to reduce dimensions of nanostructures. The typical order of sample manipulation in this study is presented in Fig. 4.1, starting from the fabrication of the sample. After fabrication the samples were imaged and then measured. The measured parameter was the resistance vs. temperature in case of wires and charging energy in case of SETs. After measurements the samples were etched by using the ion gun and after that the effect of ion etching was checked by another set of imaging and electrical measurements. The procedure was repeated as many times as possible.

## 4.2 Aluminium nanowires

All samples were fabricated on oxidized silicon substrates. Conventional EBL technique was used in patterning followed by metallization in an UHV (Ultra High Vac-

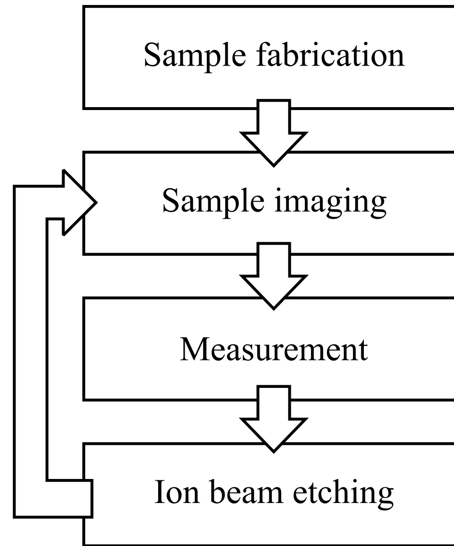


**FIGURE 4.1** *Research flow chart of different steps in testing the etching method.*

uum) chamber. Double layer PMMA/MAA resist was used to form an appropriate undercut structure for the angle evaporation. Nanowires were formed by evaporating 45 nm of aluminium on top of the substrate through the PMMA mask. Before the actual evaporation of the wire, a special technique was applied to narrow the mask further. This technique is schematically presented in Fig. 4.2. Aluminium was evaporated in high angles, $\pm 70°$, to add extra material to the hole in the mask without evaporating in silicon. The widths of the fabricated nanowires were approximately 50-80 nm. Figure 4.3 shows an AFM image of a typical sample.

## 4.3 Current-Voltage characteristics of one-dimensional nanowires

The predicted features of the I-V characteristics were presented in Fig. 2.2 and in this section the corresponding measurements are presented. Fig. 4.4 shows I-V curves measured at various temperatures, i.e. measurements corresponding to Fig 2.2b). The dashed line shows a criterion chosen for the voltage corresponding to the critical current. The corresponding temperatures and critical currents are presented in table 4.1.

As depicted in Fig. 2.2c), in case of one-dimensional wire the critical current has a linear dependence as function of $(T_\mathrm{C} - T)^{3/2}$. The corresponding measurements are presented in Fig. 4.5 and indeed the dependency is linear. Thus we have

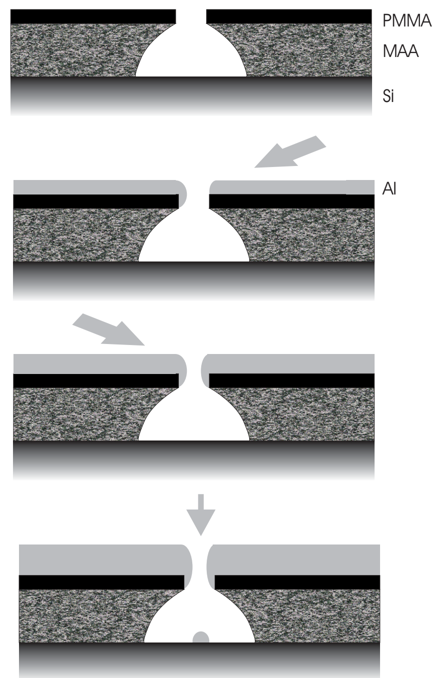


**FIGURE 4.2** *A schematic image of the technique applied to narrow the mask before the actual evaporation of a nanowire. Metal is evaporated in a high angle to make the holes in the mask smaller. The procedure is applied from both directions to maximize the effect.*

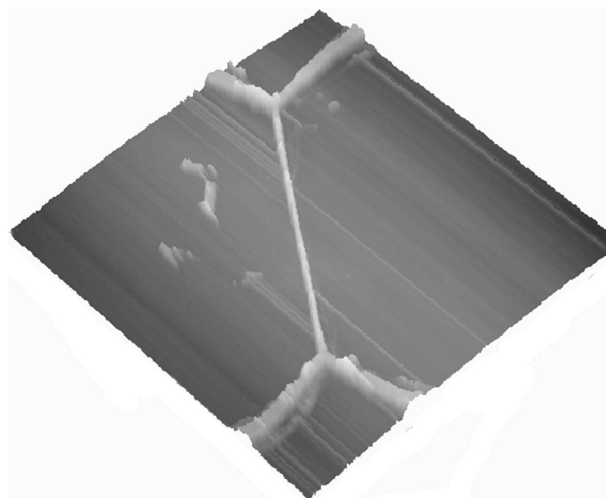

**FIGURE 4.3** *An overview AFM-image of approximately 60 nm wide and 10 $\mu$m long aluminium nanowire.*

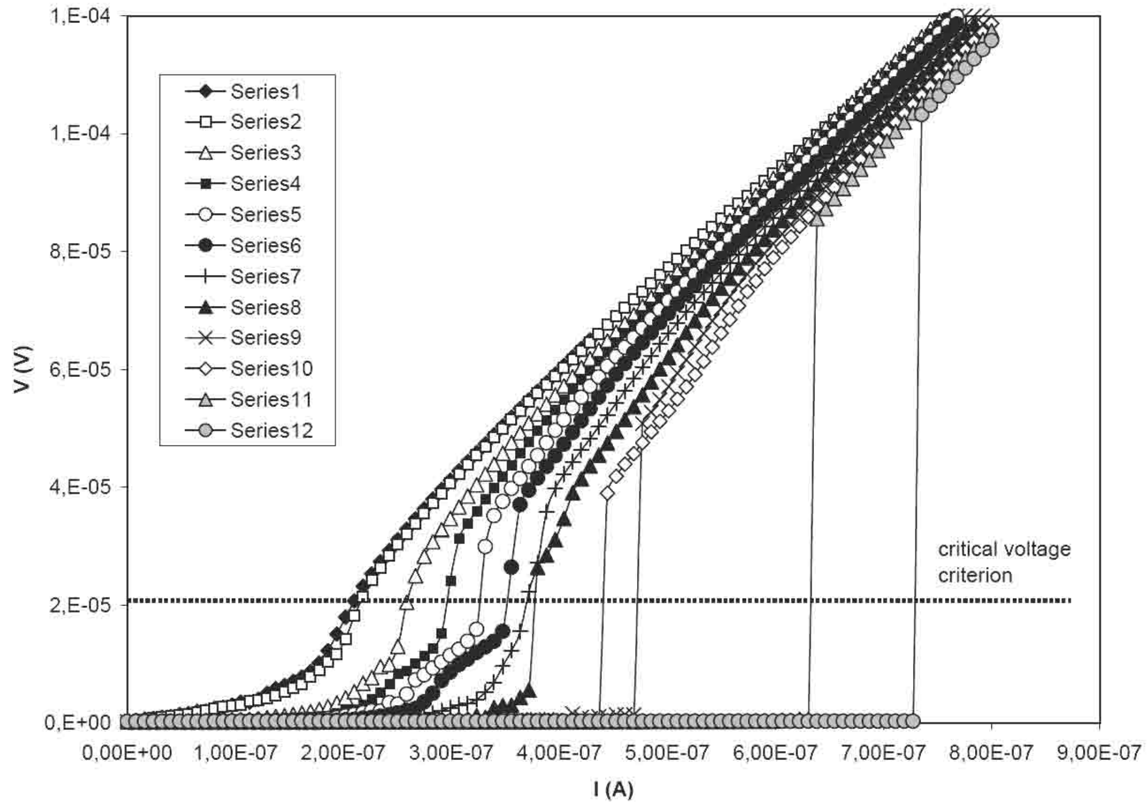


**FIGURE 4.4** *I-V characteristics obtained at temperatures listed in table 4.1. The dashed line shows a criterion chosen for the voltage corresponding to the critical current.*

a confirmation that the measured wires are one-dimensional.

In 1D wires ($d < \xi$, $L >> \xi$) at temperatures slightly below the $T_{\mathrm{C}}$ phase slip can be induced by a strong current [61]. Note, that at temperature significantly below $T_{\mathrm{C}}$, destruction of superconductivity by a current is of an avalanche nature: the superconductivity is destroyed in the weakest link and the 'hot spot' expands to the whole wire. However, at $T \lesssim T_{\mathrm{C}}$ the V(I) dependencies can have a few steps: each step corresponds to activation of a new phase slip center, and hence to a voltage step [61]. As it is shown in Fig. 4.4, there is only one step at V(I) characteristic. The 'long wire' limit requires satisfaction of a rather tough condition: $L \gg \lambda_{\mathrm{Q}}$, where $\lambda_{\mathrm{Q}}$ is the quasiparticle relaxation length (the characteristic length on which nonequilibrium quasiparticles, created while each phase slip, relax). It is not clear, what this value exactly is for aluminium [31], but from literature it is known that for this material it can exceed 10 $\mu$m scale [31, 18].

The short wire limit is represented by eq. 2.16 within the GZ-model. Not all parameters of eq. 2.16 can be easily measured experimentally. However, Fig. 4.4 clearly indicates that our wires represent the so-called 'one phase slip limit'. Hence, the simplified GZ-model (eq. 2.13-2.15) can be applied.

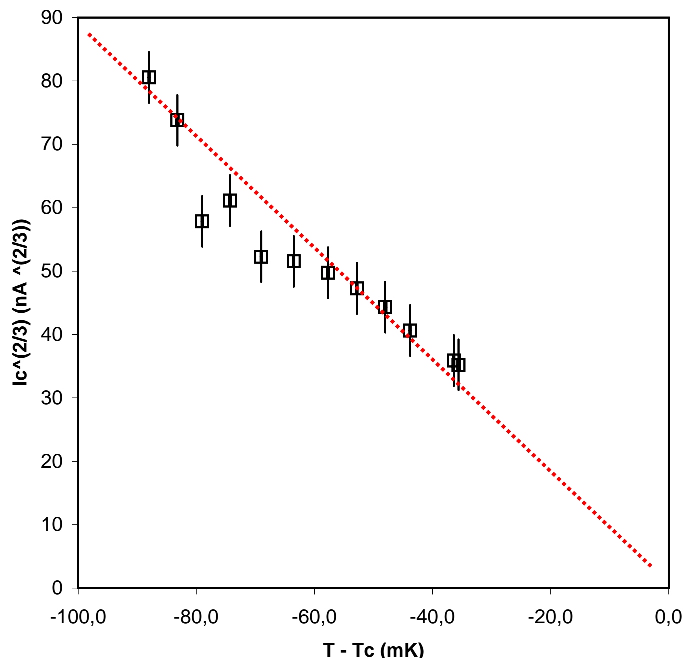


**FIGURE 4.5** *A measured linear dependency of critical current vs. scaled temperature* $(T - T_C)$.

## 4.4 Shape of superconducting transition R(T) of 1D-wires

We have measured the superconducting transition of the wires before and after application of the sputtering method. As described in more details in section 2.2.1, within the LAMH-model the shape of the superconducting transition of one-dimensional wire depends on several parameters, one being the effective diameter $\sqrt{\sigma}$, where $\sigma$ is the cross-section area.

Fig. 4.6 shows a typical effect of sputtering on the shape of superconducting transition of a wire. It is clearly seen, that the transition becomes wider and the critical temperature $T_C$ and the normal state resistance $R_N$ increase. All these observations indicate that the wire cross-section has decreased.

By comparing the predicted transition with the experimentally measured dependencies one can draw conclusions of the change in effective diameter. This is because the slope of the transition is dependent on the cross-section area of the wire. Some care should be taken though as the cross-section area is not the only parameter affecting the slope, but it is also a function of the critical magnetic field $B_C$ and mean free path $l$. Naturally, with decreasing the wire cross-section the mean free path $l$ also decreases. As it is usual in superconducting films (and wires) the critical magnetic field increases with decreasing the relevant dimension: wire cross-section

**TABLE 4.1** *Temperatures of the data of Fig. 4.4 and corresponding critical currents.*

| Series | Temperature [K] | Critical current [nA] |
|---|---|---|
| 1 | 1.3424 | 209 |
| 2 | 1.3416 | 215 |
| 3 | 1.3342 | 259 |
| 4 | 1.33 | 295 |
| 5 | 1.3252 | 325 |
| 6 | 1.3203 | 351 |
| 7 | 1.3145 | 370 |
| 8 | 1.309 | 478 |
| 9 | 1.3037 | 478 |
| 10 | 1.299 | 440 |
| 11 | 1.2948 | 634 |
| 12 | 1.29 | 723 |

**TABLE 4.2** *The fitting parameters for the LAMH-model [33, 41] for the data from Fig. 4.7.*

| | Original | After 1st sputtering | After 2nd sputtering |
|---|---|---|---|
| $T_\mathrm{C}$ [K] | 1.285 | 1.316 | 1.371 |
| $R_\mathrm{N}$ [$\Omega$] | 82 | 142 | 380 |
| $B_\mathrm{C}(0)$ [mT] | 7.0 | 7.5 | 8.0 |
| $l$ [nm] | 15.8 | 12.8 | 9.5 |
| $\sqrt{\sigma}$ [nm] | 85 | 55 | 34 |

in our case.

The cross-sections $\sigma$ obtained from the measurements of the normal state resistance correlate well with the ones used in the fitting procedure (Table 4.2). The common parameters used for the fits are the sample length $L = 10\ \mu$m, $\xi_\mathrm{BCS}(0) = 1.6\ \mu$m, $K = 0.7$, and the product of resistivity and mean free path $\rho l = 4.3 \cdot 10^{-16}\ \Omega\mathrm{m}^2$. The critical temperatures $T_\mathrm{C}$ used in fitting procedure (Table 4.2) correspond well to the experimentally observed onsets of superconductivity (Fig. 4.7). The increase of the critical temperature with the reduction of the aluminium wire cross-section (and, in general, the thickness of a film) is a well-known effect. Commonly accepted explanation for this phenomenon is not yet settled, while various models are currently discussed [50, 59].

The fitting of the experimental data with model calculations [33, 41] clearly indicates the reduction of the wire cross-section (Table 4.2) while subsequent sputtering sessions. The absence of artefacts on the experimental $R(T)$ dependencies (Fig. 4.7) suggests that the dry ion etching does not cause 'serious' damage to the sample (voids or constrictions), but removes the material from the surface gently and in a controllable way. Qualitatively similar results were obtained on many samples.

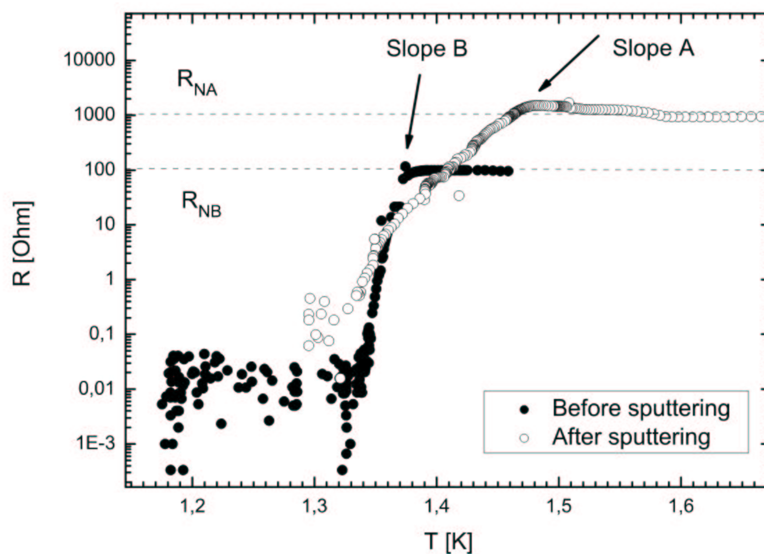


**FIGURE 4.6** *Typical measured $R(T)$-dependency of an aluminium nanowire before and after sputtering.*

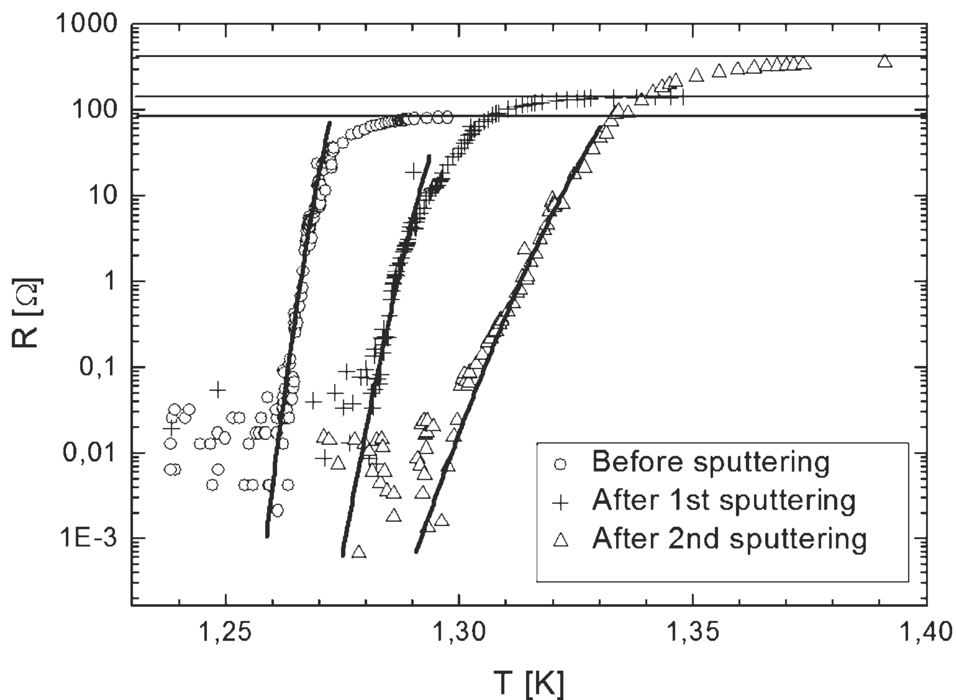


**FIGURE 4.7** *$R(T)$-dependency of an aluminium nanowire before and after sputtering. Solid lines are the theoretical fits according to LAMH-model [33, 41]. Fitting parameters are listed in table 4.2.*

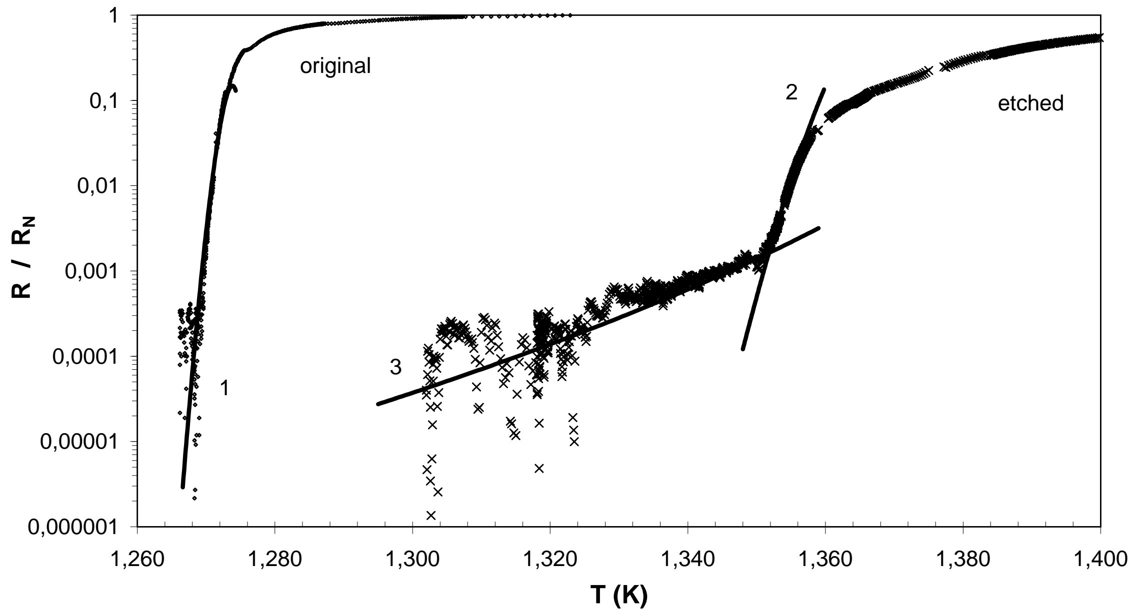


**FIGURE 4.8** *The resistive transition of aluminium nanowire after fabrication and observed qualitative change of resistive transition after sputtering session. Solid curves (1) and (2) correspond to fitting using LAMH-model (Table 4.3), curve (3) is fitted using GZ-model for QPS.*

## 4.5 Observation of the quantum phase slip phenomenon

As discussed in section 2.2.2, one might expect to see the resistivity due to quantum phase slips (QPS), when the diameter of nanowire becomes small enough ($\sim$10 nm). The extra resistance should emerge to the bottom part of the resistive transition.

We have used our ion beam sputtering method to reduce the cross-section areas of evaporated aluminium nanowires as described earlier. In some of the measured samples the expected qualitative change of the bottom part of resistive transition was indeed observed. Remarkable thing is that the extra feature emerged after ion etching; the original sample did not have it. Figure 4.8 shows the resistive transition of one of the measured samples after fabrication and after sputtering session. First of all the normal state resistance increased from 37.1 $\Omega$ to 76.5 $\Omega$, indicating the reduction of the cross-sectional area. This was also verified by fitting the LAMH-model prediction to the original transition (1) and to the top part of the transition (2) after sputtering session. The fit was successful by using wire widths 80 nm before and 35 nm after the sputtering session (table 4.3). It is clearly seen, that the emerging extra resistance has a different slope than the top part of the transition. We have checked, if the LAMH-theory alone could give a reasonable fit to the bottom part.

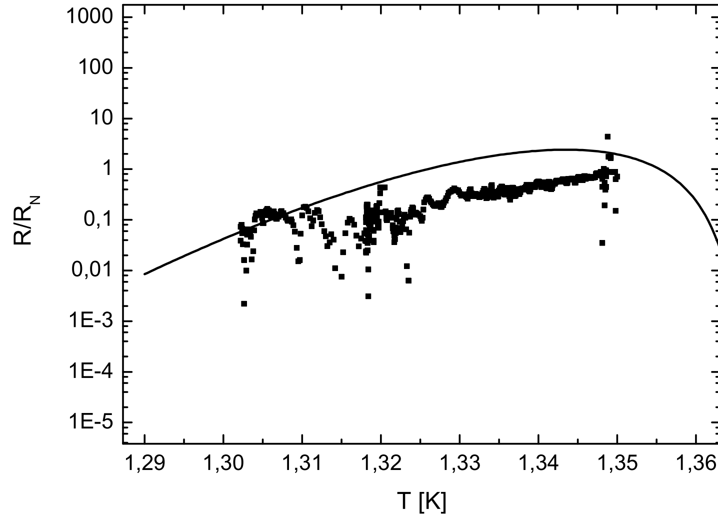


**FIGURE 4.9** *A trial LAMH-theory fit to the 'foot' feature of the resistive transition from Fig. 4.8 after sputtering, resulting in unphysical fitting parameters.*

**TABLE 4.3** *The parameters used in LAMH-model fits of Fig. 4.8. Common parameters were* $\rho l = 4.5 \cdot 10^{-16}\ \Omega m^2$ *and* $v_{\mathrm{F}} = 1.3 \cdot 10^{+6}\ m/s$.

| | Original (1) | After sputtering(2) |
|---|---|---|
| $T_{\mathrm{C}}$ [K] | 1.276 | 1.3745 |
| $R_{\mathrm{N}}$ [$\Omega$] | 37.1 | 75.6 |
| $B_{\mathrm{C}}(0)$ [mT] | 8.0 | 12.0 |
| $l$ [nm] | 25 | 8 |
| $\sqrt{\sigma}$ [nm] | 80 | 35 |

Fig. 4.9 shows this fit with approximately right slope. However, the normal state resistance $R_{\mathrm{N}}$ of the wire should be put to around 500 $\Omega$ to make the fit quantitatively correct. However, the normal state resistance was measured to be less than 100 $\Omega$. However, in this case to go on with LAMH-fitting, the mean free path should be set to millimeters. This suggests that the resistance below 1.35 mK can not be explained with LAMH-theory and is possibly generated by quantum phase slip phenomenon.

The fitting of the simplified quantum phase slip model reviewed in section 2.2.2 to the emerged bottom part feature (3) was successful when using value 0.011 for $A$ (eq. 2.14).

## 4.6 Conclusions

The developed method of progressive reduction of the wire dimensions allowed to trace the evolution of the superconducting transition $R(T)$ on same Al nanowires as

function of their cross-section.

For aluminium wires in the range from $\sqrt{\sigma}$ ∼40 nm to ∼100 nm experiments show up nice correspondence with the LAMH-model [33, 41] of the thermally activated phase slips. In the thinnest wires ($\sqrt{\sigma}$ <35 nm) a 'foot' structure develops at the very bottom part of the $R(T)$ transition. No realistic set of fitting parameters within the LAMH-model can explain the mentioned feature. It is reasonable to associate this 'foot' with quantum phase slip phenomena.

# Chapter 5

# Sputtering experiments on single electron transistors

## 5.1 Introduction

In this chapter the test of applicability of the sputtering method to decrease sizes of tunnel junctions is presented. The experimental steps are the same as in case of wires (see Fig 4.1).

By measuring the charging energy of the SET at liquid helium temperature 4.2 K before and after ion beam etching, one can determine how the areas of junctions have changed during ion etching. Here a natural assumption has been made that the thickness of the insulating layer and its dielectric constant $\varepsilon$ are not altered while etching.

SETs were fabricated with a standard shadow evaporation technique. First 45 nm thick layer of aluminium was evaporated. Aluminium oxide barrier was grown *in situ* by natural oxidation in pure oxygen atmosphere ($\sim$20 mbar) in the loading chamber of the UHV system. After oxidation another 45 nm layer of aluminium was deposited from another angle on top of the previously grown oxide layer to form tunnel junctions. Fig. 5.1 b) shows an AFM image of a typical SET with two Al-$AlO_x$-Al junctions.

## 5.2 Results

Figure 5.2 shows the charging energy of different SET samples measured after fabrication and each sputtering session. It is clearly seen that the sputtering increases the charging energy gradually, indicating that the etching has reduced the areas of the tunnel junctions. As it follows from equation (2.27), the relative height of the con-

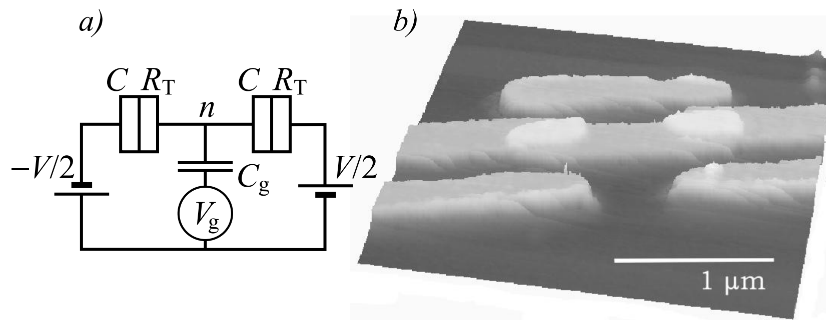


**FIGURE 5.1** *a) Schematics of a single electron transistor biased to voltage $V$, $V_g$ is gate voltage. b) AFM image of the SET after ion beam etching. This image does not show the gate electrode. The top most and the bottom most lines are parasitic structures due to two-angle evaporation method.*

ductance dip is inversely proportional to the junction area. Therefore, we conclude from the Figure 5.2, that the junction areas of the sample "SET5" have reduced by ∼40 % with respect to the original after three sputtering sessions. The tunnel junction resistances also increased while etching, additionally indicating the reduction of the tunnel junction areas. For instance, in sample "SET5" the original resistance was 37 kΩ, and it became 84 kΩ after third sputtering. Multisession sputtering was performed on many of the samples without damaging them. Actually the sputtering was not always the cause of the broken SETs; many of those were destroyed while making the electric contacts.

Since the tunnel junctions are formed by thin oxide layers in between aluminium electrodes, there exists a possibility of natural 'aging' of the samples at normal atmospheric conditions leading to changes of characteristics. Reference measurements were performed to rule out the possibility that charging energy changes 'by itself' by this natural aging. The charging energy of these samples was measured repeatedly during the time period of several days. No increases in charging energy were observed. So it is clear that the aging effect is negligible, at least at time scales used in the procedure described in Fig. 4.1.

In the first sputtering session a surface layer of approximately 25 nm was removed from the electrodes and the island forming the SET[1]. In the following 5-7 nm per session was etched. The behavior of sample "SET 5" is a bit surprising: although the sputtering conditions and estimated thickness of the removed layers were the same in sessions 2 and 3, the increase of the charging energy is much larger after the third session. It implies that either the sputtering rate changes as the dimensions of the SET structure become smaller, or a certain critical state of the system has been reached.

[1]This was determined from the contact pads of the sample.

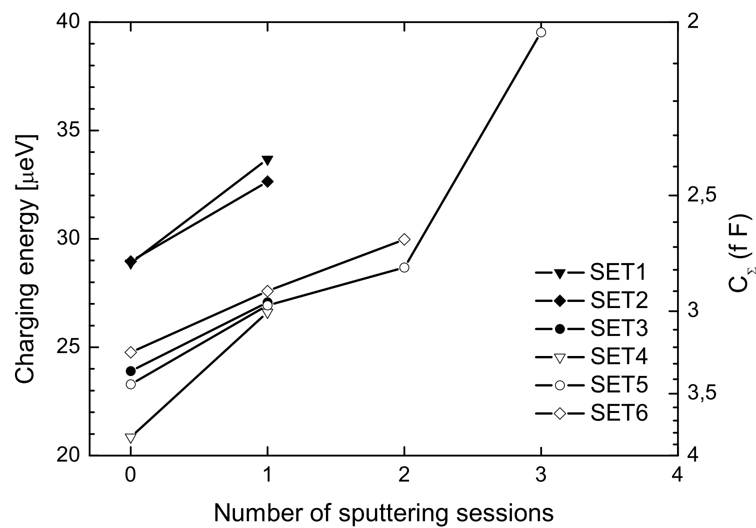


**FIGURE 5.2** *Charging energy of single electron transistors (left axis) and the total capacitance (right axis) as functions of the number of sputtering sessions.*

What could this critical state be? Fig. 5.3 a) shows a schematic drawing of the SET structure seen from the side just after fabrication. Due to the shadow evapo-

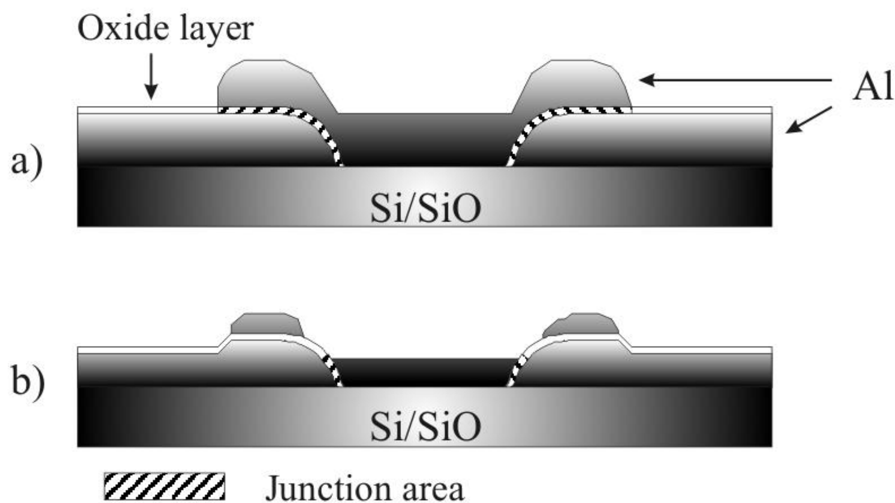


**FIGURE 5.3** *Schematic side view of a single electron transistor. Figure a) represents the SET just after fabrication and b) after sputtering.*

ration method the metal parts do overlap and the oxide layer gets its characteristic form having approximately vertical and horizontal parts. While sputtering, one finally reaches a state pictured in Fig. 5.3 b). The metallic contact between the metal of the island and the metal on top of the electrode is lost and 'suddenly' the effective junction area is much smaller. We assume, that the abrupt increase after third sputtering session for the structure "SET5" (Fig. 5.2) is at least partly due to this threshold

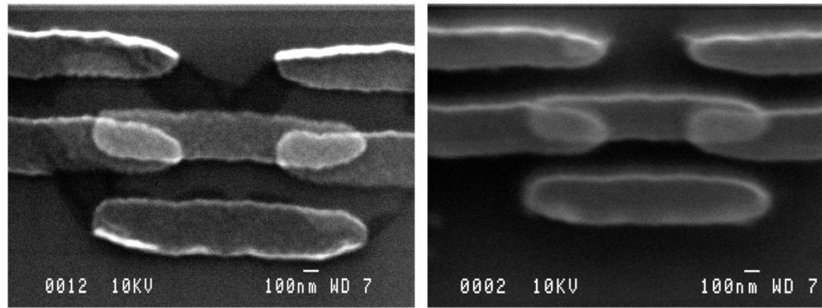


**FIGURE 5.4** *SEM images of SET. Left and right images represent the same sample before and after ion beam etching, respectively.*

effect.

The sputtering rate should not be necessarily the same for macroscopically large and nanosized objects. The calibration of sputtering rate in our experiments was done by measuring the height of the step developed between sputtered and non-sputtered regions on the large aluminium contact pads. Although the profilometer provides high vertical resolution (∼5-7Å), the lateral dimensions of the finest parts in the nanostructures studied were not resolvable. Therefore, if at some stage of sputtering the etching rate of the finest parts has dramatically increased, this would result in fast reduction of the areas of tunnel junctions and abrupt increase of the observed charging energy, e.g., after third sputtering session (Fig. 5.2). At present, knowledge about interaction of ions with low dimensional objects, like nanowires, ultra-small tunnel junctions and nano-islands, is rather scarce. Ion sputtering of nanosized objects has not been well explored yet, and various aspects of this method still have to be studied and developed in order to achieve a level suitable for various applications in nanofabrication.

SEM and AFM imaging of the sputtered samples revealed no strongly developed topography on the surface normally attributed to a high fluence ion irradiation. No trenches, craters or other extended defects on the surface were observed. On the contrary, the surface of the sputtered aluminium structures and their topography became smoother after sputtering when compared to as-fabricated state (Fig. 5.4). It should be noted that single electron transistors are usually considered as very fragile to stay 'alive' under experimental manipulations. Nevertheless, in our experiments both aluminium nanowires and SETs showed a very high degree of stability under high current ion irradiation. Even those SET samples which were 'destroyed' (the resistance became infinite), SEM and AFM observations revealed no breakages or discontinuity. This peculiarity of SETs is still unexplained; they may show infinite resistance and still look perfect. In our experiments any radiation damage fatal for the performance of the wires and SETs should be smaller than ∼5 nm in size,

otherwise they would be detected by our SEM and AFM.

## 5.3 Conclusions

The applicability of the ion beam sputtering method to decrease the areas of tunnel junctions has been verified with aluminium single electron transistors. The charging energy of SETs was found to increase indicating that the total area of the tunnel junctions decreased. Combining this result with the fact that also the cross-sectional areas of the aluminium nanowires decreased (chapter 4), it was shown that dimensions of the nanostructures can be reduced by ion sputtering in a controllable and reproducible way. The fact that the tunnel junctions 'stay alive' while sputtering makes the range of applicability of the method wider. For instance the operational temperatures of single electron devices can be extended by increasing the charging energy. However, the ultimate limit of the method is currently unknown. Furthermore, future experiments should include tests with initially smaller tunnel junctions to see how high operating temperatures could be achieved with the method.

# Chapter 6

# Single electron transistor as an electrometer

In this chapter the measurements of detecting the charge of the Cooper pair box (SCB) with a superconducting single electron transistor are presented. The samples used contained overlap structures to maximize the coupling between the box and the SET.

## 6.1 Operation principle of SET as an electrometer

The basic idea of using SET as an electrometer is that the current through SET is strongly dependent on the charge in its island. The charge on the other hand depends on gate voltage. The charge to be detected is arranged to change the gate voltage and thus current through SET. In our case the gate electrode was capacitively coupled to the island of the single Cooper pair box. When operating the box, i.e., changing the charge state one by one, the tunnelling of Cooper pairs to the box island changes rapidly the potential of the island. Since there is capacitive coupling of the islands, this potential is transferred to the gate of the SET, finally affecting the current through the SET.

## 6.2 Fabrication of an overlap gate structure to increase the gate capacitance

An overlap structure has been fabricated to increase the gate capacitance of the single electron transistor and the coupling between the measured system and the SET electrometer. The motivation for this is that the increase in gate capacitance im-

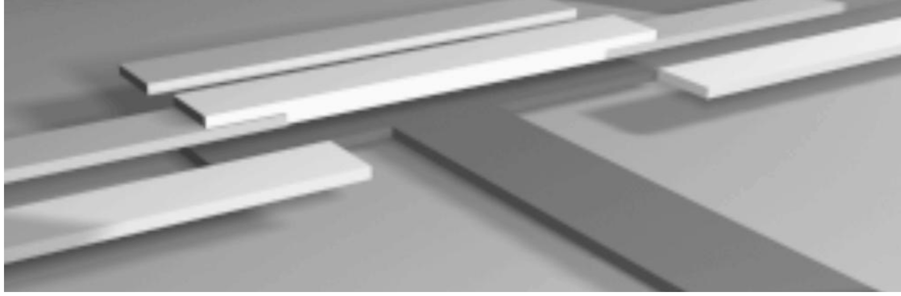

**FIGURE 6.1** *Schematic image of the multilayer structure used to increase the gate capacitance.*

proves the use of SET as an electrometer. It is seen from the plate capacitor equation $C = \varepsilon\varepsilon_0 A/d$ that the area of the capacitor plate should be maximized and the distance between the plates should be as small as possible. The distance should not be so small that the quantum mechanical tunnelling of charges becomes possible, because the gate should not be in electrical contact with the island. The typical limit of tunnelling is 5 nm.

Fig. 6.1 shows a schematic image of the fabricated overlap geometry. First the gate electrode was fabricated on silicon, and then new resist layer was spinned on the chip. The T-shaped head of the electrode was opened for evaporation by using precise alignment procedure in electron beam lithography and then 300 Å of silicon oxide (SiO) was evaporated on top of the electrode as an insulating layer. The resist layers were spinned on and alignment procedure was used again to fabricate the SET so that its island was precisely on top of the gate electrode. This resulted in ten times higher gate capacitance than with the conventional 'plane-design gate'. This is seen from the gate current modulation curves in Fig. 6.2, since the period of the modulation is $V_{\text{period}} = e/C_{\text{g}}$ in both.

## 6.3 Experiments

The bottom layer of a sample contained an evaporated gold line to make the capacitive coupling. The end of the line was covered with a thin (300 Å) insulating silicon monoxide layer, and the SET and the SCB were deposited on top of these layers, aligned with the gold line. Figure 6.3 shows a SEM image and a schematic picture of the system. The large metallic structures are ground electrodes and the vertical line is the gold line which terminates at the SCB (upper part) and the SET (lower part). The three angle evaporation procedure was needed in order to place short normal metal strips close to the junctions. These normal metal parts, made out of chromium, acted as quasiparticle filters, or traps, and are important in order to be able to ob-

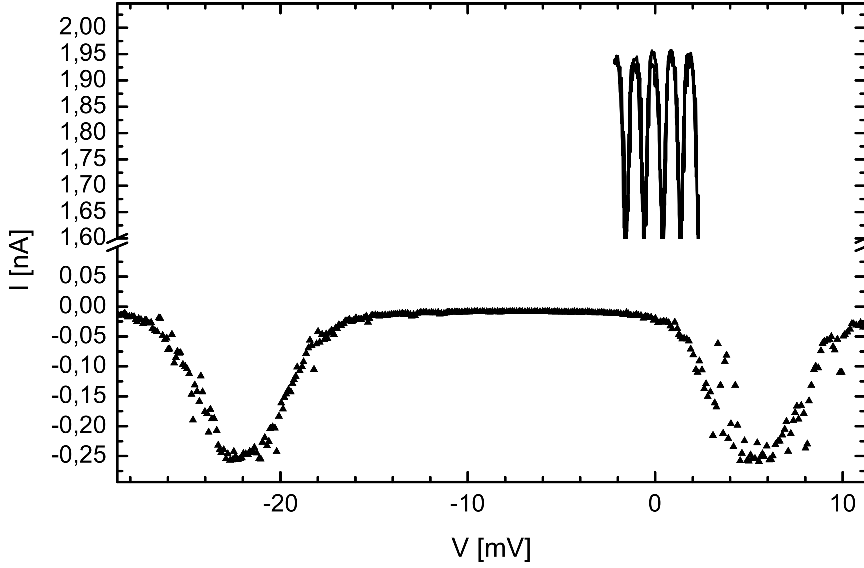


**FIGURE 6.2** *Gate current modulation curve for conventional gate (bottom) and overlap gate(top).*

serve a clear 2e-periodic gate current modulation of the SET in the superconducting case.

As can be seen from Fig. 6.3 the samples are fairly symmetric between the SCB and the SET, the only difference being the gold line, which is in metallic contact with the SET. This symmetry allowed us to interchange the roles of the components so that the nominal SCB can act as a SET and vice versa. This made it also possible to measure the important parameters of the system like gate and cross capacitances, charging energies and so on. It was also checked that there was no current between the systems through the gold line. Table 6.1 contains some parameters of the sample shown in the SEM image in Fig. 6.3. The main difference between the box and the SET was the larger total capacitance of the latter due to the gold line in contact with the island. The charging energy of both the SET and the SCB was measured at the reference temperature of liquid helium (4.2 K) using the zero-bias anomaly of the dynamic conductance [24] and applying the principle of Coulomb Blockade Thermometry. All other measurements were made at low temperature, around 100 mK, reached with a dilution refrigerator. The two gate capacitances $C_{\mathrm{g(s/b)}}$ (s refers to the SET, b to the SCB) were determined from the periodicity of the modulation of the current vs. the corresponding gate voltage $V_{\mathrm{g(s/b)}}$.

Naturally there was a cross capacitance $C_{\mathrm{cross}}$ between the box gate and the SET island and between the SET gate and the box island. We found this cross capacitance to be smaller than the gate capacitances by a factor of three. The effect was

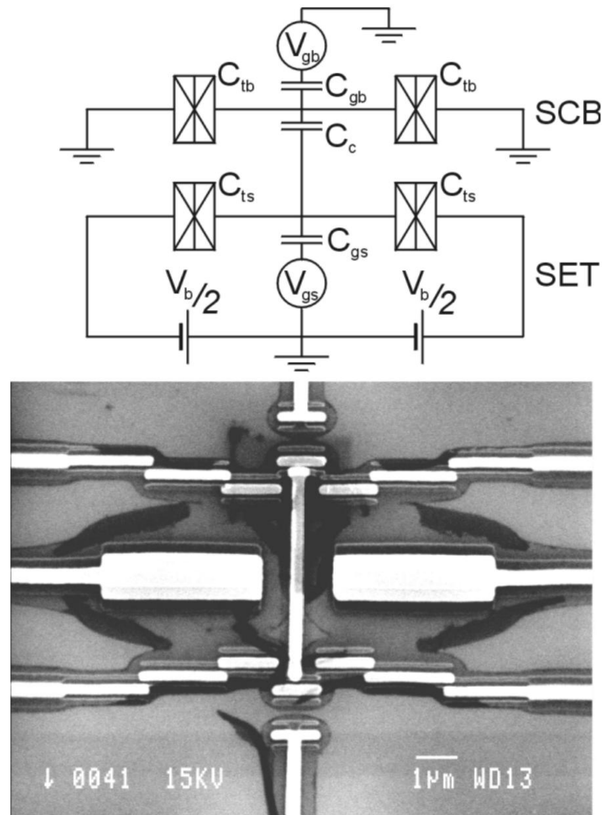


**FIGURE 6.3** *Schematic view and an SEM-image of one of the measured samples. The large structures in the vertical centre are ground electrodes.*

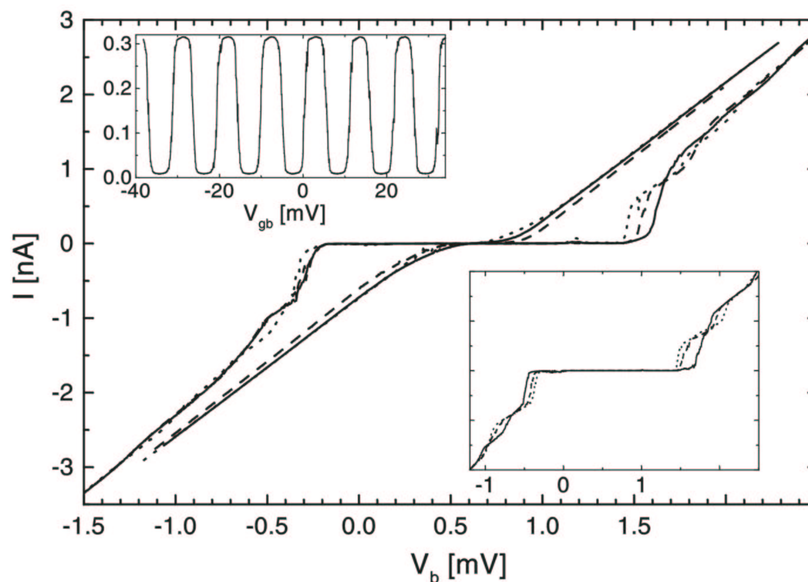


**FIGURE 6.4** *I-V characteristics measured from the SET-circuit with various gate voltages in both the superconducting and normal state. I-V curves of the SCB are depicted in the lower inset. Upper inset shows the current modulation in the SCB with the bias 1.6 mV. The modulation is not compensated and is thus due to the box gate - SET island cross capacitance. The period gives the cross capacitance directly.*

**TABLE 6.1** *The parameters of the sample of Fig. 6.3.*

| | SCB | SET |
|---|---|---|
| $E_C$ | 0.17 meV | 0.11 meV |
| $C_{Island}$ | 460 aF | 700 aF |
| $C_{g(b/s)}$ | 23.5 aF | 23.3 aF |
| $C_{Cross}$ | 7.6 aF | 7.6 aF (estimated) |

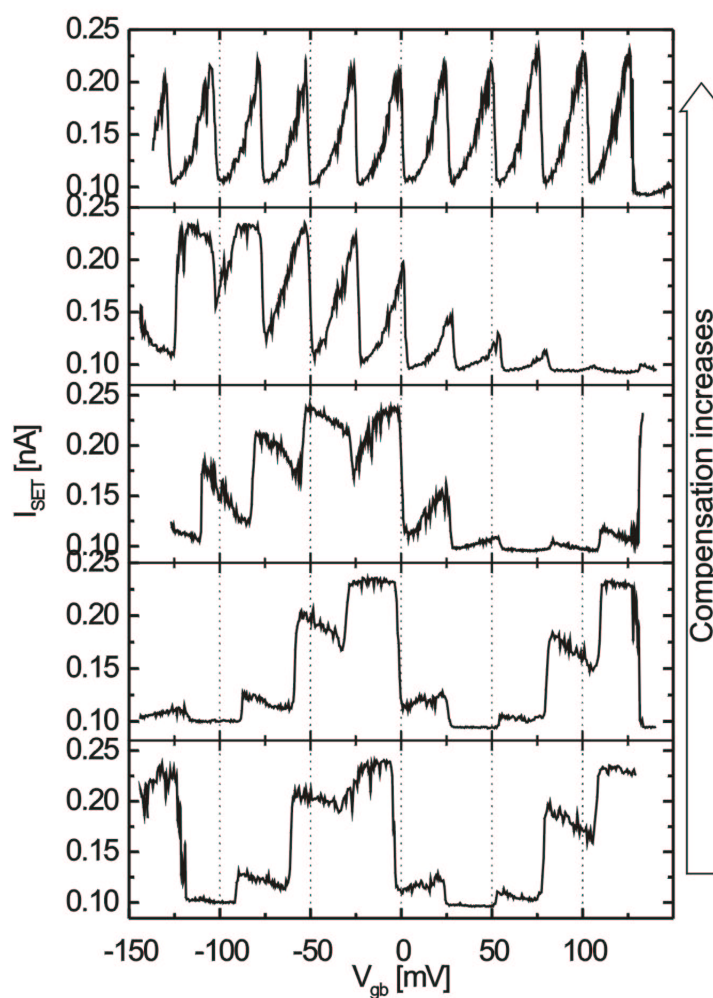


**FIGURE 6.5** *Measured SET current as a function of SCB gate voltage with different levels of compensation. The uppermost graph shows the effect of Cooper pair tunnelling.*

so large that we needed to compensate it by applying a constant fraction of the gate voltage to the other gate with inverse polarity: $V_{gs} = -(C_{\mathrm{cross}}/C_{\mathrm{gs}})V_{\mathrm{gb}}$. The optimum operating point of the SET was found by measuring I-V characteristics with different SET gate voltages. In the sample shown in Fig. 6.4, the biasing point was about 1.6 mV where the current through the SET was most sensitive to external voltages (the 0.5 mV offset in the curve has been identified as a thermoelectric effect).

After the basic characterisation of the sample the SET-electrometer was used to detect tunnelling events in the SCB. This was done by sweeping the gate voltage $V_{\mathrm{gb}}$ of the box while keeping the electrodes grounded and in addition applying the compensation procedure explained above in order to fix the SET operating point to the desired value, independent of $V_{\mathrm{gb}}$. The combination of sweeping the gate voltage and tunnelling of single Cooper pairs into or out of the box generated a sawtooth-like modulation of the island potential. This potential change affected the SET-current via the capacitive coupling between the islands. The sawtooth-like current modulation is seen with different magnitude of compensation in Fig. 6.5. In the bottom figure the effect of the cross capacitance is clearly seen as a ca. 150 mV period in the amplitude of the tunnelling event modulations with period 25 mV. In the top figure this is fully compensated away and only the effect of tunnelling of Cooper pairs is seen.

## 6.4 Conclusions

The measurement of the potential of the island of the Cooper pair box was performed with a superconducting SET capacitively coupled to the island. After the cross-coupling compensation a clear $2e$-periodic tunnelling of Cooper pairs to the SCB island was observed.

# Chapter 7

# Cotunnelling measurements with applied microwave signal

## 7.1 Introduction

Cotunnelling is an important error process in devices based on single electron tunnelling. The response of a single electron transistor to an applied high frequency signal has been studied experimentally at low temperatures and the changes in zero-bias conductance have been compared to the cotunnelling theory (Eq. 2.30). This study is in general interesting in single electron tunnelling devices where a high-frequency signal is applied to the system. This signal might cause unwanted effects like cotunnelling. All measurements presented in this chapter have been conducted at the Department of Physics of Technical University of Denmark (DTU) in co-operation with the author.

The current predicted by Eq. 2.30 has been investigated by applying coherent microwaves to 4-junction array system [6, 7] and single electron transistor [40, 8] and measuring the differential conductance using lock-in technique at zero DC-bias. The high frequency signal was applied to one electrode of the system, while the other electrode was kept at a constant potential. In all measurements reported here, samples were biased at maximum Coulomb blockade so that the next order term in cotunnelling theory, presented in Eq. 2.31, did not contribute to the cotunnelling current.

## 7.2 Experimental Setup

The samples were measured in a KelvinOx™ dilution refrigerator. A magnetic field of 1 T was used to suppress superconductivity of aluminium. The temperature of the

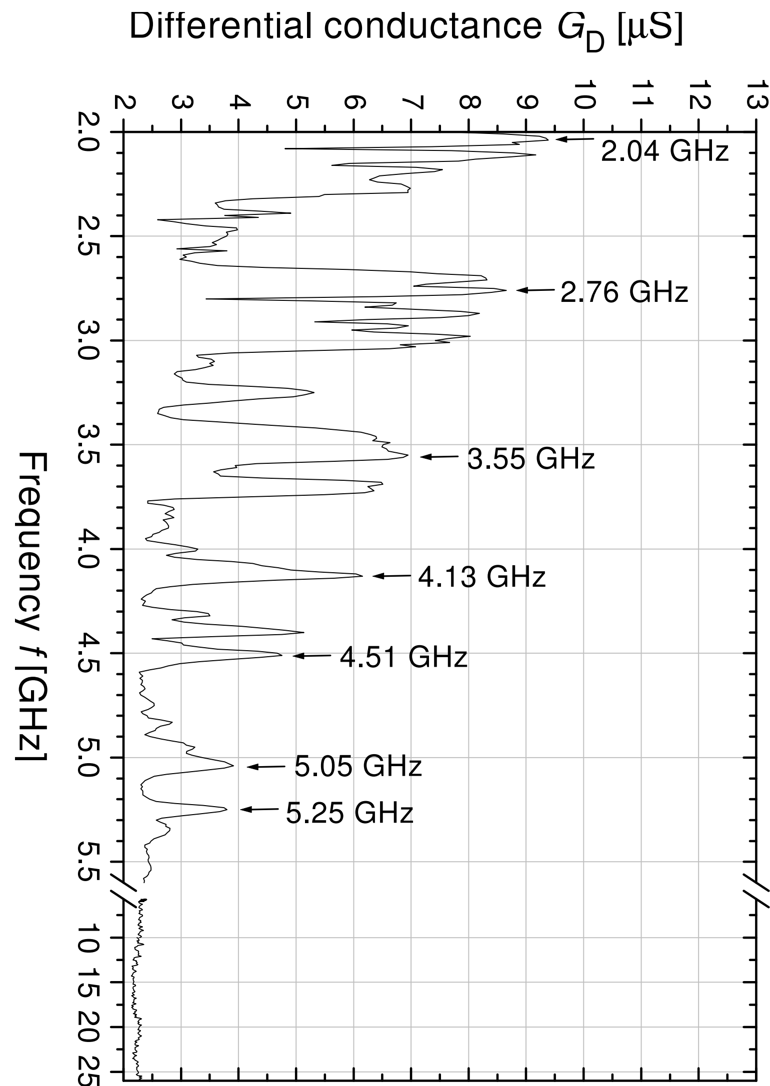


**FIGURE 7.1** *Resonances in the high-frequency line. The transistor was used as a self-detector by biasing in zero-bias, maximum blockade and applying a fixed -10 dBm signal from the microwave synthesizer. The differential conductance was recorded as a function of the frequency. Notice the break in the frequency scale.*

mixing chamber was measured with calibrated germanium and ruthenium-oxide thermometers.

The samples were biased symmetrically by using 'home-made' low noise electronics mounted in an RF tight metal box for shielding. To apply microwaves to the device, there was a separate coaxial connection to the mixing chamber. The microwave connection exhibited resonances. Those were utilized for the microwave bias, because on those the transmission is at local maximum. To determine them the SET transistor was used as a self-detector. The resonances were determined by measuring the differential conductance at zero DC bias and maximum blockade in small frequency steps. The result is shown in Fig. 7.1, where clear peaks in the differential conductance are seen at various frequencies. We used the frequencies marked by arrows in our SET measurements.

As a consequence of the distributed attenuation and resonances in the microwave transmission line, the actual power applied to the sample was unknown. It would have been meaningless to make a throughput measurement at room temperature, since the damping characteristics are different at low temperature, and the coupling to the sample was unknown. Therefore, all power values presented in case of the 4-junction array were read from the levelled output of the microwave synthesizer at room temperature. When measuring the SET, the attenuation of the line was used as a fitting parameter of the data so that quantitative comparison to the theory became possible.

The quantity studied was the differential conductance as function of microwave power and temperature. The measurements were conducted as follows:

1. Temperature was tuned to the desired value with the temperature controller.

2. Current modulation curve was measured as function of the gate voltage in order to find the gate voltage corresponding to maximum Coulomb blockade.

3. I-V curve was measured with the gate voltage adjusted to the maximum Coulomb blockade in order to locate the zero-current bias point.

4. The sample was biased with the values found above and the lock-in amplifier was set to measure the differential conductance at zero bias.

5. Different microwave powers were fed to the sample and the response was monitored with the lock-in amplifier.

## 7.3 Cotunnelling measurements of the 4-junction array

The measured device was an aluminium 4-junction array with $Al/AlO_x/Al$ tunnel junctions. The resistances of the outermost junctions were small compared to the two inner ones and the system was considered as single electron transistor with additional environmental impedance due to the two extra junctions. The device parameters were $C_\Sigma$=1.0 fF, $C_g$= 37.6 aF and $R_\Sigma$=73 kΩ. See Ref. [22] for more detailed description of the measurements.

The sample was very stable over the measurement time of approximately four days as the gate charge variation was less than 0.04$e$ during that time. However, the possible offsets of maximum blockade gate bias point and the current bias corresponding to the zero-current were monitored in between every measurement by remeasuring the IV- and current modulation curve and rebiasing the system to the correct values.

## 7.4 Results

Fig. 7.2 shows the measured microwave power vs. differential conductance curve with 3.682 GHz. The same measurement was also done with frequencies 2.2 GHz and 4.26 GHz, which had a strong coupling to the sample. It is seen that for small powers the conductance increases linearly as microwave power increases. This is in agreement with equation 2.30 as $P \propto V_{AC}^2$. It is thus confirmed that the applied microwave power affects the conductance in expected way. When making a linear fit to the low-power parts of the curves of Fig. 7.2 and collecting the conductance values from the intersection with the y-axis ($P = 0$) one should obtain, according to the cotunnelling theory, conductance values that depend on temperature as $T^2$. Figure 7.3 shows these conductances. The $T^2$-dependency predicted by the cotunnelling theory (Eq. 2.29) is clearly observed.

In these measurements the comparison of the data to the cotunnelling theory was purely qualitative, but in the measurements described in next section also quantitative comparison is given.

## 7.5 Cotunnelling measurements of single electron transistor

The procedure of measuring the single electron transistor was the same as described in case of the 4-junction array. However, more efforts were spent on determining the

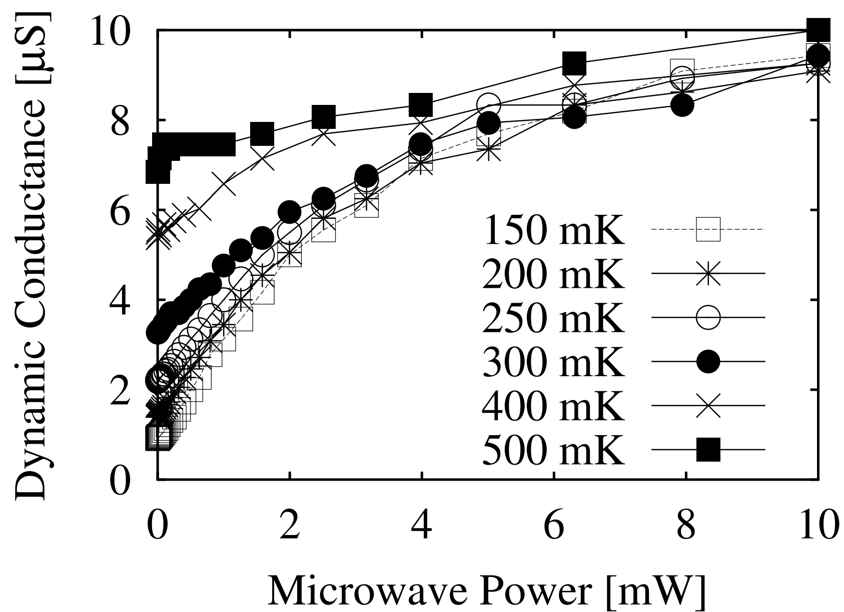


**FIGURE 7.2** *Zero DC bias conductance as a function of microwave power ($B$=1 T, $f$=3.682 GHz).*

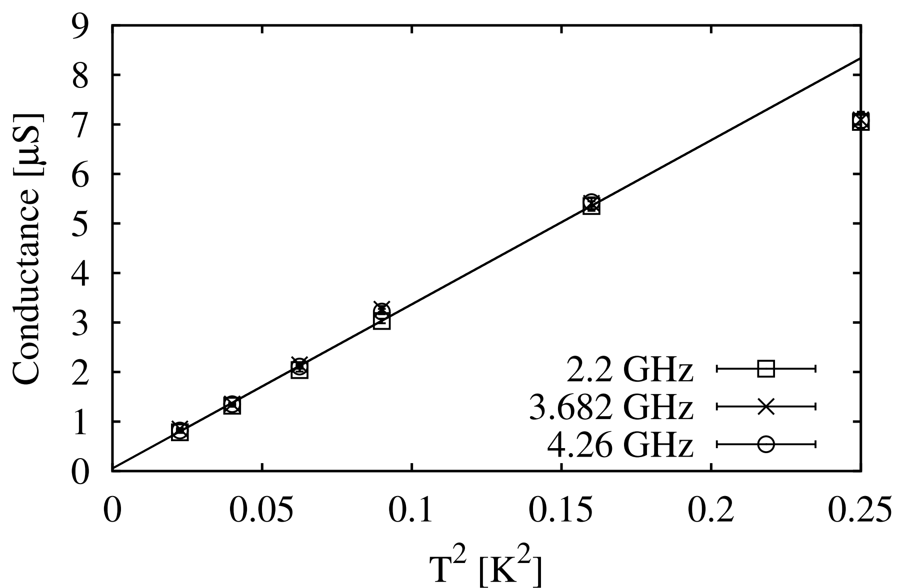


**FIGURE 7.3** *Zero bias conductance at $P = 0$ as function of $T^2$ ($B$=1 T).*

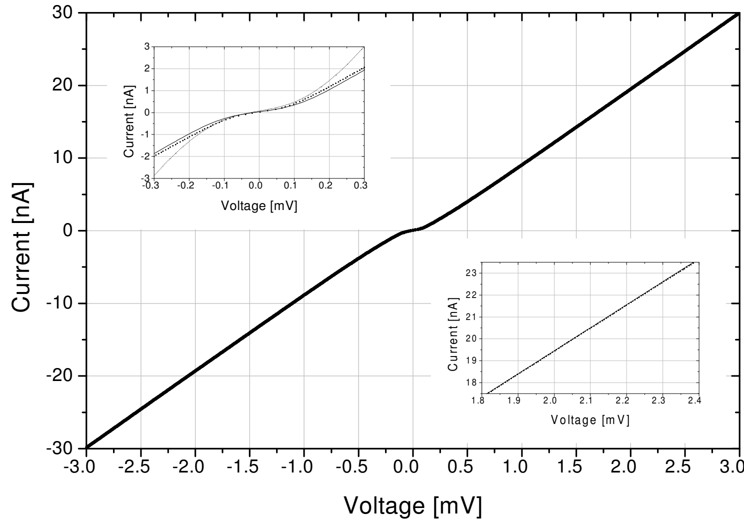


**FIGURE 7.4** *Measured $I$-$V_{\rm DC}$ curve in maximum blockade, and the sequential tunnelling prediction. The insets show enlargements of the blockade region (upper left) and the high-voltage region (lower right).*

electron temperature of the system and the damping of the microwave line in order to make quantitative comparisons to the cotunnelling theory (Eq. 2.30). A more detailed description of the analysis and results of this study is given in ref. [40].

### 7.5.1 Characteristics of the measured SET

For the particular transistor reported here, the $I$-$V_{\rm DC}$ curve (Fig. 7.4) gave the device parameters $R_\Sigma = R_1 + R_2 = 95.0\ {\rm k}\Omega$ and $C_\Sigma = 1030\ {\rm aF}$. From the gate voltage modulation curves ($V_{\rm DC}$-$V_{\rm G}$) one gets $C_{\rm G} = 0.94\ {\rm aF}$ for the gate capacitance. The gate capacitance was small because of a large distance from the gate bias line to the island. We do not expect this to have any adverse effects on the measurements. The set of $V_{\rm DC}$-$V_{\rm G}$ curves at different current biases provided evidence that the device was symmetric, which is assumed in the following. The particular sample was chosen for its high charging energy, which also results the higher tunnelling resistance (for fixed $RC$ product). The simulations showed that a high charging energy is more important than a low tunnelling resistance in obtaining a high cotunnelling/sequential tunnelling ratio.

The sequential tunnelling and cotunnelling conductances at zero-bias and maximum Coulomb blockade as function of temperature have been calculated by using the master equation approach for the orthodox theory. They are shown in Fig. 7.5 for a SET transistor with the parameters measured from the sample reported here. It is seen that the conductances have the same order of magnitude, so that sequential tunnelling has to be taken into account when interpreting the results.

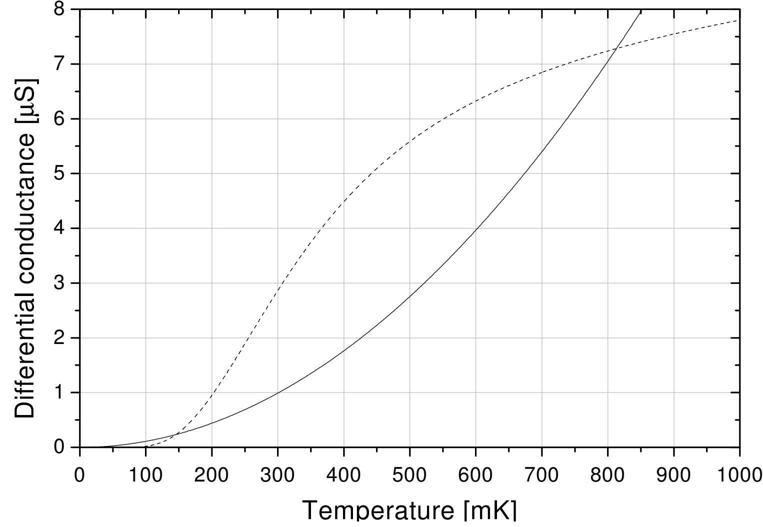


**FIGURE 7.5** *The orthodox theory (dashed) and cotunnelling theory (solid) predictions of the zero-bias, maximum Coulomb blockade conductance for a transistor as function of temperature. The simulation parameters are the same as those determined for the measured SET.*

In the following, the total conductance will be divided into *zero-bias conductance* and *excess conductance*. The zero-bias conductance is defined as the total conductance with no AC power applied from the synthesizer. The excess conductance is the difference between the total conductance with power applied and the conductance without power applied so that:

$$G_{\mathrm{Total}} = G_{\mathrm{zero-bias}} + G_{\mathrm{excess}}. \tag{7.1}$$

## 7.6 Results

### 7.6.1 $V_{\mathrm{AC}}^2$ dependence

In this section, the measurements performed at maximum blockade, where $\Delta^{\pm}$ reduce to the charging energy $E_{\mathrm{C}}$, are presented. It is seen from Eq. 2.30 and Eq. 2.31 that in this case the dynamical conductance does not depend on the frequency of the AC field. The measurements were performed by using the seven frequencies introduced in Fig 7.1. To find out the damping of the microwave line at different frequencies the attenuation at each frequency was considered as a fitting parameter of the data.[1]

Fig. 7.6 shows the main result. The theoretical prediction of the $G_{\mathrm{D}}$-$V_{\mathrm{AC}}$ curves at different temperatures are shown along with the measured values. It is seen that

[1] See [8] for more details.

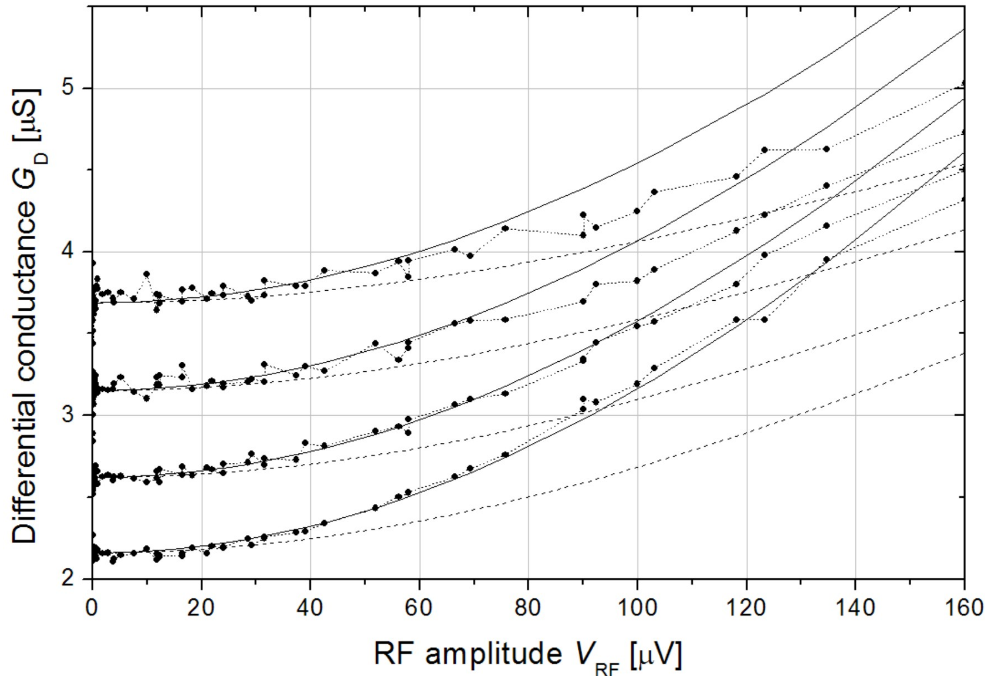


**FIGURE 7.6** *Measured differential conductance as function of the microwave amplitude assuming 37.9 dB additional damping and using the results at the seven frequencies collected by applying their relative damping (the points lay on top of each other indicating that there was no dependence on frequency). The measured values (points) are connected to guide the eye. The lines are the measured zero-bias value plus the predicted excess conductance with cotunnelling (solid) and without cotunnelling (dashed). The predictions are at temperatures 232 mK, 255 mK, 275 mK and 301 mK, respectively (bottom to top).*

the measured conductance fits the predicted one from Eq. 2.30 well at lowest measured temperatures. However, at higher temperatures the measured conductance starts to deviate from the predicted one. There were also measurements conducted at higher temperatures, but on those the deviation was even higher (see [8] Fig. 3).

To be sure that we have really seen the enhancement of cotunnelling due to microwaves we checked if it is possible to explain the results with orthodox theory only. We did not find any damping value of our microwave line to make a reasonable fit of our data to curves predicted by the orthodox theory only. So it seems clear that cotunnelling has been enhanced by microwaves in our measurements and the fit at low temperatures is very good.

## 7.7 Conclusion

The study of microwave enhanced cotunnelling has not been studied experimentally before to our knowledge. The cotunnelling current predicted by Eq. 2.30 was

verified qualitatively in case of the 4-junction system and quantitatively in case of SET. Some questions still remained, as the quantitative comparison was not perfect at higher temperatures in case of the SET. The measurements and predictions were in agreement at lowest measured temperatures but deviated from each other at higher temperatures. The lowest electron temperature obtained, 239 mK, was not much below $T_{\mathrm{C}}/4$. This means that the excess cotunneling conductance at higher temperatures might have been smaller than predicted by theory due to breaking of the low-temperature assumption $k_{\mathrm{B}}T_{\mathrm{e}} \ll \Delta^{\pm}$ of the cotunneling theory. It was not possible to explain the results with orthodox theory only, so it is clear that the microwaves really gave contribution to the current. It would have been interesting to study also the photon assisted cotunnelling introduced by Flensberg, Eq. 2.31, but then the damping of the microwave line should have been the same at all used frequencies or the possible variation should have been known exactly. Unfortunately this was not the case with our equipment and we had to limit our measurements to verify Eq. 2.30 by biasing to maximum Coulomb blockade point. In general our measurements indicate that cotunnelling due to the applied microwave signal should be taken into account and considered as a probable error source when designing high frequency single electron devices.

# Chapter 8

# Conclusions

The results from different projects with the author participating has been presented in this thesis.

Chapter 3 described a novel method in reducing dimensions of nanostructures. Despite the fact that the ultimate limits of the method are still under investigation, the current results presented in chapters 4 and 5 are promising and indicate the applicability of the sputtering method to reduce dimensions of prefabricated nanowires and tunnel junctions. Furthermore, a qualitative change of superconducting transition, possibly originating from resistance due to quantum phase slips, has been observed after sputtering aluminium nanowires.

In chapter 6 the measurement of charge in the island of a Cooper pair box by using single electron transistor as an electrometer has been presented. The tunnelling of Cooper pairs was clearly observed as step-like changing current through the SET.

The cotunnelling measurements conducted at the Technical University of Denmark in co-operation with the author has been presented in Chapter 7. The cotunnelling current through single electron transistor in case of applied microwave signal was measured and concluded to agree the cotunnelling theory.

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[3] This thesis article **A.V.**

[4] This thesis article **A.VI.**

[5] The programs can be downloaded from the web page http://www.srim.org. The site contains also information on the programs.

[6] This thesis article **A.IV.**

[7] This thesis article **III**.

[8] This thesis article **A.VII.**

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